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Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details

Product Status	Active
Architecture	MCU, FPGA
Core Processor	Dual ARM® Cortex®-A53 MPCore™ with CoreSight™, Dual ARM®Cortex™-R5 with CoreSight™
Flash Size	-
RAM Size	256KB
Peripherals	DMA, WDT
Connectivity	CANbus, EBI/EMI, Ethernet, I ² C, MMC/SD/SDIO, SPI, UART/USART, USB OTG
Speed	500MHz, 1.2GHz
Primary Attributes	Zynq®UltraScale+™ FPGA, 469K+ Logic Cells
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	900-BBGA, FCBGA
Supplier Device Package	900-FCBGA (31x31)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xczu6cg-1ffvc900i

Table 1: Absolute Maximum Ratings⁽¹⁾ (Cont'd)

Symbol	Description	Min	Max	Units
Video Codec Unit				
V _{CCINT_VCU}	Internal supply voltage for the video codec unit.	-0.500	1.000	V
PL System Monitor				
V _{CCADC}	PL System Monitor supply relative to GNDADC.	0.500	2.000	V
V _{REFP}	PL System Monitor reference input relative to GNDADC.	0.500	2.000	V
Temperature				
T _{STG}	Storage temperature (ambient).	-65	150	°C
T _{SOL}	Maximum soldering temperature. ⁽¹²⁾	-	260	°C
T _j	Maximum junction temperature. ⁽¹²⁾	-	125	°C

Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.
2. When operating outside of the recommended operating conditions, refer to [Table 6](#), [Table 7](#), and [Table 8](#) for maximum overshoot and undershoot specifications.
3. V_{CCINT_IO} must be connected to V_{CCBRAM}.
4. V_{CCAUX_IO} must be connected to V_{CCAUX}.
5. The lower absolute voltage specification always applies.
6. If V_{CCO} is 3.3V, the maximum voltage is 3.4V.
7. For I/O operation, see the *UltraScale Architecture SelectIO Resources User Guide* ([UG571](#)).
8. AC coupled operation is not supported for RX termination = floating.
9. For GTY transceivers, DC coupled operation is not supported for RX termination = GND.
10. DC coupled operation is not supported for RX termination = programmable.
11. For more information on supported GTH or GTY transceiver terminations see the *UltraScale Architecture GTH Transceiver User Guide* ([UG576](#)) or *UltraScale Architecture GTY Transceiver User Guide* ([UG578](#)).
12. For soldering guidelines and thermal considerations, see the *Zynq UltraScale+ MPSoC Packaging and Pinout Specifications* ([UG1075](#)).

Recommended Operating Conditions

 Table 2: Recommended Operating Conditions⁽¹⁾⁽²⁾

Symbol	Description	Min	Typ	Max	Units
Processor System					
V _{CC_PSINTFP} ⁽³⁾	PS full-power domain supply voltage.	0.808	0.850	0.892	V
	For -1LI and -2LE (V _{CCINT} = 0.72V) devices: PS full-power domain supply voltage.	0.808	0.850	0.892	V
	For -3E devices: PS full-power domain supply voltage.	0.873	0.900	0.927	V
V _{CC_PSINTLP}	PS low-power domain supply voltage.	0.808	0.850	0.892	V
	For -1LI and -2LE (V _{CCINT} = 0.72V) devices: PS low-power domain supply voltage.	0.808	0.850	0.892	V
	For -3E devices: PS low-power domain supply voltage.	0.873	0.900	0.927	V
V _{CC_PSAUX}	PS auxiliary supply voltage.	1.710	1.800	1.890	V
V _{CC_PSINTFP_DDR} ⁽³⁾	PS DDR controller and PHY supply voltage.	0.808	0.850	0.892	V
	For -1LI and -2LE (V _{CCINT} = 0.72V) devices: PS DDR controller and PHY supply voltage.	0.808	0.850	0.892	V
	For -3E devices: PS DDR controller and PHY supply voltage.	0.873	0.900	0.927	V
V _{CC_PSADC}	PS SYSMON ADC supply voltage relative to GND_PSADC.	1.710	1.800	1.890	V
V _{CC_PSPLL}	PS PLL supply voltage.	1.164	1.200	1.236	V
V _{PS_MGTRAVCC}	PS-GTR supply voltage.	0.825	0.850	0.875	V
V _{PS_MGTRAVTT}	PS-GTR termination voltage.	1.746	1.800	1.854	V
V _{CCO_PSDDR} ⁽⁴⁾	PS DDR I/O supply voltage.	1.06	–	1.575	V
V _{CC_PSDDR_PLL}	PS DDR PLL supply voltage.	1.710	1.800	1.890	V
V _{CCO_PSIO} ⁽⁵⁾	PS I/O supply.	1.710	–	3.465	V
V _{PSIN}	PS I/O input voltage.	–0.200	–	V _{CCO_PSIO} + 0.200	V
	PS DDR I/O input voltage.	–0.200	–	V _{CCO_PSDDR} + 0.200	
V _{CC_PSBATT} ⁽⁶⁾	PS battery-backed RAM and battery-backed real-time clock (RTC) supply voltage.	1.200	–	1.500	V
Programmable Logic					
V _{CCINT}	PL internal supply voltage.	0.825	0.850	0.876	V
	For -1LI and -2LE (V _{CCINT} = 0.72V) devices: PL internal supply voltage.	0.698	0.720	0.742	V
	For -3E devices: PL internal supply voltage.	0.873	0.900	0.927	V
V _{CCINT_IO} ⁽⁷⁾	PL internal supply voltage for the I/O banks.	0.825	0.850	0.876	V
	For -1LI and -2LE (V _{CCINT} = 0.72V) devices: PL internal supply voltage for the I/O banks.	0.825	0.850	0.876	V
	For -3E devices: PL internal supply voltage for the I/O banks.	0.873	0.900	0.927	V
V _{CCBRAM}	Block RAM supply voltage.	0.825	0.850	0.876	V
	For -3E devices: block RAM supply voltage.	0.873	0.900	0.927	V
V _{CCAUX}	Auxiliary supply voltage.	1.746	1.800	1.854	V

Table 2: Recommended Operating Conditions⁽¹⁾⁽²⁾ (Cont'd)

Symbol	Description	Min	Typ	Max	Units
V _{CCO} ⁽⁸⁾	Supply voltage for HD I/O banks.	1.140	–	3.400	V
	Supply voltage for HP I/O banks.	0.950	–	1.900	V
V _{CCAUX_IO} ⁽⁹⁾	Auxiliary I/O supply voltage.	1.746	1.800	1.854	V
V _{IN} ⁽¹⁰⁾	I/O input voltage.	–0.200	–	V _{CCO} + 0.200	V
I _{IN} ⁽¹¹⁾	Maximum current through any PL or PS pin in a powered or unpowered bank when forward biasing the clamp diode.	–	–	10	mA
GTH or GTY Transceiver					
V _{MGTAVCC} ⁽¹²⁾	Analog supply voltage for the GTH or GTY transceiver.	0.873	0.900	0.927	V
V _{MGTAVTT} ⁽¹²⁾	Analog supply voltage for the GTH or GTY transmitter and receiver termination circuits.	1.164	1.200	1.236	V
V _{MGTVCCAUX} ⁽¹²⁾	Auxiliary analog QPLL voltage supply for the transceivers.	1.746	1.800	1.854	V
V _{MGTAVTTRCAL} ⁽¹²⁾	Analog supply voltage for the resistor calibration circuit of the GTH or GTY transceiver column.	1.164	1.200	1.236	V
VCU					
V _{CCINT_VCU}	Internal supply voltage for the VCU.	0.825	0.850	0.876	V
	For -1LI and -2LE (V _{CCINT} = 0.72V) devices: Internal supply voltage for the VCU.	0.825	0.850	0.876	V
	For -3E devices: Internal supply voltage for the VCU.	0.873	0.900	0.927	V

Power Supply Sequencing

PS Power-On/Off Power Supply Sequencing

The low-power domain (LPD) must operate before the full-power domain (FPD) can function. The low-power and full-power domains can be powered simultaneously. The PS_POR_B input must be asserted to GND during the power-on sequence (see Table 37). The FPD (when used) must be powered before PS_POR_B is released.

To achieve minimum current draw and ensure that the I/Os are 3-stated at power-on, the recommended power-on sequence for the low-power domain (LPD) is listed. The recommended power-off sequence is the reverse of the power-on sequence.

1. $V_{CC_PSINTLP}$
2. V_{CC_PSAUX} , V_{CC_PSADC} , and V_{CC_PSPLL} in any order or simultaneously.
3. V_{CCO_PSIO}

To achieve minimum current draw and ensure that the I/Os are 3-stated at power-on, the recommended power-on sequence for the full-power domain (FPD) is listed. The recommended power-off sequence is the reverse of the power-on sequence.

1. $V_{CC_PSINTFP}$ and $V_{CC_PSINTFP_DDR}$ driven from the same supply source.
2. $V_{PS_MGTRAVCC}$ and $V_{CC_PSDDR_PLL}$ in any order or simultaneously.
3. $V_{PS_MGTRAVTT}$ and V_{CCO_PSDDR} in any order or simultaneously.

PL Power-On/Off Power Supply Sequencing

The recommended power-on sequence is V_{CCINT} , $V_{CCINT_IO}/V_{CCBRAM}/V_{CCINT_VCU}$, V_{CCAUX}/V_{CCAUX_IO} , and V_{CCO} to achieve minimum current draw and ensure that the I/Os are 3-stated at power-on. The recommended power-off sequence is the reverse of the power-on sequence. If V_{CCINT} and V_{CCINT_IO}/V_{CCBRAM} have the same recommended voltage levels, they can be powered by the same supply and ramped simultaneously. V_{CCINT_IO} must be connected to V_{CCBRAM} . If V_{CCAUX}/V_{CCAUX_IO} and V_{CCO} have the same recommended voltage levels, they can be powered by the same supply and ramped simultaneously. V_{CCAUX} and V_{CCAUX_IO} must be connected together. V_{CCADC} and V_{REF} can be powered at any time and have no power-up sequencing requirements.

The recommended power-on sequence to achieve minimum current draw for the GTH or GTY transceivers is V_{CCINT} , $V_{MGTAVCC}$, $V_{MGTAVTT}$ OR $V_{MGTAVCC}$, V_{CCINT} , $V_{MGTAVTT}$. There is no recommended sequencing for $V_{MGTAVCCAUX}$. Both $V_{MGTAVCC}$ and V_{CCINT} can be ramped simultaneously. The recommended power-off sequence is the reverse of the power-on sequence to achieve minimum current draw.

If these recommended sequences are not met, current drawn from $V_{MGTAVTT}$ can be higher than specifications during power-up and power-down.

Table 11: Power Supply Ramp Time (Cont'd)

Symbol	Description	Min	Max	Units
$T_{V_{CCO_PSDDR}}$	Ramp time from GND to 95% of V_{CCO_PSDDR} .	0.2	40	ms
$T_{V_{CC_PSDDR_PLL}}$	Ramp time from GND to 95% of $V_{CC_PSDDR_PLL}$.	0.2	40	ms
$T_{V_{CCO_PSIO}}$	Ramp time from GND to 95% of V_{CCO_PSIO} .	0.2	40	ms

DC Input and Output Levels

Values for V_{IL} and V_{IH} are recommended input voltages. Values for I_{OL} and I_{OH} are guaranteed over the recommended operating conditions at the V_{OL} and V_{OH} test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at a minimum V_{CCO} with the respective V_{OL} and V_{OH} voltage levels shown. Other standards are sample tested.

PS I/O Levels

Table 12: PS MIO and CONFIG DC Input and Output Levels⁽¹⁾

I/O Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
LVC MOS33	-0.300	0.800	2.000	V_{CCO_PSIO}	0.40	2.40	12	-12
LVC MOS25	-0.300	0.700	1.700	$V_{CCO_PSIO} + 0.30$	0.70	1.70	12	-12
LVC MOS18	-0.300	35% V_{CCO_PSIO}	65% V_{CCO_PSIO}	$V_{CCO_PSIO} + 0.30$	0.45	$V_{CCO_PSIO} - 0.45$	12	-12

Notes:

1. Tested according to relevant specifications.

Table 13: PS DDR DC Input and Output Levels⁽¹⁾

DDR Standard	V_{IL}		V_{IH}		V_{OL} ⁽²⁾	V_{OH} ⁽²⁾	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
DDR4	0.000	$V_{REF} - 0.100$	$V_{REF} + 0.100$	V_{CCO_PSDDR}	$0.8 \times V_{CCO_PSDDR} - 0.150$	$0.8 \times V_{CCO_PSDDR} + 0.150$	10	-0.1
LPDDR4	0.000	$V_{REF} - 0.100$	$V_{REF} + 0.100$	V_{CCO_PSDDR}	$0.3 \times V_{CCO_PSDDR} - 0.150$	$0.3 \times V_{CCO_PSDDR} + 0.150$	0.1	-10
DDR3	-0.300	$V_{REF} - 0.100$	$V_{REF} + 0.100$	V_{CCO_PSDDR}	$0.5 \times V_{CCO_PSDDR} - 0.175$	$0.5 \times V_{CCO_PSDDR} + 0.175$	8	-8
LPDDR3	0.000	$V_{REF} - 0.100$	$V_{REF} + 0.100$	V_{CCO_PSDDR}	$0.5 \times V_{CCO_PSDDR} - 0.150$	$0.5 \times V_{CCO_PSDDR} + 0.150$	8	-8
DDR3L	-0.300	$V_{REF} - 0.090$	$V_{REF} + 0.090$	V_{CCO_PSDDR}	$0.5 \times V_{CCO_PSDDR} - 0.150$	$0.5 \times V_{CCO_PSDDR} + 0.150$	8	-8

Notes:

1. Tested according to relevant specifications.
2. DDR4 V_{OL}/V_{OH} specifications are only applicable for DQ/DQS pins.

Table 19: Complementary Differential SelectIO DC Input and Output Levels for HP I/O Banks⁽¹⁾

I/O Standard	V _{ICM} (V) ⁽²⁾			V _{ID} (V) ⁽³⁾		V _{OL} (V) ⁽⁴⁾	V _{OH} (V) ⁽⁵⁾	I _{OL}	I _{OH}
	Min	Typ	Max	Min	Max	Max	Min	mA	mA
DIFF_HSTL_I	0.680	V _{CCO} /2	(V _{CCO} /2) + 0.150	0.100	–	0.400	V _{CCO} – 0.400	5.8	–5.8
DIFF_HSTL_I_12	0.400 x V _{CCO}	V _{CCO} /2	0.600 x V _{CCO}	0.100	–	0.250 x V _{CCO}	0.750 x V _{CCO}	4.1	–4.1
DIFF_HSTL_I_18	(V _{CCO} /2) – 0.175	V _{CCO} /2	(V _{CCO} /2) + 0.175	0.100	–	0.400	V _{CCO} – 0.400	6.2	–6.2
DIFF_HSUL_12	(V _{CCO} /2) – 0.120	V _{CCO} /2	(V _{CCO} /2) + 0.120	0.100	–	20% V _{CCO}	80% V _{CCO}	0.1	–0.1
DIFF_SSTL12	(V _{CCO} /2) – 0.150	V _{CCO} /2	(V _{CCO} /2) + 0.150	0.100	–	(V _{CCO} /2) – 0.150	(V _{CCO} /2) + 0.150	8.0	–8.0
DIFF_SSTL135	(V _{CCO} /2) – 0.150	V _{CCO} /2	(V _{CCO} /2) + 0.150	0.100	–	(V _{CCO} /2) – 0.150	(V _{CCO} /2) + 0.150	9.0	–9.0
DIFF_SSTL15	(V _{CCO} /2) – 0.175	V _{CCO} /2	(V _{CCO} /2) + 0.175	0.100	–	(V _{CCO} /2) – 0.175	(V _{CCO} /2) + 0.175	10.0	–10.0
DIFF_SSTL18_I	(V _{CCO} /2) – 0.175	V _{CCO} /2	(V _{CCO} /2) + 0.175	0.100	–	(V _{CCO} /2) – 0.470	(V _{CCO} /2) + 0.470	7.0	–7.0

Notes:

1. DIFF_POD10 and DIFF_POD12 HP I/O bank specifications are shown in [Table 20](#), [Table 21](#), and [Table 22](#).
2. V_{ICM} is the input common mode voltage.
3. V_{ID} is the input differential voltage.
4. V_{OL} is the single-ended low-output voltage.
5. V_{OH} is the single-ended high-output voltage.

Table 20: DC Input Levels for Differential POD10 and POD12 I/O Standards⁽¹⁾⁽²⁾

I/O Standard	V _{ICM} (V)			V _{ID} (V)	
	Min	Typ	Max	Min	Max
DIFF_POD10	0.63	0.70	0.77	0.14	–
DIFF_POD12	0.76	0.84	0.92	0.16	–

Notes:

1. Tested according to relevant specifications.
2. Standards specified using the default I/O standard configuration. For details, see the *UltraScale Architecture SelectIO Resources User Guide* ([UG571](#)).

Table 21: DC Output Levels for Single-ended and Differential POD10 and POD12 Standards⁽¹⁾⁽²⁾

Symbol	Description	V _{OUT}	Min	Typ	Max	Units
R _{OL}	Pull-down resistance.	V _{OM_DC} (as described in Table 22)	36	40	44	Ω
R _{OH}	Pull-up resistance.	V _{OM_DC} (as described in Table 22)	36	40	44	Ω

Notes:

1. Tested according to relevant specifications.
2. Standards specified using the default I/O standard configuration. For details, see the *UltraScale Architecture SelectIO Resources User Guide* ([UG571](#)).

Table 22: [Table 21](#) Definitions for DC Output Levels for POD Standards

Symbol	Description	All Speed Grades	Units
V _{OM_DC}	DC output Mid measurement level (for IV curve linearity).	0.8 x V _{CCO}	V

Table 26: Speed Grade Designations by Device (Cont'd)

Device	Speed Grade, Temperature Ranges, and V_{CCINT} Operating Voltages		
	Advance	Preliminary	Production
XCZU11EG	-3E ($V_{CCINT} = 0.90V$), -2E ($V_{CCINT} = 0.85V$) -2I ($V_{CCINT} = 0.85V$), -2LE ($V_{CCINT} = 0.85V$) -1E ($V_{CCINT} = 0.85V$), -1I ($V_{CCINT} = 0.85V$) -1LI ($V_{CCINT} = 0.85V$) -2LE ($V_{CCINT} = 0.72V$), -1LI ($V_{CCINT} = 0.72V$)		
XCZU15EG	-3E ($V_{CCINT} = 0.90V$), -2E ($V_{CCINT} = 0.85V$) -2I ($V_{CCINT} = 0.85V$), -2LE ($V_{CCINT} = 0.85V$) -1E ($V_{CCINT} = 0.85V$), -1I ($V_{CCINT} = 0.85V$) -1LI ($V_{CCINT} = 0.85V$) -2LE ($V_{CCINT} = 0.72V$), -1LI ($V_{CCINT} = 0.72V$)		
XCZU17EG	-3E ($V_{CCINT} = 0.90V$), -2E ($V_{CCINT} = 0.85V$) -2I ($V_{CCINT} = 0.85V$), -2LE ($V_{CCINT} = 0.85V$) -1E ($V_{CCINT} = 0.85V$), -1I ($V_{CCINT} = 0.85V$) -1LI ($V_{CCINT} = 0.85V$) -2LE ($V_{CCINT} = 0.72V$), -1LI ($V_{CCINT} = 0.72V$)		
XCZU19EG	-3E ($V_{CCINT} = 0.90V$), -2E ($V_{CCINT} = 0.85V$) -2I ($V_{CCINT} = 0.85V$), -2LE ($V_{CCINT} = 0.85V$) -1E ($V_{CCINT} = 0.85V$), -1I ($V_{CCINT} = 0.85V$) -1LI ($V_{CCINT} = 0.85V$) -2LE ($V_{CCINT} = 0.72V$), -1LI ($V_{CCINT} = 0.72V$)		

Notes:

1. The lowest power -1L and -2L devices, where $V_{CCINT} = 0.72V$, are listed in the Vivado Design Suite as -1LV and -2LV respectively.

Processor System (PS) Performance Characteristics

Table 28: Processor Performance

Symbol	Description	Speed Grade			Units
		-3	-2	-1	
F _{APUMAX}	Maximum APU clock frequency.	1500	1333	1200	MHz
F _{RPUMAX}	Maximum RPU clock frequency.	600	533	500	MHz
F _{GPUMAX}	Maximum GPU clock frequency.	667	600	600	MHz

Table 29: Configuration and Security Unit Performance

Symbol	Description	Speed Grade			Units
		-3	-2	-1	
F _{CSUCIBMAX}	Maximum CSU crypto interface block frequency.	400	400	400	MHz

Table 30: PS DDR Performance

Memory Standard	Package	DRAM Type	Speed Grade						Units
			-3		-2		-1		
			Min	Max	Min	Max	Min	Max	
DDR4	All FFV packages, FBVB900, and SFVC784	Single rank component	664	2400	664	2400	664	2400	Mb/s
		1 rank DIMM ⁽¹⁾⁽²⁾	664	2133	664	2133	664	2133	Mb/s
		2 rank DIMM ⁽¹⁾⁽³⁾	664	1866	664	1866	664	1866	Mb/s
	SFVA625	Single rank component	664	2133	664	2133	664	2133	Mb/s
		1 rank DIMM ⁽¹⁾⁽²⁾	664	1866	664	1866	664	1866	Mb/s
		2 rank DIMM ⁽¹⁾⁽³⁾	664	1600	664	1600	664	1600	Mb/s
	SBVA484	Single rank component	664	1066	664	1066	664	1066	Mb/s
		1 rank DIMM ⁽¹⁾⁽²⁾	664	1066	664	1066	664	1066	Mb/s
		2 rank DIMM ⁽¹⁾⁽³⁾	664	1066	664	1066	664	1066	Mb/s
LPDDR4	All FFV packages, FBVB900 and SFVC784	Single die package ⁽⁵⁾	664	2400	664	2400	664	2400	Mb/s
		Dual die package ⁽⁴⁾⁽⁵⁾	664	2133	664	2133	664	2133	Mb/s
	SFVA625	Single die package ⁽⁵⁾	664	2133	664	2133	664	2133	Mb/s
		Dual die package ⁽⁴⁾⁽⁵⁾	664	1866	664	1866	664	1866	Mb/s
	SBVA484	Single die package ⁽⁵⁾	664	1066	664	1066	664	1066	Mb/s
		Dual die package ⁽⁴⁾⁽⁵⁾	664	1066	664	1066	664	1066	Mb/s

Table 37: PS Reset Assertion Timing Requirements

Symbol	Description	Min	Typ	Max	Units
T _{PSPOR}	Required PS_POR_B assertion time. (1)	10	–	–	μs
T _{PSRST}	Required PS_SRST_B assertion time.	3	–	–	PS_REF_CLK Clock Cycles

Notes:

- PS_POR_B must be asserted Low at power-up and continue to be asserted for a duration of T_{PSPOR} after all the PS supply voltages reach minimum levels. PS_POR_B must be asserted Low for the duration of T_{POR} when the PS and PL power-up at the same time and the application uses both the PS and PL after power-up.

Table 38: PS Clocks Switching Characteristics

Symbol	Description	Speed Grade			Units
		-3	-2	-1	
F _{TOPSW_MAINMAX}	TOPSW_MAIN maximum frequency.	600	533	533	MHz
F _{TOPSW_LSBUSMAX}	TOPSW_LSBUS maximum frequency.	100	100	100	MHz
F _{GDMAMAX}	FPD-DMA maximum frequency.	600	600	600	MHz
F _{DPDMAMAX}	DisplayPort DMA maximum frequency.	600	600	600	MHz
F _{LPD_SWITCH_CTRLMAX}	LPD_SWITCH_CTRL maximum frequency.	600	500	500	MHz
F _{LPD_LSBUS_CTRLMAX}	LPD_LSBUS_CTRL maximum frequency.	100	100	100	MHz
F _{ADMAMAX}	LPD-DMA maximum frequency.	600	500	500	MHz
F _{APLL_TO_LPDMAX}	APLL_TO_LPD maximum frequency.	533	533	533	MHz
F _{DPDLL_TO_LPDMAX}	DPDLL_TO_LPD maximum frequency.	533	533	533	MHz
F _{VPDLL_TO_LPDMAX}	VPDLL_TO_LPD maximum frequency.	533	533	533	MHz
F _{IOPLL_TO_LPDMAX}	IOPLL_TO_LPD maximum frequency.	533	533	533	MHz
F _{RPLL_TO_FPDMAX}	RPLL_TO_FPD maximum frequency.	533	533	533	MHz

Table 42: Linear Quad-SPI Interface⁽¹⁾

Symbol	Description	Load Conditions ⁽²⁾	Min	Max	Units
Quad-SPI device clock frequency operating at 100 MHz. Loopback enabled. LVCMOS 1.8V I/O standard.					
T _{DCQSPICLK5}	Quad-SPI clock duty cycle.	15 pF	45	55	%
		30 pF	45	55	%
T _{QSPISSCLK5}	Slave select asserted to next clock edge. ⁽³⁾	15 pF	5.0	–	ns
		30 pF	5.0	–	ns
T _{QSPISCLKSS5}	Clock edge to slave select deasserted.	15 pF	5.0	–	ns
		30 pF	5.0	–	ns
T _{QSPICKO5}	Clock to output delay, all outputs.	15 pF	3.2	7.4	ns
		30 pF	3.2	7.4	ns
T _{QSPIDCK5}	Setup time, all inputs.	15 pF	2.4	–	ns
		30 pF	2.4	–	ns
T _{QSPICKD5}	Hold time, all inputs.	15 pF	0.0	–	ns
		30 pF	0.0	–	ns
F _{QSPIREFCLK5}	Quad-SPI reference clock frequency.	15 pF	–	200	MHz
		30 pF	–	200	MHz
F _{QSPICLK5}	Quad-SPI device clock frequency.	15 pF	–	100	MHz
		30 pF	–	100	MHz

Notes:

1. The test conditions are configured for the linear Quad-SPI interface at 100 MHz with a 12 mA drive strength and fast slew rate.
2. 30 pF loads are for stacked modes.
3. T_{QSPISSCLK5} is only valid when two reference clock cycles are programmed between chip select and clock.

PS USB Interface

 Table 43: ULPI Interface⁽¹⁾

Symbol	Description	Min	Max	Units
T _{ULPIDCK}	Input setup to ULPI clock, all inputs.	4.5	–	ns
T _{ULPICKD}	Input hold to ULPI clock, all inputs.	0	–	ns
T _{ULPICKO}	ULPI clock to output valid, all outputs.	2.0	8.86	ns
F _{ULPICLK}	ULPI reference clock frequency.	–	60	MHz

Notes:

1. The test conditions are configured to the LVCMOS 3.3V I/O standard with a 12 mA drive strength, fast slew rate, and a 15 pF load.

PS DAP Interface

Table 50: DAP Interface⁽¹⁾

Symbol	Description ⁽²⁾	Min	Max	Units
T _{PDAPDCK}	PS DAP input setup time.	3.0	–	ns
T _{PDAPCKD}	PS DAP input hold time.	2.0	–	ns
T _{PDAPCKO}	PS DAP clock to out delay.	–	10.86	ns
T _{PDAPCLK}	PS DAP clock frequency.	–	44	MHz

Notes:

1. The test conditions are configured to the LVCMOS 3.3V I/O standard with a 12 mA drive strength, fast slew rate, and a 15 pF load.
2. PS DAP interface signals connect to MIO pins.

PS UART Interface

Table 51: UART Interface⁽¹⁾

Symbol	Description	Min	Max	Units
BAUD _{TXMAX}	Transmit baud rate.	–	6.25	Mb/s
BAUD _{RXMAX}	Receive baud rate.	–	6.25	Mb/s
F _{UART_REF_CLK}	UART reference clock frequency.	–	100	MHz

Notes:

1. The test conditions are configured to the LVCMOS 3.3V I/O standard with a 12 mA drive strength, fast slew rate, and a 15 pF load.

PS General Purpose I/O Interface

Table 52: General Purpose I/O (GPIO) Interface

Symbol	Description	Min	Max	Units
T _{PWGPIOH}	Input High pulse width.	10 x 1/F _{LPD_LSBUS_CTRLMAX}	–	µs
T _{PWGPIOL}	Input Low pulse width.	10 x 1/F _{LPD_LSBUS_CTRLMAX}	–	µs

PS Trace Interface

Table 53: Trace Interface⁽¹⁾

Symbol	Description	Min	Max	Units
T _{TCECKO}	Trace clock to output delay, all outputs.	–0.5	0.5	ns
T _{DCTCECLK}	Trace clock duty cycle.	45	55	%
F _{TCECLK}	Trace clock frequency.	–	125	MHz

Notes:

1. The test conditions are configured to the LVCMOS 3.3V I/O standard with a 12 mA drive strength, fast slew rate, and a 15 pF load.

Table 67: USB 3.0 Protocol Characteristics (PS-GTR Transceivers)

Standard	Description	Line Rate (Mb/s)	Min	Max	Units
USB 3.0 Transmitter Jitter Generation					
USB 3.0	Total transmitter jitter.	5000	–	0.66	UI
USB 3.0 Receiver High Frequency Jitter Tolerance					
USB 3.0	Total receiver jitter tolerance.	5000	0.2	–	UI

Table 68: Serial-GMII Protocol Characteristics (PS-GTR Transceivers)

Standard	Description	Line Rate (Mb/s)	Min	Max	Units
Serial-GMII Transmitter Jitter Generation					
SGMII	Deterministic transmitter jitter.	1250	–	0.25	UI
Serial-GMII Receiver High Frequency Jitter Tolerance					
SGMII	Total receiver jitter tolerance.	1250	0.25	–	UI

PS System Monitor Specifications

Table 69: PS SYSMON Specifications

Parameter	Comments	Conditions	Min	Typ	Max	Units
$V_{CC_PSADC} = 1.8V \pm 3\%$, $T_j = -40^\circ C$ to $100^\circ C$, typical values at $T_j = 40^\circ C$						
ADC Accuracy ($T_j = -55^\circ C$ to $125^\circ C$) (1)						
Resolution			10	–	–	Bits
Sample rate			–	–	1	MS/s
RMS code noise	On-chip reference		–	1	–	LSBs
On-Chip Sensor Accuracy						
Temperature sensor error		$T_j = -55^\circ C$ to $110^\circ C$	–	–	± 3.5	$^\circ C$
		$T_j = 110^\circ C$ to $125^\circ C$	–	–	± 5	$^\circ C$
Supply sensor error(2)	Supply voltages less than or electrically connected to V_{CC_PSADC} .	$T_j = -40^\circ C$ to $125^\circ C$	–	–	± 1	%
	Supply voltages nominally at 1.8V but with the potential to go above V_{CC_PSADC} .	$T_j = -40^\circ C$ to $125^\circ C$	–	–	± 1.5	%
	Supply voltages nominally in the 2.0V to 3.3V range.	$T_j = -40^\circ C$ to $125^\circ C$	–	–	± 2.5	%

Notes:

- ADC offset errors are removed by enabling the ADC automatic offset calibration feature. The values are specified for when this feature is enabled.
- Supply sensor offset and gain errors are removed by enabling the automatic offset and gain calibration feature. The values are specified for when this feature is enabled.

Block RAM and FIFO Switching Characteristics

Table 80: Block RAM and FIFO Switching Characteristics

Symbol	Description	Speed Grade and V _{CCINT} Operating Voltages					Units
		0.90V	0.85V		0.72V		
		-3	-2	-1	-2	-1	
Maximum Frequency							
F _{MAX_WF_NC}	Block RAM (WRITE_FIRST and NO_CHANGE modes).	825	738	645	585	516	MHz
F _{MAX_RF}	Block RAM (READ_FIRST mode).	718	637	575	510	460	MHz
F _{MAX_FIFO}	FIFO in all modes without ECC.	825	738	645	585	516	MHz
F _{MAX_ECC}	Block RAM and FIFO in ECC configuration without PIPELINE.	718	637	575	510	460	MHz
	Block RAM and FIFO in ECC configuration with PIPELINE and Block RAM in WRITE_FIRST or NO_CHANGE mode.	825	738	645	585	516	MHz
T _{PW} ⁽¹⁾	Minimum pulse width.	495	542	543	577	578	ps
Block RAM and FIFO Clock-to-Out Delays							
T _{RCKO_DO}	Clock CLK to DOUT output (without output register).	0.91	1.02	1.11	1.46	1.53	ns, Max
T _{RCKO_DO_REG}	Clock CLK to DOUT output (with output register).	0.27	0.29	0.30	0.42	0.44	ns, Max

Notes:

1. The MMCM and PLL DUTY_CYCLE attribute should be set to 50% to meet the pulse-width requirements at the higher frequencies.

UltraRAM Switching Characteristics

The *UltraScale Architecture and Product Overview* ([DS890](#)) lists the Zynq UltraScale+ MPSoC that include this memory.

Table 81: UltraRAM Switching Characteristics

Symbol	Description	Speed Grade and V _{CCINT} Operating Voltages					Units
		0.90V	0.85V		0.72V		
		-3	-2	-1	-2	-1	
Maximum Frequency							
F _{MAX}	UltraRAM maximum frequency with OREG_B = True.	650	600	575	500	481	MHz
F _{MAX_ECC}	UltraRAM maximum frequency with OREG_B = False and EN_ECC_RD_B = True.	450	400	386	325	315	MHz
F _{MAX_NORPIPELINE}	UltraRAM maximum frequency with OREG_B = False and EN_ECC_RD_B = False.	550	500	478	425	408	MHz
T _{PW} ⁽¹⁾	Minimum pulse width.	650	700	730	800	832	ps
T _{RSTPW}	Asynchronous reset minimum pulse width. One cycle required.	1 clock cycle					

Notes:

1. The MMCM and PLL DUTY_CYCLE attribute should be set to 50% to meet the pulse-width requirements at the higher frequencies.

Input/Output Delay Switching Characteristics

Table 82: Input/Output Delay Switching Characteristics

Symbol	Description	Speed Grade and V _{CCINT} Operating Voltages					Units
		0.90V	0.85V		0.72V		
		-3	-2	-1	-2	-1	
F _{REFCLK}	REFCLK frequency for IDELAYCTRL (component mode).	300 to 800					MHz
	REFCLK frequency for BITSLICE_CONTROL (native mode). ⁽¹⁾	300 to 2666.67	300 to 2666.67	300 to 2400	300 to 2400	300 to 2133	MHz
T _{MINPER_CLK}	Minimum period for IODELAY clock.	3.195	3.195	3.195	3.195	3.195	ns
T _{MINPER_RST}	Minimum reset pulse width.	52.00					ns
T _{IDELAY_RESOLUTION} / T _{ODELAY_RESOLUTION}	IDELAY/ODELAY chain resolution.	2.1 to 12					ps

Notes:

1. PLL settings could restrict the minimum allowable data rate. For example, when using a PLL with CLKOUTPHY_MODE = VCO_HALF, the minimum frequency is PLL_FVCOMIN/2.

Table 91: Global Clock Input Setup and Hold With MMCM

Symbol	Description	Device	Speed Grade and V _{CCIINT} Operating Voltages					Units	
			0.90V	0.85V		0.72V			
			-3	-2	-1	-2	-1		
Input Setup and Hold Time Relative to Global Clock Input Signal using SSTL15 Standard. (1)(2)(3)									
T _{PSMMCMCC_ZU2}	Global clock input and input flip-flop (or latch) with MMCM.	Setup	XCZU2	N/A	1.83	1.96	2.29	2.48	ns
T _{PHMMCMCC_ZU2}		Hold			-0.19	-0.19	0.13	0.13	ns
T _{PSMMCMCC_ZU3}		Setup	XCZU3	N/A	1.83	1.96	2.29	2.48	ns
T _{PHMMCMCC_ZU3}		Hold			-0.19	-0.19	0.13	0.13	ns
T _{PSMMCMCC_ZU4}		Setup	XCZU4	1.96	1.96	2.10	2.49	2.59	ns
T _{PHMMCMCC_ZU4}		Hold		-0.12	-0.12	-0.12	0.27	0.48	ns
T _{PSMMCMCC_ZU5}		Setup	XCZU5	1.96	1.96	2.10	2.49	2.59	ns
T _{PHMMCMCC_ZU5}		Hold		-0.12	-0.12	-0.12	0.27	0.48	ns
T _{PSMMCMCC_ZU6}		Setup	XCZU6	1.97	2.00	2.12	2.26	2.44	ns
T _{PHMMCMCC_ZU6}		Hold		-0.11	-0.11	-0.11	0.16	0.18	ns
T _{PSMMCMCC_ZU7}		Setup	XCZU7	1.91	1.91	2.02	2.45	2.70	ns
T _{PHMMCMCC_ZU7}		Hold		-0.14	-0.14	-0.14	0.37	0.38	ns
T _{PSMMCMCC_ZU9}		Setup	XCZU9	1.97	2.00	2.12	2.26	2.44	ns
T _{PHMMCMCC_ZU9}		Hold		-0.11	-0.11	-0.11	0.16	0.18	ns
T _{PSMMCMCC_ZU11}		Setup	XCZU11	2.08	2.08	2.23	2.59	2.75	ns
T _{PHMMCMCC_ZU11}		Hold		-0.08	-0.08	0.04	0.35	0.74	ns
T _{PSMMCMCC_ZU15}		Setup	XCZU15	1.96	1.99	2.12	2.26	2.44	ns
T _{PHMMCMCC_ZU15}		Hold		-0.10	-0.10	-0.10	0.17	0.19	ns
T _{PSMMCMCC_ZU17}		Setup	XCZU17	1.89	1.89	2.03	2.36	2.55	ns
T _{PHMMCMCC_ZU17}		Hold		-0.16	-0.16	-0.16	0.31	0.34	ns
T _{PSMMCMCC_ZU19}	Setup	XCZU19	1.89	1.89	2.03	2.36	2.55	ns	
T _{PHMMCMCC_ZU19}	Hold		-0.16	-0.16	-0.16	0.31	0.34	ns	

Notes:

1. Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, slowest temperature, and slowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, fastest temperature, and fastest voltage.
2. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible I/O and CLB flip-flops are clocked by the global clock net.
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 99: GTH Transceiver Reference Clock Switching Characteristics

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
F _{GCLK}	Reference clock frequency range.		60	–	820	MHz
T _{RCLK}	Reference clock rise time.	20% – 80%	–	200	–	ps
T _{FCLK}	Reference clock fall time.	80% – 20%	–	200	–	ps
T _{DCREF}	Reference clock duty cycle.	Transceiver PLL only	40	50	60	%

Table 100: GTH Transceiver Reference Clock Oscillator Selection Phase Noise Mask

Symbol	Description	Offset Frequency	Min	Typ	Max	Units
QPLL _{REFCLKMASK} ⁽¹⁾⁽²⁾	QPLL0/QPLL1 reference clock select phase noise mask at REFCLK frequency = 312.5 MHz.	10 kHz	–	–	–105	dBc/Hz
		100 kHz	–	–	–124	
		1 MHz	–	–	–130	
CPLL _{REFCLKMASK} ⁽¹⁾⁽²⁾	CPLL reference clock select phase noise mask at REFCLK frequency = 312.5 MHz.	10 kHz	–	–	–105	dBc/Hz
		100 kHz	–	–	–124	
		1 MHz	–	–	–130	
		50 MHz	–	–	–140	

Notes:

- For reference clock frequencies other than 312.5 MHz, adjust the phase-noise mask values by 20 x Log(N/312.5) where N is the new reference clock frequency in MHz.
- This reference clock phase-noise mask is superseded by any reference clock phase-noise mask that is specified in a supported protocol, e.g., PCIe.

Table 101: GTH Transceiver PLL/Lock Time Adaptation

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
T _{LOCK}	Initial PLL lock.		–	–	1	ms
T _{DLOCK}	Clock recovery phase acquisition and adaptation time for decision feedback equalizer (DFE).	After the PLL is locked to the reference clock, this is the time it takes to lock the clock data recovery (CDR) to the data present at the input.	–	50,000	37 x 10 ⁶	UI
	Clock recovery phase acquisition and adaptation time for low-power mode (LPM) when the DFE is disabled.		–	50,000	2.3 x 10 ⁶	UI

Table 102: GTH Transceiver User Clock Switching Characteristics⁽¹⁾

Symbol	Description	Data Width Conditions (Bit)		Speed Grade and V _{CCINT} Operating Voltages					Units
				0.90V		0.85V		0.72V	
		Internal Logic	Interconnect Logic	-3 ⁽²⁾	-2 ⁽²⁾⁽³⁾	-1 ⁽⁴⁾⁽⁵⁾	-2 ⁽³⁾	-1 ⁽⁵⁾	
F _{TXOUTPMA}	TXOUTCLK maximum frequency sourced from OUTCLKPMA			511.719	511.719	390.625	390.625	322.266	MHz
F _{RXOUTPMA}	RXOUTCLK maximum frequency sourced from OUTCLKPMA			511.719	511.719	390.625	390.625	322.266	MHz

Table 103: GTH Transceiver Transmitter Switching Characteristics

Symbol	Description	Condition	Min	Typ	Max	Units
F _{GTHTX}	Serial data rate range		0.500	–	F _{GTHMAX}	Gb/s
T _{RTX}	TX rise time	20%–80%	–	21	–	ps
T _{FTX}	TX fall time	80%–20%	–	21	–	ps
T _{LLSKEW}	TX lane-to-lane skew ⁽¹⁾		–	–	500.00	ps
T _{J16.375}	Total jitter ⁽²⁾⁽⁴⁾	16.375 Gb/s	–	–	0.28	UI
D _{J16.375}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J15.0}	Total jitter ⁽²⁾⁽⁴⁾	15.0 Gb/s	–	–	0.28	UI
D _{J15.0}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J14.1}	Total jitter ⁽²⁾⁽⁴⁾	14.1 Gb/s	–	–	0.28	UI
D _{J14.1}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J14.1}	Total jitter ⁽²⁾⁽⁴⁾	14.025 Gb/s	–	–	0.28	UI
D _{J14.1}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J13.1}	Total jitter ⁽²⁾⁽⁴⁾	13.1 Gb/s	–	–	0.28	UI
D _{J13.1}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J12.5_QPLL}	Total jitter ⁽²⁾⁽⁴⁾	12.5 Gb/s	–	–	0.28	UI
D _{J12.5_QPLL}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J12.5_CPLL}	Total jitter ⁽³⁾⁽⁴⁾	12.5 Gb/s	–	–	0.33	UI
D _{J12.5_CPLL}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.17	UI
T _{J11.3_QPLL}	Total jitter ⁽²⁾⁽⁴⁾	11.3 Gb/s	–	–	0.28	UI
D _{J11.3_QPLL}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J10.3125_QPLL}	Total jitter ⁽²⁾⁽⁴⁾	10.3125 Gb/s	–	–	0.28	UI
D _{J10.3125_QPLL}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J10.3125_CPLL}	Total jitter ⁽³⁾⁽⁴⁾	10.3125 Gb/s	–	–	0.33	UI
D _{J10.3125_CPLL}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.17	UI
T _{J9.953_QPLL}	Total jitter ⁽²⁾⁽⁴⁾	9.953 Gb/s	–	–	0.28	UI
D _{J9.953_QPLL}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J9.953_CPLL}	Total jitter ⁽³⁾⁽⁴⁾	9.953 Gb/s	–	–	0.33	UI
D _{J9.953_CPLL}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.17	UI
T _{J8.0}	Total jitter ⁽³⁾⁽⁴⁾	8.0 Gb/s	–	–	0.32	UI
D _{J8.0}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.17	UI
T _{J6.6}	Total jitter ⁽³⁾⁽⁴⁾	6.6 Gb/s	–	–	0.30	UI
D _{J6.6}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.15	UI
T _{J5.0}	Total jitter ⁽³⁾⁽⁴⁾	5.0 Gb/s	–	–	0.30	UI
D _{J5.0}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.15	UI
T _{J4.25}	Total jitter ⁽³⁾⁽⁴⁾	4.25 Gb/s	–	–	0.30	UI
D _{J4.25}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.15	UI
T _{J4.0}	Total jitter ⁽³⁾⁽⁴⁾	4.0 Gb/s	–	–	0.32	UI
D _{J4.0}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.16	UI
T _{J3.20}	Total jitter ⁽³⁾⁽⁴⁾	3.20 Gb/s ⁽⁵⁾	–	–	0.20	UI
D _{J3.20}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.10	UI

Table 115: GTY Transceiver Transmitter Switching Characteristics

Symbol	Description	Condition	Min	Typ	Max	Units
F _{GTYTX}	Serial data rate range		0.500	–	F _{GTYMAX}	Gb/s
T _{RTX}	TX rise time	20%–80%	–	21	–	ps
T _{FTX}	TX fall time	80%–20%	–	21	–	ps
T _{LLSKEW}	TX lane-to-lane skew ⁽¹⁾		–	–	500.00	ps
T _{J32.75}	Total jitter ⁽²⁾⁽⁴⁾	32.75 Gb/s	–	–	0.35	UI
D _{J32.75}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.19	UI
T _{J28.21}	Total jitter ⁽²⁾⁽⁴⁾	28.21 Gb/s	–	–	0.28	UI
D _{J28.21}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J16.375}	Total jitter ⁽²⁾⁽⁴⁾	16.375 Gb/s	–	–	0.28	UI
D _{J16.375}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J15.0}	Total jitter ⁽²⁾⁽⁴⁾	15.0 Gb/s	–	–	0.28	UI
D _{J15.0}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J14.1}	Total jitter ⁽²⁾⁽⁴⁾	14.1 Gb/s	–	–	0.28	UI
D _{J14.1}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J14.1}	Total jitter ⁽²⁾⁽⁴⁾	14.025 Gb/s	–	–	0.28	UI
D _{J14.1}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J13.1}	Total jitter ⁽²⁾⁽⁴⁾	13.1 Gb/s	–	–	0.28	UI
D _{J13.1}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J12.5_QPLL}	Total jitter ⁽²⁾⁽⁴⁾	12.5 Gb/s	–	–	0.28	UI
D _{J12.5_QPLL}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J12.5_CPLL}	Total jitter ⁽³⁾⁽⁴⁾	12.5 Gb/s	–	–	0.33	UI
D _{J12.5_CPLL}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.17	UI
T _{J11.3_QPLL}	Total jitter ⁽²⁾⁽⁴⁾	11.3 Gb/s	–	–	0.28	UI
D _{J11.3_QPLL}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J10.3125_QPLL}	Total jitter ⁽²⁾⁽⁴⁾	10.3125 Gb/s	–	–	0.28	UI
D _{J10.3125_QPLL}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J10.3125_CPLL}	Total jitter ⁽³⁾⁽⁴⁾	10.3125 Gb/s	–	–	0.33	UI
D _{J10.3125_CPLL}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.17	UI
T _{J9.953_QPLL}	Total jitter ⁽²⁾⁽⁴⁾	9.953 Gb/s	–	–	0.28	UI
D _{J9.953_QPLL}	Deterministic jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
T _{J9.953_CPLL}	Total jitter ⁽³⁾⁽⁴⁾	9.953 Gb/s	–	–	0.33	UI
D _{J9.953_CPLL}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.17	UI
T _{J8.0}	Total jitter ⁽³⁾⁽⁴⁾	8.0 Gb/s	–	–	0.32	UI
D _{J8.0}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.17	UI
T _{J6.6}	Total jitter ⁽³⁾⁽⁴⁾	6.6 Gb/s	–	–	0.30	UI
D _{J6.6}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.15	UI
T _{J5.0}	Total jitter ⁽³⁾⁽⁴⁾	5.0 Gb/s	–	–	0.30	UI
D _{J5.0}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.15	UI
T _{J4.25}	Total jitter ⁽³⁾⁽⁴⁾	4.25 Gb/s	–	–	0.30	UI
D _{J4.25}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.15	UI

PL SYSMON I2C/PMBus Interfaces

Table 125: PL SYSMON I2C Fast Mode Interface Switching Characteristics⁽¹⁾

Symbol	Description	Min	Max	Units
T_{SMFCKL}	SCL Low time	1.3	–	μ s
T_{SMFCKH}	SCL High time	0.6	–	μ s
T_{SMFCKO}	SDAO clock-to-out delay	–	900	ns
T_{SMFDCK}	SDAI setup time	100	–	ns
F_{SMFCLK}	SCL clock frequency	–	400	kHz

Notes:

1. The test conditions are configured to the LVCMOS 1.8V I/O standard.

Table 126: PL SYSMON I2C Standard Mode Interface Switching Characteristics⁽¹⁾

Symbol	Description	Min	Max	Units
T_{SMSCKL}	SCL Low time	4.7	–	μ s
T_{SMSCKH}	SCL High time	4.0	–	μ s
T_{SMSCKO}	SDAO clock-to-out delay	–	3450	ns
T_{SMSDCK}	SDAI setup time	250	–	ns
F_{SMSCLK}	SCL clock frequency	–	100	kHz

Notes:

1. The test conditions are configured to the LVCMOS 1.8V I/O standard.

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