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Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details

Product Status	Active
Architecture	MCU, FPGA
Core Processor	Dual ARM® Cortex®-A53 MPCore™ with CoreSight™, Dual ARM®Cortex™-R5 with CoreSight™
Flash Size	-
RAM Size	256KB
Peripherals	DMA, WDT
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, MMC/SD/SDIO, SPI, UART/USART, USB OTG
Speed	533MHz, 1.3GHz
Primary Attributes	Zynq®UltraScale+™ FPGA, 504K+ Logic Cells
Operating Temperature	0°C ~ 100°C (TJ)
Package / Case	900-BBGA, FCBGA
Supplier Device Package	900-FCBGA (31x31)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xczu7cg-2fbvb900e

Table 1: **Absolute Maximum Ratings**[1] *(Cont'd)*

Symbol	Description	Min	Max	Units
Video Codec Unit				
V_{CCINT_VCU}	Internal supply voltage for the video codec unit.	−0.500	1.000	V
PL System Monitor				
V_{CCADC}	PL System Monitor supply relative to GNDADC.	0.500	2.000	V
V_{REFP}	PL System Monitor reference input relative to GNDADC.	0.500	2.000	V
Temperature				
T_{STG}	Storage temperature (ambient).	−65	150	°C
T_{SOL}	Maximum soldering temperature.[12]	–	260	°C
T_j	Maximum junction temperature.[12]	–	125	°C

Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.
2. When operating outside of the recommended operating conditions, refer to Table 6, Table 7, and Table 8 for maximum overshoot and undershoot specifications.
3. V_{CCINT_IO} must be connected to V_{CCBRAM}.
4. V_{CCAUX_IO} must be connected to V_{CCAUX}.
5. The lower absolute voltage specification always applies.
6. If V_{CCO} is 3.3V, the maximum voltage is 3.4V.
7. For I/O operation, see the *UltraScale Architecture SelectIO Resources User Guide* (UG571).
8. AC coupled operation is not supported for RX termination = floating.
9. For GTY transceivers, DC coupled operation is not supported for RX termination = GND.
10. DC coupled operation is not supported for RX termination = programmable.
11. For more information on supported GTH or GTY transceiver terminations see the *UltraScale Architecture GTH Transceiver User Guide* (UG576) or *UltraScale Architecture GTY Transceiver User Guide* (UG578).
12. For soldering guidelines and thermal considerations, see the *Zynq UltraScale+ MPSoC Packaging and Pinout Specifications* (UG1075).

Table 8: **V$_{PSIN}$ Maximum Allowed AC Voltage Overshoot and Undershoot for PS I/O Banks**[1]

AC Voltage Overshoot	% of UI at −40°C to 100°C	AC Voltage Undershoot	% of UI at −40°C to 100°C
V$_{CCO\_PSIO}$ + 0.30	100%	−0.30	100%
V$_{CCO\_PSIO}$ + 0.35	100%	−0.35	75%
V$_{CCO\_PSIO}$ + 0.40	100%	−0.40	45%
V$_{CCO\_PSIO}$ + 0.45	100%	−0.45	40%
V$_{CCO\_PSIO}$ + 0.50	75%	−0.50	10%
V$_{CCO\_PSIO}$ + 0.55	75%	−0.55	6%
V$_{CCO\_PSIO}$ + 0.60	60%	−0.60	2%
V$_{CCO\_PSIO}$ + 0.65	30%	−0.65	0%
V$_{CCO\_PSIO}$ + 0.70	20%	−0.70	0%
V$_{CCO\_PSIO}$ + 0.75	10%	−0.75	0%
V$_{CCO\_PSIO}$ + 0.80	10%	−0.80	0%
V$_{CCO\_PSIO}$ + 0.85	8%	−0.85	0%
V$_{CCO\_PSIO}$ + 0.90	6%	−0.90	0%
V$_{CCO\_PSIO}$ + 0.95	6%	−0.95	0%

Notes:
1. A total of 200 mA per bank should not be exceeded.

Table 11: **Power Supply Ramp Time** *(Cont'd)*

Symbol	Description	Min	Max	Units
T_{VCCO_PSDDR}	Ramp time from GND to 95% of V_{CCO_PSDDR}.	0.2	40	ms
$T_{VCC\_PSDDR\_PLL}$	Ramp time from GND to 95% of $V_{CC\_PSDDR\_PLL}$.	0.2	40	ms
T_{VCCO_PSIO}	Ramp time from GND to 95% of V_{CCO_PSIO}.	0.2	40	ms

DC Input and Output Levels

Values for V_{IL} and V_{IH} are recommended input voltages. Values for I_{OL} and I_{OH} are guaranteed over the recommended operating conditions at the V_{OL} and V_{OH} test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at a minimum V_{CCO} with the respective V_{OL} and V_{OH} voltage levels shown. Other standards are sample tested.

PS I/O Levels

Table 12: **PS MIO and CONFIG DC Input and Output Levels**[1]

I/O Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
LVCMOS33	−0.300	0.800	2.000	V_{CCO_PSIO}	0.40	2.40	12	−12
LVCMOS25	−0.300	0.700	1.700	V_{CCO_PSIO} + 0.30	0.70	1.70	12	−12
LVCMOS18	−0.300	35% V_{CCO_PSIO}	65% V_{CCO_PSIO}	V_{CCO_PSIO} + 0.30	0.45	V_{CCO_PSIO} − 0.45	12	−12

Notes:
1. Tested according to relevant specifications.

Table 13: **PS DDR DC Input and Output Levels**[1]

DDR Standard	V_{IL}		V_{IH}		V_{OL} [2]	V_{OH} [2]	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
DDR4	0.000	V_{REF} − 0.100	V_{REF} + 0.100	V_{CCO_PSDDR}	0.8 x V_{CCO_PSDDR} − 0.150	0.8 x V_{CCO_PSDDR} + 0.150	10	−0.1
LPDDR4	0.000	V_{REF} − 0.100	V_{REF} + 0.100	V_{CCO_PSDDR}	0.3 x V_{CCO_PSDDR} − 0.150	0.3 x V_{CCO_PSDDR} + 0.150	0.1	−10
DDR3	−0.300	V_{REF} − 0.100	V_{REF} + 0.100	V_{CCO_PSDDR}	0.5 x V_{CCO_PSDDR} − 0.175	0.5 x V_{CCO_PSDDR} + 0.175	8	−8
LPDDR3	0.000	V_{REF} − 0.100	V_{REF} + 0.100	V_{CCO_PSDDR}	0.5 x V_{CCO_PSDDR} − 0.150	0.5 x V_{CCO_PSDDR} + 0.150	8	−8
DDR3L	−0.300	V_{REF} − 0.090	V_{REF} + 0.090	V_{CCO_PSDDR}	0.5 x V_{CCO_PSDDR} − 0.150	0.5 x V_{CCO_PSDDR} + 0.150	8	−8

Notes:
1. Tested according to relevant specifications.
2. DDR4 V_{OL}/V_{OH} specifications are only applicable for DQ/DQS pins.

Table 26: **Speed Grade Designations by Device** *(Cont'd)*

Device	Speed Grade, Temperature Ranges, and V_{CCINT} Operating Voltages		
	Advance	**Preliminary**	**Production**
XCZU11EG	-3E (V_{CCINT} = 0.90V), -2E (V_{CCINT} = 0.85V) -2I (V_{CCINT} = 0.85V), -2LE (V_{CCINT} = 0.85V) -1E (V_{CCINT} = 0.85V), -1I (V_{CCINT} = 0.85V) -1LI (V_{CCINT} = 0.85V) -2LE (V_{CCINT} = 0.72V), -1LI (V_{CCINT} = 0.72V)		
XCZU15EG	-3E (V_{CCINT} = 0.90V), -2E (V_{CCINT} = 0.85V) -2I (V_{CCINT} = 0.85V), -2LE (V_{CCINT} = 0.85V) -1E (V_{CCINT} = 0.85V), -1I (V_{CCINT} = 0.85V) -1LI (V_{CCINT} = 0.85V) -2LE (V_{CCINT} = 0.72V), -1LI (V_{CCINT} = 0.72V)		
XCZU17EG	-3E (V_{CCINT} = 0.90V), -2E (V_{CCINT} = 0.85V) -2I (V_{CCINT} = 0.85V), -2LE (V_{CCINT} = 0.85V) -1E (V_{CCINT} = 0.85V), -1I (V_{CCINT} = 0.85V) -1LI (V_{CCINT} = 0.85V) -2LE (V_{CCINT} = 0.72V), -1LI (V_{CCINT} = 0.72V)		
XCZU19EG	-3E (V_{CCINT} = 0.90V), -2E (V_{CCINT} = 0.85V) -2I (V_{CCINT} = 0.85V), -2LE (V_{CCINT} = 0.85V) -1E (V_{CCINT} = 0.85V), -1I (V_{CCINT} = 0.85V) -1LI (V_{CCINT} = 0.85V) -2LE (V_{CCINT} = 0.72V), -1LI (V_{CCINT} = 0.72V)		

Notes:

1. The lowest power -1L and -2L devices, where V_{CCINT} = 0.72V, are listed in the Vivado Design Suite as -1LV and -2LV respectively.

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Table 30: **PS DDR Performance** *(Cont'd)*

Memory Standard	Package	DRAM Type	Speed Grade						Units
			-3		-2		-1		
			Min	Max	Min	Max	Min	Max	
DDR3	All FFV packages, FBVB900 and SFVC784	Single rank component	664	2133	664	2133	664	2133	Mb/s
		1 rank DIMM[1][2]	664	1866	664	1866	664	1866	Mb/s
		2 rank DIMM[1][3]	664	1600	664	1600	664	1600	Mb/s
	SFVA625	Single rank component	664	1866	664	1866	664	1866	Mb/s
		1 rank DIMM[1][2]	664	1600	664	1600	664	1600	Mb/s
		2 rank DIMM[1][3]	664	1333	664	1333	664	1333	Mb/s
	SBVA484	Single rank component	664	1066	664	1066	664	1066	Mb/s
		1 rank DIMM[1][2]	664	1066	664	1066	664	1066	Mb/s
		2 rank DIMM[1][3]	664	1066	664	1066	664	1066	Mb/s
DDR3L	All FFV packages, FBVB900 and SFVC784	Single rank component	664	1866	664	1866	664	1866	Mb/s
		1 rank DIMM[1][2]	664	1600	664	1600	664	1600	Mb/s
		2 rank DIMM[1][3]	664	1333	664	1333	664	1333	Mb/s
	SFVA625	Single rank component	664	1600	664	1600	664	1600	Mb/s
		1 rank DIMM[1][2]	664	1333	664	1333	664	1333	Mb/s
		2 rank DIMM[1][3]	664	1066	664	1066	664	1066	Mb/s
	SBVA484	Single rank component	664	1066	664	1066	664	1066	Mb/s
		1 rank DIMM[1][2]	664	1066	664	1066	664	1066	Mb/s
		2 rank DIMM[1][3]	664	1066	664	1066	664	1066	Mb/s
LPDDR3	All FFV packages, FBVB900 and SFVC784	Single die package[6]	664	1600	664	1600	664	1600	Mb/s
		Dual die package[6]	664	1333	664	1333	664	1333	Mb/s
	SFVA625	Single die package[6]	664	1333	664	1333	664	1333	Mb/s
		Dual die package[6]	664	1066	664	1066	664	1066	Mb/s
	SBVA484	Single die package[6]	664	1066	664	1066	664	1066	Mb/s
		Dual die package[6]	664	1066	664	1066	664	1066	Mb/s

Notes:
1. Dual in-line memory module (DIMM) includes RDIMM, SODIMM, and UDIMM.
2. Includes: 1 rank 1 slot, dual-die package 2 rank.
3. Includes: 2 rank 1 slot.
4. Dual die package includes single die with ECC.
5. LPDDR4 support is only available as a 32-bit interface.
6. 64-bit LPDDR3 interface performance values are defined without ECC support.

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PS Switching Characteristics

PS Clocks

Table 34: **PS Reference Clock Requirements**[1]

Symbol	Description	Min	Typ	Max	Units
$T_{RMSJPSCLK}$	PS_REF_CLK input RMS clock jitter.	–	–	3	ps
$T_{PJPSCLK}$	PS_REF_CLK input period jitter (peak-to-peak). Number of clock cycles = 10,000	–	–	50	ps
$T_{DCPSCLK}$	PS_REF_CLK duty cycle.	45	–	55	%
$T_{RFPSCLK}$	PS_REF_CLK rise time (20%–80%) and fall time (80%–20%).	–	–	2.22	ns
F_{PSCLK}	PS_REF_CLK frequency.	27	–	60	MHz

Notes:
1. The values in this table are applicable to alternative PS reference clock inputs ALT_REF_CLK, AUX_REF_CLK, and VIDEO_CLK.

Table 35: **PS RTC Crystal Requirements**[1]

Symbol	Description	Min	Typ	Max	Units
F_{XTAL}	Parallel resonance crystal frequency.	–	32.8	–	KHz
T_{FTXTAL}	Frequency tolerance.	–20	–	20	ppm
C_{XTAL}	Load capacitance for crystal parallel resonance.	–	12.5	–	pF
R_{ESR}	Crystal ESR (16.8 and 19.2 MHz).	–	70	–	KΩ
C_{SHUNT}	Crystal shunt capacitance.	–	1.4	–	pF

Notes:
1. Required board components: Feedback resistor = 4.7 MΩ, PCB and pad capacitance = 1.5 pF, C_1 and C_2 capacitance = 21 pF.

Table 36: **PS PLL Switching Characteristics**

Symbol	Description	Speed Grade			Units
		-3	**-2**	**-1**	
$F_{LOCKPSPLL}$	PLL maximum lock time.	100	100	100	μs
$F_{PSPLLMAX}$	PLL maximum output frequency.	1600	1600	1600	MHz
$F_{PSPLLMIN}$	PLL minimum output frequency.	750	750	750	MHz
$F_{PSPLLVCOMAX}$	PLL maximum VCO frequency.	3000	3000	3000	MHz
$F_{PSPLLVCOMIN}$	PLL minimum VCO frequency.	1500	1500	1500	MHz

PS Configuration

Table 39: **Processor Configuration Access Port Switching Characteristics**

| Symbol | Description | Speed Grade and V_{CCINT} Operating Voltages | | | | | Units |
| | | 0.90V | 0.85V | | 0.72V | | |
		-3	-2	-1	-2	-1	
F_{PCAPCK}	Maximum processor configuration access port (PCAP) frequency.	200	200	200	150	150	MHz

Table 40: **Boundary-Scan Port Switching Characteristics**

| Symbol | Description | Speed Grade and V_{CCINT} Operating Voltages | | | | | Units |
| | | 0.90V | 0.85V | | 0.72V | | |
		-3	-2	-1	-2	-1	
F_{TCK}	JTAG clock maximum frequency.	25	25	25	15	15	MHz
T_{TAPTCK}/T_{TCKTAP}	TMS and TDI setup and hold.	4.0/2.0	4.0/2.0	4.0/2.0	5.0/2.0	5.0/2.0	ns, Min
T_{TCKTDO}	TCK falling edge to TDO output.	16.1	16.1	16.1	24	24	ns, Max

Notes:

1. The test conditions are configured to the LVCMOS 3.3V I/O standard with a 12 mA drive strength.

PS I2C Controller Interface

Table 47: **I2C Interface**[1]

Symbol	Description	Min	Max	Units
I2C Fast-mode Interface				
$T_{I2CFCKL}$	SCL Low time.	1.3	–	µs
$T_{I2CFCKH}$	SCL High time.	0.6	–	µs
$T_{I2CFCKO}$	SDA clock to out delay.	–	900	ns
$T_{I2CFDCK}$	SDA input setup time.	100	–	ns
$F_{I2CFCLK}$	SCL clock frequency.	–	400	KHz
I2C Standard-mode Interface				
$T_{I2CSCKL}$	SCL Low time.	4.7	–	µs
$T_{I2CSCKH}$	SCL High time.	4.0	–	µs
$T_{I2CSCKO}$	SDA clock to out delay.	–	3450	ns
$T_{I2CSDCK}$	SDA input setup time.	250	–	ns
$F_{I2CSCLK}$	SCL clock frequency.	–	100	KHz

Notes:

1. The test conditions are configured to the LVCMOS 3.3V I/O standard with a 12 mA drive strength, fast slew rate, and a 15 pF load.

Table 74: **Maximum Physical Interface (PHY) Rate for Memory Interfaces** *(Cont'd)*

Memory Standard	Package[1]	DRAM Type	Speed Grade and V_{CCINT} Operating Voltages					Units
			0.90V	0.85V		0.72V		
			-3	-2	-1	-2	-1	
DDR3L	All FFV packages and FBVB900	Single rank component	1866	1866	1866	1866	1600	Mb/s
		1 rank DIMM[2][3]	1600	1600	1600	1600	1333	Mb/s
		2 rank DIMM[2][5]	1333	1333	1333	1333	1066	Mb/s
		4 rank DIMM[2][6]	800	800	800	800	606	Mb/s
	SFVC784	Single rank component	1600	1600	1600	1600	1600	Mb/s
		1 rank DIMM[2][3]	1600	1600	1600	1600	1333	Mb/s
		2 rank DIMM[2][5]	1333	1333	1333	1333	1066	Mb/s
		4 rank DIMM[2][6]	800	800	800	800	606	Mb/s
QDR II+	All	Single rank component[7]	633	633	600	600	550	MHz
RLDRAM 3	All FFV packages and FBVB900	Single rank component	1200	1200	1066	1066	933	MHz
	SFVC784	Single rank component	1066	1066	933	933	800	MHz
QDR IV XP	All	Single rank component	1066	1066	1066	933	933	MHz
LPDDR3	All	Single rank component	1600	1600	1600	1600	1600	Mb/s

Notes:
1. The SBVA484 and SFVA625 packages do not support the PL memory interfaces.
2. Dual in-line memory module (DIMM) includes RDIMM, SODIMM, UDIMM, and LRDIMM.
3. Includes: 1 rank 1 slot, DDP 2 rank, LRDIMM 2 or 4 rank 1 slot.
4. For the DDR4 DDP components at -3 and -2 speed grades and V_{CCINT} = 0.85V, the maximum data rate is 2133 Mb/s for six or more DDP devices. For five or less DDP devices, use the single rank DIMM data rates for the -3 and -2 speed grades at 0.85V.
5. Includes: 2 rank 1 slot, 1 rank 2 slot, LRDIMM 2 rank 2 slot.
6. Includes: 2 rank 2 slot, 4 rank 1 slot.
7. The QDRII+ performance specifications are for burst-length 4 (BL = 4) implementations.

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Table 76: **IOB High Performance (HP) Switching Characteristics** *(Cont'd)*

I/O Standards	$T_{INBUF\_DELAY\_PAD\_I}$					$T_{OUTBUF\_DELAY\_O\_PAD}$					$T_{OUTBUF\_DELAY\_TD\_PAD}$					Units
	0.90V	0.85V		0.72V		0.90V	0.85V		0.72V		0.90V	0.85V		0.72V		
	-3	-2	-1	-2	-1	-3	-2	-1	-2	-1	-3	-2	-1	-2	-1	
DIFF_SSTL12_F	0.394	0.394	0.402	0.394	0.402	0.412	0.412	0.430	0.412	0.430	0.538	0.538	0.566	0.538	0.566	ns
DIFF_SSTL12_M	0.394	0.394	0.402	0.394	0.402	0.553	0.553	0.584	0.553	0.584	0.641	0.641	0.676	0.641	0.676	ns
DIFF_SSTL12_S	0.394	0.394	0.402	0.394	0.402	0.758	0.758	0.808	0.758	0.808	0.823	0.823	0.879	0.823	0.879	ns
DIFF_SSTL135_DCI_F	0.371	0.371	0.402	0.371	0.402	0.411	0.411	0.428	0.411	0.428	0.537	0.537	0.565	0.537	0.565	ns
DIFF_SSTL135_DCI_M	0.371	0.371	0.402	0.371	0.402	0.551	0.551	0.582	0.551	0.582	0.645	0.645	0.685	0.645	0.685	ns
DIFF_SSTL135_DCI_S	0.371	0.371	0.402	0.371	0.402	0.746	0.746	0.799	0.746	0.799	0.829	0.829	0.893	0.829	0.893	ns
DIFF_SSTL135_F	0.375	0.375	0.402	0.375	0.402	0.408	0.408	0.428	0.408	0.428	0.528	0.528	0.561	0.528	0.561	ns
DIFF_SSTL135_M	0.375	0.375	0.402	0.375	0.402	0.555	0.555	0.585	0.555	0.585	0.641	0.641	0.679	0.641	0.679	ns
DIFF_SSTL135_S	0.375	0.375	0.402	0.375	0.402	0.772	0.772	0.823	0.772	0.823	0.827	0.827	0.878	0.827	0.878	ns
DIFF_SSTL15_DCI_F	0.397	0.397	0.417	0.397	0.417	0.412	0.412	0.429	0.412	0.429	0.531	0.531	0.563	0.531	0.563	ns
DIFF_SSTL15_DCI_M	0.397	0.397	0.417	0.397	0.417	0.553	0.553	0.583	0.553	0.583	0.645	0.645	0.685	0.645	0.685	ns
DIFF_SSTL15_DCI_S	0.397	0.397	0.417	0.397	0.417	0.768	0.768	0.822	0.768	0.822	0.847	0.847	0.912	0.847	0.912	ns
DIFF_SSTL15_F	0.404	0.404	0.417	0.404	0.417	0.424	0.424	0.445	0.424	0.445	0.551	0.551	0.577	0.551	0.577	ns
DIFF_SSTL15_M	0.404	0.404	0.417	0.404	0.417	0.554	0.554	0.585	0.554	0.585	0.639	0.639	0.677	0.639	0.677	ns
DIFF_SSTL15_S	0.404	0.404	0.417	0.404	0.417	0.767	0.767	0.817	0.767	0.817	0.813	0.813	0.867	0.813	0.867	ns
DIFF_SSTL18_I_DCI_F	0.320	0.320	0.336	0.320	0.336	0.445	0.445	0.461	0.445	0.461	0.566	0.566	0.595	0.566	0.595	ns
DIFF_SSTL18_I_DCI_M	0.320	0.320	0.336	0.320	0.336	0.554	0.554	0.585	0.554	0.585	0.644	0.644	0.683	0.644	0.683	ns
DIFF_SSTL18_I_DCI_S	0.320	0.320	0.336	0.320	0.336	0.762	0.762	0.818	0.762	0.818	0.837	0.837	0.899	0.837	0.899	ns
DIFF_SSTL18_I_F	0.316	0.316	0.336	0.316	0.336	0.454	0.454	0.476	0.454	0.476	0.578	0.578	0.608	0.578	0.608	ns
DIFF_SSTL18_I_M	0.316	0.316	0.336	0.316	0.336	0.571	0.571	0.603	0.571	0.603	0.652	0.652	0.692	0.652	0.692	ns
DIFF_SSTL18_I_S	0.316	0.316	0.336	0.316	0.336	0.782	0.782	0.835	0.782	0.835	0.816	0.816	0.870	0.816	0.870	ns
HSLVDCI_15_F	0.393	0.393	0.415	0.393	0.415	0.425	0.425	0.443	0.425	0.443	0.548	0.548	0.579	0.548	0.579	ns
HSLVDCI_15_M	0.393	0.393	0.415	0.393	0.415	0.552	0.552	0.581	0.552	0.581	0.644	0.644	0.684	0.644	0.684	ns
HSLVDCI_15_S	0.393	0.393	0.415	0.393	0.415	0.748	0.748	0.802	0.748	0.802	0.827	0.827	0.890	0.827	0.890	ns
HSLVDCI_18_F	0.424	0.424	0.447	0.424	0.447	0.445	0.445	0.461	0.445	0.461	0.566	0.566	0.595	0.566	0.595	ns
HSLVDCI_18_M	0.424	0.424	0.447	0.424	0.447	0.567	0.567	0.598	0.567	0.598	0.658	0.658	0.699	0.658	0.699	ns
HSLVDCI_18_S	0.424	0.424	0.447	0.424	0.447	0.761	0.761	0.817	0.761	0.817	0.836	0.836	0.900	0.836	0.900	ns
HSTL_I_12_F	0.378	0.378	0.399	0.378	0.399	0.423	0.423	0.443	0.423	0.443	0.553	0.553	0.582	0.553	0.582	ns
HSTL_I_12_M	0.378	0.378	0.399	0.378	0.399	0.551	0.551	0.582	0.551	0.582	0.642	0.642	0.679	0.642	0.679	ns
HSTL_I_12_S	0.378	0.378	0.399	0.378	0.399	0.750	0.750	0.799	0.750	0.799	0.813	0.813	0.868	0.813	0.868	ns
HSTL_I_18_F	0.322	0.322	0.339	0.322	0.339	0.456	0.456	0.474	0.456	0.474	0.576	0.576	0.606	0.576	0.606	ns
HSTL_I_18_M	0.322	0.322	0.339	0.322	0.339	0.569	0.569	0.602	0.569	0.602	0.653	0.653	0.692	0.653	0.692	ns
HSTL_I_18_S	0.322	0.322	0.339	0.322	0.339	0.781	0.781	0.833	0.781	0.833	0.816	0.816	0.871	0.816	0.871	ns
HSTL_I_DCI_12_F	0.378	0.378	0.399	0.378	0.399	0.406	0.406	0.429	0.406	0.429	0.534	0.534	0.564	0.534	0.564	ns
HSTL_I_DCI_12_M	0.378	0.378	0.399	0.378	0.399	0.556	0.556	0.586	0.556	0.586	0.654	0.654	0.694	0.654	0.694	ns
HSTL_I_DCI_12_S	0.378	0.378	0.399	0.378	0.399	0.754	0.754	0.803	0.754	0.803	0.842	0.842	0.907	0.842	0.907	ns
HSTL_I_DCI_18_F	0.321	0.321	0.339	0.321	0.339	0.445	0.445	0.461	0.445	0.461	0.566	0.566	0.595	0.566	0.595	ns
HSTL_I_DCI_18_M	0.321	0.321	0.339	0.321	0.339	0.554	0.554	0.585	0.554	0.585	0.643	0.643	0.684	0.643	0.684	ns
HSTL_I_DCI_18_S	0.321	0.321	0.339	0.321	0.339	0.761	0.761	0.817	0.761	0.817	0.836	0.836	0.900	0.836	0.900	ns
HSTL_I_DCI_F	0.393	0.393	0.415	0.393	0.415	0.431	0.431	0.445	0.431	0.445	0.555	0.555	0.575	0.555	0.575	ns
HSTL_I_DCI_M	0.393	0.393	0.415	0.393	0.415	0.552	0.552	0.581	0.552	0.581	0.644	0.644	0.684	0.644	0.684	ns

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Table 76: **IOB High Performance (HP) Switching Characteristics** *(Cont'd)*

I/O Standards	$T_{INBUF\_DELAY\_PAD\_I}$					$T_{OUTBUF\_DELAY\_O\_PAD}$					$T_{OUTBUF\_DELAY\_TD\_PAD}$					Units
	0.90V	0.85V		0.72V		0.90V	0.85V		0.72V		0.90V	0.85V		0.72V		
	-3	-2	-1	-2	-1	-3	-2	-1	-2	-1	-3	-2	-1	-2	-1	
HSTL_I_DCI_S	0.393	0.393	0.415	0.393	0.415	0.766	0.766	0.821	0.766	0.821	0.847	0.847	0.912	0.847	0.912	ns
HSTL_I_F	0.378	0.378	0.399	0.378	0.399	0.423	0.423	0.443	0.423	0.443	0.549	0.549	0.581	0.549	0.581	ns
HSTL_I_M	0.378	0.378	0.399	0.378	0.399	0.554	0.554	0.585	0.554	0.585	0.640	0.640	0.677	0.640	0.677	ns
HSTL_I_S	0.378	0.378	0.399	0.378	0.399	0.766	0.766	0.816	0.766	0.816	0.811	0.811	0.866	0.811	0.866	ns
HSUL_12_DCI_F	0.378	0.378	0.399	0.378	0.399	0.425	0.425	0.443	0.425	0.443	0.558	0.558	0.586	0.558	0.586	ns
HSUL_12_DCI_M	0.378	0.378	0.399	0.378	0.399	0.556	0.556	0.586	0.556	0.586	0.654	0.654	0.694	0.654	0.694	ns
HSUL_12_DCI_S	0.378	0.378	0.399	0.378	0.399	0.736	0.736	0.784	0.736	0.784	0.821	0.821	0.886	0.821	0.886	ns
HSUL_12_F	0.378	0.378	0.399	0.378	0.399	0.412	0.412	0.430	0.412	0.430	0.538	0.538	0.566	0.538	0.566	ns
HSUL_12_M	0.378	0.378	0.399	0.378	0.399	0.551	0.551	0.582	0.551	0.582	0.642	0.642	0.679	0.642	0.679	ns
HSUL_12_S	0.378	0.378	0.399	0.378	0.399	0.750	0.750	0.799	0.750	0.799	0.813	0.813	0.868	0.813	0.868	ns
LVCMOS12_F_2	0.512	0.512	0.555	0.512	0.555	0.672	0.672	0.692	0.672	0.692	0.898	0.898	0.922	0.898	0.922	ns
LVCMOS12_F_4	0.512	0.512	0.555	0.512	0.555	0.504	0.504	0.521	0.504	0.521	0.664	0.664	0.693	0.664	0.693	ns
LVCMOS12_F_6	0.512	0.512	0.555	0.512	0.555	0.485	0.485	0.507	0.485	0.507	0.634	0.634	0.669	0.634	0.669	ns
LVCMOS12_F_8	0.512	0.512	0.555	0.512	0.555	0.465	0.465	0.489	0.465	0.489	0.611	0.611	0.666	0.611	0.666	ns
LVCMOS12_M_2	0.512	0.512	0.555	0.512	0.555	0.708	0.708	0.727	0.708	0.727	0.916	0.916	0.945	0.916	0.945	ns
LVCMOS12_M_4	0.512	0.512	0.555	0.512	0.555	0.550	0.550	0.573	0.550	0.573	0.664	0.664	0.690	0.664	0.690	ns
LVCMOS12_M_6	0.512	0.512	0.555	0.512	0.555	0.527	0.527	0.554	0.527	0.554	0.622	0.622	0.652	0.622	0.652	ns
LVCMOS12_M_8	0.512	0.512	0.555	0.512	0.555	0.540	0.540	0.571	0.540	0.571	0.614	0.614	0.649	0.614	0.649	ns
LVCMOS12_S_2	0.512	0.512	0.555	0.512	0.555	0.767	0.767	0.803	0.767	0.803	0.990	0.990	1.024	0.990	1.024	ns
LVCMOS12_S_4	0.512	0.512	0.555	0.512	0.555	0.666	0.666	0.704	0.666	0.704	0.803	0.803	0.848	0.803	0.848	ns
LVCMOS12_S_6	0.512	0.512	0.555	0.512	0.555	0.657	0.657	0.695	0.657	0.695	0.732	0.732	0.774	0.732	0.774	ns
LVCMOS12_S_8	0.512	0.512	0.555	0.512	0.555	0.708	0.708	0.761	0.708	0.761	0.745	0.745	0.790	0.745	0.790	ns
LVCMOS15_F_12	0.414	0.414	0.445	0.414	0.445	0.500	0.500	0.522	0.500	0.522	0.647	0.647	0.682	0.647	0.682	ns
LVCMOS15_F_2	0.414	0.414	0.445	0.414	0.445	0.702	0.702	0.722	0.702	0.722	0.919	0.919	0.940	0.919	0.940	ns
LVCMOS15_F_4	0.414	0.414	0.445	0.414	0.445	0.579	0.579	0.601	0.579	0.601	0.755	0.755	0.781	0.755	0.781	ns
LVCMOS15_F_6	0.414	0.414	0.445	0.414	0.445	0.547	0.547	0.569	0.547	0.569	0.711	0.711	0.742	0.711	0.742	ns
LVCMOS15_F_8	0.414	0.414	0.445	0.414	0.445	0.518	0.518	0.538	0.518	0.538	0.686	0.686	0.703	0.686	0.703	ns
LVCMOS15_M_12	0.414	0.414	0.445	0.414	0.445	0.607	0.607	0.644	0.607	0.644	0.637	0.637	0.676	0.637	0.676	ns
LVCMOS15_M_2	0.414	0.414	0.445	0.414	0.445	0.741	0.741	0.770	0.741	0.770	0.938	0.938	0.962	0.938	0.962	ns
LVCMOS15_M_4	0.414	0.414	0.445	0.414	0.445	0.625	0.625	0.651	0.625	0.651	0.754	0.754	0.786	0.754	0.786	ns
LVCMOS15_M_6	0.414	0.414	0.445	0.414	0.445	0.576	0.576	0.604	0.576	0.604	0.674	0.674	0.710	0.674	0.710	ns
LVCMOS15_M_8	0.414	0.414	0.445	0.414	0.445	0.568	0.568	0.601	0.568	0.601	0.639	0.639	0.681	0.639	0.681	ns
LVCMOS15_S_12	0.414	0.414	0.445	0.414	0.445	0.788	0.788	0.855	0.788	0.855	0.695	0.695	0.733	0.695	0.733	ns
LVCMOS15_S_2	0.414	0.414	0.445	0.414	0.445	0.829	0.829	0.864	0.829	0.864	1.039	1.039	1.079	1.039	1.079	ns
LVCMOS15_S_4	0.414	0.414	0.445	0.414	0.445	0.687	0.687	0.725	0.687	0.725	0.813	0.813	0.851	0.813	0.851	ns
LVCMOS15_S_6	0.414	0.414	0.445	0.414	0.445	0.671	0.671	0.710	0.671	0.710	0.726	0.726	0.763	0.726	0.763	ns
LVCMOS15_S_8	0.414	0.414	0.445	0.414	0.445	0.704	0.704	0.755	0.704	0.755	0.721	0.721	0.758	0.721	0.758	ns
LVCMOS18_F_12	0.418	0.418	0.445	0.418	0.445	0.573	0.573	0.601	0.573	0.601	0.731	0.731	0.769	0.731	0.769	ns
LVCMOS18_F_2	0.418	0.418	0.445	0.418	0.445	0.739	0.739	0.760	0.739	0.760	0.945	0.945	0.971	0.945	0.971	ns
LVCMOS18_F_4	0.418	0.418	0.445	0.418	0.445	0.609	0.609	0.630	0.609	0.630	0.778	0.778	0.802	0.778	0.802	ns
LVCMOS18_F_6	0.418	0.418	0.445	0.418	0.445	0.603	0.603	0.633	0.603	0.633	0.781	0.781	0.808	0.781	0.808	ns

Input Delay Measurement Methodology

Table 78 shows the test setup parameters used for measuring input delay.

Table 78: **Input Delay Measurement Methodology**

Description	I/O Standard Attribute	V_L [1][2]	V_H [1][2]	V_{MEAS} [1][4][6]	V_{REF} [1][3][5]
LVCMOS, 1.2V	LVCMOS12	0.1	1.1	0.6	–
LVCMOS, LVDCI, HSLVDCI, 1.5V	LVCMOS15, LVDCI_15, HSLVDCI_15	0.1	1.4	0.75	–
LVCMOS, LVDCI, HSLVDCI, 1.8V	LVCMOS18, LVDCI_18, HSLVDCI_18	0.1	1.7	0.9	–
LVCMOS, 2.5V	LVCMOS25	0.1	2.4	1.25	–
LVCMOS, 3.3V	LVCMOS33	0.1	3.2	1.65	–
LVTTL, 3.3V	LVTTL	0.1	3.2	1.65	–
HSTL (high-speed transceiver logic), class I, 1.2V	HSTL_I_12	$V_{REF} - 0.25$	$V_{REF} + 0.25$	V_{REF}	0.6
HSTL, class I, 1.5V	HSTL_I	$V_{REF} - 0.325$	$V_{REF} + 0.325$	V_{REF}	0.75
HSTL, class I, 1.8V	HSTL_I_18	$V_{REF} - 0.4$	$V_{REF} + 0.4$	V_{REF}	0.9
HSUL (high-speed unterminated logic), 1.2V	HSUL_12	$V_{REF} - 0.25$	$V_{REF} + 0.25$	V_{REF}	0.6
SSTL12 (stub series terminated logic), 1.2V	SSTL12	$V_{REF} - 0.25$	$V_{REF} + 0.25$	V_{REF}	0.6
SSTL135 and SSTL135 class II, 1.35V	SSTL135, SSTL135_II	$V_{REF} - 0.2875$	$V_{REF} + 0.2875$	V_{REF}	0.675
SSTL15 and SSTL15 class II, 1.5V	SSTL15, SSTL15_II	$V_{REF} - 0.325$	$V_{REF} + 0.325$	V_{REF}	0.75
SSTL18, class I and II, 1.8V	SSTL18_I, SSTL18_II	$V_{REF} - 0.4$	$V_{REF} + 0.4$	V_{REF}	0.9
POD10, 1.0V	POD10	$V_{REF} - 0.2$	$V_{REF} + 0.2$	V_{REF}	0.7
POD12, 1.2V	POD12	$V_{REF} - 0.24$	$V_{REF} + 0.24$	V_{REF}	0.84
DIFF_HSTL, class I, 1.2V	DIFF_HSTL_I_12	$0.6 - 0.25$	$0.6 + 0.25$	0 [6]	–
DIFF_HSTL, class I, 1.5V	DIFF_HSTL_I	$0.75 - 0.325$	$0.75 + 0.325$	0 [6]	–
DIFF_HSTL, class I, 1.8V	DIFF_HSTL_I_18	$0.9 - 0.4$	$0.9 + 0.4$	0 [6]	–
DIFF_HSUL, 1.2V	DIFF_HSUL_12	$0.6 - 0.25$	$0.6 + 0.25$	0 [6]	–
DIFF_SSTL, 1.2V	DIFF_SSTL12	$0.6 - 0.25$	$0.6 + 0.25$	0 [6]	–
DIFF_SSTL135 and DIFF_SSTL135 class II, 1.35V	DIFF_SSTL135, DIFF_SSTL135_II	$0.675 - 0.2875$	$0.675 + 0.2875$	0 [6]	–
DIFF_SSTL15 and DIFF_SSTL15 class II, 1.5V	DIFF_SSTL15, DIFF_SSTL15_II	$0.75 - 0.325$	$0.75 + 0.325$	0 [6]	–
DIFF_SSTL18_I, DIFF_SSTL18_II, 1.8V	DIFF_SSTL18_I, DIFF_SSTL18_II	$0.9 - 0.4$	$0.9 + 0.4$	0 [6]	–
DIFF_POD10, 1.0V	DIFF_POD10	$0.5 - 0.2$	$0.5 + 0.2$	0 [6]	–
DIFF_POD12, 1.2V	DIFF_POD12	$0.6 - 0.25$	$0.6 + 0.25$	0 [6]	–
LVDS (low-voltage differential signaling), 1.8V	LVDS	$0.9 - 0.125$	$0.9 + 0.125$	0 [6]	–
LVDS_25, 2.5V	LVDS_25	$1.25 - 0.125$	$1.25 + 0.125$	0 [6]	–

GTH Transceiver Switching Characteristics

Consult the *UltraScale Architecture GTH Transceiver User Guide* (UG576) for further information.

Table 97: **GTH Transceiver Performance**

Symbol	Description	Output Divider	Speed Grade and V_{CCINT} Operating Voltages										Units
			0.90V		**0.85V**				**0.72V**				
			-3		**-2**		**-1**		**-2**		**-1**		
F_{GTHMAX}	GTH maximum line rate.		16.375[1]		16.375[1]		12.5		12.5		10.3125		Gb/s
F_{GTHMIN}	GTH minimum line rate.		0.5		0.5		0.5		0.5		0.5		Gb/s
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
$F_{GTHCRANGE}$	CPLL line rate range[2].	1	4	12.5	4	12.5	4	8.5	4	8.5	4	8.5	Gb/s
		2	2	6.25	2	6.25	2	4.25	2	4.25	2	4.25	Gb/s
		4	1	3.125	1	3.125	1	2.125	1	2.125	1	2.125	Gb/s
		8	0.5	1.5625	0.5	1.5625	0.5	1.0625	0.5	1.0625	0.5	1.0625	Gb/s
		16	N/A										Gb/s
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
$F_{GTHQRANGE1}$	QPLL0 line rate range[3].	1	9.8	16.375	9.8	16.375	9.8	12.5	9.8	12.5	9.8	10.3125	Gb/s
		2	4.9	8.1875	4.9	8.1875	4.9	8.15	4.9	8.1875	4.9	8.15	Gb/s
		4	2.45	4.0938	2.45	4.0938	2.45	4.075	2.45	4.0938	2.45	4.075	Gb/s
		8	1.225	2.0469	1.225	2.0469	1.225	2.0375	1.225	2.0469	1.225	2.0375	Gb/s
		16	0.6125	1.0234	0.6125	1.0234	0.6125	1.0188	0.6125	1.0234	0.6125	1.0188	Gb/s
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
$F_{GTHQRANGE2}$	QPLL1 line rate range[4].	1	8.0	13.0	8.0	13.0	8.0	12.5	8.0	12.5	8.0	10.3125	Gb/s
		2	4.0	6.5	4.0	6.5	4.0	6.5	4.0	6.5	4.0	6.5	Gb/s
		4	2.0	3.25	2.0	3.25	2.0	3.25	2.0	3.25	2.0	3.25	Gb/s
		8	1.0	1.625	1.0	1.625	1.0	1.625	1.0	1.625	1.0	1.625	Gb/s
		16	0.5	0.8125	0.5	0.8125	0.5	0.8125	0.5	0.8125	0.5	0.8125	Gb/s
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
$F_{CPLLRANGE}$	CPLL frequency range.		2	6.25	2	6.25	2	4.25	2	4.25	2	4.25	GHz
$F_{QPLL0RANGE}$	QPLL0 frequency range.		9.8	16.375	9.8	16.375	9.8	16.375	9.8	16.375	9.8	16.375	GHz
$F_{QPLL1RANGE}$	QPLL1 frequency range.		8	13	8	13	8	13	8	13	8	13	GHz

Notes:
1. GTH transceiver line rates in the SFVC784 package support data rates up to 12.5 Gb/s.
2. The values listed are the rounded results of the calculated equation (2 x CPLL_Frequency)/Output_Divider.
3. The values listed are the rounded results of the calculated equation (QPLL0_Frequency)/Output_Divider.
4. The values listed are the rounded results of the calculated equation (QPLL1_Frequency)/Output_Divider.

Table 98: **GTH Transceiver Dynamic Reconfiguration Port (DRP) Switching Characteristics**

Symbol	Description	All Speed Grades	Units
$F_{GTHDRPCLK}$	GTHDRPCLK maximum frequency.	250	MHz

Table 102: **GTH Transceiver User Clock Switching Characteristics**[1] *(Cont'd)*

Symbol	Description	Data Width Conditions (Bit)		Speed Grade and V_{CCINT} Operating Voltages					Units
				0.90V	0.85V		0.72V		
		Internal Logic	Interconnect Logic	-3[2]	-2[2][3]	-1[4][5]	-2[3]	-1[5]	
$F_{TXOUTPROGDIV}$	TXOUTCLK maximum frequency sourced from TXPROGDIVCLK			511.719	511.719	511.719	511.719	511.719	MHz
$F_{RXOUTPROGDIV}$	RXOUTCLK maximum frequency sourced from RXPROGDIVCLK			511.719	511.719	511.719	511.719	511.719	MHz
F_{TXIN}	TXUSRCLK[6] maximum frequency	16	16, 32	511.719	511.719	390.625	390.625	322.266	MHz
		32	32, 64	511.719	511.719	390.625	390.625	322.266	MHz
		20	20, 40	409.375	409.375	312.500	312.500	257.813	MHz
		40	40, 80	409.375	409.375	312.500	312.500	257.813	MHz
F_{RXIN}	RXUSRCLK[6] maximum frequency	16	16, 32	511.719	511.719	390.625	390.625	322.266	MHz
		32	32, 64	511.719	511.719	390.625	390.625	322.266	MHz
		20	20, 40	409.375	409.375	312.500	312.500	257.813	MHz
		40	40, 80	409.375	409.375	312.500	312.500	257.813	MHz
F_{TXIN2}	TXUSRCLK2[6] maximum frequency	16	16	511.719	511.719	390.625	390.625	322.266	MHz
		16	32	255.859	255.859	195.313	195.313	161.133	MHz
		32	32	511.719	511.719	390.625	390.625	322.266	MHz
		32	64	255.859	255.859	195.313	195.313	161.133	MHz
		20	20	409.375	409.375	312.500	312.500	257.813	MHz
		20	40	204.688	204.688	156.250	156.250	128.906	MHz
		40	40	409.375	409.375	312.500	312.500	257.813	MHz
		40	80	204.688	204.688	156.250	156.250	128.906	MHz
F_{RXIN2}	RXUSRCLK2[6] maximum frequency	16	16	511.719	511.719	390.625	390.625	322.266	MHz
		16	32	255.859	255.859	195.313	195.313	161.133	MHz
		32	32	511.719	511.719	390.625	390.625	322.266	MHz
		32	64	255.859	255.859	195.313	195.313	161.133	MHz
		20	20	409.375	409.375	312.500	312.500	257.813	MHz
		20	40	204.688	204.688	156.250	156.250	128.906	MHz
		40	40	409.375	409.375	312.500	312.500	257.813	MHz
		40	80	204.688	204.688	156.250	156.250	128.906	MHz

Notes:

1. Clocking must be implemented as described in *UltraScale Architecture GTH Transceiver User Guide* (UG576).
2. For speed grades -3E, -2E, and -2I, a 16-bit and 20-bit internal data path can only be used for line rates less than 8.1875 Gb/s.
3. For speed grade -2LE, a 16-bit and 20-bit internal data path can only be used for line rates less than 8.1875 Gb/s when V_{CCINT} = 0.85V or 6.25 Gb/s when V_{CCINT} = 0.72V.
4. For speed grades -1E and -1I, a 16-bit and 20-bit internal data path can only be used for line rates less than 6.25 Gb/s.
5. For speed grade -1LI, a 16-bit and 20-bit internal data path can only be used for line rates less than 6.25 Gb/s when V_{CCINT} = 0.85V or 5.15625 Gb/s when V_{CCINT} = 0.72V.
6. When the gearbox is used, these maximums refer to the XCLK. For more information, see the *Valid Data Width Combinations for TX Asynchronous Gearbox* table in the *UltraScale Architecture GTH Transceiver User Guide* (UG576).

GTY Transceiver Switching Characteristics

Consult the *UltraScale Architecture GTY Transceiver User Guide* (UG578) for further information.

Table 109: **GTY Transceiver Performance**

Symbol	Description	Output Divider	Speed Grade and V_{CCINT} Operating Voltages										Units
			0.90V		0.85V				0.72V				
			-3		-2		-1		-2		-1		
F_{GTYMAX}	GTY maximum line rate		32.75		28.21		25.7813		28.21		12.5		Gb/s
F_{GTYMIN}	GTY minimum line rate		0.5		0.5		0.5		0.5		0.5		Gb/s
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
$F_{GTYCRANGE}$	CPLL line rate range[1]	1	4.0	12.5	4.0	12.5	4.0	8.5	4.0	12.5	4.0	8.5	Gb/s
		2	2.0	6.25	2.0	6.25	2.0	4.25	2.0	6.25	2.0	4.25	Gb/s
		4	1.0	3.125	1.0	3.125	1.0	2.125	1.0	3.125	1.0	2.125	Gb/s
		8	0.5	1.5625	0.5	1.5625	0.5	1.0625	0.5	1.5625	0.5	1.0625	Gb/s
		16	N/A										Gb/s
		32	N/A										Gb/s
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
$F_{GTYQRANGE1}$	QPLL0 line rate range[2]	1	19.6	32.75	19.6	28.21	19.6	25.7813	19.6	28.21	N/A		Gb/s
		1	9.8	16.375	9.8	16.375	9.8	12.5	9.8	16.375	9.8	12.5	Gb/s
		2	4.9	8.1875	4.9	8.1875	4.9	8.1875	4.9	8.1875	4.9	8.1875	Gb/s
		4	2.45	4.0938	2.45	4.0938	2.45	4.0938	2.45	4.0938	2.45	4.0938	Gb/s
		8	1.225	2.0469	1.225	2.0469	1.225	2.0469	1.225	2.0469	1.225	2.0469	Gb/s
		16	0.6125	1.0234	0.6125	1.0234	0.6125	1.0234	0.6125	1.0234	0.6125	1.0234	Gb/s
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
$F_{GTYQRANGE2}$	QPLL1 line rate range[3]	1	16.0	26.0	16.0	26.0	19.6	25.7813	16.0	26.0	N/A		Gb/s
		1	8.0	13.0	8.0	13.0	8.0	12.5	8.0	13.0	8.0	12.5	Gb/s
		2	4.0	6.5	4.0	6.5	4.0	6.5	4.0	6.5	4.0	6.5	Gb/s
		4	2.0	3.25	2.0	3.25	2.0	3.25	2.0	3.25	2.0	3.25	Gb/s
		8	1.0	1.625	1.0	1.625	1.0	1.625	1.0	1.625	1.0	1.625	Gb/s
		16	0.5	0.8125	0.5	0.8125	0.5	0.8125	0.5	0.8125	0.5	0.8125	Gb/s
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
$F_{CPLLRANGE}$	CPLL frequency range		2.0	6.25	2.0	6.25	2.0	4.25	2.0	6.25	2.0	4.25	GHz
$F_{QPLL0RANGE}$	QPLL0 frequency range		9.8	16.375	9.8	16.375	9.8	16.375	9.8	16.375	9.8	16.375	GHz
$F_{QPLL1RANGE}$	QPLL1 frequency range		8.0	13.0	8.0	13.0	8.0	13.0	8.0	13.0	8.0	13.0	GHz

Notes:
1. The values listed are the rounded results of the calculated equation (2 x CPLL_Frequency)/Output_Divider.
2. The values listed are the rounded results of the calculated equation (2 x QPLL0_Frequency)/Output_Divider.
3. The values listed are the rounded results of the calculated equation (2 x QPLL1_Frequency)/Output_Divider.

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Table 116: **GTY Transceiver Receiver Switching Characteristics**

Symbol	Description	Condition	Min	Typ	Max	Units
F_{GTYRX}	Serial data rate		0.500	–	F_{GTYMAX}	Gb/s
R_{XSST}	Receiver spread-spectrum tracking[1]	Modulated at 33 kHz	–5000	–	0	ppm
R_{XRL}	Run length (CID)		–	–	256	UI
$R_{XPPMTOL}$	Data/REFCLK PPM offset tolerance	Bit rates ≤ 6.6 Gb/s	–1250	–	1250	ppm
		Bit rates > 6.6 Gb/s and ≤ 8.0 Gb/s	–700	–	700	ppm
		Bit rates > 8.0 Gb/s	–200	–	200	ppm
SJ Jitter Tolerance[2]						
$J_{T\_SJ32.75}$	Sinusoidal jitter (QPLL)[3]	32.75 Gb/s	0.25	–	–	UI
$J_{T\_SJ28.21}$	Sinusoidal jitter (QPLL)[3]	28.21 Gb/s	0.30	–	–	UI
$J_{T\_SJ16.375}$	Sinusoidal jitter (QPLL)[3]	16.375 Gb/s	0.30	–	–	UI
$J_{T\_SJ15.0}$	Sinusoidal jitter (QPLL)[3]	15.0 Gb/s	0.30	–	–	UI
$J_{T\_SJ14.1}$	Sinusoidal jitter (QPLL)[3]	14.1 Gb/s	0.30	–	–	UI
$J_{T\_SJ13.1}$	Sinusoidal jitter (QPLL)[3]	13.1 Gb/s	0.30	–	–	UI
$J_{T\_SJ12.5}$	Sinusoidal jitter (QPLL)[3]	12.5 Gb/s	0.30	–	–	UI
$J_{T\_SJ11.3}$	Sinusoidal jitter (QPLL)[3]	11.3 Gb/s	0.30	–	–	UI
$J_{T\_SJ10.32\_QPLL}$	Sinusoidal jitter (QPLL)[3]	10.32 Gb/s	0.30	–	–	UI
$J_{T\_SJ10.32\_CPLL}$	Sinusoidal jitter (CPLL)[3]	10.32 Gb/s	0.30	–	–	UI
$J_{T\_SJ9.953\_QPLL}$	Sinusoidal jitter (QPLL)[3]	9.953 Gb/s	0.30	–	–	UI
$J_{T\_SJ9.953\_CPLL}$	Sinusoidal jitter (CPLL)[3]	9.953 Gb/s	0.30	–	–	UI
$J_{T\_SJ8.0}$	Sinusoidal jitter (CPLL)[3]	8.0 Gb/s	0.42	–	–	UI
$J_{T\_SJ6.6}$	Sinusoidal jitter (CPLL)[3]	6.6 Gb/s	0.44	–	–	UI
$J_{T\_SJ5.0}$	Sinusoidal jitter (CPLL)[3]	5.0 Gb/s	0.44	–	–	UI
$J_{T\_SJ4.25}$	Sinusoidal jitter (CPLL)[3]	4.25 Gb/s	0.44	–	–	UI
$J_{T\_SJ3.2}$	Sinusoidal jitter (CPLL)[3]	3.2 Gb/s[4]	0.45	–	–	UI
$J_{T\_SJ2.5}$	Sinusoidal jitter (CPLL)[3]	2.5 Gb/s[5]	0.30	–	–	UI
$J_{T\_SJ1.25}$	Sinusoidal jitter (CPLL)[3]	1.25 Gb/s[6]	0.30	–	–	UI
J_{T_SJ500}	Sinusoidal jitter (CPLL)[3]	500 Mb/s[7]	0.30	–	–	UI
SJ Jitter Tolerance with Stressed Eye[2]						
$J_{T\_TJSE3.2}$	Total jitter with stressed eye[8]	3.2 Gb/s	0.70	–	–	UI
$J_{T\_TJSE6.6}$		6.6 Gb/s	0.70	–	–	UI
$J_{T\_SJSE3.2}$	Sinusoidal jitter with stressed eye[8]	3.2 Gb/s	0.10	–	–	UI
$J_{T\_SJSE6.6}$		6.6 Gb/s	0.10	–	–	UI

Notes:
1. Using RXOUT_DIV = 1, 2, and 4.
2. All jitter values are based on a bit error ratio of 10^{-12}.
3. The frequency of the injected sinusoidal jitter is 80 MHz.
4. CPLL frequency at 3.2 GHz and RXOUT_DIV = 2.
5. CPLL frequency at 2.5 GHz and RXOUT_DIV = 2.
6. CPLL frequency at 2.5 GHz and RXOUT_DIV = 4.
7. CPLL frequency at 2.0 GHz and RXOUT_DIV = 8.
8. Composite jitter with RX equalizer enabled. DFE disabled.

Table 117: **GTY Transceiver Protocol List** *(Cont'd)*

Protocol	Specification	Serial Rate (Gb/s)	Electrical Compliance
Serial RapidIO	RapidIO specification 3.1	1.25–10.3125	Compliant
DisplayPort	DP 1.2B CTS	1.62–5.4	Compliant[3]
Fibre channel	FC-PI-4	1.0625–14.025	Compliant
SATA Gen1, 2, 3	Serial ATA revision 3.0 specification	1.5, 3.0, and 6.0	Compliant
SAS Gen1, 2, 3	T10/BSR INCITS 519	3.0, 6.0, and 12.0	Compliant
SFI-5	OIF-SFI5-01.0	0.625 - 12.5	Compliant
Aurora	CEI-6G, CEI-11G-LR	All rates	Compliant

Notes:

1. 25 dB loss at Nyquist without FEC.
2. The transition time of the transmitter is faster than the IEEE Std 802.3-2012 specification.
3. This protocol requires external circuitry to achieve compliance.

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Table 119: **Maximum Performance for Interlaken 6 x 25.78125 Gb/s and 6 x 28.21 Gb/s Protocol and Lane Logic Mode Designs**

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages										Units
		0.90V		0.85V				0.72V				
		-3[1]		-2[1]		-1		-2		-1		
$F_{RX\_SERDES\_CLK}$	Receive serializer/ deserializer clock	440.79		440.79		N/A		402.84		N/A		MHz
$F_{TX\_SERDES\_CLK}$	Transmit serializer/ deserializer clock	440.79		440.79		N/A		402.84		N/A		MHz
F_{DRP_CLK}	Dynamic reconfiguration port clock	250.00		250.00		N/A		250.00		N/A		MHz
		Min[2]	Max	Min[2]	Max	Min	Max	Min[2]	Max	Min	Max	
F_{CORE_CLK}	Interlaken core clock	412.50[3]	479.20	412.50[3]	479.20	N/A		412.50	429.69	N/A		MHz
F_{LBUS_CLK}	Interlaken local bus clock	300.00[4]	349.52	300.00[4]	349.52	N/A		300.00	349.52	N/A		MHz

Notes:

1. 6 x 28.21 mode is only supported in the -2 (V_{CCINT}=0.85V) and -3 (V_{CCINT}=0.90V) speed grades.
2. These are the minimum clock frequencies at the maximum lane performance.
3. The minimum value for CORE_CLK is 451.36 MHz for the 6 x 28.21 Gb/s protocol.
4. The minimum value for LBUS_CLK is 330.00 MHz for the 6 x 28.21 Gb/s protocol.

Table 120: **Maximum Performance for Interlaken 12 x 25.78125 Gb/s Lane Logic Only Mode Designs**

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages					Units
		0.90V	0.85V		0.72V		
		-3	-2	-1	-2	-1	
$F_{RX\_SERDES\_CLK}$	Receive serializer/ deserializer clock	402.84	402.84	N/A	N/A	N/A	MHz
$F_{TX\_SERDES\_CLK}$	Transmit serializer/ deserializer clock	402.84	402.84	N/A	N/A	N/A	MHz
F_{DRP_CLK}	Dynamic reconfiguration port clock	250.00	250.00	N/A	N/A	N/A	MHz
F_{CORE_CLK}	Interlaken core clock	412.50	412.50	N/A	N/A	N/A	MHz
F_{LBUS_CLK}	Interlaken local bus clock	349.52	349.52	N/A	N/A	N/A	MHz

Date	Version	Description of Revisions
02/10/2017	1.2	Updated some of the maximum voltages in the Processor System (PS) section and other specifications in the Programmable Logic (PL) and GTH or GTY Transceiver sections of Table 1. Updated Table 2, Table 4, Table 6, Table 7, and Table 9. Revised the Power Supply Sequencing section including Table 10. Added PS and VCU ramp times to Table 11. Revised V_{ODIFF} in Table 24. Updated Table 25. Added Note 1 to Table 26. Table 30 replaces the previous three PS memory performance tables. Added values to Table 34, Table 37, and Table 38. Deleted the waveforms in the PS Switching Characteristics section (Figures 1-16 and Figures 25-26). Revised values in the *PS NAND Memory Controller Interface* section. Added and updated data in Table 40. Added Note 3 to Table 41. Added Note 3 to Table 42. Added Note 1 to Table 45. Updated Table 48 and removed Note 3. Added data to Table 56. Updated Table 60. Added Table 61. Updated Table 63. Revised Table 69. Added data to Table 70. Added Note 2 to Table 71. Updated Table 74 and added Note 4. Updated V_L and V_H values in Table 78. Added T_{MINPER_CLK}, revised F_{REFCLK}, and Note 1 to Table 82. Added MMCM_F_{DPRCLK_MAX} to Table 85 and PLL_F_{DPRCLK_MAX} to Table 86. Added data to Table 94, Table 96, Table 98, Table 101, and updated the note references in Table 102. Updated Table 103 and added Note 8. Updated Table 104 and added Note 7. Added more protocols, Note 1 and Note 2 to Table 105. Removed the *GTH Transceiver Protocol Jitter Characteristics* section because it is covered in Table 105. Added Note 1 to Table 109. Added data to Table 106, Table 108, Table 110, Table 113. Added Note 2 to Table 112. Added note references in Table 114. Updated Table 115 and added Note 8. Updated Table 116 and added Note 7. Added more protocols and Note 3 to Table 117. Removed the *GTY Transceiver Protocol Jitter Characteristics* section because it is covered in Table 117. Revised Table 124. Added T_{POR} and updated F_{ICAPCK} in Table 127. Updated the Automotive Applications Disclaimer.
06/20/2016	1.1	Updated the Summary description. In Table 1, revised V_{IN} for HP I/O banks and added clarifications to some descriptions and symbols. Added I_{RPU}, I_{RPD}, and Note 4 to Table 2 and updated $V_{PS\_MGTRAVCC}$, the PL System Monitor section, and Note 3 and Note 5. Updated Note 5 in Table 4. Updated the PS Power-On/Off Power Supply Sequencing section including all the voltage supply names. Added MIPI_DPHY_DCI to Table 14, Table 15, and Table 17. Updated Table 23, including removing the V_{CCO} specification and adding Note 1. Added Note 1 to Table 24. Updated Table 25 speed specifications for Vivado Design Suite 2016.1. Added values to Table 28. Updated the -2 value in Table 29. Added $F_{DPLIVEVIDEO}$ and updated $F_{FCIDMACLK}$ in Table 33. Added VCO frequencies to Table 36. Added the T_{PSPOR} minimum to Table 37 and updated Note 1. Added Table 38. Added value delineation over V_{CCINT} operating voltages in Table 39. Revised values for F_{TCK} and T_{TAPTCK}/T_{TCKTAP} in Table 40 and added value delineation over V_{CCINT} operating voltages. Updated the *PS NAND Memory Controller Interface* section. Revised some units and Note 1 in Table 41 and Table 42. Removed Figure 6: Quad-SPI Interface (Feedback Clock Disabled) Timing. Updated Note 1 of Table 43. Added $F_{TSI\_REF\_CLK}$ to Table 44 and updated Note 1. In Table 45, revised $T_{DCSDHSCLK1}$, $T_{DCSDHSCLK2}$, and $T_{DCSDHSCLK3}$ and Note 1. In Table 46, revised Note 1. In Table 47, revised Note 1. Revised Table 48, including Note 1, and added Note 2 and Note 3. In Table 49, Table 50, Table 51, and Table 53, revised Note 1. Updated Table 71. Replaced Table 74. Updated Table 75 and Table 76. Updated Table 78 and Table 79. In Table 80, added the Block RAM and FIFO Clock-to-Out Delays section. Updated the R_{IN} and C_{EXT} values in Table 57 and Table 95. Updated the -2 (0.72V) and -1 (0.72V) values and added Note 1 to Table 97. Added Table 100 and Table 112. Added Note 2 to Table 106. Revised data in Table 109. Revised Table 114. Revised data and added notes in the Integrated Interface Block for Interlaken section and Table 121. Moved Table 123. Revised INL in Table 124. Added notes to Table 125 and Table 126. In the *eFUSE and Programming Conditions* table, updated the I_{PSFS} description.
11/24/2015	1.0	Initial Xilinx release.

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