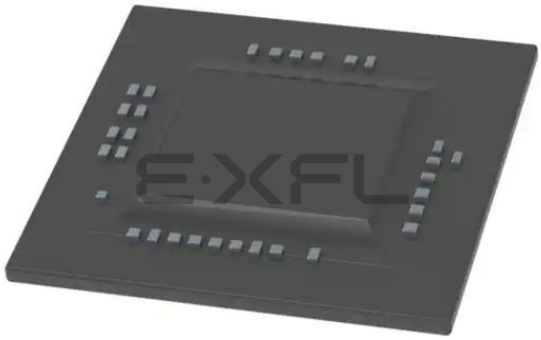

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## Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

**Embedded - System On Chip (SoC)** refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

## What are Embedded - System On Chip (SoC)?

**System On Chip (SoC)** integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

| Details | |
|---|---|
| Product Status | Active |
| Architecture | MCU, FPGA |
| Core Processor | Dual ARM® Cortex®-A53 MPCore™ with CoreSight™, Dual ARM®Cortex™-R5 with CoreSight™ |
| Flash Size | - |
| RAM Size | 256KB |
| Peripherals | DMA, WDT |
| Connectivity | CANbus, EBI/EMI, Ethernet, I²C, MMC/SD/SDIO, SPI, UART/USART, USB OTG |
| Speed | 533MHz, 1.3GHz |
| Primary Attributes | Zynq®UltraScale+™ FPGA, 504K+ Logic Cells |
| Operating Temperature | -40°C ~ 100°C (TJ) |
| Package / Case | 900-BBGA, FCBGA |
| Supplier Device Package | 900-FCBGA (31x31) |
| Purchase URL | https://www.e-xfl.com/product-detail/xilinx/xczu7cg-2fbvb900i |

*Table 1:* **Absolute Maximum Ratings[1] *(Cont'd)***

| Symbol | Description | Min | Max | Units |
|---|---|---|---|---|
| $V_{CCO\_PSDDR}$ | PS DDR I/O supply voltage. | –0.500 | 1.650 | V |
| $V_{CC\_PSDDR\_PLL}$ | PS DDR PLL supply voltage. | –0.500 | 2.000 | V |
| $V_{CCO\_PSIO}$ | PS I/O supply. | –0.500 | 3.630 | V |
| $V_{PSIN}$[2] | PS I/O input voltage. | –0.500 | $V_{CCO\_PSIO}$ + 0.550 | V |
| | PS DDR I/O input voltage. | –0.500 | $V_{CCO\_PSDDR}$ + 0.550 | V |
| $V_{CC\_PSBATT}$ | PS battery-backed RAM and battery-backed real-time clock (RTC) supply voltage. | –0.500 | 2.000 | V |
| **Programmable Logic (PL)** | | | | |
| $V_{CCINT}$ | Internal supply voltage. | –0.500 | 1.000 | V |
| $V_{CCINT\_IO}$[3] | Internal supply voltage for the I/O banks. | –0.500 | 1.000 | V |
| $V_{CCAUX}$ | Auxiliary supply voltage. | –0.500 | 2.000 | V |
| $V_{CCBRAM}$ | Supply voltage for the block RAM memories. | –0.500 | 1.000 | V |
| $V_{CCO}$ | Output drivers supply voltage for HD I/O banks. | –0.500 | 3.400 | V |
| | Output drivers supply voltage for HP I/O banks. | –0.500 | 2.000 | V |
| $V_{CCAUX\_IO}$[4] | Auxiliary supply voltage for the I/O banks. | –0.500 | 2.000 | V |
| $V_{REF}$ | Input reference voltage. | –0.500 | 2.000 | V |
| $V_{IN}$[2][5][7] | I/O input voltage for HD I/O banks.[6] | –0.550 | $V_{CCO}$ + 0.550 | V |
| | I/O input voltage for HP I/O banks. | –0.550 | $V_{CCO}$ + 0.550 | V |
| $I_{DC}$ | Available output current at the pad. | –20 | 20 | mA |
| $I_{RMS}$ | Available RMS output current at the pad. | –20 | 20 | mA |
| **GTH or GTY Transceiver** | | | | |
| $V_{MGTAVCC}$ | Analog supply voltage for transceiver circuits. | –0.500 | 1.000 | V |
| $V_{MGTAVTT}$ | Analog supply voltage for transceiver termination circuits. | –0.500 | 1.300 | V |
| $V_{MGTVCCAUX}$ | Auxiliary analog Quad PLL (QPLL) voltage supply for transceivers. | –0.500 | 1.900 | V |
| $V_{MGTREFCLK}$ | Transceiver reference clock absolute input voltage. | –0.500 | 1.300 | V |
| $V_{MGTAVTTRCAL}$ | Analog supply voltage for the resistor calibration circuit of the transceiver column. | –0.500 | 1.300 | V |
| $V_{IN}$ | Receiver (RXP/RXN) and transmitter (TXP/TXN) absolute input voltage. | –0.500 | 1.200 | V |
| $I_{DCIN-FLOAT}$ | DC input current for receiver input pins DC coupled RX termination = floating.[8] | – | 10 | mA |
| $I_{DCIN-MGTAVTT}$ | DC input current for receiver input pins DC coupled RX termination = $V_{MGTAVTT}$. | – | 10 | mA |
| $I_{DCIN-GND}$ | DC input current for receiver input pins DC coupled RX termination = GND.[9] | – | 0 | mA |
| $I_{DCIN-PROG}$ | DC input current for receiver input pins DC coupled RX termination = programmable.[10] | – | 0 | mA |
| $I_{DCOUT-FLOAT}$ | DC output current for transmitter pins DC coupled RX termination = floating. | – | 6 | mA |
| $I_{DCOUT-MGTAVTT}$ | DC output current for transmitter pins DC coupled RX termination = $V_{MGTAVTT}$. | – | 6 | mA |

# $V_{IN}$ Maximum Allowed AC Voltage Overshoot and Undershoot

*Table 6:* **$V_{IN}$ Maximum Allowed AC Voltage Overshoot and Undershoot for HD I/O Banks(1)**

| AC Voltage Overshoot | % of UI at –40°C to 100°C | AC Voltage Undershoot | % of UI at –40°C to 100°C |
|---|---|---|---|
| $V_{CCO}$ + 0.30 | 100% | –0.30 | 100% |
| $V_{CCO}$ + 0.35 | 100% | –0.35 | 90% |
| $V_{CCO}$ + 0.40 | 100% | –0.40 | 78% |
| $V_{CCO}$ + 0.45 | 100% | –0.45 | 40% |
| $V_{CCO}$ + 0.50 | 100% | –0.50 | 24% |
| $V_{CCO}$ + 0.55 | 100% | –0.55 | 18.0% |
| $V_{CCO}$ + 0.60 | 100% | –0.60 | 13.0% |
| $V_{CCO}$ + 0.65 | 100% | –0.65 | 10.8% |
| $V_{CCO}$ + 0.70 | 92% | –0.70 | 9.0% |
| $V_{CCO}$ + 0.75 | 92% | –0.75 | 7.0% |
| $V_{CCO}$ + 0.80 | 92% | –0.80 | 6.0% |
| $V_{CCO}$ + 0.85 | 92% | –0.85 | 5.0% |
| $V_{CCO}$ + 0.90 | 92% | –0.90 | 4.0% |
| $V_{CCO}$ + 0.95 | 92% | –0.95 | 2.5% |

**Notes:**

1. A total of 200 mA per bank should not be exceeded.

*Table 7:* **$V_{IN}$ Maximum Allowed AC Voltage Overshoot and Undershoot for HP I/O Banks(1)(2)**

| AC Voltage Overshoot | % of UI at –40°C to 100°C | AC Voltage Undershoot | % of UI at –40°C to 100°C |
|---|---|---|---|
| $V_{CCO}$ + 0.30 | 100% | –0.30 | 100% |
| $V_{CCO}$ + 0.35 | 100% | –0.35 | 100% |
| $V_{CCO}$ + 0.40 | 92% | –0.40 | 92% |
| $V_{CCO}$ + 0.45 | 50% | –0.45 | 50% |
| $V_{CCO}$ + 0.50 | 20% | –0.50 | 20% |
| $V_{CCO}$ + 0.55 | 10% | –0.55 | 10% |
| $V_{CCO}$ + 0.60 | 6% | –0.60 | 6% |
| $V_{CCO}$ + 0.65 | 2% | –0.65 | 2% |
| $V_{CCO}$ + 0.70 | 2% | –0.70 | 2% |

**Notes:**

1. A total of 200 mA per bank should not be exceeded.
2. For UI smaller than 20 µs.

## PS-PL Power Sequencing

The PS and PL power supplies are fully independent. All PS power supplies can be powered before or after any PL power supplies. The PS and PL power regions are isolated to prevent damage.

## Power Supply Requirements

Table 10 shows the minimum current, in addition to $I_{CCQ}$ maximum, required by each Zynq UltraScale+ device for proper power-on and configuration. If the current minimums shown in Table 10 are met, the device powers on after all supplies have passed through their power-on reset threshold voltages. The device must not be configured until after $V_{CCINT}$ is applied. Once initialized and configured, use the Xilinx Power Estimator (XPE) tools to estimate current drain on these supplies.

*Table 10:* **Power-on Current by Device(1)**

| $I_{CC}$ Min = | $I_{CCQ}$ + | XCZU2 | XCZU3 | XCZU4 | XCZU5 | XCZU6 | XCZU7 | XCZU9 | XCZU11 | XCZU15 | XCZU17 | XCZU19 | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $I_{CCINTMIN}$ | $I_{CCINTQ}$+ | 464 | 464 | 770 | 770 | 1800 | 1514 | 1800 | 1961 | 2242 | 3433 | 3433 | mA |
| $I_{CCINT\_IOMIN}$+ $I_{CCBRAMMIN}$ | $I_{CCBRAMQ}$+ $I_{CCINT\_IOQ}$+ | 155 | 155 | 257 | 257 | 600 | 505 | 600 | 654 | 748 | 1145 | 1145 | mA |
| $I_{CCOMIN}$ | $I_{CCOQ}$+ | 50 | 50 | 50 | 50 | 50 | 50 | 50 | 55 | 63 | 96 | 96 | mA |
| $I_{CCAUXMIN}$+ $I_{CCAUX\_IOMIN}$ | $I_{CCAUXQ}$+ $I_{CCAUX\_IOQ}$+ | 111 | 111 | 386 | 386 | 650 | 362 | 650 | 709 | 810 | 1240 | 1240 | mA |

**Notes:**

1. Use the Xilinx Power Estimator (XPE) spreadsheet tool (download at www.xilinx.com/power) to estimate power-on current for all supplies.

Table 11 shows the power supply ramp time.

*Table 11:* **Power Supply Ramp Time**

| Symbol | Description | Min | Max | Units |
|---|---|---|---|---|
| $T_{VCCINT}$ | Ramp time from GND to 95% of $V_{CCINT}$. | 0.2 | 40 | ms |
| $T_{VCCINT\_IO}$ | Ramp time from GND to 95% of $V_{CCINT\_IO}$. | 0.2 | 40 | ms |
| $T_{VCCINT\_VCU}$ | Ramp time from GND to 95% of $V_{CCINT\_VCU}$. | 0.2 | 40 | ms |
| $T_{VCCO}$ | Ramp time from GND to 95% of $V_{CCO}$. | 0.2 | 40 | ms |
| $T_{VCCAUX}$ | Ramp time from GND to 95% of $V_{CCAUX}$. | 0.2 | 40 | ms |
| $T_{VCCBRAM}$ | Ramp time from GND to 95% of $V_{CCBRAM}$. | 0.2 | 40 | ms |
| $T_{MGTAVCC}$ | Ramp time from GND to 95% of $V_{MGTAVCC}$. | 0.2 | 40 | ms |
| $T_{MGTAVTT}$ | Ramp time from GND to 95% of $V_{MGTAVTT}$. | 0.2 | 40 | ms |
| $T_{MGTVCCAUX}$ | Ramp time from GND to 95% of $V_{MGTVCCAUX}$. | 0.2 | 40 | ms |
| $T_{VCC\_PSINTFP}$ | Ramp time from GND to 95% of $V_{CC\_PSINTFP}$. | 0.2 | 40 | ms |
| $T_{VCC\_PSINTLP}$ | Ramp time from GND to 95% of $V_{CC\_PSINTLP}$. | 0.2 | 40 | ms |
| $T_{VCC\_PSAUX}$ | Ramp time from GND to 95% of $V_{CC\_PSAUX}$. | 0.2 | 40 | ms |
| $T_{VCC\_PSINTFP\_DDR}$ | Ramp time from GND to 95% of $V_{CC\_PSINTFP\_DDR}$. | 0.2 | 40 | ms |
| $T_{VCC\_PSADC}$ | Ramp time from GND to 95% of $V_{CC\_PSADC}$. | 0.2 | 40 | ms |
| $T_{VCC\_PSPLL}$ | Ramp time from GND to 95% of $V_{CC\_PSPLL}$. | 0.2 | 40 | ms |
| $T_{PS\_MGTRAVCC}$ | Ramp time from GND to 95% of $V_{CC\_MGTRAVCC}$. | 0.2 | 40 | ms |
| $T_{PS\_MGTRAVTT}$ | Ramp time from GND to 95% of $V_{CC\_MGTRAVTT}$. | 0.2 | 40 | ms |

*Table 11:* **Power Supply Ramp Time *(Cont'd)***

| Symbol | Description | Min | Max | Units |
|---|---|---|---|---|
| $T_{VCCO\_PSDDR}$ | Ramp time from GND to 95% of $V_{CCO\_PSDDR}$. | 0.2 | 40 | ms |
| $T_{VCC\_PSDDR\_PLL}$ | Ramp time from GND to 95% of $V_{CC\_PSDDR\_PLL}$. | 0.2 | 40 | ms |
| $T_{VCCO\_PSIO}$ | Ramp time from GND to 95% of $V_{CCO\_PSIO}$. | 0.2 | 40 | ms |

# DC Input and Output Levels

Values for $V_{IL}$ and $V_{IH}$ are recommended input voltages. Values for $I_{OL}$ and $I_{OH}$ are guaranteed over the recommended operating conditions at the $V_{OL}$ and $V_{OH}$ test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at a minimum $V_{CCO}$ with the respective $V_{OL}$ and $V_{OH}$ voltage levels shown. Other standards are sample tested.

## PS I/O Levels

*Table 12:* **PS MIO and CONFIG DC Input and Output Levels(1)**

| I/O Standard | $V_{IL}$ | | $V_{IH}$ | | $V_{OL}$ | $V_{OH}$ | $I_{OL}$ | $I_{OH}$ |
|---|---|---|---|---|---|---|---|---|
| | V, Min | V, Max | V, Min | V, Max | V, Max | V, Min | mA | mA |
| LVCMOS33 | –0.300 | 0.800 | 2.000 | $V_{CCO\_PSIO}$ | 0.40 | 2.40 | 12 | –12 |
| LVCMOS25 | –0.300 | 0.700 | 1.700 | $V_{CCO\_PSIO}$ + 0.30 | 0.70 | 1.70 | 12 | –12 |
| LVCMOS18 | –0.300 | 35% $V_{CCO\_PSIO}$ | 65% $V_{CCO\_PSIO}$ | $V_{CCO\_PSIO}$ + 0.30 | 0.45 | $V_{CCO\_PSIO}$ – 0.45 | 12 | –12 |

**Notes:**
1. Tested according to relevant specifications.

*Table 13:* **PS DDR DC Input and Output Levels(1)**

| DDR Standard | $V_{IL}$ | | $V_{IH}$ | | $V_{OL}$(2) | $V_{OH}$(2) | $I_{OL}$ | $I_{OH}$ |
|---|---|---|---|---|---|---|---|---|
| | V, Min | V, Max | V, Min | V, Max | V, Max | V, Min | mA | mA |
| DDR4 | 0.000 | $V_{REF}$ – 0.100 | $V_{REF}$ + 0.100 | $V_{CCO\_PSDDR}$ | 0.8 x $V_{CCO\_PSDDR}$ – 0.150 | 0.8 x $V_{CCO\_PSDDR}$ + 0.150 | 10 | –0.1 |
| LPDDR4 | 0.000 | $V_{REF}$ – 0.100 | $V_{REF}$ + 0.100 | $V_{CCO\_PSDDR}$ | 0.3 x $V_{CCO\_PSDDR}$ – 0.150 | 0.3 x $V_{CCO\_PSDDR}$ + 0.150 | 0.1 | –10 |
| DDR3 | –0.300 | $V_{REF}$ – 0.100 | $V_{REF}$ + 0.100 | $V_{CCO\_PSDDR}$ | 0.5 x $V_{CCO\_PSDDR}$ – 0.175 | 0.5 x $V_{CCO\_PSDDR}$ + 0.175 | 8 | –8 |
| LPDDR3 | 0.000 | $V_{REF}$ – 0.100 | $V_{REF}$ + 0.100 | $V_{CCO\_PSDDR}$ | 0.5 x $V_{CCO\_PSDDR}$ – 0.150 | 0.5 x $V_{CCO\_PSDDR}$ + 0.150 | 8 | –8 |
| DDR3L | –0.300 | $V_{REF}$ – 0.090 | $V_{REF}$ + 0.090 | $V_{CCO\_PSDDR}$ | 0.5 x $V_{CCO\_PSDDR}$ – 0.150 | 0.5 x $V_{CCO\_PSDDR}$ + 0.150 | 8 | –8 |

**Notes:**
1. Tested according to relevant specifications.
2. DDR4 $V_{OL}/V_{OH}$ specifications are only applicable for DQ/DQS pins.

*Table 15:* **SelectIO DC Input and Output Levels for HP I/O Banks(1)(2)(3)**

| I/O Standard | $V_{IL}$ | | $V_{IH}$ | | $V_{OL}$ | $V_{OH}$ | $I_{OL}$ | $I_{OH}$ |
|---|---|---|---|---|---|---|---|---|
| | V, Min | V, Max | V, Min | V, Max | V, Max | V, Min | mA | mA |
| HSTL_I | –0.300 | $V_{REF}$ – 0.100 | $V_{REF}$ + 0.100 | $V_{CCO}$ + 0.300 | 0.400 | $V_{CCO}$ – 0.400 | 5.8 | –5.8 |
| HSTL_I_12 | –0.300 | $V_{REF}$ – 0.080 | $V_{REF}$ + 0.080 | $V_{CCO}$ + 0.300 | 25% $V_{CCO}$ | 75% $V_{CCO}$ | 4.1 | –4.1 |
| HSTL_I_18 | –0.300 | $V_{REF}$ – 0.100 | $V_{REF}$ + 0.100 | $V_{CCO}$ + 0.300 | 0.400 | $V_{CCO}$ – 0.400 | 6.2 | –6.2 |
| HSUL_12 | –0.300 | $V_{REF}$ – 0.130 | $V_{REF}$ + 0.130 | $V_{CCO}$ + 0.300 | 20% $V_{CCO}$ | 80% $V_{CCO}$ | 0.1 | –0.1 |
| LVCMOS12 | –0.300 | 35% $V_{CCO}$ | 65% $V_{CCO}$ | $V_{CCO}$ + 0.300 | 0.400 | $V_{CCO}$ – 0.400 | Note 4 | Note 4 |
| LVCMOS15 | –0.300 | 35% $V_{CCO}$ | 65% $V_{CCO}$ | $V_{CCO}$ + 0.300 | 0.450 | $V_{CCO}$ – 0.450 | Note 5 | Note 5 |
| LVCMOS18 | –0.300 | 35% $V_{CCO}$ | 65% $V_{CCO}$ | $V_{CCO}$ + 0.300 | 0.450 | $V_{CCO}$ – 0.450 | Note 5 | Note 5 |
| LVDCI_15 | –0.300 | 35% $V_{CCO}$ | 65% $V_{CCO}$ | $V_{CCO}$ + 0.300 | 0.450 | $V_{CCO}$ – 0.450 | 7.0 | –7.0 |
| LVDCI_18 | –0.300 | 35% $V_{CCO}$ | 65% $V_{CCO}$ | $V_{CCO}$ + 0.300 | 0.450 | $V_{CCO}$ – 0.450 | 7.0 | –7.0 |
| SSTL12 | –0.300 | $V_{REF}$ – 0.100 | $V_{REF}$ + 0.100 | $V_{CCO}$ + 0.300 | $V_{CCO}$/2 – 0.150 | $V_{CCO}$/2 + 0.150 | 8.0 | –8.0 |
| SSTL135 | –0.300 | $V_{REF}$ – 0.090 | $V_{REF}$ + 0.090 | $V_{CCO}$ + 0.300 | $V_{CCO}$/2 – 0.150 | $V_{CCO}$/2 + 0.150 | 9.0 | –9.0 |
| SSTL15 | –0.300 | $V_{REF}$ – 0.100 | $V_{REF}$ + 0.100 | $V_{CCO}$ + 0.300 | $V_{CCO}$/2 – 0.175 | $V_{CCO}$/2 + 0.175 | 10.0 | –10.0 |
| SSTL18_I | –0.300 | $V_{REF}$ – 0.125 | $V_{REF}$ + 0.125 | $V_{CCO}$ + 0.300 | $V_{CCO}$/2 – 0.470 | $V_{CCO}$/2 + 0.470 | 7.0 | –7.0 |
| MIPI_DPHY_DCI_LP(6) | –0.300 | 0.550 | 0.880 | $V_{CCO}$ + 0.300 | 0.050 | 1.100 | 0.01 | –0.01 |

**Notes:**

1. Tested according to relevant specifications.
2. Standards specified using the default I/O standard configuration. For details, see the *UltraScale Architecture SelectIO Resources User Guide* (UG571).
3. POD10 and POD12 DC input and output levels are shown in Table 16, Table 20, Table 21, and Table 22.
4. Supported drive strengths of 2, 4, 6, or 8 mA in HP I/O banks.
5. Supported drive strengths of 2, 4, 6, 8, or 12 mA in HP I/O banks.
6. Low-power option for MIPI_DPHY_DCI.

*Table 16:* **DC Input Levels for Single-ended POD10 and POD12 I/O Standards(1)(2)**

| I/O Standard | $V_{IL}$ | | $V_{IH}$ | |
|---|---|---|---|---|
| | V, Min | V, Max | V, Min | V, Max |
| POD10 | –0.300 | $V_{REF}$ – 0.068 | $V_{REF}$ + 0.068 | $V_{CCO}$ + 0.300 |
| POD12 | –0.300 | $V_{REF}$ – 0.068 | $V_{REF}$ + 0.068 | $V_{CCO}$ + 0.300 |

**Notes:**

1. Tested according to relevant specifications.
2. Standards specified using the default I/O standard configuration. For details, see the *UltraScale Architecture SelectIO Resources User Guide* (UG571).

*Table 19:* **Complementary Differential SelectIO DC Input and Output Levels for HP I/O Banks(1)**

| I/O Standard | $V_{ICM}$ (V)(2) | | | $V_{ID}$ (V)(3) | | $V_{OL}$ (V)(4) | $V_{OH}$ (V)(5) | $I_{OL}$ | $I_{OH}$ |
|---|---|---|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Max | Max | Min | mA | mA |
| DIFF_HSTL_I | 0.680 | $V_{CCO}/2$ | ($V_{CCO}/2$) + 0.150 | 0.100 | – | 0.400 | $V_{CCO}$ – 0.400 | 5.8 | –5.8 |
| DIFF_HSTL_I_12 | 0.400 x $V_{CCO}$ | $V_{CCO}/2$ | 0.600 x $V_{CCO}$ | 0.100 | – | 0.250 x $V_{CCO}$ | 0.750 x $V_{CCO}$ | 4.1 | –4.1 |
| DIFF_HSTL_I_18 | ($V_{CCO}/2$) – 0.175 | $V_{CCO}/2$ | ($V_{CCO}/2$) + 0.175 | 0.100 | – | 0.400 | $V_{CCO}$ – 0.400 | 6.2 | –6.2 |
| DIFF_HSUL_12 | ($V_{CCO}/2$) – 0.120 | $V_{CCO}/2$ | ($V_{CCO}/2$) + 0.120 | 0.100 | – | 20% $V_{CCO}$ | 80% $V_{CCO}$ | 0.1 | –0.1 |
| DIFF_SSTL12 | ($V_{CCO}/2$) – 0.150 | $V_{CCO}/2$ | ($V_{CCO}/2$) + 0.150 | 0.100 | – | ($V_{CCO}/2$) – 0.150 | ($V_{CCO}/2$) + 0.150 | 8.0 | –8.0 |
| DIFF_SSTL135 | ($V_{CCO}/2$) – 0.150 | $V_{CCO}/2$ | ($V_{CCO}/2$) + 0.150 | 0.100 | – | ($V_{CCO}/2$) – 0.150 | ($V_{CCO}/2$) + 0.150 | 9.0 | –9.0 |
| DIFF_SSTL15 | ($V_{CCO}/2$) – 0.175 | $V_{CCO}/2$ | ($V_{CCO}/2$) + 0.175 | 0.100 | – | ($V_{CCO}/2$) – 0.175 | ($V_{CCO}/2$) + 0.175 | 10.0 | –10.0 |
| DIFF_SSTL18_I | ($V_{CCO}/2$) – 0.175 | $V_{CCO}/2$ | ($V_{CCO}/2$) + 0.175 | 0.100 | – | ($V_{CCO}/2$) – 0.470 | ($V_{CCO}/2$) + 0.470 | 7.0 | –7.0 |

**Notes:**

1. DIFF_POD10 and DIFF_POD12 HP I/O bank specifications are shown in Table 20, Table 21, and Table 22.
2. $V_{ICM}$ is the input common mode voltage.
3. $V_{ID}$ is the input differential voltage.
4. $V_{OL}$ is the single-ended low-output voltage.
5. $V_{OH}$ is the single-ended high-output voltage.

*Table 20:* **DC Input Levels for Differential POD10 and POD12 I/O Standards(1)(2)**

| I/O Standard | $V_{ICM}$ (V) | | | $V_{ID}$ (V) | |
|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Max |
| DIFF_POD10 | 0.63 | 0.70 | 0.77 | 0.14 | – |
| DIFF_POD12 | 0.76 | 0.84 | 0.92 | 0.16 | – |

**Notes:**

1. Tested according to relevant specifications.
2. Standards specified using the default I/O standard configuration. For details, see the *UltraScale Architecture SelectIO Resources User Guide* (UG571).

*Table 21:* **DC Output Levels for Single-ended and Differential POD10 and POD12 Standards(1)(2)**

| Symbol | Description | $V_{OUT}$ | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $R_{OL}$ | Pull-down resistance. | $V_{OM\_DC}$ (as described in Table 22) | 36 | 40 | 44 | Ω |
| $R_{OH}$ | Pull-up resistance. | $V_{OM\_DC}$ (as described in Table 22) | 36 | 40 | 44 | Ω |

**Notes:**

1. Tested according to relevant specifications.
2. Standards specified using the default I/O standard configuration. For details, see the *UltraScale Architecture SelectIO Resources User Guide* (UG571).

*Table 22:* **Table 21 Definitions for DC Output Levels for POD Standards**

| Symbol | Description | All Speed Grades | Units |
|---|---|---|---|
| $V_{OM\_DC}$ | DC output Mid measurement level (for IV curve linearity). | 0.8 x $V_{CCO}$ | V |

# PS Gigabit Ethernet Controller Interface

*Table 44:* **RGMII Interface(1)**

| Symbol | Description | Min | Max | Units |
|---|---|---|---|---|
| $T_{DCGEMTXCLK}$ | Transmit clock duty cycle. | 45 | 55 | % |
| $T_{GEMTXCKO}$ | TXD output clock to out time. | –0.5 | 0.5 | ns |
| $T_{GEMRXDCK}$ | RXD input setup time. | 0.8 | – | ns |
| $T_{GEMRXCKD}$ | RXD input hold time. | 0.8 | – | ns |
| $T_{MDIOCLK}$ | MDC output clock period. | 400 | – | ns |
| $T_{MDIOCKL}$ | MDC low time. | 160 | – | ns |
| $T_{MDIOCKH}$ | MDC high time. | 160 | – | ns |
| $T_{MDIODCK}$ | MDIO input data setup time. | 80 | – | ns |
| $T_{MDIOCKD}$ | MDIO input data hold time. | 0.0 | – | ns |
| $T_{MDIOCKO}$ | MDIO output data delay time. | –1.0 | 15 | ns |
| $F_{GETXCLK}$ | RGMII_TX_CLK transmit clock frequency. | – | 125 | MHz |
| $F_{GERXCLK}$ | RGMII_RX_CLK receive clock frequency. | – | 125 | MHz |
| $F_{ENET\_REF\_CLK}$ | Ethernet reference clock frequency. | – | 125 | MHz |

**Notes:**

1. The test conditions are configured to the LVCMOS 2.5V I/O standard with a 12 mA drive strength, fast slew rate, and a 15 pF load.

# PS SD/SDIO Controller Interface

*Table 45:* **SD/SDIO Interface(1)**

| Symbol | Description | Min | Max | Units |
|---|---|---|---|---|
| **SD/SDIO Interface DDR50 Mode** | | | | |
| $T_{DCDDRCLK}$ | SD device clock duty cycle. | 45 | 55 | % |
| $T_{SDDDRCKO1}$ | Clock to output delay, data.(2) | 1.0 | 6.8 | ns |
| $T_{SDDRIVW}$ | Input valid data window.(3) | 3.5 | – | ns |
| $T_{SDDDRDCK2}$ | Input setup time, command. | 4.7 | – | ns |
| $T_{SDDDRCKD2}$ | Input hold time, command. | 1.5 | – | ns |
| $T_{SDDDRCKO2}$ | Clock to output delay, command. | 1.0 | 13.8 | ns |
| $F_{SDDDRCLK}$ | High-speed mode SD device clock frequency. | – | 50 | MHz |
| **SD/SDIO Interface SDR104** | | | | |
| $T_{DCSDHSCLK1}$ | SD device clock duty cycle. | 40 | 60 | % |
| $T_{SDSDRCKO1}$ | Clock to output delay, all outputs.(2) | 1.0 | 3.2 | ns |
| $T_{SDSDR1IVW}$ | Input valid data window.(3) | 0.5 | – | UI |
| $F_{SDSDRCLK1}$ | SDR104 mode device clock frequency. | – | 200 | MHz |
| **SD/SDIO Interface SDR50/25** | | | | |
| $T_{DCSDHSCLK2}$ | SD device clock duty cycle. | 40 | 60 | % |
| $T_{SDSDRCKO2}$ | Clock to output delay, all outputs.(2) | 1.0 | 6.8 | ns |
| $T_{SDSDR2IVW}$ | Input valid data window.(3) | 0.3 | – | UI |

# PS eMMC Standard Interface

*Table 46:* **eMMC Standard Interface(1)**

| Symbol | Description | Min | Max | Units |
|---|---|---|---|---|
| **eMMC Standard Interface** | | | | |
| $T_{DCEMMCHSCLK}$ | eMMC clock duty cycle. | 45 | 55 | % |
| $T_{EMMCHSCKO}$ | Clock to output delay, all outputs. | –2.0 | 4.5 | ns |
| $T_{EMMCHSDCK}$ | Input setup time, all inputs. | 2.0 | – | ns |
| $T_{EMMCHSCKD}$ | Input hold time, all inputs. | 2.0 | – | ns |
| $F_{EMMCHSCLK}$ | eMMC clock frequency. | – | 25 | MHz |
| **eMMC High-Speed SDR Interface** | | | | |
| $T_{DCEMMCHSCLK}$ | eMMC high-speed SDR clock duty cycle. | 45 | 55 | % |
| $T_{EMMCHSCKO}$ | Clock to output delay, all outputs.(2) | 3.2 | 16.8 | ns |
| $T_{EMMCHSDIVW}$ | Input valid data window.(3) | 0.4 | – | UI |
| $F_{EMMCHSCLK}$ | eMMC high speed SDR clock frequency. | – | 50 | MHz |
| **eMMC High-Speed DDR Interface** | | | | |
| $T_{DCEMMCDDRCLK}$ | eMMC high-speed DDR clock duty cycle. | 45 | 55 | % |
| $T_{EMMCDDRSCKO1}$ | Data clock to output delay.(2) | 2.7 | 7.3 | ns |
| $T_{EMMCSDRIVW}$ | Input valid data window.(3) | 3.5 | – | ns |
| $T_{EMMCDDRSCKO2}$ | Command clock to output delay. | 3.2 | 16 | ns |
| $T_{EMMCDDRDCK2}$ | Command input setup time. | 3.9 | – | ns |
| $T_{EMMCDDRCKD2}$ | Command input hold time. | 2.5 | – | ns |
| $F_{EMMCDDRCLK}$ | eMMC high-speed DDR clock frequency. | – | 50 | MHz |
| **eMMC HS200 Interface** | | | | |
| $T_{DCEMMCHS200CLK}$ | eMMC HS200 clock duty cycle. | 40 | 60 | % |
| $T_{EMMCHS200CKO}$ | Clock to output delay, all outputs.(2) | 1.0 | 3.4 | ns |
| $T_{EMMCSDR1IVW}$ | Input valid data window.(3) | 0.4 | – | UI |
| $F_{EMMCHS200CLK}$ | eMMC HS200 clock frequency. | – | 200 | MHz |

**Notes:**

1. The test conditions for eMMC standard mode use an 8 mA drive strength, fast slew rate, and a 30 pF load. For eMMC high-speed mode, the test conditions use a 12 mA drive strength, fast slew rate, and a 30 pF load. For other eMMC modes, the test conditions use a 12 mA drive strength, fast slew rate, and a 15 pF load.
2. This specification is achieved using pre-determined DLL tuning.
3. This specification is required for capturing input data using DLL tuning.

# PS DAP Interface

*Table 50:* **DAP Interface(1)**

| Symbol | Description(2) | Min | Max | Units |
|---|---|---|---|---|
| $T_{PDAPDCK}$ | PS DAP input setup time. | 3.0 | – | ns |
| $T_{PDAPCKD}$ | PS DAP input hold time. | 2.0 | – | ns |
| $T_{PDAPCKO}$ | PS DAP clock to out delay. | – | 10.86 | ns |
| $T_{PDAPCLK}$ | PS DAP clock frequency. | – | 44 | MHz |

**Notes:**

1. The test conditions are configured to the LVCMOS 3.3V I/O standard with a 12 mA drive strength, fast slew rate, and a 15 pF load.
2. PS DAP interface signals connect to MIO pins.

# PS UART Interface

*Table 51:* **UART Interface(1)**

| Symbol | Description | Min | Max | Units |
|---|---|---|---|---|
| $BAUD_{TXMAX}$ | Transmit baud rate. | – | 6.25 | Mb/s |
| $BAUD_{RXMAX}$ | Receive baud rate. | – | 6.25 | Mb/s |
| $F_{UART\_REF\_CLK}$ | UART reference clock frequency. | – | 100 | MHz |

**Notes:**

1. The test conditions are configured to the LVCMOS 3.3V I/O standard with a 12 mA drive strength, fast slew rate, and a 15 pF load.

# PS General Purpose I/O Interface

*Table 52:* **General Purpose I/O (GPIO) Interface**

| Symbol | Description | Min | Max | Units |
|---|---|---|---|---|
| $T_{PWGPIOH}$ | Input High pulse width. | 10 x $1/F_{LPD\_LSBUS\_CTRLMAX}$ | – | µs |
| $T_{PWGPIOL}$ | Input Low pulse width. | 10 x $1/F_{LPD\_LSBUS\_CTRLMAX}$ | – | µs |

# PS Trace Interface

*Table 53:* **Trace Interface(1)**

| Symbol | Description | Min | Max | Units |
|---|---|---|---|---|
| $T_{TCECKO}$ | Trace clock to output delay, all outputs. | –0.5 | 0.5 | ns |
| $T_{DCTCECLK}$ | Trace clock duty cycle. | 45 | 55 | % |
| $F_{TCECLK}$ | Trace clock frequency. | – | 125 | MHz |

**Notes:**

1. The test conditions are configured to the LVCMOS 3.3V I/O standard with a 12 mA drive strength, fast slew rate, and a 15 pF load.

*Table 63:* **PS-GTR Transceiver Receiver Switching Characteristics**

| Symbol | Description | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $F_{GTRRX}$ | Serial data rate. | | 1.25 | – | 6 | Gb/s |
| $RX_{SST}$ | Receiver spread-spectrum tracking. | Modulated at 33 KHz | –5000 | – | 0 | ppm |
| $RX_{PPMTOL}$ | Data/REFCLK PPM offset tolerance. | All data rates | –350 | – | 350 | ppm |

*Table 64:* **PCI Express Protocol Characteristics (PS-GTR Transceivers)(1)**

| Standard | Description | Line Rate (Mb/s) | Min | Max | Units |
|---|---|---|---|---|---|
| **PCI Express Transmitter Jitter Generation** | | | | | |
| PCI Express Gen 1 | Total transmitter jitter. | 2500 | – | 0.25 | UI |
| PCI Express Gen 2 | Total transmitter jitter. | 5000 | – | 0.25 | UI |
| **PCI Express Receiver High Frequency Jitter Tolerance** | | | | | |
| PCI Express Gen 1 | Total receiver jitter tolerance. | 2500 | 0.65 | – | UI |
| PCI Express Gen 2(2) | Receiver inherent timing error. | 5000 | 0.4 | – | UI |
| | Receiver inherent deterministic timing error. | 5000 | 0.3 | – | UI |

**Notes:**
1. Tested per card electromechanical (CEM) methodology.
2. Between 1 MHz and 10 MHz the minimum sinusoidal jitter roll-off with a slope of 20 dB/decade.

*Table 65:* **Serial ATA (SATA) Protocol Characteristics (PS-GTR Transceivers)**

| Standard | Description | Line Rate (Mb/s) | Min | Max | Units |
|---|---|---|---|---|---|
| **Serial ATA Transmitter Jitter Generation** | | | | | |
| SATA Gen 1 | Total transmitter jitter. | 1500 | – | 0.37 | UI |
| SATA Gen 2 | Total transmitter jitter. | 3000 | – | 0.37 | UI |
| SATA Gen 3 | Total transmitter jitter. | 6000 | – | 0.52 | UI |
| **Serial ATA Receiver High Frequency Jitter Tolerance** | | | | | |
| SATA Gen 1 | Total receiver jitter tolerance. | 1500 | 0.27 | – | UI |
| SATA Gen 2 | Total receiver jitter tolerance. | 3000 | 0.27 | – | UI |
| SATA Gen 2 | Total receiver jitter tolerance. | 6000 | 0.16 | – | UI |

*Table 66:* **DisplayPort Protocol Characteristics (PS-GTR Transceivers)(1)**

| Standard | Description | Line Rate (Mb/s) | Min | Max | Units |
|---|---|---|---|---|---|
| **DisplayPort Transmitter Jitter Generation** | | | | | |
| RBR | Total transmitter jitter. | 1620 | – | 0.42 | UI |
| HBR | Total transmitter jitter. | 2700 | – | 0.42 | UI |
| HBR2 D10.2 | Total transmitter jitter. | 5400 | – | 0.40 | UI |
| HBR2 CPAT | Total transmitter jitter. | 5400 | – | 0.58 | UI |

**Notes:**
1. Only the transmitter is supported.

*Table 67:* **USB 3.0 Protocol Characteristics (PS-GTR Transceivers)**

| Standard | Description | Line Rate (Mb/s) | Min | Max | Units |
|---|---|---|---|---|---|
| **USB 3.0 Transmitter Jitter Generation** | | | | | |
| USB 3.0 | Total transmitter jitter. | 5000 | – | 0.66 | UI |
| **USB 3.0 Receiver High Frequency Jitter Tolerance** | | | | | |
| USB 3.0 | Total receiver jitter tolerance. | 5000 | 0.2 | – | UI |

*Table 68:* **Serial-GMII Protocol Characteristics (PS-GTR Transceivers)**

| Standard | Description | Line Rate (Mb/s) | Min | Max | Units |
|---|---|---|---|---|---|
| **Serial-GMII Transmitter Jitter Generation** | | | | | |
| SGMII | Deterministic transmitter jitter. | 1250 | – | 0.25 | UI |
| **Serial-GMII Receiver High Frequency Jitter Tolerance** | | | | | |
| SGMII | Total receiver jitter tolerance. | 1250 | 0.25 | – | UI |

# PS System Monitor Specifications

*Table 69:* **PS SYSMON Specifications**

| Parameter | Comments | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{CC\_PSADC}$ = 1.8V ±3%, $T_j$ = –40°C to 100°C, typical values at $T_j$ = 40°C | | | | | | |
| **ADC Accuracy ($T_j$ = –55°C to 125°C)** (1) | | | | | | |
| Resolution | | | 10 | – | – | Bits |
| Sample rate | | | – | – | 1 | MS/s |
| RMS code noise | On-chip reference | | – | 1 | – | LSBs |
| **On-Chip Sensor Accuracy** | | | | | | |
| Temperature sensor error | | $T_j$ = –55°C to 110°C | – | – | ±3.5 | °C |
| | | $T_j$ = 110°C to 125°C | – | – | ±5 | °C |
| Supply sensor error(2) | Supply voltages less than or electrically connected to $V_{CC\_PSADC}$. | $T_j$ = –40°C to 125°C | – | – | ±1 | % |
| | Supply voltages nominally at 1.8V but with the potential to go above $V_{CC\_PSADC}$. | $T_j$ = –40°C to 125°C | – | – | ±1.5 | % |
| | Supply voltages nominally in the 2.0V to 3.3V range. | $T_j$ = –40°C to 125°C | – | – | ±2.5 | % |

**Notes:**

1. ADC offset errors are removed by enabling the ADC automatic offset calibration feature. The values are specified for when this feature is enabled.
2. Supply sensor offset and gain errors are removed by enabling the automatic offset and gain calibration feature. The values are specified for when this feature is enabled.

# Output Delay Measurement Methodology

Output delays are measured with short output traces. Standard termination was used for all testing. The propagation delay of the trace is characterized separately and subtracted from the final measurement, and is therefore not included in the generalized test setups shown in Figure 1 and Figure 2.

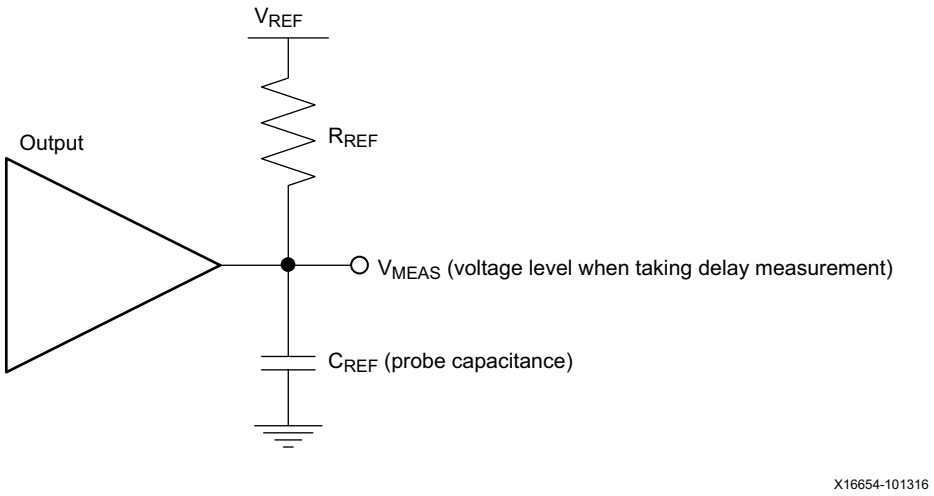


*Figure 1:* **Single-Ended Test Setup**

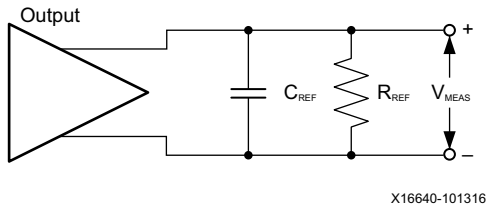


*Figure 2:* **Differential Test Setup**

Parameters $V_{REF}$, $R_{REF}$, $C_{REF}$, and $V_{MEAS}$ fully describe the test conditions for each I/O standard. The most accurate prediction of propagation delay in any given application can be obtained through IBIS simulation, using this method:

1. Simulate the output driver of choice into the generalized test setup using values from Table 79.
2. Record the time to $V_{MEAS}$.
3. Simulate the output driver of choice into the actual PCB trace and load using the appropriate IBIS model or capacitance value to represent the load.
4. Record the time to $V_{MEAS}$.
5. Compare the results of step 2 and step 4. The increase or decrease in delay yields the actual propagation delay of the PCB trace.

# DSP48 Slice Switching Characteristics

*Table 83:* **DSP48 Slice Switching Characteristics**

| Symbol | Description | Speed Grade and $V_{CCINT}$ Operating Voltages | | | | | Units |
|---|---|---|---|---|---|---|---|
| | | 0.90V | 0.85V | | 0.72V | | |
| | | -3 | -2 | -1 | -2 | -1 | |
| **Maximum Frequency** | | | | | | | |
| $F_{MAX}$ | With all registers used. | 891 | 775 | 645 | 644 | 600 | MHz |
| $F_{MAX\_PATDET}$ | With pattern detector. | 794 | 687 | 571 | 562 | 524 | MHz |
| $F_{MAX\_MULT\_NOMREG}$ | Two register multiply without MREG. | 635 | 544 | 456 | 440 | 413 | MHz |
| $F_{MAX\_MULT\_NOMREG\_PATDET}$ | Two register multiply without MREG with pattern detect. | 577 | 492 | 410 | 395 | 371 | MHz |
| $F_{MAX\_PREADD\_NOADREG}$ | Without ADREG. | 655 | 565 | 468 | 453 | 423 | MHz |
| $F_{MAX\_NOPIPELINEREG}$ | Without pipeline registers (MREG, ADREG). | 483 | 410 | 338 | 323 | 304 | MHz |
| $F_{MAX\_NOPIPELINEREG\_PATDET}$ | Without pipeline registers (MREG, ADREG) with pattern detect. | 448 | 379 | 314 | 299 | 280 | MHz |

# Clock Buffers and Networks

*Table 84:* **Clock Buffers Switching Characteristics**

| Symbol | Description | Speed Grade and $V_{CCINT}$ Operating Voltages | | | | | Units |
|---|---|---|---|---|---|---|---|
| | | 0.90V | 0.85V | | 0.72V | | |
| | | -3 | -2 | -1 | -2 | -1 | |
| **Global Clock Switching Characteristics (Including BUFGCTRL)** | | | | | | | |
| $F_{MAX}$ | Maximum frequency of a global clock tree (BUFG). | 891 | 775 | 667 | 725 | 667 | MHz |
| **Global Clock Buffer with Input Divide Capability (BUFGCE_DIV)** | | | | | | | |
| $F_{MAX}$ | Maximum frequency of a global clock buffer with input divide capability (BUFGCE_DIV). | 891 | 775 | 667 | 725 | 667 | MHz |
| **Global Clock Buffer with Clock Enable (BUFGCE)** | | | | | | | |
| $F_{MAX}$ | Maximum frequency of a global clock buffer with clock enable (BUFGCE). | 891 | 775 | 667 | 725 | 667 | MHz |
| **Leaf Clock Buffer with Clock Enable (BUFCE_LEAF)** | | | | | | | |
| $F_{MAX}$ | Maximum frequency of a leaf clock buffer with clock enable (BUFCE_LEAF). | 891 | 775 | 667 | 725 | 667 | MHz |
| **GTH or GTY Clock Buffer with Clock Enable and Clock Input Divide Capability (BUFG_GT)** | | | | | | | |
| $F_{MAX}$ | Maximum frequency of a serial transceiver clock buffer with clock enable and clock input divide capability. | 512 | 512 | 512 | 512 | 512 | MHz |

*Table 91:* **Global Clock Input Setup and Hold With MMCM**

| Symbol | Description | | Device | Speed Grade and $V_{CCINT}$ Operating Voltages | | | | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | | 0.90V | 0.85V | | 0.72V | | |
| | | | | -3 | -2 | -1 | -2 | -1 | |
| **Input Setup and Hold Time Relative to Global Clock Input Signal using SSTL15 Standard.(1)(2)(3)** | | | | | | | | | |
| $T_{PSMMCMCC\_ZU2}$ | Global clock input and input flip-flop (or latch) with MMCM. | Setup | XCZU2 | N/A | 1.83 | 1.96 | 2.29 | 2.48 | ns |
| $T_{PHMMCMCC\_ZU2}$ | | Hold | | | –0.19 | –0.19 | 0.13 | 0.13 | ns |
| $T_{PSMMCMCC\_ZU3}$ | | Setup | XCZU3 | N/A | 1.83 | 1.96 | 2.29 | 2.48 | ns |
| $T_{PHMMCMCC\_ZU3}$ | | Hold | | | –0.19 | –0.19 | 0.13 | 0.13 | ns |
| $T_{PSMMCMCC\_ZU4}$ | | Setup | XCZU4 | 1.96 | 1.96 | 2.10 | 2.49 | 2.59 | ns |
| $T_{PHMMCMCC\_ZU4}$ | | Hold | | –0.12 | –0.12 | –0.12 | 0.27 | 0.48 | ns |
| $T_{PSMMCMCC\_ZU5}$ | | Setup | XCZU5 | 1.96 | 1.96 | 2.10 | 2.49 | 2.59 | ns |
| $T_{PHMMCMCC\_ZU5}$ | | Hold | | –0.12 | –0.12 | –0.12 | 0.27 | 0.48 | ns |
| $T_{PSMMCMCC\_ZU6}$ | | Setup | XCZU6 | 1.97 | 2.00 | 2.12 | 2.26 | 2.44 | ns |
| $T_{PHMMCMCC\_ZU6}$ | | Hold | | –0.11 | –0.11 | –0.11 | 0.16 | 0.18 | ns |
| $T_{PSMMCMCC\_ZU7}$ | | Setup | XCZU7 | 1.91 | 1.91 | 2.02 | 2.45 | 2.70 | ns |
| $T_{PHMMCMCC\_ZU7}$ | | Hold | | –0.14 | –0.14 | –0.14 | 0.37 | 0.38 | ns |
| $T_{PSMMCMCC\_ZU9}$ | | Setup | XCZU9 | 1.97 | 2.00 | 2.12 | 2.26 | 2.44 | ns |
| $T_{PHMMCMCC\_ZU9}$ | | Hold | | –0.11 | –0.11 | –0.11 | 0.16 | 0.18 | ns |
| $T_{PSMMCMCC\_ZU11}$ | | Setup | XCZU11 | 2.08 | 2.08 | 2.23 | 2.59 | 2.75 | ns |
| $T_{PHMMCMCC\_ZU11}$ | | Hold | | –0.08 | –0.08 | 0.04 | 0.35 | 0.74 | ns |
| $T_{PSMMCMCC\_ZU15}$ | | Setup | XCZU15 | 1.96 | 1.99 | 2.12 | 2.26 | 2.44 | ns |
| $T_{PHMMCMCC\_ZU15}$ | | Hold | | –0.10 | –0.10 | –0.10 | 0.17 | 0.19 | ns |
| $T_{PSMMCMCC\_ZU17}$ | | Setup | XCZU17 | 1.89 | 1.89 | 2.03 | 2.36 | 2.55 | ns |
| $T_{PHMMCMCC\_ZU17}$ | | Hold | | –0.16 | –0.16 | –0.16 | 0.31 | 0.34 | ns |
| $T_{PSMMCMCC\_ZU19}$ | | Setup | XCZU19 | 1.89 | 1.89 | 2.03 | 2.36 | 2.55 | ns |
| $T_{PHMMCMCC\_ZU19}$ | | Hold | | –0.16 | –0.16 | –0.16 | 0.31 | 0.34 | ns |

**Notes:**

1. Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, slowest temperature, and slowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, fastest temperature, and fastest voltage.
2. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible I/O and CLB flip-flops are clocked by the global clock net.
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

*Table 114:* **GTY Transceiver User Clock Switching Characteristics[1] *(Cont'd)***

| Symbol | Description | Data Width Conditions (Bit) | | Speed Grade and $V_{CCINT}$ Operating Voltages | | | | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | | 0.90V | 0.85V | | 0.72V | | |
| | | Internal Logic | Interconnect Logic | -3[2] | -2[2][3] | -1[4][5] | -2[3] | -1[5] | |
| $F_{TXIN2}$ | TXUSRCLK2[6] maximum frequency | 16 | 16 | 511.719 | 511.719 | 390.625 | 390.625 | 322.266 | MHz |
| | | 16 | 32 | 255.859 | 255.859 | 195.313 | 195.313 | 161.133 | MHz |
| | | 32 | 32 | 511.719 | 511.719 | 390.625 | 390.625 | 322.266 | MHz |
| | | 32 | 64 | 255.859 | 255.859 | 195.313 | 195.313 | 161.133 | MHz |
| | | 64 | 64 | 511.719 | 440.781 | 402.832 | 402.832 | 195.313 | MHz |
| | | 64 | 128 | 255.859 | 220.391 | 201.416 | 201.416 | 97.656 | MHz |
| | | 20 | 20 | 409.375 | 409.375 | 312.500 | 312.500 | 257.813 | MHz |
| | | 20 | 40 | 204.688 | 204.688 | 156.250 | 156.250 | 128.906 | MHz |
| | | 40 | 40 | 409.375 | 409.375 | 312.500 | 350.000 | 257.813 | MHz |
| | | 40 | 80 | 204.688 | 204.688 | 156.250 | 175.000 | 128.906 | MHz |
| | | 80 | 80 | 409.375 | 352.625 | 322.266 | 352.625 | 156.250 | MHz |
| | | 80 | 160 | 204.688 | 176.313 | 161.133 | 176.313 | 78.125 | MHz |
| $F_{RXIN2}$ | RXUSRCLK2[6] maximum frequency | 16 | 16 | 511.719 | 511.719 | 390.625 | 390.625 | 322.266 | MHz |
| | | 16 | 32 | 255.859 | 255.859 | 195.313 | 195.313 | 161.133 | MHz |
| | | 32 | 32 | 511.719 | 511.719 | 390.625 | 390.625 | 322.266 | MHz |
| | | 32 | 64 | 255.859 | 255.859 | 195.313 | 195.313 | 161.133 | MHz |
| | | 64 | 64 | 511.719 | 440.781 | 402.832 | 402.832 | 195.313 | MHz |
| | | 64 | 128 | 255.859 | 220.391 | 201.416 | 201.416 | 97.656 | MHz |
| | | 20 | 20 | 409.375 | 409.375 | 312.500 | 312.500 | 257.813 | MHz |
| | | 20 | 40 | 204.688 | 204.688 | 156.250 | 156.250 | 128.906 | MHz |
| | | 40 | 40 | 409.375 | 409.375 | 312.500 | 350.000 | 257.813 | MHz |
| | | 40 | 80 | 204.688 | 204.688 | 156.250 | 175.000 | 128.906 | MHz |
| | | 80 | 80 | 409.375 | 352.625 | 322.266 | 352.625 | 156.250 | MHz |
| | | 80 | 160 | 204.688 | 176.313 | 161.133 | 176.313 | 78.125 | MHz |

**Notes:**

1. Clocking must be implemented as described in the *UltraScale Architecture GTY Transceiver User Guide* (UG578).
2. For speed grades -3E, -2E, and -2I, a 16-bit and 20-bit internal data path can only be used for line rates less than 8.1875 Gb/s.
3. For speed grade -2LE, a 16-bit and 20-bit internal data path can only be used for line rates less than 8.1875 Gb/s when $V_{CCINT}$ = 0.85V or 6.25 Gb/s when $V_{CCINT}$ = 0.72V.
4. For speed grades -1E and -1I, a 16-bit and 20-bit internal data path can only be used for line rates less than 6.25 Gb/s.
5. For speed grade -1LI, a 16-bit and 20-bit internal data path can only be used for line rates less than 6.25 Gb/s when $V_{CCINT}$ = 0.85V or 5.15625 Gb/s when $V_{CCINT}$ = 0.72V.
6. When the gearbox is used, these maximums refer to the XCLK. For more information, see the *Valid Data Width Combinations for TX Asynchronous Gearbox* table in the *UltraScale Architecture GTY Transceiver User Guide* (UG578).

*Table 117:* **GTY Transceiver Protocol List *(Cont'd)***

| Protocol | Specification | Serial Rate (Gb/s) | Electrical Compliance |
|---|---|---|---|
| Serial RapidIO | RapidIO specification 3.1 | 1.25–10.3125 | Compliant |
| DisplayPort | DP 1.2B CTS | 1.62–5.4 | Compliant(3) |
| Fibre channel | FC-PI-4 | 1.0625–14.025 | Compliant |
| SATA Gen1, 2, 3 | Serial ATA revision 3.0 specification | 1.5, 3.0, and 6.0 | Compliant |
| SAS Gen1, 2, 3 | T10/BSR INCITS 519 | 3.0, 6.0, and 12.0 | Compliant |
| SFI-5 | OIF-SFI5-01.0 | 0.625 - 12.5 | Compliant |
| Aurora | CEI-6G, CEI-11G-LR | All rates | Compliant |

**Notes:**

1. 25 dB loss at Nyquist without FEC.
2. The transition time of the transmitter is faster than the IEEE Std 802.3-2012 specification.
3. This protocol requires external circuitry to achieve compliance.

# PL SYSMON I2C/PMBus Interfaces

*Table 125:* **PL SYSMON I2C Fast Mode Interface Switching Characteristics(1)**

| Symbol | Description | Min | Max | Units |
|---|---|---|---|---|
| $T_{SMFCKL}$ | SCL Low time | 1.3 | – | µs |
| $T_{SMFCKH}$ | SCL High time | 0.6 | – | µs |
| $T_{SMFCKO}$ | SDAO clock-to-out delay | – | 900 | ns |
| $T_{SMFDCK}$ | SDAI setup time | 100 | – | ns |
| $F_{SMFCLK}$ | SCL clock frequency | – | 400 | kHz |

**Notes:**
1. The test conditions are configured to the LVCMOS 1.8V I/O standard.

*Table 126:* **PL SYSMON I2C Standard Mode Interface Switching Characteristics(1)**

| Symbol | Description | Min | Max | Units |
|---|---|---|---|---|
| $T_{SMSCKL}$ | SCL Low time | 4.7 | – | µs |
| $T_{SMSCKH}$ | SCL High time | 4.0 | – | µs |
| $T_{SMSCKO}$ | SDAO clock-to-out delay | – | 3450 | ns |
| $T_{SMSDCK}$ | SDAI setup time | 250 | – | ns |
| $F_{SMSCLK}$ | SCL clock frequency | – | 100 | kHz |

**Notes:**
1. The test conditions are configured to the LVCMOS 1.8V I/O standard.

# Revision History

The following table shows the revision history for this document.

| Date | Version | Description of Revisions |
|---|---|---|
| 04/20/2017 | 1.3 | Updated Table 25, Table 26, and Table 27 to production release for the following devices/speed/temperature grades in Vivado Design Suite 2017.1.<br>XCZU2CG and XCZU2EG: –2E, -2I, -1E, -1I<br>XCZU3CG and XCZU3EG: –2E, -2I, -1E, -1I<br>XCZU6CG and XCZU6EG: –2E, -2I, -1E, -1I<br>XCZU9CG and XCZU9EG: –2E, -2I, -1E, -1I<br>Added -2E ($V_{CCINT}$ = 0.85V) speed grade where applicable. Removed -3E speed grade from the XCZU2 and XCZU3 devices in Table 26 and where applicable.<br>In Table 1, updated values and Note 2. In Table 2, added or updated many of the notes. Updated Table 4 including the notes and added Note 6. Moved and updated Table 5. Added Table 8. Updated Table 9 and added Note 4. Updated Table 10 and added Note 1.<br>Revised $V_{ICM}$ in Table 23. Updated Table 30 and removed Note 1. Added Table 31 and Table 32. Updated Table 33 and removed $F_{FTMCLK}$. Updated $T_{RFPSCLK}$ in Table 34. Updated Note 1 in Table 37. Updated Table 39. Removed the *PS NAND Memory Controller Interface* section. Significant changes to Table 41 and removed Note 3. Significant changes to Table 42 and updated Note 1. Removed $F_{TSU\_REF\_CLK}$ from Table 44. Revised Table 45 and added Note 2 and Note 3. Revised Table 46 and added Note 2 and Note 3. Updated Table 48. Updated Table 51 and removed Note 2. Revised Table 52. Revised many of the tables in the PS-GTR Transceiver section. Revised Table 70 and Table 71. Removed Note 8 from Table 74.<br>Updated the values in Table 75, Table 76, Table 77, Table 80, Table 87, Table 88, Table 89, Table 90,and Table 91 to the Vivado Design Suite 2017.1 speed specifications.<br>Updated the values in Table 81 and Table 82. Added values to Table 92. Updated Table 93. Revised $D_{VPPOUT}$ in Table 94. Update the values in Table 96. Added Note 6 to Table 102. Updated Table 103 and Table 104. Revised $D_{VPPOUT}$ in Table 106. Updated the values in Table 108. In Table 109 updated the -1 (0.85V) specifications and removed Note 1. In Table 114 updated the -1 (0.85V) specifications and added Note 6. In Table 115 and Table 116, added the 28.21 jitter tolerance values and revised the notes. Revised the Integrated Interface Block for Interlaken and Integrated Interface Block for 100G Ethernet MAC and PCS sections. Revised the Configuration Switching Characteristics section. Removed the *eFUSE Programming Conditions* table and added the specifications to Table 2 and Table 3. |

| Date | Version | Description of Revisions |
|---|---|---|
| 02/10/2017 | 1.2 | Updated some of the maximum voltages in the Processor System (PS) section and other specifications in the Programmable Logic (PL) and GTH or GTY Transceiver sections of Table 1. Updated Table 2, Table 4, Table 6, Table 7, and Table 9. Revised the Power Supply Sequencing section including Table 10. Added PS and VCU ramp times to Table 11. Revised $V_{ODIFF}$ in Table 24. Updated Table 25. Added Note 1 to Table 26. Table 30 replaces the previous three PS memory performance tables. Added values to Table 34, Table 37, and Table 38. Deleted the waveforms in the PS Switching Characteristics section (Figures 1-16 and Figures 25-26). Revised values in the *PS NAND Memory Controller Interface* section. Added and updated data in Table 40. Added Note 3 to Table 41. Added Note 3 to Table 42. Added Note 1 to Table 45. Updated Table 48 and removed Note 3. Added data to Table 56. Updated Table 60. Added Table 61. Updated Table 63. Revised Table 69. Added data to Table 70. Added Note 2 to Table 71. Updated Table 74 and added Note 4. Updated $V_L$ and $V_H$ values in Table 78. Added $T_{MINPER\_CLK}$, revised $F_{REFCLK}$, and Note 1 to Table 82. Added MMCM_$F_{DPRCLK_MAX}$ to Table 85 and PLL_$F_{DPRCLK_MAX}$ to Table 86. Added data to Table 94, Table 96, Table 98, Table 101, and updated the note references in Table 102. Updated Table 103 and added Note 8. Updated Table 104 and added Note 7. Added more protocols, Note 1 and Note 2 to Table 105. Removed the *GTH Transceiver Protocol Jitter Characteristics* section because it is covered in Table 105. Added Note 1 to Table 109. Added data to Table 106, Table 108, Table 110, Table 113. Added Note 2 to Table 112. Added note references in Table 114. Updated Table 115 and added Note 8. Updated Table 116 and added Note 7. Added more protocols and Note 3 to Table 117. Removed the *GTY Transceiver Protocol Jitter Characteristics* section because it is covered in Table 117. Revised Table 124. Added $T_{POR}$ and updated $F_{ICAPCK}$ in Table 127. Updated the Automotive Applications Disclaimer. |
| 06/20/2016 | 1.1 | Updated the Summary description. In Table 1, revised $V_{IN}$ for HP I/O banks and added clarifications to some descriptions and symbols. Added $I_{RPU}$, $I_{RPD}$, and Note 4 to Table 2 and updated $V_{PS\_MGTRAVCC}$, the PL System Monitor section, and Note 3 and Note 5. Updated Note 5 in Table 4. Updated the PS Power-On/Off Power Supply Sequencing section including all the voltage supply names. Added MIPI_DPHY_DCI to Table 14, Table 15, and Table 17. Updated Table 23, including removing the $V_{CCO}$ specification and adding Note 1. Added Note 1 to Table 24. Updated Table 25 speed specifications for Vivado Design Suite 2016.1. Added values to Table 28. Updated the -2 value in Table 29. Added $F_{DPLIVEVIDEO}$ and updated $F_{FCIDMACLK}$ in Table 33. Added VCO frequencies to Table 36. Added the $T_{PSPOR}$ minimum to Table 37 and updated Note 1. Added Table 38. Added value delineation over $V_{CCINT}$ operating voltages in Table 39. Revised values for $F_{TCK}$ and $T_{TAPTCK}/T_{TCKTAP}$ in Table 40 and added value delineation over $V_{CCINT}$ operating voltages. Updated the *PS NAND Memory Controller Interface* section. Revised some units and Note 1 in Table 41 and Table 42. Removed Figure 6: Quad-SPI Interface (Feedback Clock Disabled) Timing. Updated Note 1 of Table 43. Added $F_{TSI\_REF\_CLK}$ to Table 44 and updated Note 1. In Table 45, revised $T_{DCSDHSCLK1}$, $T_{DCSDHSCLK2}$, and $T_{DCSDHSCLK3}$ and Note 1. In Table 46, revised Note 1. In Table 47, revised Note 1. Revised Table 48, including Note 1, and added Note 2 and Note 3. In Table 49, Table 50, Table 51, and Table 53, revised Note 1. Updated Table 71. Replaced Table 74. Updated Table 75 and Table 76. Updated Table 78 and Table 79. In Table 80, added the Block RAM and FIFO Clock-to-Out Delays section. Updated the $R_{IN}$ and $C_{EXT}$ values in Table 57 and Table 95. Updated the -2 (0.72V) and -1 (0.72V) values and added Note 1 to Table 97. Added Table 100 and Table 112. Added Note 2 to Table 106. Revised data in Table 109. Revised Table 114. Revised data and added notes in the Integrated Interface Block for Interlaken section and Table 121. Moved Table 123. Revised INL in Table 124. Added notes to Table 125 and Table 126. In the *eFUSE and Programming Conditions* table, updated the $I_{PSFS}$ description. |
| 11/24/2015 | 1.0 | Initial Xilinx release. |

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