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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	162000
Number of Logic Elements/Cells	2835000
Total RAM Bits	396150400
Number of I/O	448
Number of Gates	-
Voltage - Supply	0.873V ~ 0.927V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 100°C (TJ)
Package / Case	2577-BBGA, FCBGA
Supplier Device Package	2577-FCBGA (52.5x52.5)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xcvu11p-3flga2577e

Recommended Operating Conditions

Table 2: Recommended Operating Conditions⁽¹⁾⁽²⁾

Symbol	Description	Min	Typ	Max	Units
FPGA Logic					
V_{CCINT}	Internal supply voltage.	0.825	0.850	0.876	V
	For -2LE ($V_{CCINT} = 0.72V$) devices: internal supply voltage.	0.698	0.720	0.742	V
	For -3E devices: internal supply voltage.	0.873	0.900	0.927	V
$V_{CCINT_IO}^{(3)}$	Internal supply voltage for the I/O banks.	0.825	0.850	0.876	V
	For -2LE devices ($V_{CCINT} = 0.85V$): internal supply voltage for the I/O banks.	0.825	0.850	0.876	V
	For -3E devices: internal supply voltage for the I/O banks.	0.873	0.900	0.927	V
V_{CCBRAM}	Block RAM supply voltage.	0.825	0.850	0.876	V
	For -3E devices: block RAM supply voltage.	0.873	0.900	0.927	V
V_{CCAUX}	Auxiliary supply voltage.	1.746	1.800	1.854	V
$V_{CCO}^{(4)(5)}$	Supply voltage for I/O banks.	0.950	–	1.900	V
$V_{CCAUX_IO}^{(6)}$	Auxiliary I/O supply voltage.	1.746	1.800	1.854	V
$V_{IN}^{(7)}$	I/O input voltage.	–0.200	–	$V_{CCO} + 0.200$	V
$I_{IN}^{(8)}$	Maximum current through any pin in a powered or unpowered bank when forward biasing the clamp diode.	–	–	10	mA
$V_{BATT}^{(9)}$	Battery voltage.	1.000	–	1.890	V
GTy Transceiver					
$V_{MGTAVCC}^{(10)}$	Analog supply voltage for the GTy transceiver.	0.873	0.900	0.927	V
$V_{MGTAVTT}^{(10)}$	Analog supply voltage for the GTy transmitter and receiver termination circuits.	1.164	1.20	1.236	V
$V_{MGTVCCAUX}^{(10)}$	Auxiliary analog QPLL voltage supply for the transceivers.	1.746	1.80	1.854	V
$V_{MGTAVTTRCAL}^{(10)}$	Analog supply voltage for the resistor calibration circuit of the GTy transceiver column.	1.164	1.20	1.236	V

Table 2: Recommended Operating Conditions⁽¹⁾⁽²⁾ (Cont'd)

Symbol	Description	Min	Typ	Max	Units
SYSMON					
V _{CCADC}	SYSMON supply relative to GNDADC.	1.746	1.800	1.854	V
V _{REFP}	SYSMON externally supplied reference voltage relative to GNDADC.	1.200	1.250	1.300	V
Temperature					
T _j ⁽¹¹⁾	Junction temperature operating range for extended (E) temperature devices. ⁽¹²⁾	0	–	100	°C
	Junction temperature operating range for industrial (I) temperature devices.	–40	–	100	°C
	Junction temperature operating range for eFUSE programming. ⁽¹³⁾	–40	–	125	°C

Notes:

- All voltages are relative to GND.
- For the design of the power distribution system consult *UltraScale Architecture PCB Design Guide* ([UG583](#)).
- V_{CCINT_IO} must be connected to V_{CCBRAM}.
- For V_{CCO_0}, the minimum recommended operating voltage for power on and during configuration is 1.425V. After configuration, data is retained even if V_{CCO} drops to 0V.
- Includes V_{CCO} of 1.0V, 1.2V, 1.35V, 1.5V, and 1.8V.
- V_{CCAUX_IO} must be connected to V_{CCAUX}.
- The lower absolute voltage specification always applies.
- A total of 200 mA per bank should not be exceeded.
- If battery is not used, connect V_{BATT} to either GND or V_{CCAUX}.
- Each voltage listed requires filtering as described in the *UltraScale Architecture GTY Transceiver User Guide* ([UG578](#)).
- Xilinx recommends measuring the T_j of a device using the system monitor as described in the *UltraScale Architecture System Monitor User Guide* ([UG580](#)). The SYSMON temperature measurement errors (that are described in [Table 58](#)) must be accounted for in your design. For example, by using an external reference of 1.25V, when SYSMON reports 97°C, there is a measurement error ±3°C. A reading of 97°C is considered the maximum adjusted T_j (100°C – 3°C = 97°C).
- Devices labeled with the speed/temperature grade of -2LE can operate for a limited time at a junction temperature of 110°C. Timing parameters adhere to the same speed file at 110°C as they do below 110°C, regardless of operating voltage (nominal voltage of 0.85V or a low-voltage of 0.72V). Operation at T_j = 110°C is limited to 1% of the device lifetime and can occur sequentially or at regular intervals as long as the total time does not exceed 1% of the device lifetime.
- Do not program eFUSE during device configuration (e.g., during configuration, during configuration readback, or when readback CRC is active).

V_{IN} Maximum Allowed AC Voltage Overshoot and Undershoot

Table 4: V_{IN} Maximum Allowed AC Voltage Overshoot and Undershoot for HP I/O Banks⁽¹⁾⁽²⁾

AC Voltage Overshoot	% of UI at –40°C to 100°C	AC Voltage Undershoot	% of UI at –40°C to 100°C
V _{CCO} + 0.30	100%	–0.30	100%
V _{CCO} + 0.35	100%	–0.35	90%
V _{CCO} + 0.40	92%	–0.40	92%
V _{CCO} + 0.45	50%	–0.45	50%
V _{CCO} + 0.50	20%	–0.50	20%
V _{CCO} + 0.55	10%	–0.55	10%
V _{CCO} + 0.60	6%	–0.60	6%
V _{CCO} + 0.65	2%	–0.65	2%
V _{CCO} + 0.70	2%	–0.70	2%

Notes:

1. A total of 200 mA per bank should not be exceeded.
2. For UI smaller than 20 μs.

Quiescent Supply Current

Table 5: Typical Quiescent Supply Current⁽¹⁾⁽²⁾⁽³⁾

Symbol	Description	Device	Speed Grade and V _{CCINT} Operating Voltages				Units
			0.90V	0.85V		0.72V	
			-3	-2	-1	-2	
I _{CCINTQ}	Quiescent V _{CCINT} supply current.	XCVU3P	2384	2276	2276	2017	mA
		XCVU5P	4769	4552	4552	4034	mA
		XCVU7P	4769	4552	4552	4034	mA
		XCVU9P	7153	6828	6828	6050	mA
		XCVU11P	7567	7202	7202	6332	mA
		XCVU13P	10090	9602	9602	8442	mA
I _{CCINT_IOQ}	Quiescent current for V _{CCINT_IO} supply.	XCVU3P	149	144	144	144	mA
		XCVU5P	298	287	287	287	mA
		XCVU7P	298	287	287	287	mA
		XCVU9P	447	431	431	431	mA
		XCVU11P	182	176	176	176	mA
		XCVU13P	243	234	234	234	mA
I _{CCOQ}	Quiescent V _{CCO} supply current.	All devices	1	1	1	1	mA
I _{CCAUXQ}	Quiescent V _{CCAUX} supply current.	XCVU3P	268	268	268	268	mA
		XCVU5P	535	535	535	535	mA
		XCVU7P	535	535	535	535	mA
		XCVU9P	1015	1015	1015	1015	mA
		XCVU11P	819	819	819	819	mA
		XCVU13P	1091	1091	1091	1091	mA

Table 13: DC Output Levels for Single-ended and Differential POD10 and POD12 Standards⁽¹⁾⁽²⁾

Symbol	Description	V_{OUT}	Min	Typ	Max	Units
R_{OL}	Pull-down resistance.	V_{OM_DC} (as described in Table 14)	36	40	44	Ω
R_{OH}	Pull-up resistance.	V_{OM_DC} (as described in Table 14)	36	40	44	Ω

Notes:

1. Tested according to relevant specifications.
2. Standards specified using the default I/O standard configuration. For details, see the *UltraScale Architecture SelectIO Resources User Guide* (UG571).

Table 14: Table 13 Definitions for DC Output Levels for POD Standards

Symbol	Description	All Speed Grades	Units
V_{OM_DC}	DC output Mid measurement level (for IV curve linearity).	$0.8 \times V_{CCO}$	V

LVDS DC Specifications (LVDS)

Table 15: LVDS DC Specifications

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{CCO} ⁽¹⁾	Supply voltage.		1.710	1.800	1.890	V
V_{ODIFF} ⁽²⁾	Differential output voltage: ($Q - \bar{Q}$), $Q = \text{High}$ ($\bar{Q} - Q$), $\bar{Q} = \text{High}$	$R_T = 100\Omega$ across Q and $\bar{Q}$ signals	247	350	454	mV
V_{OCM} ⁽²⁾	Output common-mode voltage.	$R_T = 100\Omega$ across Q and $\bar{Q}$ signals	1.000	1.250	1.425	V
V_{IDIFF}	Differential input voltage: ($Q - \bar{Q}$), $Q = \text{High}$ ($\bar{Q} - Q$), $\bar{Q} = \text{High}$		100	350	600 ⁽³⁾	mV
V_{ICM_DC} ⁽⁴⁾	Input common-mode voltage (DC coupling).		0.300	1.200	1.425	V
V_{ICM_AC} ⁽⁵⁾	Input common-mode voltage (AC coupling).		0.600	–	1.100	V

Notes:

1. In I/O banks, when LVDS is used with input-only functionality, it can be placed in a bank where the V_{CCO} levels are different from the specified level only if internal differential termination is not used. In this scenario, V_{CCO} must be chosen to ensure the input pin voltage levels do not violate the *Recommended Operating Condition* (Table 2) specification for the V_{IN} I/O pin voltage.
2. V_{OCM} and V_{ODIFF} values are for LVDS_PRE_EMPHASIS = FALSE.
3. Maximum V_{IDIFF} value is specified for the maximum V_{ICM} specification. With a lower V_{ICM} , a higher V_{IDIFF} is tolerated only when the recommended operating conditions and overshoot/undershoot V_{IN} specifications are maintained.
4. Input common mode voltage for DC coupled configurations. EQUALIZATION = EQ_NONE (Default).
5. External input common mode voltage specification for AC coupled configurations. EQUALIZATION = EQ_LEVEL0, EQ_LEVEL1, EQ_LEVEL2, EQ_LEVEL3, EQ_LEVEL4.

Speed Grade Designations

Since individual family members are produced at different times, the migration from one category to another depends completely on the status of the fabrication process for each device. Table 16 correlates the current status of the Virtex UltraScale+ FPGA on a per speed grade basis.

Table 17: Speed Grade Designations by Device

Device	Speed Grade, Temperature Ranges, and V_{CCINT} Operating Voltages		
	Advance	Preliminary	Production
XCVU3P	-3E ($V_{CCINT} = 0.90V$) -2LE ($V_{CCINT} = 0.85V$) -2LE ($V_{CCINT} = 0.72V$) ⁽¹⁾		-2I ($V_{CCINT} = 0.85V$) -1E ($V_{CCINT} = 0.85V$) -1I ($V_{CCINT} = 0.85V$)
XCVU5P	-3E ($V_{CCINT} = 0.90V$) -2I ($V_{CCINT} = 0.85V$), -2LE ($V_{CCINT} = 0.85V$) -1E ($V_{CCINT} = 0.85V$), -1I ($V_{CCINT} = 0.85V$) -2LE ($V_{CCINT} = 0.72V$) ⁽¹⁾		
XCVU7P	-3E ($V_{CCINT} = 0.90V$) -2I ($V_{CCINT} = 0.85V$), -2LE ($V_{CCINT} = 0.85V$) -1E ($V_{CCINT} = 0.85V$), -1I ($V_{CCINT} = 0.85V$) -2LE ($V_{CCINT} = 0.72V$) ⁽¹⁾		
XCVU9P	-3E ($V_{CCINT} = 0.90V$) -2I ($V_{CCINT} = 0.85V$), -2LE ($V_{CCINT} = 0.85V$) -1E ($V_{CCINT} = 0.85V$), -1I ($V_{CCINT} = 0.85V$) -2LE ($V_{CCINT} = 0.72V$) ⁽¹⁾		
XCVU11P	-3E ($V_{CCINT} = 0.90V$) -2I ($V_{CCINT} = 0.85V$), -2LE ($V_{CCINT} = 0.85V$) -1E ($V_{CCINT} = 0.85V$), -1I ($V_{CCINT} = 0.85V$), -2LE ($V_{CCINT} = 0.72V$) ⁽¹⁾		
XCVU13P	-3E ($V_{CCINT} = 0.90V$) -2I ($V_{CCINT} = 0.85V$), -2LE ($V_{CCINT} = 0.85V$) -1E ($V_{CCINT} = 0.85V$), -1I ($V_{CCINT} = 0.85V$) -2LE ($V_{CCINT} = 0.72V$) ⁽¹⁾		

Notes:

1. The lowest power -2L devices, where $V_{CCINT} = 0.72V$, are listed in the Vivado Design Suite as -2LV.

Table 24: IOB High Performance (HP) Switching Characteristics (Cont'd)

I/O Standards	T _{INBUF_DELAY_PAD_I}				T _{OUTBUF_DELAY_O_PAD}				T _{OUTBUF_DELAY_TD_PAD}				Units
	0.90V	0.85V		0.72V	0.90V	0.85V		0.72V	0.90V	0.85V		0.72V	
	-3	-2	-1	-2	-3	-2	-1	-2	-3	-2	-1	-2	
DIFF_POD10_DCI_F	0.411	0.411	0.430	0.411	0.425	0.425	0.444	0.425	0.555	0.555	0.584	0.555	ns
DIFF_POD10_DCI_M	0.411	0.411	0.430	0.411	0.542	0.542	0.571	0.542	0.640	0.640	0.681	0.640	ns
DIFF_POD10_DCI_S	0.411	0.411	0.430	0.411	0.754	0.754	0.815	0.754	0.850	0.850	0.917	0.850	ns
DIFF_POD10_F	0.411	0.411	0.433	0.411	0.438	0.438	0.459	0.438	0.569	0.569	0.601	0.569	ns
DIFF_POD10_M	0.411	0.411	0.433	0.411	0.538	0.538	0.568	0.538	0.630	0.630	0.667	0.630	ns
DIFF_POD10_S	0.411	0.411	0.433	0.411	0.766	0.766	0.821	0.766	0.836	0.836	0.894	0.836	ns
DIFF_POD12_DCI_F	0.407	0.407	0.432	0.407	0.425	0.425	0.443	0.425	0.558	0.558	0.586	0.558	ns
DIFF_POD12_DCI_M	0.407	0.407	0.432	0.407	0.543	0.543	0.572	0.543	0.638	0.638	0.678	0.638	ns
DIFF_POD12_DCI_S	0.407	0.407	0.432	0.407	0.772	0.772	0.822	0.772	0.862	0.862	0.929	0.862	ns
DIFF_POD12_F	0.409	0.409	0.430	0.409	0.455	0.455	0.476	0.455	0.595	0.595	0.626	0.595	ns
DIFF_POD12_M	0.409	0.409	0.430	0.409	0.551	0.551	0.582	0.551	0.641	0.641	0.679	0.641	ns
DIFF_POD12_S	0.409	0.409	0.430	0.409	0.767	0.767	0.817	0.767	0.832	0.832	0.889	0.832	ns
DIFF_SSTL12_DCI_F	0.381	0.381	0.400	0.381	0.425	0.425	0.443	0.425	0.558	0.558	0.586	0.558	ns
DIFF_SSTL12_DCI_M	0.381	0.381	0.400	0.381	0.557	0.557	0.587	0.557	0.654	0.654	0.694	0.654	ns
DIFF_SSTL12_DCI_S	0.381	0.381	0.400	0.381	0.754	0.754	0.803	0.754	0.842	0.842	0.908	0.842	ns
DIFF_SSTL12_F	0.394	0.394	0.402	0.394	0.412	0.412	0.430	0.412	0.538	0.538	0.566	0.538	ns
DIFF_SSTL12_M	0.394	0.394	0.402	0.394	0.553	0.553	0.584	0.553	0.641	0.641	0.676	0.641	ns
DIFF_SSTL12_S	0.394	0.394	0.402	0.394	0.758	0.758	0.808	0.758	0.823	0.823	0.879	0.823	ns
DIFF_SSTL135_DCI_F	0.371	0.371	0.402	0.371	0.411	0.411	0.428	0.411	0.537	0.537	0.565	0.537	ns
DIFF_SSTL135_DCI_M	0.371	0.371	0.402	0.371	0.551	0.551	0.582	0.551	0.645	0.645	0.685	0.645	ns
DIFF_SSTL135_DCI_S	0.371	0.371	0.402	0.371	0.746	0.746	0.799	0.746	0.829	0.829	0.893	0.829	ns
DIFF_SSTL135_F	0.375	0.375	0.402	0.375	0.408	0.408	0.428	0.408	0.528	0.528	0.561	0.528	ns
DIFF_SSTL135_M	0.375	0.375	0.402	0.375	0.555	0.555	0.585	0.555	0.641	0.641	0.679	0.641	ns
DIFF_SSTL135_S	0.375	0.375	0.402	0.375	0.772	0.772	0.823	0.772	0.827	0.827	0.878	0.827	ns
DIFF_SSTL15_DCI_F	0.397	0.397	0.417	0.397	0.412	0.412	0.429	0.412	0.531	0.531	0.563	0.531	ns
DIFF_SSTL15_DCI_M	0.397	0.397	0.417	0.397	0.553	0.553	0.583	0.553	0.645	0.645	0.685	0.645	ns
DIFF_SSTL15_DCI_S	0.397	0.397	0.417	0.397	0.768	0.768	0.822	0.768	0.847	0.847	0.912	0.847	ns
DIFF_SSTL15_F	0.404	0.404	0.417	0.404	0.424	0.424	0.445	0.424	0.551	0.551	0.577	0.551	ns
DIFF_SSTL15_M	0.404	0.404	0.417	0.404	0.554	0.554	0.585	0.554	0.639	0.639	0.677	0.639	ns
DIFF_SSTL15_S	0.404	0.404	0.417	0.404	0.767	0.767	0.817	0.767	0.813	0.813	0.867	0.813	ns
DIFF_SSTL18_I_DCI_F	0.320	0.320	0.336	0.320	0.445	0.445	0.461	0.445	0.566	0.566	0.595	0.566	ns
DIFF_SSTL18_I_DCI_M	0.320	0.320	0.336	0.320	0.554	0.554	0.585	0.554	0.644	0.644	0.683	0.644	ns
DIFF_SSTL18_I_DCI_S	0.320	0.320	0.336	0.320	0.762	0.762	0.818	0.762	0.837	0.837	0.899	0.837	ns
DIFF_SSTL18_I_F	0.316	0.316	0.336	0.316	0.454	0.454	0.476	0.454	0.578	0.578	0.608	0.578	ns
DIFF_SSTL18_I_M	0.316	0.316	0.336	0.316	0.571	0.571	0.603	0.571	0.652	0.652	0.692	0.652	ns
DIFF_SSTL18_I_S	0.316	0.316	0.336	0.316	0.782	0.782	0.835	0.782	0.816	0.816	0.870	0.816	ns
HSLVDCI_15_F	0.393	0.393	0.415	0.393	0.425	0.425	0.443	0.425	0.548	0.548	0.579	0.548	ns
HSLVDCI_15_M	0.393	0.393	0.415	0.393	0.552	0.552	0.581	0.552	0.644	0.644	0.684	0.644	ns
HSLVDCI_15_S	0.393	0.393	0.415	0.393	0.748	0.748	0.802	0.748	0.827	0.827	0.890	0.827	ns
HSLVDCI_18_F	0.424	0.424	0.447	0.424	0.445	0.445	0.461	0.445	0.566	0.566	0.595	0.566	ns
HSLVDCI_18_M	0.424	0.424	0.447	0.424	0.567	0.567	0.598	0.567	0.658	0.658	0.699	0.658	ns

Table 24: IOB High Performance (HP) Switching Characteristics (Cont'd)

I/O Standards	T _{INBUF_DELAY_PAD_I}				T _{OUTBUF_DELAY_O_PAD}				T _{OUTBUF_DELAY_TD_PAD}				Units
	0.90V	0.85V		0.72V	0.90V	0.85V		0.72V	0.90V	0.85V		0.72V	
	-3	-2	-1	-2	-3	-2	-1	-2	-3	-2	-1	-2	
POD12_DCI_F	0.409	0.409	0.431	0.409	0.425	0.425	0.443	0.425	0.558	0.558	0.586	0.558	ns
POD12_DCI_M	0.409	0.409	0.431	0.409	0.543	0.543	0.572	0.543	0.638	0.638	0.678	0.638	ns
POD12_DCI_S	0.409	0.409	0.431	0.409	0.772	0.772	0.822	0.772	0.862	0.862	0.929	0.862	ns
POD12_F	0.409	0.409	0.431	0.409	0.455	0.455	0.476	0.455	0.595	0.595	0.626	0.595	ns
POD12_M	0.409	0.409	0.431	0.409	0.551	0.551	0.582	0.551	0.641	0.641	0.679	0.641	ns
POD12_S	0.409	0.409	0.431	0.409	0.767	0.767	0.817	0.767	0.832	0.832	0.889	0.832	ns
SLVS_400_18	0.539	0.539	0.620	0.539	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	ns
SSTL12_DCI_F	0.381	0.381	0.399	0.381	0.425	0.425	0.443	0.425	0.558	0.558	0.586	0.558	ns
SSTL12_DCI_M	0.381	0.381	0.399	0.381	0.557	0.557	0.587	0.557	0.654	0.654	0.694	0.654	ns
SSTL12_DCI_S	0.381	0.381	0.399	0.381	0.754	0.754	0.803	0.754	0.842	0.842	0.908	0.842	ns
SSTL12_F	0.403	0.403	0.403	0.403	0.412	0.412	0.430	0.412	0.538	0.538	0.566	0.538	ns
SSTL12_M	0.403	0.403	0.403	0.403	0.553	0.553	0.584	0.553	0.641	0.641	0.676	0.641	ns
SSTL12_S	0.403	0.403	0.403	0.403	0.758	0.758	0.808	0.758	0.823	0.823	0.879	0.823	ns
SSTL135_DCI_F	0.366	0.366	0.399	0.366	0.411	0.411	0.428	0.411	0.537	0.537	0.565	0.537	ns
SSTL135_DCI_M	0.366	0.366	0.399	0.366	0.551	0.551	0.582	0.551	0.645	0.645	0.685	0.645	ns
SSTL135_DCI_S	0.366	0.366	0.399	0.366	0.746	0.746	0.799	0.746	0.829	0.829	0.893	0.829	ns
SSTL135_F	0.378	0.378	0.399	0.378	0.408	0.408	0.428	0.408	0.528	0.528	0.561	0.528	ns
SSTL135_M	0.378	0.378	0.399	0.378	0.555	0.555	0.585	0.555	0.641	0.641	0.679	0.641	ns
SSTL135_S	0.378	0.378	0.399	0.378	0.772	0.772	0.823	0.772	0.827	0.827	0.878	0.827	ns
SSTL15_DCI_F	0.402	0.402	0.417	0.402	0.412	0.412	0.429	0.412	0.531	0.531	0.563	0.531	ns
SSTL15_DCI_M	0.402	0.402	0.417	0.402	0.553	0.553	0.583	0.553	0.645	0.645	0.685	0.645	ns
SSTL15_DCI_S	0.402	0.402	0.417	0.402	0.768	0.768	0.822	0.768	0.847	0.847	0.912	0.847	ns
SSTL15_F	0.371	0.371	0.400	0.371	0.408	0.408	0.428	0.408	0.530	0.530	0.556	0.530	ns
SSTL15_M	0.371	0.371	0.400	0.371	0.554	0.554	0.585	0.554	0.639	0.639	0.677	0.639	ns
SSTL15_S	0.371	0.371	0.400	0.371	0.767	0.767	0.817	0.767	0.813	0.813	0.867	0.813	ns
SSTL18_I_DCI_F	0.329	0.329	0.336	0.329	0.445	0.445	0.461	0.445	0.566	0.566	0.595	0.566	ns
SSTL18_I_DCI_M	0.329	0.329	0.336	0.329	0.554	0.554	0.585	0.554	0.644	0.644	0.683	0.644	ns
SSTL18_I_DCI_S	0.329	0.329	0.336	0.329	0.762	0.762	0.818	0.762	0.837	0.837	0.899	0.837	ns
SSTL18_I_F	0.316	0.316	0.337	0.316	0.454	0.454	0.476	0.454	0.578	0.578	0.608	0.578	ns
SSTL18_I_M	0.316	0.316	0.337	0.316	0.571	0.571	0.603	0.571	0.652	0.652	0.692	0.652	ns
SSTL18_I_S	0.316	0.316	0.337	0.316	0.782	0.782	0.835	0.782	0.816	0.816	0.870	0.816	ns
SUB_LVDS	0.539	0.539	0.620	0.539	0.660	0.660	0.692	0.660	969.863	969.863	969.863	969.863	ns

Output Delay Measurement Methodology

Output delays are measured with short output traces. Standard termination was used for all testing. The propagation delay of the trace is characterized separately and subtracted from the final measurement, and is therefore not included in the generalized test setups shown in [Figure 1](#) and [Figure 2](#).

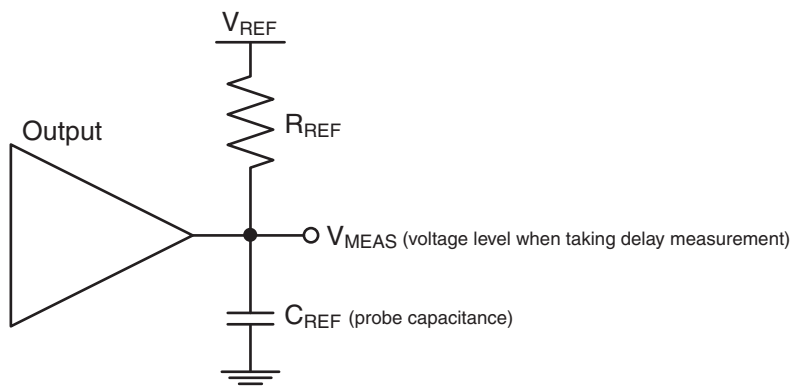


Figure 1: Single-Ended Test Setup

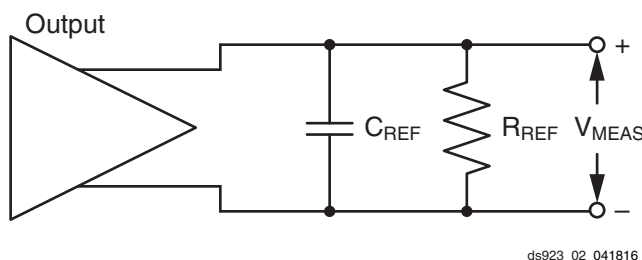


Figure 2: Differential Test Setup

Parameters V_{REF} , R_{REF} , C_{REF} , and V_{MEAS} fully describe the test conditions for each I/O standard. The most accurate prediction of propagation delay in any given application can be obtained through IBIS simulation, using this method:

1. Simulate the output driver of choice into the generalized test setup using values from [Table 27](#).
2. Record the time to V_{MEAS} .
3. Simulate the output driver of choice into the actual PCB trace and load using the appropriate IBIS model or capacitance value to represent the load.
4. Record the time to V_{MEAS} .
5. Compare the results of [step 2](#) and [step 4](#). The increase or decrease in delay yields the actual propagation delay of the PCB trace.

Table 27: Output Delay Measurement Methodology

Description	I/O Standard Attribute	R _{REF} (Ω)	C _{REF} ⁽¹⁾ (pF)	V _{MEAS} (V)	V _{REF} (V)
LVC MOS, 1.2V	LVC MOS12	1M	0	0.6	0
LVC MOS, 1.5V	LVC MOS15	1M	0	0.75	0
LVC MOS, 1.8V	LVC MOS18	1M	0	0.9	0
LVDCI, HSLVDCI, 1.5V	LVDCI_15, HSLVDCI_15	50	0	V _{REF}	0.75
LVDCI, HSLVDCI, 1.8V	LVDCI_15, HSLVDCI_18	50	0	V _{REF}	0.9
HSTL (high-speed transceiver logic), class I, 1.2V	HSTL_I_12	50	0	V _{REF}	0.6
HSTL, class I, 1.5V	HSTL_I	50	0	V _{REF}	0.75
HSTL, class I, 1.8V	HSTL_I_18	50	0	V _{REF}	0.9
HSUL (high-speed unterminated logic), 1.2V	HSUL_12	50	0	V _{REF}	0.6
SSTL12 (stub series terminated logic), 1.2V	SSTL12	50	0	V _{REF}	0.6
SSTL135, 1.35V	SSTL135	50	0	V _{REF}	0.675
SSTL15, 1.5V	SSTL15	50	0	V _{REF}	0.75
SSTL18, class I, 1.8V	SSTL18_I	50	0	V _{REF}	0.9
POD10, 1.0V	POD10	50	0	V _{REF}	1.0
POD12, 1.2V	POD12	50	0	V _{REF}	1.2
DIFF_HSTL, class I, 1.2V	DIFF_HSTL_I_12	50	0	V _{REF}	0.6
DIFF_HSTL, class I, 1.5V	DIFF_HSTL_I	50	0	V _{REF}	0.75
DIFF_HSTL, class I, 1.8V	DIFF_HSTL_I_18	50	0	V _{REF}	0.9
DIFF_HSUL, 1.2V	DIFF_HSUL_12	50	0	V _{REF}	0.6
DIFF_SSTL12, 1.2V	DIFF_SSTL12	50	0	V _{REF}	0.6
DIFF_SSTL135, 1.35V	DIFF_SSTL135	50	0	V _{REF}	0.675
DIFF_SSTL15, 1.5V	DIFF_SSTL15	50	0	V _{REF}	0.75
DIFF_SSTL18, 1.8V	DIFF_SSTL18_I	50	0	V _{REF}	0.9
DIFF_POD10, 1.0V	DIFF_POD10	50	0	V _{REF}	1.0
DIFF_POD12, 1.2V	DIFF_POD12	50	0	V _{REF}	1.2
LVDS (low-voltage differential signaling), 1.8V	LVDS	100	0	0 ⁽²⁾	0
SUB_LVDS, 1.8V	SUB_LVDS	100	0	0 ⁽²⁾	0
MIPI D-PHY (high speed) 1.2V	MIPI_DPHY_DCI_HS	100	0	0 ⁽²⁾	0
MIPI D-PHY (low power) 1.2V	MIPI_DPHY_DCI_LP	1M	0	0.6	0

Notes:

1. C_{REF} is the capacitance of the probe, nominally 0 pF.
2. The value given is the differential output voltage.

Input/Output Delay Switching Characteristics

Table 30: Input/Output Delay Switching Characteristics

Symbol	Description	Speed Grade and V _{CCINT} Operating Voltages				Units
		0.90V	0.85V		0.72V	
		-3	-2	-1	-2	
F _{REFCLK}	REFCLK frequency for IDELAYCTRL (component mode).	300 to 800				MHz
	REFCLK frequency for BITSlice_CONTROL (native mode). ⁽¹⁾	300 to 2666.67	300 to 2666.67	300 to 2400	300 to 2400	MHz
T _{MINPER_CLK}	Minimum period for IODELAY clock.	3.195	3.195	3.195	3.195	ns
T _{MINPER_RST}	Minimum reset pulse width.	52.00				ns
T _{IDELAY_RESOLUTION} / T _{ODELAY_RESOLUTION}	IDELAY/ODELAY chain resolution.	2.1 to 12				ps

Notes:

1. PLL settings could restrict the minimum allowable data rate. For example, when using a PLL with CLKOUTPHY_MODE = VCO_HALF, the minimum frequency is PLL_FVCOMIN/2.

DSP48 Slice Switching Characteristics

Table 31: DSP48 Slice Switching Characteristics

Symbol	Description	Speed Grade and V _{CCINT} Operating Voltages				Units
		0.90V	0.85V		0.72V	
		-3	-2	-1	-2	
Maximum Frequency						
F _{MAX}	With all registers used.	891	775	645	644	MHz
F _{MAX_PATDET}	With pattern detector.	794	687	571	562	MHz
F _{MAX_MULT_NOMREG}	Two register multiply without MREG.	635	544	456	440	MHz
F _{MAX_MULT_NOMREG_PATDET}	Two register multiply without MREG with pattern detect.	577	492	410	395	MHz
F _{MAX_PREADD_NOADREG}	Without ADREG.	655	565	468	453	MHz
F _{MAX_NOPIPELINEREG}	Without pipeline registers (MREG, ADREG).	483	410	338	323	MHz
F _{MAX_NOPIPELINEREG_PATDET}	Without pipeline registers (MREG, ADREG) with pattern detect.	448	379	314	299	MHz

MMCM Switching Characteristics

Table 33: MMCM Specification

Symbol	Description	Speed Grade and V _{CCINT} Operating Voltages				Units
		0.90V	0.85V		0.72V	
		-3	-2	-1	-2	
MMCM_F _{INMAX}	Maximum input clock frequency.	1066	933	800	933	MHz
MMCM_F _{INMIN}	Minimum input clock frequency.	10	10	10	10	MHz
MMCM_F _{INJITTER}	Maximum input clock period jitter.	< 20% of clock input period or 1 ns Max				
MMCM_F _{INDUTY}	Input duty cycle range: 10–49 MHz.	25–75				%
	Input duty cycle range: 50–199 MHz.	30–70				%
	Input duty cycle range: 200–399 MHz.	35–65				%
	Input duty cycle range: 400–499 MHz.	40–60				%
	Input duty cycle range: >500 MHz.	45–55				%
MMCM_F _{MIN_PSCLK}	Minimum dynamic phase shift clock frequency.	0.01	0.01	0.01	0.01	MHz
MMCM_F _{MAX_PSCLK}	Maximum dynamic phase shift clock frequency.	550	500	450	500	MHz
MMCM_F _{VCOMIN}	Minimum MMCM VCO frequency.	800	800	800	800	MHz
MMCM_F _{VCOMAX}	Maximum MMCM VCO frequency.	1600	1600	1600	1600	MHz
MMCM_F _{BANDWIDTH}	Low MMCM bandwidth at typical. ⁽¹⁾	1.00	1.00	1.00	1.00	MHz
	High MMCM bandwidth at typical. ⁽¹⁾	4.00	4.00	4.00	4.00	MHz
MMCM_T _{STATPHAOFFSET}	Static phase offset of the MMCM outputs. ⁽²⁾	0.12	0.12	0.12	0.12	ns
MMCM_T _{OUTJITTER}	MMCM output jitter.	Note 3				
MMCM_T _{OUTDUTY}	MMCM output clock duty cycle precision. ⁽⁴⁾	0.165	0.20	0.20	0.20	ns
MMCM_T _{LOCKMAX}	MMCM maximum lock time for MMCM_F _{PFDMIN} .	100	100	100	100	μs
MMCM_F _{OUTMAX}	MMCM maximum output frequency.	891	775	667	725	MHz
MMCM_F _{OUTMIN}	MMCM minimum output frequency. ⁽⁴⁾⁽⁵⁾	6.25	6.25	6.25	6.25	MHz
MMCM_T _{EXTFDVAR}	External clock feedback variation.	< 20% of clock input period or 1 ns Max				
MMCM_RST _{MINPULSE}	Minimum reset pulse width.	5.00	5.00	5.00	5.00	ns
MMCM_F _{PFDMAX}	Maximum frequency at the phase frequency detector.	550	500	450	500	MHz
MMCM_F _{PFDMIN}	Minimum frequency at the phase frequency detector.	10	10	10	10	MHz
MMCM_T _{FBDELAY}	Maximum delay in the feedback path.	5 ns Max or one clock cycle				
MMCM_F _{DRPCLK_MAX}	Maximum DRP clock frequency	250	250	250	250	MHz

Notes:

1. The MMCM does not filter typical spread-spectrum input clocks because they are usually far below the bandwidth filter frequencies.
2. The static offset is measured between any MMCM outputs with identical phase.
3. Values for this parameter are available in the Clocking Wizard.
4. Includes global clock buffer.
5. Calculated as F_{VCO}/128 assuming output duty cycle is 50%.

PLL Switching Characteristics

Table 34: PLL Specification⁽¹⁾

Symbol	Description	Speed Grade and V _{CCINT} Operating Voltages				Units
		0.90V	0.85V		0.72V	
		-3	-2	-1	-2	
PLL_F _{INMAX}	Maximum input clock frequency.	1066	933	800	933	MHz
PLL_F _{INMIN}	Minimum input clock frequency.	70	70	70	70	MHz
PLL_F _{INJITTER}	Maximum input clock period jitter.	< 20% of clock input period or 1 ns Max				
PLL_F _{INDUTY}	Input duty cycle range: 70–399 MHz.	35–65				%
	Input duty cycle range: 400–499 MHz.	40–60				%
	Input duty cycle range: >500 MHz.	45–55				%
PLL_F _{VCOMIN}	Minimum PLL VCO frequency.	750	750	750	750	MHz
PLL_F _{VCOMAX}	Maximum PLL VCO frequency.	1500	1500	1500	1500	MHz
PLL_T _{STATPHAOFFSET}	Static phase offset of the PLL outputs. ⁽²⁾	0.12	0.12	0.12	0.12	ns
PLL_T _{OUTJITTER}	PLL output jitter.	Note 3				
PLL_T _{OUTDUTY}	PLL CLKOUT0, CLKOUT0B, CLKOUT1, CLKOUT1B duty-cycle precision. ⁽⁴⁾	0.165	0.20	0.20	0.20	ns
PLL_T _{LOCKMAX}	PLL maximum lock time.	100				µs
PLL_F _{OUTMAX}	PLL maximum output frequency at CLKOUT0, CLKOUT0B, CLKOUT1, CLKOUT1B.	891	775	667	725	MHz
	PLL maximum output frequency at CLKOUTPHY.	2667	2667	2400	2400	MHz
PLL_F _{OUTMIN}	PLL minimum output frequency at CLKOUT0, CLKOUT0B, CLKOUT1, CLKOUT1B. ⁽⁵⁾	5.86	5.86	5.86	5.86	MHz
	PLL minimum output frequency at CLKOUTPHY.	2 x VCO mode: 1500 1 x VCO mode: 750 0.5 x VCO mode: 375				MHz
PLL_RST _{MINPULSE}	Minimum reset pulse width.	5.00	5.00	5.00	5.00	ns
PLL_F _{PFDMAX}	Maximum frequency at the phase frequency detector.	667.5	667.5	667.5	667.5	MHz
PLL_F _{PFDMIN}	Minimum frequency at the phase frequency detector.	70	70	70	70	MHz
PLL_F _{BANDWIDTH}	PLL bandwidth at typical.	14	14	14	14	MHz
PLL_F _{DPRCLK_MAX}	Maximum DRP clock frequency	250	250	250	250	MHz

Notes:

1. The PLL does not filter typical spread-spectrum input clocks because they are usually far below the loop filter frequencies.
2. The static offset is measured between any PLL outputs with identical phase.
3. Values for this parameter are available in the Clocking Wizard.
4. Includes global clock buffer.
5. Calculated as F_{VCO}/128 assuming output duty cycle is 50%.

Device Pin-to-Pin Output Parameter Guidelines

The pin-to-pin numbers in Table 35 through Table 37 are based on the clock root placement in the center of the device. The actual pin-to-pin values will vary if the root placement selected is different. Consult the Vivado Design Suite timing report for the actual pin-to-pin values.

Table 35: Global Clock Input to Output Delay Without MMCM (Near Clock Region)

Symbol	Description	Device	Speed Grade and V _{CCINT} Operating Voltages				Units
			0.90V	0.85V		0.72V	
			-3	-2	-1	-2	
SSTL15 Global Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, <i>without</i> MMCM.							
T _{ICKOF}	Global clock input and output flip-flop <i>without</i> MMCM (near clock region).	XCVU3P	4.08	4.77	5.09	5.28	ns
		XCVU5P	4.08	4.77	5.09	5.28	ns
		XCVU7P	4.08	4.77	5.09	5.28	ns
		XCVU9P	4.08	4.77	5.09	5.28	ns
		XCVU11P	3.93	4.59	4.90	5.07	ns
		XCVU13P	3.93	4.59	4.90	5.07	ns

Notes:

- This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible I/O and CLB flip-flops are clocked by the global clock net in a single SLR.

Table 36: Global Clock Input to Output Delay Without MMCM (Far Clock Region)

Symbol	Description	Device	Speed Grade and V _{CCINT} Operating Voltages				Units
			0.90V	0.85V		0.72V	
			-3	-2	-1	-2	
SSTL15 Global Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, <i>without</i> MMCM.							
T _{ICKOF_FAR}	Global clock input and output flip-flop <i>without</i> MMCM (far clock region).	XCVU3P	4.53	5.33	5.69	5.92	ns
		XCVU5P	4.53	5.33	5.69	5.92	ns
		XCVU7P	4.53	5.33	5.69	5.92	ns
		XCVU9P	4.53	5.33	5.69	5.92	ns
		XCVU11P	4.10	4.79	5.11	5.28	ns
		XCVU13P	4.10	4.79	5.11	5.28	ns

Notes:

- This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible I/O and CLB flip-flops are clocked by the global clock net in a single SLR.

Package Parameter Guidelines

The parameters in this section provide the necessary values for calculating timing budgets for clock transmitter and receiver data-valid windows.

Table 40: Package Skew

Symbol	Description	Device	Package	Value	Units
PKGSKEW	Package Skew	XCVU3P	FFVC1517	197	ps
		XCVU5P	FLVA2104	175	ps
			FLVB2104	225	ps
			FLVC2104	216	ps
		XCVU7P	FLVA2104	175	ps
			FLVB2104	225	ps
			FLVC2104	216	ps
		XCVU9P	FLGA2104	217	ps
			FLGB2104	275	ps
			FLGC2104	299	ps
			FSGD2104	229	ps
			FLGA2577	149	ps
		XCVU11P	FLGF1924	180	ps
			FLGB2104	216	ps
			FLGC2104		ps
			FSGD2104		ps
			FLGA2577	154	ps
		XCVU13P	FHGA2104		ps
			FHGB2104	259	ps
			FHGC2104	182	ps
			FIGD2104		ps
			FLGA2577	140	ps

Notes:

- These values represent the worst-case skew between any two SelectIO resources in the package: shortest delay to longest delay from die pad to ball.
- Package delay information is available for these device/package combinations. This information can be used to deskew the package.

GTY Transceiver Specifications

The *UltraScale Architecture and Product Overview* ([DS890](#)) lists the Virtex UltraScale+ FPGAs that include the GTY transceivers.

GTY Transceiver DC Input and Output Levels

[Table 41](#) summarizes the DC specifications of the GTY transceivers in Virtex UltraScale+ FPGAs. Consult the *UltraScale Architecture GTY Transceiver User Guide* ([UG578](#)) for further information.

Table 41: GTY Transceiver DC Specifications

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
DV _{PPIN}	Differential peak-to-peak input voltage (external AC coupled)	> 10.3125 Gb/s	150	–	1250	mV
		6.6 Gb/s to 10.3125 Gb/s	150	–	1250	mV
		≤ 6.6 Gb/s	150	–	2000	mV
V _{IN}	Single-ended input voltage. Voltage measured at the pin referenced to GND.	DC coupled V _{MGTAVTT} = 1.2V	–400	–	V _{MGTAVTT}	mV
V _{CMIN}	Common mode input voltage	DC coupled V _{MGTAVTT} = 1.2V	–	2/3 V _{MGTAVTT}	–	mV
D _{VPPOUT}	Differential peak-to-peak output voltage ⁽¹⁾	Transmitter output swing is set to 1010	800	–	–	mV
V _{CMOUTDC}	Common mode output voltage: DC coupled (equation based)	When remote RX is terminated to GND	$V_{MGTAVTT}/2 - D_{VPPOUT}/4$			mV
		When remote RX termination is floating	$V_{MGTAVTT} - D_{VPPOUT}/2$			mV
		When remote RX is terminated to V _{RX_TERM} ⁽²⁾	$V_{MGTAVTT} - \frac{D_{VPPOUT}}{4} - \left(\frac{V_{MGTAVTT} - V_{RX_TERM}}{2} \right)$			mV
V _{CMOUTAC}	Common mode output voltage: AC coupled	Equation based	$V_{MGTAVTT} - D_{VPPOUT}/2$			mV
R _{IN}	Differential input resistance		–	100	–	Ω
R _{OUT}	Differential output resistance		–	100	–	Ω
T _{OSKEW}	Transmitter output pair (TXP and TXN) intra-pair skew		–	–	10	ps
C _{EXT}	Recommended external AC coupling capacitor ⁽³⁾		–	100	–	nF

Notes:

1. The output swing and pre-emphasis levels are programmable using the GTY transceiver attributes discussed in the *UltraScale Architecture GTY Transceiver User Guide* ([UG578](#)) and can result in values lower than reported in this table.
2. V_{RX_TERM} is the remote RX termination voltage.
3. Other values can be used as appropriate to conform to specific protocols and standards.

Table 50: GTY Transceiver Transmitter Switching Characteristics (Cont'd)

Symbol	Description	Condition	Min	Typ	Max	Units
T _{J3.20}	Total jitter ⁽³⁾⁽⁴⁾	3.20 Gb/s ⁽⁵⁾	–	–	0.20	UI
D _{J3.20}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.10	UI
T _{J2.5}	Total jitter ⁽³⁾⁽⁴⁾	2.5 Gb/s ⁽⁶⁾	–	–	0.20	UI
D _{J2.5}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.10	UI
T _{J1.25}	Total jitter ⁽³⁾⁽⁴⁾	1.25 Gb/s ⁽⁷⁾	–	–	0.15	UI
D _{J1.25}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.06	UI
T _{J500}	Total jitter ⁽³⁾⁽⁴⁾	500 Mb/s ⁽⁸⁾	–	–	0.10	UI
D _{J500}	Deterministic jitter ⁽³⁾⁽⁴⁾		–	–	0.03	UI

Notes:

1. Using same REFCLK input with TX phase alignment enabled for up to four consecutive transmitters (one fully populated GTY Quad) at maximum line rate.
2. Using QPLL_FBDIV = 40, 20-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
3. Using CPLL_FBDIV = 2, 20-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
4. All jitter values are based on a bit-error ratio of 10⁻¹².
5. CPLL frequency at 3.2 GHz and TXOUT_DIV = 2.
6. CPLL frequency at 2.5 GHz and TXOUT_DIV = 2.
7. CPLL frequency at 2.5 GHz and TXOUT_DIV = 4.
8. CPLL frequency at 2.0 GHz and TXOUT_DIV = 8.

GTY Transceiver Electrical Compliance

The *UltraScale Architecture GTY Transceiver User Guide* ([UG578](#)) contains recommended use modes that ensure compliance for the protocols listed in [Table 52](#). The transceiver wizard provides the recommended settings for those use cases and for protocol specific characteristics.

Table 52: GTY Transceiver Protocol List

Protocol	Specification	Serial Rate (Gb/s)	Electrical Compliance
CAUI-4	IEEE 802.3-2012	25.78125	Compliant
28 Gb/s backplane	CEI-25G-LR	25–28.05	Compliant
Interlaken	OIF-CEI-6G, OIF-CEI-11GSR, OIF-CEI-28G-MR	4.25–25.78125	Compliant
100GBASE-KR4	IEEE 802.3bj-2014, CEI-25G-LR	25.78125	Compliant ⁽¹⁾
100GBASE-CR4	IEEE 802.3bj-2014, CEI-25G-LR	25.78125	Compliant ⁽¹⁾
50GBASE-KR4	IEEE 802.3by-2014, CEI-25G-LR	25.78125	Compliant ⁽¹⁾
50GBASE-CR4	IEEE 802.3by-2014, CEI-25G-LR	25.78125	Compliant ⁽¹⁾
25GBASE-KR4	IEEE 802.3by-2014, CEI-25G-LR	25.78125	Compliant ⁽¹⁾
25GBASE-CR4	IEEE 802.3by-2014, CEI-25G-LR	25.78125	Compliant ⁽¹⁾
OTU4 (OTL4.4) CFP2	OIF-CEI-28G-VSR	27.952493–32.75	Compliant
OTU4 (OTL4.4) CFP	OIF-CEI-11G-MR	11.18–13.1	Compliant
CAUI-10	IEEE 802.3-2012	10.3125	Compliant
nPPI	IEEE 802.3-2012	10.3125	Compliant
10GBASE-KR ⁽²⁾	IEEE 802.3-2012	10.3125	Compliant
SFP+	SFF-8431 (SR and LR)	9.95328–11.10	Compliant
XFP	INF-8077i, revision 4.5	10.3125	Compliant
RXAUI	CEI-6G-SR	6.25	Compliant
XAUI	IEEE 802.3-2012	3.125	Compliant
1000BASE-X	IEEE 802.3-2012	1.25	Compliant
5.0G Ethernet	IEEE 802.3bx (PAR)	5	Compliant
2.5G Ethernet	IEEE 802.3bx (PAR)	2.5	Compliant
HiGig, HiGig+, HiGig2	IEEE 802.3-2012	3.74, 6.6	Compliant
QSGMII	QSGMII v1.2 (Cisco System, ENG-46158)	5	Compliant
OTU2	ITU G.8251	10.709225	Compliant
OTU4 (OTL4.10)	OIF-CEI-11G-SR	11.180997	Compliant
OC-3/12/48/192	GR-253-CORE	0.1555–9.956	Compliant
PCIe Gen1, 2, 3	PCI Express base 3.0	2.5, 5.0, and 8.0	Compliant
SDI ⁽³⁾	SMPTE 424M-2006	0.27–2.97	Compliant
UHD-SDI ⁽³⁾	SMPTE ST-2081 6G, SMPTE ST-2082 12G	6 and 12	Compliant
Hybrid memory cube (HMC)	HMC-15G-SR	10, 12.5, and 15.0	Compliant
MoSys bandwidth engine	CEI-11-SR and CEI-11-SR (overclocked)	10.3125, 15.5	Compliant
CPRI	CPRI_v_6_1_2014-07-01	0.6144–12.165	Compliant
Passive optical network (PON)	10G-EPON, 1G-EPON, NG-PON2, XG-PON, and 2.5G-PON	0.155–10.3125	Compliant
JESD204a/b	OIF-CEI-6G, OIF-CEI-11G	3.125–12.5	Compliant

Table 54: Maximum Performance for Interlaken 6 x 25.78125 Gb/s and 6 x 28.21 Gb/s Protocol and Lane Logic Mode Designs

Symbol	Description	Speed Grade and V _{CCINT} Operating Voltages										Units
		0.90V		0.85V			0.72V					
		-3 ⁽¹⁾	-2 ⁽¹⁾	-1	-2	-1						
F _{RX_SERDES_CLK}	Receive serializer/ deserializer clock	440.79	440.79	N/A	402.84	N/A	MHz					
F _{TX_SERDES_CLK}	Transmit serializer/ deserializer clock	440.79	440.79	N/A	402.84	N/A	MHz					
F _{DRP_CLK}	Dynamic reconfiguration port clock	250.00	250.00	N/A	250.00	N/A	MHz					
		Min ⁽²⁾	Max	Min ⁽²⁾	Max	Min	Max	Min ⁽²⁾	Max	Min	Max	
F _{CORE_CLK}	Interlaken core clock	412.50 ⁽³⁾	479.20	412.50 ⁽³⁾	479.20	N/A	412.50	429.69	N/A	MHz		
F _{LBUS_CLK}	Interlaken local bus clock	300.00 ⁽⁴⁾	349.52	300.00 ⁽⁴⁾	349.52	N/A	300.00	349.52	N/A	MHz		

Notes:

- 6 x 28.21 mode is only supported in the -2 (V_{CCINT}=0.85V) and -3 (V_{CCINT}=0.90V) speed grades.
- These are the minimum clock frequencies at the maximum lane performance.
- The minimum value for CORE_CLK is 451.36 MHz for the 6 x 28.21 Gb/s protocol.
- The minimum value for LBUS_CLK is 330.00 MHz for the 6 x 28.21 Gb/s protocol.

Table 55: Maximum Performance for Interlaken 12 x 25.78125 Gb/s Lane Logic Only Mode Designs

Symbol	Description	Speed Grade and V _{CCINT} Operating Voltages					Units
		0.90V	0.85V		0.72V		
		-3	-2	-1	-2	-1	
F _{RX_SERDES_CLK}	Receive serializer/ deserializer clock	402.84	402.84	N/A	N/A	N/A	MHz
F _{TX_SERDES_CLK}	Transmit serializer/ deserializer clock	402.84	402.84	N/A	N/A	N/A	MHz
F _{DRP_CLK}	Dynamic reconfiguration port clock	250.00	250.00	N/A	N/A	N/A	MHz
F _{CORE_CLK}	Interlaken core clock	412.50	412.50	N/A	N/A	N/A	MHz
F _{LBUS_CLK}	Interlaken local bus clock	349.52	349.52	N/A	N/A	N/A	MHz

Table 61: Configuration Switching Characteristics (Cont'd)

Symbol	Description		Speed Grade and V _{CCINT} Operating Voltages				Units
			0.90V	0.85V		0.72V	
			-3	-2	-1	-2	
SelectMAP Mode Programming Switching							
T _{SMDCK} /T _{SMCKD}	D[31:00] setup/hold.	XCVU3P, XCVU5P, XCVU7P, XCVU9P	4.0/0	4.0/0	4.0/0	5.0/0	ns, Min
		XCVU11P, XCVU13P	4.5/0	4.5/0	4.5/0	7.5/0	ns, Min
T _{SMCCK} /T _{SMCKCS}	CSI_B setup/hold.	XCVU3P, XCVU5P, XCVU7P, XCVU9P	4.0/0	4.0/0	4.0/0	5.0/0	ns, Min
		XCVU11P, XCVU13P	4.5/0	4.5/0	4.5/0	7.5/0	ns, Min
T _{SMWCK} /T _{SMCKW}	RDWR_B setup/hold.	XCVU3P, XCVU5P, XCVU7P, XCVU9P	10.0/0	10.0/0	10.0/0	11.0/0	ns, Min
		XCVU11P, XCVU13P	11.0/0	11.0/0	11.0/0	17.0/0	ns, Min
T _{SMCKCSO}	CSO_B clock to out (330Ω pull-up resistor required).		7.0	7.0	7.0	7.0	ns, Max
T _{SMCO}	D[31:00] clock to out in readback.		8.0	8.0	8.0	8.0	ns, Max
F _{RBCK}	Readback frequency.	XCVU3P, XCVU5P, XCVU7P, XCVU9P	125	125	125	100	MHz, Max
		XCVU11P, XCVU13P	125	125	125	66	MHz, Max
Boundary-Scan Port Timing Specifications							
T _{TAPTCK} /T _{TCKTAP}	TMS and TDI setup/hold.	XCVU3P	3.0/ 2.0	3.0/ 2.0	3.0/ 2.0	3.0/ 2.0	ns, Min
		XCVU5P, XCVU7P, XCVU9P, XCVU11P, XCVU13P	8.5/ 2.0	8.5/ 2.0	8.5/ 2.0	8.5/ 2.0	ns, Min
T _{TCKTDO}	TCK falling edge to TDO output.	XCVU3P	7.0	7.0	7.0	7.0	ns, Max
		XCVU5P, XCVU7P, XCVU9P, XCVU11P, XCVU13P	15.0	15.0	15.0	15.0	ns, Max
F _{TCK}	TCK frequency.	XCVU3P	66	66	66	66	MHz, Max
		XCVU5P, XCVU7P, XCVU9P, XCVU11P, XCVU13P	20	20	20	20	MHz, Max
BPI Master Flash Mode Programming Switching							
T _{BPICCO}	A[28:00], RS[1:0], FCS_B, FOE_B, FWE_B, ADV_B clock to out.		10	10	10	10	ns, Max
T _{BPIDCC} /T _{BPICCD}	D[15:00] setup/hold.	XCVU3P, XCVU5P, XCVU7P, XCVU9P	4.0/0	4.0/0	4.0/0	5.0/0	ns, Min
		XCVU11P, XCVU13P	4.5/0	4.5/0	4.5/0	7.5/0	ns, Min
SPI Master Flash Mode Programming Switching							
T _{SPIDCC} /T _{SPICCD}	D[03:00] setup/hold.		3.0/0	3.0/0	3.0/0	4.0/0	ns, Min
T _{SPIDCC} /T _{SPICCD}	D[07:04] setup/hold.	XCVU3P, XCVU5P, XCVU7P, XCVU9P	4.0/0	4.0/0	4.0/0	5.0/0	ns, Min
		XCVU11P, XCVU13P	4.5/0	4.5/0	4.5/0	7.5/0	ns, Min
T _{SPICCM}	MOSI clock to out.		8.0	8.0	8.0	8.0	ns, Max
T _{SPICCF}	FCS_B clock to out.		8.0	8.0	8.0	8.0	ns, Max

Revision History

The following table shows the revision history for this document.

Date	Version	Description of Revisions
04/19/2017	1.1	Updated the Summary description. In Table 1 , updated Note 6 , added data, and added Note 7 , Note 8 , and Note 9 . Updated and added data to Table 2 through Table 6 . Removed the -1LI speed grade. Updated Table 16 , Table 17 , and Table 18 to production release in Vivado Design Suite 2017.1 for the XCVU3P: -2E, -2I, -1E, -1I. Updated Table 15 . Added Note 1 to Table 17 . Updated Table 19 , Table 20 , Table 24 , Table 25 , Table 26 , Table 28 , Table 29 , and Table 30 . Added Table 21 . Added MMCM_FDPRCLK_MAX to Table 33 and PLL_FDPRCLK_MAX to Table 34 . Updated to Vivado Design Suite 2017.1 Table 35 , Table 36 , Table 37 , and Table 38 . Added data to Table 39 and Table 40 . Updated the GTY Transceiver Specifications section. Revised the Integrated Interface Block for Interlaken section. Updated the System Monitor Specifications section adding notes to the tables. Updated the Configuration Switching Characteristics section. Removed the <i>eFUSE Programming Conditions</i> table and added the specifications to Table 2 and Table 3 . Updated the Automotive Applications Disclaimer .
04/20/2016	1.0	Initial Xilinx release.

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