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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	162000
Number of Logic Elements/Cells	2835000
Total RAM Bits	396150400
Number of I/O	572
Number of Gates	-
Voltage - Supply	0.873V ~ 0.927V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 100°C (TJ)
Package / Case	2104-BBGA, FCBGA
Supplier Device Package	2104-FCBGA (47.5x47.5)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xcvu11p-3flgb2104e

Recommended Operating Conditions

Table 2: **Recommended Operating Conditions(1)(2)**

Symbol	Description	Min	Typ	Max	Units
FPGA Logic					
V_{CCINT}	Internal supply voltage.	0.825	0.850	0.876	V
	For -2LE (V_{CCINT} = 0.72V) devices: internal supply voltage.	0.698	0.720	0.742	V
	For -3E devices: internal supply voltage.	0.873	0.900	0.927	V
V_{CCINT_IO}(3)	Internal supply voltage for the I/O banks.	0.825	0.850	0.876	V
	For -2LE devices (V_{CCINT} = 0.85V): internal supply voltage for the I/O banks.	0.825	0.850	0.876	V
	For -3E devices: internal supply voltage for the I/O banks.	0.873	0.900	0.927	V
V_{CCBRAM}	Block RAM supply voltage.	0.825	0.850	0.876	V
	For -3E devices: block RAM supply voltage.	0.873	0.900	0.927	V
V_{CCAUX}	Auxiliary supply voltage.	1.746	1.800	1.854	V
V_{CCO}(4)(5)	Supply voltage for I/O banks.	0.950	–	1.900	V
V_{CCAUX_IO}(6)	Auxiliary I/O supply voltage.	1.746	1.800	1.854	V
V_{IN}(7)	I/O input voltage.	–0.200	–	V_{CCO} + 0.200	V
I_{IN}(8)	Maximum current through any pin in a powered or unpowered bank when forward biasing the clamp diode.	–	–	10	mA
V_{BATT}(9)	Battery voltage.	1.000	–	1.890	V
GTY Transceiver					
$V_{MGTAVCC}$(10)	Analog supply voltage for the GTY transceiver.	0.873	0.900	0.927	V
$V_{MGTAVTT}$(10)	Analog supply voltage for the GTY transmitter and receiver termination circuits.	1.164	1.20	1.236	V
$V_{MGTVCCAUX}$(10)	Auxiliary analog QPLL voltage supply for the transceivers.	1.746	1.80	1.854	V
$V_{MGTAVTTRCAL}$(10)	Analog supply voltage for the resistor calibration circuit of the GTY transceiver column.	1.164	1.20	1.236	V

Table 3: **DC Characteristics Over Recommended Operating Conditions *(Cont'd)***

Symbol	Description	Min	Typ(1)	Max	Units
Uncalibrated programmable on-die termination in I/O banks (measured per JEDEC specification)					
$R^{(9)}$	Thevenin equivalent resistance of programmable input termination to $V_{CCO}/2$ where ODT = RTT_40.	–50%	40	+50%	Ω
	Thevenin equivalent resistance of programmable input termination to $V_{CCO}/2$ where ODT = RTT_48.	–50%	48	+50%	Ω
	Thevenin equivalent resistance of programmable input termination to $V_{CCO}/2$ where ODT = RTT_60.	–50%	60	+50%	Ω
	Programmable input termination to V_{CCO} where ODT = RTT_40.	–50%	40	+50%	Ω
	Programmable input termination to V_{CCO} where ODT = RTT_48.	–50%	48	+50%	Ω
	Programmable input termination to V_{CCO} where ODT = RTT_60.	–50%	60	+50%	Ω
	Programmable input termination to V_{CCO} where ODT = RTT_120.	–50%	120	+50%	Ω
	Programmable input termination to V_{CCO} where ODT = RTT_240.	–50%	240	+50%	Ω
Internal V_{REF}	50% V_{CCO}	V_{CCO} x 0.49	V_{CCO} x 0.50	V_{CCO} x 0.51	V
	70% V_{CCO}	V_{CCO} x 0.69	V_{CCO} x 0.70	V_{CCO} x 0.71	V
Differential termination	Programmable differential termination (TERM_100) for the I/O banks.	–35%	100	+35%	Ω
n	Temperature diode ideality factor.	–	1.026	–	–
r	Temperature diode series resistance.	–	2	–	Ω

Notes:

1. Typical values are specified at nominal voltage, 25°C.
2. For the I/O banks with a V_{CCO} of 1.8V and separated V_{CCO} and V_{CCAUX_IO} power supplies, the I_L maximum current is 70 µA.
3. This measurement represents the die capacitance at the pad, not including the package.
4. Maximum value specified for worst case process at 25°C.
5. I_{BATT} is measured when the battery-backed RAM (BBRAM) is enabled.
6. Do not program eFUSE during device configuration (e.g., during configuration, during configuration readback, or when readback CRC is active).
7. If VRP resides at a different bank (DCI cascade), the range increases to ±15%.
8. VRP resistor tolerance is (240Ω ±1%)
9. On-die input termination resistance, for more information see the *UltraScale Architecture SelectIO Resources User Guide* (UG571).

V_{IN} Maximum Allowed AC Voltage Overshoot and Undershoot

Table 4: **V_{IN} Maximum Allowed AC Voltage Overshoot and Undershoot for HP I/O Banks(1)(2)**

AC Voltage Overshoot	% of UI at –40°C to 100°C	AC Voltage Undershoot	% of UI at –40°C to 100°C
V_{CCO} + 0.30	100%	–0.30	100%
V_{CCO} + 0.35	100%	–0.35	90%
V_{CCO} + 0.40	92%	–0.40	92%
V_{CCO} + 0.45	50%	–0.45	50%
V_{CCO} + 0.50	20%	–0.50	20%
V_{CCO} + 0.55	10%	–0.55	10%
V_{CCO} + 0.60	6%	–0.60	6%
V_{CCO} + 0.65	2%	–0.65	2%
V_{CCO} + 0.70	2%	–0.70	2%

Notes:
1. A total of 200 mA per bank should not be exceeded.
2. For UI smaller than 20 µs.

Quiescent Supply Current

Table 5: **Typical Quiescent Supply Current(1)(2)(3)**

Symbol	Description	Device	Speed Grade and V_{CCINT} Operating Voltages				Units
			0.90V	0.85V		0.72V	
			-3	-2	-1	-2	
I_{CCINTQ}	Quiescent V_{CCINT} supply current.	XCVU3P	2384	2276	2276	2017	mA
		XCVU5P	4769	4552	4552	4034	mA
		XCVU7P	4769	4552	4552	4034	mA
		XCVU9P	7153	6828	6828	6050	mA
		XCVU11P	7567	7202	7202	6332	mA
		XCVU13P	10090	9602	9602	8442	mA
I_{CCINT_IOQ}	Quiescent current for V_{CCINT_IO} supply.	XCVU3P	149	144	144	144	mA
		XCVU5P	298	287	287	287	mA
		XCVU7P	298	287	287	287	mA
		XCVU9P	447	431	431	431	mA
		XCVU11P	182	176	176	176	mA
		XCVU13P	243	234	234	234	mA
I_{CCOQ}	Quiescent V_{CCO} supply current.	All devices	1	1	1	1	mA
I_{CCAUXQ}	Quiescent V_{CCAUX} supply current.	XCVU3P	268	268	268	268	mA
		XCVU5P	535	535	535	535	mA
		XCVU7P	535	535	535	535	mA
		XCVU9P	1015	1015	1015	1015	mA
		XCVU11P	819	819	819	819	mA
		XCVU13P	1091	1091	1091	1091	mA

FPGA Logic Performance Characteristics

This section provides the performance characteristics of some common functions and designs implemented in Virtex UltraScale+ FPGAs. These values are subject to the same guidelines as the AC Switching Characteristics, page 13.

Table 19: **LVDS Component Mode Performance**

Description	Speed Grade and V_{CCINT} Operating Voltages								Units
	0.90V		0.85V				0.72V		
	-3		-2		-1		-2		
	Min	Max	Min	Max	Min	Max	Min	Max	
LVDS TX DDR (OSERDES 4:1, 8:1)	0	1250	0	1250	0	1250	0	1250	Mb/s
LVDS TX SDR (OSERDES 2:1, 4:1)	0	625	0	625	0	625	0	625	Mb/s
LVDS RX DDR (ISERDES 1:4, 1:8)(1)	0	1250	0	1250	0	1250	0	1250	Mb/s
LVDS RX SDR (ISERDES 1:2, 1:4)(1)	0	625	0	625	0	625	0	625	Mb/s

Notes:

1. LVDS receivers are typically bounded with certain applications to achieve maximum performance. Package skews are not included and should be removed through PCB routing.

Table 20: **LVDS Native Mode Performance(1)(2)**

Description	DATA_WIDTH	Speed Grade and V_{CCINT} Operating Voltages								Units
		0.90V		0.85V				0.72V		
		-3		-2		-1		-2		
		Min	Max	Min	Max	Min	Max	Min	Max	
LVDS TX DDR (TX_BITSLICE)	4	375	1600	375	1600	375	1260	375	1400	Mb/s
	8	375	1600	375	1600	375	1260	375	1600	Mb/s
LVDS TX SDR (TX_BITSLICE)	4	187.5	800	187.5	800	187.5	630	187.5	700	Mb/s
	8	187.5	800	187.5	800	187.5	630	187.5	800	Mb/s
LVDS RX DDR (RX_BITSLICE)(3)	4	375	1600	375	1600	375	1260	375	1400	Mb/s
	8	375	1600	375	1600	375	1260	375	1600	Mb/s
LVDS RX SDR (RX_BITSLICE)(3)	4	187.5	800	187.5	800	187.5	630	187.5	700	Mb/s
	8	187.5	800	187.5	800	187.5	630	187.5	800	Mb/s

Notes:

1. Native mode is supported through the High-Speed SelectIO Interface Wizard available with the Vivado Design Suite.
2. PLL settings can restrict the minimum allowable data rate. For example, when using the PLL with CLKOUTPHY_MODE = VCO_HALF the minimum frequency is PLL_FVCOMIN/2.
3. LVDS receivers are typically bounded with certain applications to achieve maximum performance. Package skews are not included and should be removed through PCB routing.

Table 21: **MIPI D-PHY Performance**

Description	Speed Grade and V_{CCINT} Operating Voltages				Units
	0.90V	0.85V		0.72V	
	-3	-2	-1	-2	
MIPI D-PHY transmitter or receiver.	1500	1500	1260	1260	Mb/s

Table 24: **IOB High Performance (HP) Switching Characteristics *(Cont'd)***

I/O Standards	$T_{INBUF\_DELAY\_PAD\_I}$				$T_{OUTBUF\_DELAY\_O\_PAD}$				$T_{OUTBUF\_DELAY\_TD\_PAD}$				Units
	0.90V	0.85V		0.72V	0.90V	0.85V		0.72V	0.90V	0.85V		0.72V	
	-3	-2	-1	-2	-3	-2	-1	-2	-3	-2	-1	-2	
POD12_DCI_F	0.409	0.409	0.431	0.409	0.425	0.425	0.443	0.425	0.558	0.558	0.586	0.558	ns
POD12_DCI_M	0.409	0.409	0.431	0.409	0.543	0.543	0.572	0.543	0.638	0.638	0.678	0.638	ns
POD12_DCI_S	0.409	0.409	0.431	0.409	0.772	0.772	0.822	0.772	0.862	0.862	0.929	0.862	ns
POD12_F	0.409	0.409	0.431	0.409	0.455	0.455	0.476	0.455	0.595	0.595	0.626	0.595	ns
POD12_M	0.409	0.409	0.431	0.409	0.551	0.551	0.582	0.551	0.641	0.641	0.679	0.641	ns
POD12_S	0.409	0.409	0.431	0.409	0.767	0.767	0.817	0.767	0.832	0.832	0.889	0.832	ns
SLVS_400_18	0.539	0.539	0.620	0.539	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	ns
SSTL12_DCI_F	0.381	0.381	0.399	0.381	0.425	0.425	0.443	0.425	0.558	0.558	0.586	0.558	ns
SSTL12_DCI_M	0.381	0.381	0.399	0.381	0.557	0.557	0.587	0.557	0.654	0.654	0.694	0.654	ns
SSTL12_DCI_S	0.381	0.381	0.399	0.381	0.754	0.754	0.803	0.754	0.842	0.842	0.908	0.842	ns
SSTL12_F	0.403	0.403	0.403	0.403	0.412	0.412	0.430	0.412	0.538	0.538	0.566	0.538	ns
SSTL12_M	0.403	0.403	0.403	0.403	0.553	0.553	0.584	0.553	0.641	0.641	0.676	0.641	ns
SSTL12_S	0.403	0.403	0.403	0.403	0.758	0.758	0.808	0.758	0.823	0.823	0.879	0.823	ns
SSTL135_DCI_F	0.366	0.366	0.399	0.366	0.411	0.411	0.428	0.411	0.537	0.537	0.565	0.537	ns
SSTL135_DCI_M	0.366	0.366	0.399	0.366	0.551	0.551	0.582	0.551	0.645	0.645	0.685	0.645	ns
SSTL135_DCI_S	0.366	0.366	0.399	0.366	0.746	0.746	0.799	0.746	0.829	0.829	0.893	0.829	ns
SSTL135_F	0.378	0.378	0.399	0.378	0.408	0.408	0.428	0.408	0.528	0.528	0.561	0.528	ns
SSTL135_M	0.378	0.378	0.399	0.378	0.555	0.555	0.585	0.555	0.641	0.641	0.679	0.641	ns
SSTL135_S	0.378	0.378	0.399	0.378	0.772	0.772	0.823	0.772	0.827	0.827	0.878	0.827	ns
SSTL15_DCI_F	0.402	0.402	0.417	0.402	0.412	0.412	0.429	0.412	0.531	0.531	0.563	0.531	ns
SSTL15_DCI_M	0.402	0.402	0.417	0.402	0.553	0.553	0.583	0.553	0.645	0.645	0.685	0.645	ns
SSTL15_DCI_S	0.402	0.402	0.417	0.402	0.768	0.768	0.822	0.768	0.847	0.847	0.912	0.847	ns
SSTL15_F	0.371	0.371	0.400	0.371	0.408	0.408	0.428	0.408	0.530	0.530	0.556	0.530	ns
SSTL15_M	0.371	0.371	0.400	0.371	0.554	0.554	0.585	0.554	0.639	0.639	0.677	0.639	ns
SSTL15_S	0.371	0.371	0.400	0.371	0.767	0.767	0.817	0.767	0.813	0.813	0.867	0.813	ns
SSTL18_I_DCI_F	0.329	0.329	0.336	0.329	0.445	0.445	0.461	0.445	0.566	0.566	0.595	0.566	ns
SSTL18_I_DCI_M	0.329	0.329	0.336	0.329	0.554	0.554	0.585	0.554	0.644	0.644	0.683	0.644	ns
SSTL18_I_DCI_S	0.329	0.329	0.336	0.329	0.762	0.762	0.818	0.762	0.837	0.837	0.899	0.837	ns
SSTL18_I_F	0.316	0.316	0.337	0.316	0.454	0.454	0.476	0.454	0.578	0.578	0.608	0.578	ns
SSTL18_I_M	0.316	0.316	0.337	0.316	0.571	0.571	0.603	0.571	0.652	0.652	0.692	0.652	ns
SSTL18_I_S	0.316	0.316	0.337	0.316	0.782	0.782	0.835	0.782	0.816	0.816	0.870	0.816	ns
SUB_LVDS	0.539	0.539	0.620	0.539	0.660	0.660	0.692	0.660	969.863	969.863	969.863	969.863	ns

Table 26: **Input Delay Measurement Methodology *(Cont'd)***

Description	I/O Standard Attribute	V_L (1)(2)	V_H (1)(2)	V_{MEAS} (1)(4)(6)	V_{REF} (1)(3)(5)
DIFF_HSUL, 1.2V	DIFF_HSUL_12	0.6 – 0.25	0.6 + 0.25	0(6)	–
DIFF_SSTL, 1.2V	DIFF_SSTL12	0.6 – 0.25	0.6 + 0.25	0(6)	–
DIFF_SSTL135 and DIFF_SSTL135 class II, 1.35V	DIFF_SSTL135, DIFF_SSTL135_II	0.675 – 0.2875	0.675 + 0.2875	0(6)	–
DIFF_SSTL15 and DIFF_SSTL15 class II, 1.5V	DIFF_SSTL15, DIFF_SSTL15_II	0.75 – 0.325	0.75 + 0.325	0(6)	–
DIFF_SSTL18_I, DIFF_SSTL18_II, 1.8V	DIFF_SSTL18_I, DIFF_SSTL18_II	0.9 – 0.4	0.9 + 0.4	0(6)	–
DIFF_POD10, 1.0V	DIFF_POD10	0.5 – 0.2	0.5 + 0.2	0(6)	–
DIFF_POD12, 1.2V	DIFF_POD12	0.6 – 0.25	0.6 + 0.25	0(6)	–
LVDS (low-voltage differential signaling), 1.8V	LVDS	0.9 – 0.125	0.9 + 0.125	0(6)	–
SUB_LVDS, 1.8V	SUB_LVDS	0.9 – 0.125	0.9 + 0.125	0(6)	–
SLVS, 1.8V	SLVS_400_18	0.9 – 0.125	0.9 + 0.125	0(6)	–
MIPI D-PHY (high speed) 1.2V	MIPI_DPHY_DCI_HS	0.2 – 0.125	0.2 + 0.125	0(6)	–
MIPI D-PHY (low power) 1.2V	MIPI_DPHY_DCI_LP	0.715 – 0.2	0.715 + 0.2	0(6)	–

Notes:

1. The input delay measurement methodology parameters for LVDCI/HSLVDCI are the same for LVCMOS standards of the same voltage. Parameters for all other DCI standards are the same for the corresponding non-DCI standards.
2. Input waveform switches between V_L and V_H.
3. Measurements are made at typical, minimum, and maximum V_{REF} values. Reported delays reflect worst case of these measurements. V_{REF} values listed are typical.
4. Input voltage level from which measurement starts.
5. This is an input voltage reference that bears no relation to the V_{REF}/V_{MEAS} parameters found in IBIS models and/or noted in Figure 1.
6. The value given is the differential input voltage.

Output Delay Measurement Methodology

Output delays are measured with short output traces. Standard termination was used for all testing. The propagation delay of the trace is characterized separately and subtracted from the final measurement, and is therefore not included in the generalized test setups shown in Figure 1 and Figure 2.

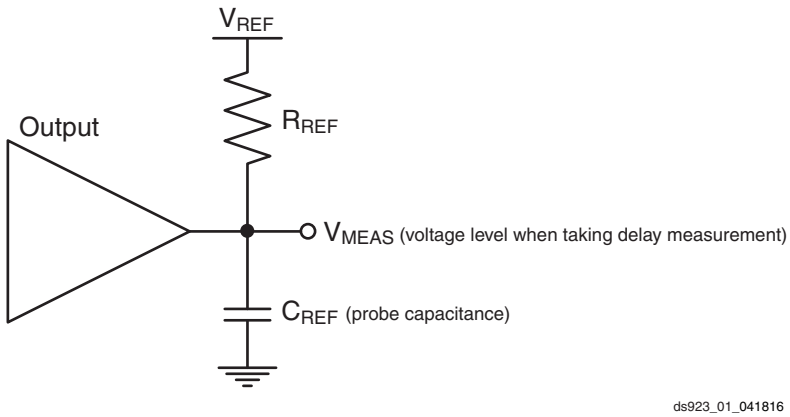

Figure 1: **Single-Ended Test Setup**

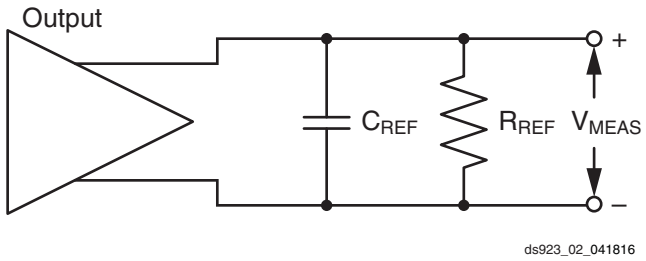

Figure 2: **Differential Test Setup**

Parameters V_{REF}, R_{REF}, C_{REF}, and V_{MEAS} fully describe the test conditions for each I/O standard. The most accurate prediction of propagation delay in any given application can be obtained through IBIS simulation, using this method:

1. Simulate the output driver of choice into the generalized test setup using values from Table 27.
2. Record the time to V_{MEAS}.
3. Simulate the output driver of choice into the actual PCB trace and load using the appropriate IBIS model or capacitance value to represent the load.
4. Record the time to V_{MEAS}.
5. Compare the results of step 2 and step 4. The increase or decrease in delay yields the actual propagation delay of the PCB trace.

Table 27: **Output Delay Measurement Methodology**

Description	I/O Standard Attribute	R_{REF} (Ω)	C_{REF}[1] (pF)	V_{MEAS} (V)	V_{REF} (V)
LVCMOS, 1.2V	LVCMOS12	1M	0	0.6	0
LVCMOS, 1.5V	LVCMOS15	1M	0	0.75	0
LVCMOS, 1.8V	LVCMOS18	1M	0	0.9	0
LVDCI, HSLVDCI, 1.5V	LVDCI_15, HSLVDCI_15	50	0	V_{REF}	0.75
LVDCI, HSLVDCI, 1.8V	LVDCI_15, HSLVDCI_18	50	0	V_{REF}	0.9
HSTL (high-speed transceiver logic), class I, 1.2V	HSTL_I_12	50	0	V_{REF}	0.6
HSTL, class I, 1.5V	HSTL_I	50	0	V_{REF}	0.75
HSTL, class I, 1.8V	HSTL_I_18	50	0	V_{REF}	0.9
HSUL (high-speed unterminated logic), 1.2V	HSUL_12	50	0	V_{REF}	0.6
SSTL12 (stub series terminated logic), 1.2V	SSTL12	50	0	V_{REF}	0.6
SSTL135, 1.35V	SSTL135	50	0	V_{REF}	0.675
SSTL15, 1.5V	SSTL15	50	0	V_{REF}	0.75
SSTL18, class I, 1.8V	SSTL18_I	50	0	V_{REF}	0.9
POD10, 1.0V	POD10	50	0	V_{REF}	1.0
POD12, 1.2V	POD12	50	0	V_{REF}	1.2
DIFF_HSTL, class I, 1.2V	DIFF_HSTL_I_12	50	0	V_{REF}	0.6
DIFF_HSTL, class I, 1.5V	DIFF_HSTL_I	50	0	V_{REF}	0.75
DIFF_HSTL, class I, 1.8V	DIFF_HSTL_I_18	50	0	V_{REF}	0.9
DIFF_HSUL, 1.2V	DIFF_HSUL_12	50	0	V_{REF}	0.6
DIFF_SSTL12, 1.2V	DIFF_SSTL12	50	0	V_{REF}	0.6
DIFF_SSTL135, 1.35V	DIFF_SSTL135	50	0	V_{REF}	0.675
DIFF_SSTL15, 1.5V	DIFF_SSTL15	50	0	V_{REF}	0.75
DIFF_SSTL18, 1.8V	DIFF_SSTL18_I	50	0	V_{REF}	0.9
DIFF_POD10, 1.0V	DIFF_POD10	50	0	V_{REF}	1.0
DIFF_POD12, 1.2V	DIFF_POD12	50	0	V_{REF}	1.2
LVDS (low-voltage differential signaling), 1.8V	LVDS	100	0	0[2]	0
SUB_LVDS, 1.8V	SUB_LVDS	100	0	0[2]	0
MIPI D-PHY (high speed) 1.2V	MIPI_DPHY_DCI_HS	100	0	0[2]	0
MIPI D-PHY (low power) 1.2V	MIPI_DPHY_DCI_LP	1M	0	0.6	0

Notes:

1. C_{REF} is the capacitance of the probe, nominally 0 pF.
2. The value given is the differential output voltage.

Clock Buffers and Networks

Table 32: **Clock Buffers Switching Characteristics**

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages				Units
		0.90V	0.85V		0.72V	
		-3	-2	-1	-2	
Global Clock Switching Characteristics (Including BUFGCTRL)						
F_{MAX}	Maximum frequency of a global clock tree (BUFG).	891	775	667	725	MHz
Global Clock Buffer with Input Divide Capability (BUFGCE_DIV)						
F_{MAX}	Maximum frequency of a global clock buffer with input divide capability (BUFGCE_DIV).	891	775	667	725	MHz
Global Clock Buffer with Clock Enable (BUFGCE)						
F_{MAX}	Maximum frequency of a global clock buffer with clock enable (BUFGCE).	891	775	667	725	MHz
Leaf Clock Buffer with Clock Enable (BUFCE_LEAF)						
F_{MAX}	Maximum frequency of a leaf clock buffer with clock enable (BUFCE_LEAF).	891	775	667	725	MHz
GTY Clock Buffer with Clock Enable and Clock Input Divide Capability (BUFG_GT)						
F_{MAX}	Maximum frequency of a serial transceiver clock buffer with clock enable and clock input divide capability.	512	512	512	512	MHz

MMCM Switching Characteristics

Table 33: **MMCM Specification**

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages				Units
		0.90V	0.85V		0.72V	
		-3	-2	-1	-2	
MMCM_F_{INMAX}	Maximum input clock frequency.	1066	933	800	933	MHz
MMCM_F_{INMIN}	Minimum input clock frequency.	10	10	10	10	MHz
MMCM_$F_{INJITTER}$	Maximum input clock period jitter.	< 20% of clock input period or 1 ns Max				
MMCM_F_{INDUTY}	Input duty cycle range: 10–49 MHz.	25–75				%
	Input duty cycle range: 50–199 MHz.	30–70				%
	Input duty cycle range: 200–399 MHz.	35–65				%
	Input duty cycle range: 400–499 MHz.	40–60				%
	Input duty cycle range: >500 MHz.	45–55				%
MMCM_F_{MIN_PSCLK}	Minimum dynamic phase shift clock frequency.	0.01	0.01	0.01	0.01	MHz
MMCM_F_{MAX_PSCLK}	Maximum dynamic phase shift clock frequency.	550	500	450	500	MHz
MMCM_F_{VCOMIN}	Minimum MMCM VCO frequency.	800	800	800	800	MHz
MMCM_F_{VCOMAX}	Maximum MMCM VCO frequency.	1600	1600	1600	1600	MHz
MMCM_$F_{BANDWIDTH}$	Low MMCM bandwidth at typical.(1)	1.00	1.00	1.00	1.00	MHz
	High MMCM bandwidth at typical.(1)	4.00	4.00	4.00	4.00	MHz
MMCM_$T_{STATPHAOFFSET}$	Static phase offset of the MMCM outputs.(2)	0.12	0.12	0.12	0.12	ns
MMCM_$T_{OUTJITTER}$	MMCM output jitter.	Note 3				
MMCM_$T_{OUTDUTY}$	MMCM output clock duty cycle precision.(4)	0.165	0.20	0.20	0.20	ns
MMCM_$T_{LOCKMAX}$	MMCM maximum lock time for MMCM_F_{PFDMIN}.	100	100	100	100	µs
MMCM_F_{OUTMAX}	MMCM maximum output frequency.	891	775	667	725	MHz
MMCM_F_{OUTMIN}	MMCM minimum output frequency.(4)(5)	6.25	6.25	6.25	6.25	MHz
MMCM_$T_{EXTFDVAR}$	External clock feedback variation.	< 20% of clock input period or 1 ns Max				
MMCM_$RST_{MINPULSE}$	Minimum reset pulse width.	5.00	5.00	5.00	5.00	ns
MMCM_F_{PFDMAX}	Maximum frequency at the phase frequency detector.	550	500	450	500	MHz
MMCM_F_{PFDMIN}	Minimum frequency at the phase frequency detector.	10	10	10	10	MHz
MMCM_$T_{FBDELAY}$	Maximum delay in the feedback path.	5 ns Max or one clock cycle				
MMCM_F_{DPRCLK_MAX}	Maximum DRP clock frequency	250	250	250	250	MHz

Notes:

1. The MMCM does not filter typical spread-spectrum input clocks because they are usually far below the bandwidth filter frequencies.
2. The static offset is measured between any MMCM outputs with identical phase.
3. Values for this parameter are available in the Clocking Wizard.
4. Includes global clock buffer.
5. Calculated as F_{VCO}/128 assuming output duty cycle is 50%.

PLL Switching Characteristics

Table 34: **PLL Specification(1)**

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages				Units
		0.90V	0.85V		0.72V	
		-3	-2	-1	-2	
PLL_F_{INMAX}	Maximum input clock frequency.	1066	933	800	933	MHz
PLL_F_{INMIN}	Minimum input clock frequency.	70	70	70	70	MHz
PLL_$F_{INJITTER}$	Maximum input clock period jitter.	< 20% of clock input period or 1 ns Max				
PLL_F_{INDUTY}	Input duty cycle range: 70–399 MHz.	35–65				%
	Input duty cycle range: 400–499 MHz.	40–60				%
	Input duty cycle range: >500 MHz.	45–55				%
PLL_F_{VCOMIN}	Minimum PLL VCO frequency.	750	750	750	750	MHz
PLL_F_{VCOMAX}	Maximum PLL VCO frequency.	1500	1500	1500	1500	MHz
PLL_$T_{STATPHAOFFSET}$	Static phase offset of the PLL outputs.(2)	0.12	0.12	0.12	0.12	ns
PLL_$T_{OUTJITTER}$	PLL output jitter.	Note 3				
PLL_$T_{OUTDUTY}$	PLL CLKOUT0, CLKOUT0B, CLKOUT1, CLKOUT1B duty-cycle precision.(4)	0.165	0.20	0.20	0.20	ns
PLL_$T_{LOCKMAX}$	PLL maximum lock time.	100				µs
PLL_F_{OUTMAX}	PLL maximum output frequency at CLKOUT0, CLKOUT0B, CLKOUT1, CLKOUT1B.	891	775	667	725	MHz
	PLL maximum output frequency at CLKOUTPHY.	2667	2667	2400	2400	MHz
PLL_F_{OUTMIN}	PLL minimum output frequency at CLKOUT0, CLKOUT0B, CLKOUT1, CLKOUT1B.(5)	5.86	5.86	5.86	5.86	MHz
	PLL minimum output frequency at CLKOUTPHY.	2 x VCO mode: 1500 1 x VCO mode: 750 0.5 x VCO mode: 375				MHz
PLL_$RST_{MINPULSE}$	Minimum reset pulse width.	5.00	5.00	5.00	5.00	ns
PLL_F_{PFDMAX}	Maximum frequency at the phase frequency detector.	667.5	667.5	667.5	667.5	MHz
PLL_F_{PFDMIN}	Minimum frequency at the phase frequency detector.	70	70	70	70	MHz
PLL_$F_{BANDWIDTH}$	PLL bandwidth at typical.	14	14	14	14	MHz
PLL_F_{DPRCLK_MAX}	Maximum DRP clock frequency	250	250	250	250	MHz

Notes:

1. The PLL does not filter typical spread-spectrum input clocks because they are usually far below the loop filter frequencies.
2. The static offset is measured between any PLL outputs with identical phase.
3. Values for this parameter are available in the Clocking Wizard.
4. Includes global clock buffer.
5. Calculated as $F_{VCO}/128$ assuming output duty cycle is 50%.

GTY Transceiver Switching Characteristics

Consult www.xilinx.com/products/technology/high-speed-serial for further information.

Table 44: **GTY Transceiver Performance**

Symbol	Description	Output Divider	Speed Grade and V_{CCINT} Operating Voltages								Units
			0.90V		0.85V				0.72V		
			-3		-2		-1		-2		
F_{GTYMAX}	GTY maximum line rate		32.75(1)		28.21(1)		25.7813(1)		28.21(1)		Gb/s
F_{GTYMIN}	GTY minimum line rate		0.5		0.5		0.5		0.5		Gb/s
			Min	Max	Min	Max	Min	Max	Min	Max	
$F_{GTYCRANGE}$	CPLL line rate range(2)	1	4.0	12.5	4.0	12.5	4.0	8.5	4.0	12.5	Gb/s
		2	2.0	6.25	2.0	6.25	2.0	4.25	2.0	6.25	Gb/s
		4	1.0	3.125	1.0	3.125	1.0	2.125	1.0	3.125	Gb/s
		8	0.5	1.5625	0.5	1.5625	0.5	1.0625	0.5	1.5625	Gb/s
		16	N/A								Gb/s
		32	N/A								Gb/s
			Min	Max	Min	Max	Min	Max	Min	Max	
$F_{GTYQRANGE1}$	QPLL0 line rate range(3)	1	19.6	32.75	19.6	28.21	19.6	25.7813	19.6	28.21	Gb/s
		1	9.8	16.375	9.8	16.375	9.8	12.5	9.8	16.375	Gb/s
		2	4.9	8.1875	4.9	8.1875	4.9	8.1875	4.9	8.1875	Gb/s
		4	2.45	4.09375	2.45	4.09375	2.45	4.09375	2.45	4.09375	Gb/s
		8	1.225	2.04688	1.225	2.04688	1.225	2.04688	1.225	2.04688	Gb/s
		16	0.6125	1.02344	0.6125	1.02344	0.6125	1.02344	0.6125	1.02344	Gb/s
			Min	Max	Min	Max	Min	Max	Min	Max	
$F_{GTYQRANGE2}$	QPLL1 line rate range(4)	1	16.0	26.0	16.0	26.0	19.6	25.7813	16.0	26.0	Gb/s
		1	8.0	13.0	8.0	13.0	8.0	12.5	8.0	13.0	Gb/s
		2	4.0	6.5	4.0	6.5	4.0	6.5	4.0	6.5	Gb/s
		4	2.0	3.25	2.0	3.25	2.0	3.25	2.0	3.25	Gb/s
		8	1.0	1.625	1.0	1.625	1.0	1.625	1.0	1.625	Gb/s
		16	0.5	0.8125	0.5	0.8125	0.5	0.8125	0.5	0.8125	Gb/s
			Min	Max	Min	Max	Min	Max	Min	Max	
$F_{CPLLRANGE}$	CPLL frequency range		2.0	6.25	2.0	6.25	2.0	4.25	2.0	6.25	GHz
$F_{QPLL0RANGE}$	QPLL0 frequency range		9.8	16.375	9.8	16.375	9.8	16.375	9.8	16.375	GHz
$F_{QPLL1RANGE}$	QPLL1 frequency range		8.0	13.0	8.0	13.0	8.0	13.0	8.0	13.0	GHz

Notes:

1. XCVU11P devices in the FLGF1924 package have a maximum GTY transceiver line rate of 16.3 Gb/s.
2. The values listed are the rounded results of the calculated equation (2 x CPLL_Frequency)/Output_Divider.
3. The values listed are the rounded results of the calculated equation (2 x QPLL0_Frequency)/Output_Divider.
4. The values listed are the rounded results of the calculated equation (2 x QPLL1_Frequency)/Output_Divider.

Table 45: **GTY Transceiver Dynamic Reconfiguration Port (DRP) Switching Characteristics**

Symbol	Description	All Speed Grades	Units
$F_{GTYDRPCLK}$	GTYDRPCLK maximum frequency.	250	MHz

Table 46: **GTY Transceiver Reference Clock Switching Characteristics**

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
F_{GCLK}	Reference clock frequency range.		60	–	820	MHz
T_{RCLK}	Reference clock rise time.	20% – 80%	–	200	–	ps
T_{FCLK}	Reference clock fall time.	80% – 20%	–	200	–	ps
T_{DCREF}	Reference clock duty cycle.	Transceiver PLL only	40	50	60	%

Table 47: **GTY Transceiver Reference Clock Oscillator Selection Phase Noise Mask(1)**

Symbol	Description	Offset Frequency	Min	Typ	Max	Units
$QPLL_{REFCLKMASK}$	QPLL0/QPLL1 reference clock select phase noise mask at REFCLK frequency = 156.25 MHz.	10 kHz	–	–	–112	dBc/Hz
		100 kHz	–	–	–128	
		1 MHz	–	–	–145	
	QPLL0/QPLL1 reference clock select phase noise mask at REFCLK frequency = 312.5 MHz.	10 kHz	–	–	–103	dBc/Hz
		100 kHz	–	–	–123	
		1 MHz	–	–	–143	
	QPLL0/QPLL1 reference clock select phase noise mask at REFCLK frequency =625 MHz.	10 kHz	–	–	–98	dBc/Hz
		100 kHz	–	–	–117	
		1 MHz	–	–	–140	
$CPLL_{REFCLKMASK}$	CPLL reference clock select phase noise mask at REFCLK frequency = 156.25 MHz.	10 kHz	–	–	–112	dBc/Hz
		100 kHz	–	–	–128	
		1 MHz	–	–	–145	
		50 MHz	–	–	–145	
	CPLL reference clock select phase noise mask at REFCLK frequency = 312.5 MHz.	10 kHz	–	–	–103	dBc/Hz
		100 kHz	–	–	–123	
		1 MHz	–	–	–143	
		50 MHz	–	–	–145	
	CPLL reference clock select phase noise mask at REFCLK frequency = 625 MHz.	10 kHz	–	–	–98	dBc/Hz
		100 kHz	–	–	–117	
		1 MHz	–	–	–140	
		50 MHz	–	–	–144	

Notes:

1. For reference clock frequencies not in this table, use the phase-noise mask for the nearest reference clock frequency.

Table 48: **GTY Transceiver PLL/Lock Time Adaptation**

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
T_{LOCK}	Initial PLL lock.		–	–	1	ms
T_{DLOCK}	Clock recovery phase acquisition and adaptation time for decision feedback equalizer (DFE).	After the PLL is locked to the reference clock, this is the time it takes to lock the clock data recovery (CDR) to the data present at the input.	–	50,000	37×10^6	UI
	Clock recovery phase acquisition and adaptation time for low-power mode (LPM) when the DFE is disabled.		–	50,000	2.3×10^6	UI

Table 49: **GTY Transceiver User Clock Switching Characteristics(1)**

Symbol	Description	Data Width Conditions (Bit)		Speed Grade and V_{CCINT} Operating Voltages				Units
				0.90V	0.85V		0.72V	
		Internal Logic	Interconnect Logic	-3	-2	-1	-2	
$F_{TXOUTPMA}$	TXOUTCLK maximum frequency sourced from OUTCLKPMA			511.719	511.719	402.833	402.833	MHz
$F_{RXOUTPMA}$	RXOUTCLK maximum frequency sourced from OUTCLKPMA			511.719	511.719	402.833	402.833	MHz
$F_{TXOUTPROGDIV}$	TXOUTCLK maximum frequency sourced from TXPROGDIVCLK			511.719	511.719	511.719	511.719	MHz
$F_{RXOUTPROGDIV}$	RXOUTCLK maximum frequency sourced from RXPROGDIVCLK			511.719	511.719	511.719	511.719	MHz
F_{TXIN}	TXUSRCLK(2) maximum frequency	16	16, 32	511.719	511.719	390.625	390.625	MHz
		32	32, 64	511.719	511.719	390.625	390.625	MHz
		64	64, 128	511.719	440.781	402.832	402.832	MHz
		20	20, 40	409.375	409.375	312.500	312.500	MHz
		40	40, 80	409.375	409.375	312.500	350.000	MHz
		80	80, 160	409.375	352.625	322.266	352.625	MHz
F_{RXIN}	RXUSRCLK(2) maximum frequency	16	16, 32	511.719	511.719	390.625	390.625	MHz
		32	32, 64	511.719	511.719	390.625	390.625	MHz
		64	64, 128	511.719	440.781	402.832	402.832	MHz
		20	20, 40	409.375	409.375	312.500	312.500	MHz
		40	40, 80	409.375	409.375	312.500	350.000	MHz
		80	80, 160	409.375	352.625	322.266	352.625	MHz

Table 50: **GTY Transceiver Transmitter Switching Characteristics *(Cont'd)***

Symbol	Description	Condition	Min	Typ	Max	Units
$T_{J3.20}$	Total jitter(3)(4)	3.20 Gb/s(5)	–	–	0.20	UI
$D_{J3.20}$	Deterministic jitter(3)(4)		–	–	0.10	UI
$T_{J2.5}$	Total jitter(3)(4)	2.5 Gb/s(6)	–	–	0.20	UI
$D_{J2.5}$	Deterministic jitter(3)(4)		–	–	0.10	UI
$T_{J1.25}$	Total jitter(3)(4)	1.25 Gb/s(7)	–	–	0.15	UI
$D_{J1.25}$	Deterministic jitter(3)(4)		–	–	0.06	UI
T_{J500}	Total jitter(3)(4)	500 Mb/s(8)	–	–	0.10	UI
D_{J500}	Deterministic jitter(3)(4)		–	–	0.03	UI

Notes:

1. Using same REFCLK input with TX phase alignment enabled for up to four consecutive transmitters (one fully populated GTY Quad) at maximum line rate.
2. Using QPLL_FBDIV = 40, 20-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
3. Using CPLL_FBDIV = 2, 20-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
4. All jitter values are based on a bit-error ratio of 10^{-12}.
5. CPLL frequency at 3.2 GHz and TXOUT_DIV = 2.
6. CPLL frequency at 2.5 GHz and TXOUT_DIV = 2.
7. CPLL frequency at 2.5 GHz and TXOUT_DIV = 4.
8. CPLL frequency at 2.0 GHz and TXOUT_DIV = 8.

Table 52: **GTY Transceiver Protocol List *(Cont'd)***

Protocol	Specification	Serial Rate (Gb/s)	Electrical Compliance
Serial RapidIO	RapidIO specification 3.1	1.25–10.3125	Compliant
DisplayPort (source only)	DP 1.2B CTS	1.62–5.4	Compliant(3)
Fibre channel	FC-PI-4	1.0625–14.025	Compliant
SATA Gen1, 2, 3	Serial ATA revision 3.0 specification	1.5, 3.0, and 6.0	Compliant
SAS Gen1, 2, 3	T10/BSR INCITS 519	3.0, 6.0, and 12.0	Compliant
SFI-5	OIF-SFI5-01.0	0.625 - 12.5	Compliant
Aurora	CEI-6G, CEI-11G-LR	All rates	Compliant

Notes:

1. 25 dB loss at Nyquist without FEC.
2. The transition time of the transmitter is faster than the IEEE Std 802.3-2012 specification.
3. This protocol requires external circuitry to achieve compliance.

Integrated Interface Block for Interlaken

More information and documentation on solutions using the integrated interface block for Interlaken can be found at UltraScale Interlaken. The *UltraScale Architecture and Product Overview* (DS890) lists how many blocks are in each Virtex UltraScale+ FPGA. This section describes the following Interlaken configurations.

- 12 x 12.5 Gb/s protocol and lane logic mode (Table 53).
- 6 x 25.78125 Gb/s and 6 x 28.21 Gb/s protocol and lane logic mode (Table 54).
- 12 x 25.78125 Gb/s lane logic only mode (Table 55).

XCVU11P devices in the FLVF1924 package are only supported using the 12 x 12.5 Gb/s Interlaken configuration. See Table 44 for the F_{GTYMAX} description.

Table 53: **Maximum Performance for Interlaken 12 x 12.5 Gb/s Protocol and Lane Logic Mode Designs**

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages										Units
		0.90V		0.85V				0.72V				
		-3		-2		-1		-2		-1		
$F_{RX\_SERDES\_CLK}$	Receive serializer/ deserializer clock	195.32		195.32		195.32		195.32		195.32		MHz
$F_{TX\_SERDES\_CLK}$	Transmit serializer/ deserializer clock	195.32		195.32		195.32		195.32		195.32		MHz
F_{DRP_CLK}	Dynamic reconfiguration port clock	250.00		250.00		250.00		250.00		250.00		MHz
		Min(1)	Max	Min(1)	Max	Min(1)	Max	Min(1)	Max	Min(1)	Max	
F_{CORE_CLK}	Interlaken core clock	300.00	322.27	300.00	322.27	300.00	322.27	300.00	322.27	300.00	322.27	MHz
F_{LBUS_CLK}	Interlaken local bus clock	300.00	322.27	300.00	322.27	300.00	322.27	300.00	322.27	300.00	322.27	MHz

Notes:

1. These are the minimum clock frequencies at the maximum lane performance.

Table 54: **Maximum Performance for Interlaken 6 x 25.78125 Gb/s and 6 x 28.21 Gb/s Protocol and Lane Logic Mode Designs**

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages										Units
		0.90V		0.85V				0.72V				
		-3(1)		-2(1)		-1		-2		-1		
$F_{RX\_SERDES\_CLK}$	Receive serializer/ deserializer clock	440.79		440.79		N/A		402.84		N/A		MHz
$F_{TX\_SERDES\_CLK}$	Transmit serializer/ deserializer clock	440.79		440.79		N/A		402.84		N/A		MHz
F_{DRP_CLK}	Dynamic reconfiguration port clock	250.00		250.00		N/A		250.00		N/A		MHz
		Min(2)	Max	Min(2)	Max	Min	Max	Min(2)	Max	Min	Max	
F_{CORE_CLK}	Interlaken core clock	412.50(3)	479.20	412.50(3)	479.20	N/A		412.50	429.69	N/A		MHz
F_{LBUS_CLK}	Interlaken local bus clock	300.00(4)	349.52	300.00(4)	349.52	N/A		300.00	349.52	N/A		MHz

Notes:

1. 6 x 28.21 mode is only supported in the -2 (V_{CCINT}=0.85V) and -3 (V_{CCINT}=0.90V) speed grades.
2. These are the minimum clock frequencies at the maximum lane performance.
3. The minimum value for CORE_CLK is 451.36 MHz for the 6 x 28.21 Gb/s protocol.
4. The minimum value for LBUS_CLK is 330.00 MHz for the 6 x 28.21 Gb/s protocol.

Table 55: **Maximum Performance for Interlaken 12 x 25.78125 Gb/s Lane Logic Only Mode Designs**

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages					Units
		0.90V	0.85V		0.72V		
		-3	-2	-1	-2	-1	
$F_{RX\_SERDES\_CLK}$	Receive serializer/ deserializer clock	402.84	402.84	N/A	N/A	N/A	MHz
$F_{TX\_SERDES\_CLK}$	Transmit serializer/ deserializer clock	402.84	402.84	N/A	N/A	N/A	MHz
F_{DRP_CLK}	Dynamic reconfiguration port clock	250.00	250.00	N/A	N/A	N/A	MHz
F_{CORE_CLK}	Interlaken core clock	412.50	412.50	N/A	N/A	N/A	MHz
F_{LBUS_CLK}	Interlaken local bus clock	349.52	349.52	N/A	N/A	N/A	MHz

Table 58: **System Monitor Specifications *(Cont'd)***

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
Supply sensor error(4)		Supply voltages 0.72V to 1.2V, T_j = –40°C to 100°C (with external REF)	–	–	±0.5	%
		Supply voltages 0.72V to 1.2V, T_j = –55°C to 125°C (with external REF)	–	–	±1.0	%
		All other supply voltages, T_j = –40°C to 100°C (with external REF)	–	–	±1.0	%
		All other supply voltages, T_j = –55°C to 125°C (with external REF)	–	–	±2.0	%
		Supply voltages 0.72V to 1.2V, T_j = –40°C to 100°C (with internal REF)	–	–	±1.0	%
		Supply voltages 0.72V to 1.2V, T_j = –55°C to 125°C (with internal REF)	–	–	±2.0	%
		All other supply voltages, T_j = –40°C to 100°C (with internal REF)	–	–	±1.5	%
		All other supply voltages, T_j = –55°C to 125°C (with internal REF)	–	–	±2.5	%
Conversion Rate(5)						
Conversion time—continuous	t_{CONV}	Number of ADCCLK cycles	26	–	32	Cycles
Conversion time—event	t_{CONV}	Number of ADCCLK cycles	–	–	21	Cycles
DRP clock frequency	DCLK	DRP clock frequency	8	–	250	MHz
ADC clock frequency	ADCCLK	Derived from DCLK	1	–	5.2	MHz
DCLK duty cycle			40	–	60	%
SYSMON Reference(6)						
External reference	V_{REFP}	Externally supplied reference voltage	1.20	1.25	1.30	V
On-chip reference		Ground V_{REFP} pin to AGND, T_j = –40°C to 100°C	1.2375	1.25	1.2625	V
		Ground V_{REFP} pin to AGND, T_j = –55°C to 125°C	1.225	1.25	1.275	V

Notes:

1. ADC offset errors are removed by enabling the ADC automatic offset calibration feature. The values are specified for when this feature is enabled.
2. See the *Analog Input* section in the *UltraScale Architecture System Monitor User Guide* (UG580).
3. When reading temperature values directly from the PMBus interface, the SYSMON has a +4°C offset due to the transfer function used by the PMBus application. For example, the external REF temperature sensor error's range of ±3°C becomes +1°C to +7°C when the temperature is read through the PMBus interface.
4. Supply sensor offset and gain errors are removed by enabling the automatic offset and gain calibration feature. The values are specified for when this feature is enabled.
5. See the *Adjusting the Acquisition Settling Time* section in the *UltraScale Architecture System Monitor User Guide* (UG580).
6. Any variation in the reference voltage from the nominal V_{REFP} = 1.25V and V_{REFN} = 0V will result in a deviation from the ideal transfer function. This also impacts the accuracy of the internal sensor measurements (i.e., temperature and power supply). However, for external ratiometric type applications allowing reference to vary by ±4% is permitted.

Table 61: **Configuration Switching Characteristics *(Cont'd)***

Symbol	Description		Speed Grade and V_{CCINT} Operating Voltages				Units
			0.90V	0.85V		0.72V	
			-3	-2	-1	-2	
SelectMAP Mode Programming Switching							
T_{SMDCCK}/T_{SMCCKD}	D[31:00] setup/hold.	XCVU3P, XCVU5P, XCVU7P, XCVU9P	4.0/0	4.0/0	4.0/0	5.0/0	ns, Min
		XCVU11P, XCVU13P	4.5/0	4.5/0	4.5/0	7.5/0	ns, Min
$T_{SMCSCCK}/T_{SMCCKCS}$	CSI_B setup/hold.	XCVU3P, XCVU5P, XCVU7P, XCVU9P	4.0/0	4.0/0	4.0/0	5.0/0	ns, Min
		XCVU11P, XCVU13P	4.5/0	4.5/0	4.5/0	7.5/0	ns, Min
T_{SMWCCK}/T_{SMCCKW}	RDWR_B setup/hold.	XCVU3P, XCVU5P, XCVU7P, XCVU9P	10.0/0	10.0/0	10.0/0	11.0/0	ns, Min
		XCVU11P, XCVU13P	11.0/0	11.0/0	11.0/0	17.0/0	ns, Min
$T_{SMCKCSO}$	CSO_B clock to out (330Ω pull-up resistor required).		7.0	7.0	7.0	7.0	ns, Max
T_{SMCO}	D[31:00] clock to out in readback.		8.0	8.0	8.0	8.0	ns, Max
F_{RBCCK}	Readback frequency.	XCVU3P, XCVU5P, XCVU7P, XCVU9P	125	125	125	100	MHz, Max
		XCVU11P, XCVU13P	125	125	125	66	MHz, Max
Boundary-Scan Port Timing Specifications							
T_{TAPTCK}/T_{TCKTAP}	TMS and TDI setup/hold.	XCVU3P	3.0/ 2.0	3.0/ 2.0	3.0/ 2.0	3.0/ 2.0	ns, Min
		XCVU5P, XCVU7P, XCVU9P, XCVU11P, XCVU13P	8.5/ 2.0	8.5/ 2.0	8.5/ 2.0	8.5/ 2.0	ns, Min
T_{TCKTDO}	TCK falling edge to TDO output.	XCVU3P	7.0	7.0	7.0	7.0	ns, Max
		XCVU5P, XCVU7P, XCVU9P, XCVU11P, XCVU13P	15.0	15.0	15.0	15.0	ns, Max
F_{TCK}	TCK frequency.	XCVU3P	66	66	66	66	MHz, Max
		XCVU5P, XCVU7P, XCVU9P, XCVU11P, XCVU13P	20	20	20	20	MHz, Max
BPI Master Flash Mode Programming Switching							
T_{BPICCO}	A[28:00], RS[1:0], FCS_B, FOE_B, FWE_B, ADV_B clock to out.		10	10	10	10	ns, Max
T_{BPIDCC}/T_{BPICCD}	D[15:00] setup/hold.	XCVU3P, XCVU5P, XCVU7P, XCVU9P	4.0/0	4.0/0	4.0/0	5.0/0	ns, Min
		XCVU11P, XCVU13P	4.5/0	4.5/0	4.5/0	7.5/0	ns, Min
SPI Master Flash Mode Programming Switching							
T_{SPIDCC}/T_{SPICCD}	D[03:00] setup/hold.		3.0/0	3.0/0	3.0/0	4.0/0	ns, Min
T_{SPIDCC}/T_{SPICCD}	D[07:04] setup/hold.	XCVU3P, XCVU5P, XCVU7P, XCVU9P	4.0/0	4.0/0	4.0/0	5.0/0	ns, Min
		XCVU11P, XCVU13P	4.5/0	4.5/0	4.5/0	7.5/0	ns, Min
T_{SPICCM}	MOSI clock to out.		8.0	8.0	8.0	8.0	ns, Max
$T_{SPICCFC}$	FCS_B clock to out.		8.0	8.0	8.0	8.0	ns, Max