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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | 162000 |
| Number of Logic Elements/Cells | 2835000 |
| Total RAM Bits | 396150400 |
| Number of I/O | 416 |
| Number of Gates | - |
| Voltage - Supply | 0.873V ~ 0.927V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 100°C (TJ) |
| Package / Case | 2104-BBGA, FCBGA |
| Supplier Device Package | 2104-FCBGA (47.5x47.5) |
| Purchase URL | https://www.e-xfl.com/product-detail/xilinx/xcvu11p-3flgc2104e |

*Table 2:* **Recommended Operating Conditions(1)(2) *(Cont'd)***

| Symbol | Description | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| **SYSMON** | | | | | |
| $V_{CCADC}$ | SYSMON supply relative to GNDADC. | 1.746 | 1.800 | 1.854 | V |
| $V_{REFP}$ | SYSMON externally supplied reference voltage relative to GNDADC. | 1.200 | 1.250 | 1.300 | V |
| **Temperature** | | | | | |
| $T_j$(11) | Junction temperature operating range for extended (E) temperature devices.(12) | 0 | – | 100 | °C |
| | Junction temperature operating range for industrial (I) temperature devices. | –40 | – | 100 | °C |
| | Junction temperature operating range for eFUSE programming.(13) | –40 | – | 125 | °C |

**Notes:**

1. All voltages are relative to GND.
2. For the design of the power distribution system consult *UltraScale Architecture PCB Design Guide* (UG583).
3. $V_{CCINT\_IO}$ must be connected to $V_{CCBRAM}$.
4. For $V_{CCO\_0}$, the minimum recommended operating voltage for power on and during configuration is 1.425V. After configuration, data is retained even if $V_{CCO}$ drops to 0V.
5. Includes $V_{CCO}$ of 1.0V, 1.2V, 1.35V, 1.5V, and 1.8V.
6. $V_{CCAUX\_IO}$ must be connected to $V_{CCAUX}$.
7. The lower absolute voltage specification always applies.
8. A total of 200 mA per bank should not be exceeded.
9. If battery is not used, connect $V_{BATT}$ to either GND or $V_{CCAUX}$.
10. Each voltage listed requires filtering as described in the *UltraScale Architecture GTY Transceiver User Guide* (UG578).
11. Xilinx recommends measuring the Tj of a device using the system monitor as described in the *UltraScale Architecture System Monitor User Guide* (UG580). The SYSMON temperature measurement errors (that are described in Table 58) must be accounted for in your design. For example, by using an external reference of 1.25V, when SYSMON reports 97°C, there is a measurement error ±3°C. A reading of 97°C is considered the maximum adjusted Tj (100°C – 3°C = 97°C).
12. Devices labeled with the speed/temperature grade of -2LE can operate for a limited time at a junction temperature of 110°C. Timing parameters adhere to the same speed file at 110°C as they do below 110°C, regardless of operating voltage (nominal voltage of 0.85V or a low-voltage of 0.72V). Operation at Tj = 110°C is limited to 1% of the device lifetime and can occur sequentially or at regular intervals as long as the total time does not exceed 1% of the device lifetime.
13. Do not program eFUSE during device configuration (e.g., during configuration, during configuration readback, or when readback CRC is active).

# $V_{IN}$ Maximum Allowed AC Voltage Overshoot and Undershoot

*Table 4:* **$V_{IN}$ Maximum Allowed AC Voltage Overshoot and Undershoot for HP I/O Banks(1)(2)**

| AC Voltage Overshoot | % of UI at –40°C to 100°C | AC Voltage Undershoot | % of UI at –40°C to 100°C |
|---|---|---|---|
| $V_{CCO}$ + 0.30 | 100% | –0.30 | 100% |
| $V_{CCO}$ + 0.35 | 100% | –0.35 | 90% |
| $V_{CCO}$ + 0.40 | 92% | –0.40 | 92% |
| $V_{CCO}$ + 0.45 | 50% | –0.45 | 50% |
| $V_{CCO}$ + 0.50 | 20% | –0.50 | 20% |
| $V_{CCO}$ + 0.55 | 10% | –0.55 | 10% |
| $V_{CCO}$ + 0.60 | 6% | –0.60 | 6% |
| $V_{CCO}$ + 0.65 | 2% | –0.65 | 2% |
| $V_{CCO}$ + 0.70 | 2% | –0.70 | 2% |

**Notes:**
1. A total of 200 mA per bank should not be exceeded.
2. For UI smaller than 20 µs.

# Quiescent Supply Current

*Table 5:* **Typical Quiescent Supply Current(1)(2)(3)**

| Symbol | Description | Device | Speed Grade and $V_{CCINT}$ Operating Voltages | | | | Units |
|---|---|---|---|---|---|---|---|
| | | | 0.90V | 0.85V | | 0.72V | |
| | | | -3 | -2 | -1 | -2 | |
| $I_{CCINTQ}$ | Quiescent $V_{CCINT}$ supply current. | XCVU3P | 2384 | 2276 | 2276 | 2017 | mA |
| | | XCVU5P | 4769 | 4552 | 4552 | 4034 | mA |
| | | XCVU7P | 4769 | 4552 | 4552 | 4034 | mA |
| | | XCVU9P | 7153 | 6828 | 6828 | 6050 | mA |
| | | XCVU11P | 7567 | 7202 | 7202 | 6332 | mA |
| | | XCVU13P | 10090 | 9602 | 9602 | 8442 | mA |
| $I_{CCINT\_IOQ}$ | Quiescent current for $V_{CCINT\_IO}$ supply. | XCVU3P | 149 | 144 | 144 | 144 | mA |
| | | XCVU5P | 298 | 287 | 287 | 287 | mA |
| | | XCVU7P | 298 | 287 | 287 | 287 | mA |
| | | XCVU9P | 447 | 431 | 431 | 431 | mA |
| | | XCVU11P | 182 | 176 | 176 | 176 | mA |
| | | XCVU13P | 243 | 234 | 234 | 234 | mA |
| $I_{CCOQ}$ | Quiescent $V_{CCO}$ supply current. | All devices | 1 | 1 | 1 | 1 | mA |
| $I_{CCAUXQ}$ | Quiescent $V_{CCAUX}$ supply current. | XCVU3P | 268 | 268 | 268 | 268 | mA |
| | | XCVU5P | 535 | 535 | 535 | 535 | mA |
| | | XCVU7P | 535 | 535 | 535 | 535 | mA |
| | | XCVU9P | 1015 | 1015 | 1015 | 1015 | mA |
| | | XCVU11P | 819 | 819 | 819 | 819 | mA |
| | | XCVU13P | 1091 | 1091 | 1091 | 1091 | mA |

# Power Supply Requirements

Table 6 shows the minimum current, in addition to $I_{CCQ}$ maximum, required by each Virtex UltraScale+ FPGA for proper power-on and configuration. If the current minimums shown in Table 6 are met, the device powers on after all supplies have passed through their power-on reset threshold voltages. The device must not be configured until after $V_{CCINT}$ is applied. Once initialized and configured, use the Xilinx Power Estimator (XPE) tools to estimate current drain on these supplies.

*Table 6:* **Power-on Current by Device(1)**

| Device | $I_{CCINTMIN}$ | $I_{CCINT\_IOMIN} + I_{CCBRAMMIN}$ | $I_{CCOMIN}$ | $I_{CCAUXMIN} + I_{CCAUX\_IOMIN}$ | Units |
|---|---|---|---|---|---|
| XCVU3P | $I_{CCINTQ}$ + 2000 | $I_{CCBRAMQ} + I_{CCINT\_IOQ}$ + 950 | $I_{CCOQ}$ + 50 | $I_{CCAUXQ} + I_{CCAUX\_IOQ}$ + 350 | mA |
| XCVU5P | $I_{CCINTQ}$ + 4000 | $I_{CCBRAMQ} + I_{CCINT\_IOQ}$ + 1900 | $I_{CCOQ}$ + 100 | $I_{CCAUXQ} + I_{CCAUX\_IOQ}$ + 700 | mA |
| XCVU7P | $I_{CCINTQ}$ + 4000 | $I_{CCBRAMQ} + I_{CCINT\_IOQ}$ + 1900 | $I_{CCOQ}$ + 100 | $I_{CCAUXQ} + I_{CCAUX\_IOQ}$ + 700 | mA |
| XCVU9P | $I_{CCINTQ}$ + 6000 | $I_{CCBRAMQ} + I_{CCINT\_IOQ}$ + 2850 | $I_{CCOQ}$ + 150 | $I_{CCAUXQ} + I_{CCAUX\_IOQ}$ + 1050 | mA |
| XCVU11P | $I_{CCINTQ}$ + 6549 | $I_{CCBRAMQ} + I_{CCINT\_IOQ}$ + 3111 | $I_{CCOQ}$ + 164 | $I_{CCAUXQ} + I_{CCAUX\_IOQ}$ + 1146 | mA |
| XCVU13P | $I_{CCINTQ}$ + 8731 | $I_{CCBRAMQ} + I_{CCINT\_IOQ}$ + 4148 | $I_{CCOQ}$ + 219 | $I_{CCAUXQ} + I_{CCAUX\_IOQ}$ + 1528 | mA |

**Notes:**

1. Use the Xilinx Power Estimator (XPE) spreadsheet tool (download at www.xilinx.com/power) to estimate power-on current for all supplies.

Table 7 shows the power supply ramp time.

*Table 7:* **Power Supply Ramp Time**

| Symbol | Description | Min | Max | Units |
|---|---|---|---|---|
| $T_{VCCINT}$ | Ramp time from GND to 95% of $V_{CCINT}$. | 0.2 | 40 | ms |
| $T_{VCCINT\_IO}$ | Ramp time from GND to 95% of $V_{CCINT\_IO}$. | 0.2 | 40 | ms |
| $T_{VCCO}$ | Ramp time from GND to 95% of $V_{CCO}$. | 0.2 | 40 | ms |
| $T_{VCCAUX}$ | Ramp time from GND to 95% of $V_{CCAUX}$. | 0.2 | 40 | ms |
| $T_{VCCBRAM}$ | Ramp time from GND to 95% of $V_{CCBRAM}$. | 0.2 | 40 | ms |
| $T_{MGTAVCC}$ | Ramp time from GND to 95% of $V_{MGTAVCC}$. | 0.2 | 40 | ms |
| $T_{MGTAVTT}$ | Ramp time from GND to 95% of $V_{MGTAVTT}$. | 0.2 | 40 | ms |
| $T_{MGTVCCAUX}$ | Ramp time from GND to 95% of $V_{MGTVCCAUX}$. | 0.2 | 40 | ms |

# DC Input and Output Levels

Values for $V_{IL}$ and $V_{IH}$ are recommended input voltages. Values for $I_{OL}$ and $I_{OH}$ are guaranteed over the recommended operating conditions at the $V_{OL}$ and $V_{OH}$ test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at a minimum $V_{CCO}$ with the respective $V_{OL}$ and $V_{OH}$ voltage levels shown. Other standards are sample tested.

*Table 8:* **SelectIO DC Input and Output Levels for the I/O Banks(1)(2)(3)**

| I/O Standard | $V_{IL}$ | | $V_{IH}$ | | $V_{OL}$ | $V_{OH}$ | $I_{OL}$ | $I_{OH}$ |
|---|---|---|---|---|---|---|---|---|
| | V, Min | V, Max | V, Min | V, Max | V, Max | V, Min | mA | mA |
| HSTL_I | –0.300 | $V_{REF}$ – 0.100 | $V_{REF}$ + 0.100 | $V_{CCO}$ + 0.300 | 0.400 | $V_{CCO}$ – 0.400 | 5.8 | –5.8 |
| HSTL_I_12 | –0.300 | $V_{REF}$ – 0.080 | $V_{REF}$ + 0.080 | $V_{CCO}$ + 0.300 | 25% $V_{CCO}$ | 75% $V_{CCO}$ | 4.1 | –4.1 |
| HSTL_I_18 | –0.300 | $V_{REF}$ – 0.100 | $V_{REF}$ + 0.100 | $V_{CCO}$ + 0.300 | 0.400 | $V_{CCO}$ – 0.400 | 6.2 | –6.2 |
| HSUL_12 | –0.300 | $V_{REF}$ – 0.130 | $V_{REF}$ + 0.130 | $V_{CCO}$ + 0.300 | 20% $V_{CCO}$ | 80% $V_{CCO}$ | 0.1 | –0.1 |
| LVCMOS12 | –0.300 | 35% $V_{CCO}$ | 65% $V_{CCO}$ | $V_{CCO}$ + 0.300 | 0.400 | $V_{CCO}$ – 0.400 | Note 4 | Note 4 |
| LVCMOS15 | –0.300 | 35% $V_{CCO}$ | 65% $V_{CCO}$ | $V_{CCO}$ + 0.300 | 0.450 | $V_{CCO}$ – 0.450 | Note 5 | Note 5 |
| LVCMOS18 | –0.300 | 35% $V_{CCO}$ | 65% $V_{CCO}$ | $V_{CCO}$ + 0.300 | 0.450 | $V_{CCO}$ – 0.450 | Note 5 | Note 5 |
| LVDCI_15 | –0.300 | 35% $V_{CCO}$ | 65% $V_{CCO}$ | $V_{CCO}$ + 0.300 | 0.450 | $V_{CCO}$ – 0.450 | 7.0 | –7.0 |
| LVDCI_18 | –0.300 | 35% $V_{CCO}$ | 65% $V_{CCO}$ | $V_{CCO}$ + 0.300 | 0.450 | $V_{CCO}$ – 0.450 | 7.0 | –7.0 |
| SSTL12 | –0.300 | $V_{REF}$ – 0.100 | $V_{REF}$ + 0.100 | $V_{CCO}$ + 0.300 | $V_{CCO}$/2 – 0.150 | $V_{CCO}$/2 + 0.150 | 8.0 | –8.0 |
| SSTL135 | –0.300 | $V_{REF}$ – 0.090 | $V_{REF}$ + 0.090 | $V_{CCO}$ + 0.300 | $V_{CCO}$/2 – 0.150 | $V_{CCO}$/2 + 0.150 | 9.0 | –9.0 |
| SSTL15 | –0.300 | $V_{REF}$ – 0.100 | $V_{REF}$ + 0.100 | $V_{CCO}$ + 0.300 | $V_{CCO}$/2 – 0.175 | $V_{CCO}$/2 + 0.175 | 10.0 | –10.0 |
| SSTL18_I | –0.300 | $V_{REF}$ – 0.125 | $V_{REF}$ + 0.125 | $V_{CCO}$ + 0.300 | $V_{CCO}$/2 – 0.470 | $V_{CCO}$/2 + 0.470 | 7.0 | –7.0 |
| MIPI_DPHY_DCI_LP(6) | –0.300 | 0.550 | 0.880 | $V_{CCO}$ + 0.300 | 0.050 | 1.100 | 0.01 | –0.01 |

**Notes:**

1. Tested according to relevant specifications.
2. Standards specified using the default I/O standard configuration. For details, see the *UltraScale Architecture SelectIO Resources User Guide* (UG571).
3. POD10 and POD12 DC input and output levels are shown in Table 9, Table 13, and Table 14.
4. Supported drive strengths of 2, 4, 6, or 8 mA in the I/O banks.
5. Supported drive strengths of 2, 4, 6, 8, or 12 mA in the I/O banks.
6. Low-power option for MIPI_DPHY_DCI.

*Table 9:* **DC Input Levels for Single-ended POD10 and POD12 I/O Standards(1)(2)**

| I/O Standard | $V_{IL}$ | | $V_{IH}$ | |
|---|---|---|---|---|
| | V, Min | V, Max | V, Min | V, Max |
| POD10 | –0.300 | $V_{REF}$ – 0.068 | $V_{REF}$ + 0.068 | $V_{CCO}$ + 0.300 |
| POD12 | –0.300 | $V_{REF}$ – 0.068 | $V_{REF}$ + 0.068 | $V_{CCO}$ + 0.300 |

**Notes:**

1. Tested according to relevant specifications.
2. Standards specified using the default I/O standard configuration. For details, see the *UltraScale Architecture SelectIO Resources User Guide* (UG571).

# AC Switching Characteristics

All values represented in this data sheet are based on the speed specifications in the Vivado® Design Suite as outlined in Table 16.

*Table 16:* **Speed Specification Version By Device**

| 2017.1 | Device |
|---|---|
| 1.10 | XCVU3P, XCVU7P, XCVU9P, XCVU5P, XCVU11P, XCVU13P |

Switching characteristics are specified on a per-speed-grade basis and can be designated as Advance, Preliminary, or Production. Each designation is defined as follows:

**Advance Product Specification**

These specifications are based on simulations only and are typically available soon after device design specifications are frozen. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

**Preliminary Product Specification**

These specifications are based on complete ES (engineering sample) silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting delays is greatly reduced as compared to Advance data.

**Product Specification**

These specifications are released once enough production silicon of a particular device family member has been characterized to provide full correlation between specifications and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to production before faster speed grades.

## Testing of AC Switching Characteristics

Internal timing parameters are derived from measuring internal test patterns. All AC switching characteristics are representative of worst-case supply voltage and junction temperature conditions.

For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer and back-annotate to the simulation net list. Unless otherwise noted, values apply to all Virtex UltraScale+ FPGAs.

## Production Silicon and Software Status

In some cases, a particular family member (and speed grade) is released to production before a speed specification is released with the correct label (Advance, Preliminary, Production). Any labeling discrepancies are corrected in subsequent speed specification releases.

Table 18 lists the production released Virtex UltraScale+ FPGA, speed grade, and the minimum corresponding supported speed specification version and Vivado software revisions. The Vivado software and speed specifications listed are the minimum releases required for production. All subsequent releases of software and speed specifications are valid.

*Table 18:* **Virtex UltraScale+ FPGA Device Production Software and Speed Specification Release**

| Device | Speed Grade and $V_{CCINT}$ Operating Voltages | | | | |
|---|---|---|---|---|---|
| | 0.90V | 0.85V | | | 0.72V |
| | -3 | -2 | -1 | -2L | -2L |
| XCVU3P | | Vivado tools 2017.1 v1.10 | | | |
| XCVU5P | | | | | |
| XCVU7P | | | | | |
| XCVU9P | | | | | |
| XCVU11P | | | | | |
| XCVU13P | | | | | |

**Notes:**

1. Blank entries indicate a device and/or speed grade in Advance or Preliminary status.

# FPGA Logic Performance Characteristics

This section provides the performance characteristics of some common functions and designs implemented in Virtex UltraScale+ FPGAs. These values are subject to the same guidelines as the AC Switching Characteristics, page 13.

*Table 19:* **LVDS Component Mode Performance**

| Description | Speed Grade and $V_{CCINT}$ Operating Voltages | | | | | | | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | 0.90V | | 0.85V | | | | 0.72V | | |
| | -3 | | -2 | | -1 | | -2 | | |
| | Min | Max | Min | Max | Min | Max | Min | Max | |
| LVDS TX DDR (OSERDES 4:1, 8:1) | 0 | 1250 | 0 | 1250 | 0 | 1250 | 0 | 1250 | Mb/s |
| LVDS TX SDR (OSERDES 2:1, 4:1) | 0 | 625 | 0 | 625 | 0 | 625 | 0 | 625 | Mb/s |
| LVDS RX DDR (ISERDES 1:4, 1:8)(1) | 0 | 1250 | 0 | 1250 | 0 | 1250 | 0 | 1250 | Mb/s |
| LVDS RX SDR (ISERDES 1:2, 1:4)(1) | 0 | 625 | 0 | 625 | 0 | 625 | 0 | 625 | Mb/s |

**Notes:**

1. LVDS receivers are typically bounded with certain applications to achieve maximum performance. Package skews are not included and should be removed through PCB routing.

*Table 20:* **LVDS Native Mode Performance(1)(2)**

| Description | DATA_WIDTH | Speed Grade and $V_{CCINT}$ Operating Voltages | | | | | | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | | 0.90V | | 0.85V | | | | 0.72V | | |
| | | -3 | | -2 | | -1 | | -2 | | |
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| LVDS TX DDR (TX_BITSLICE) | 4 | 375 | 1600 | 375 | 1600 | 375 | 1260 | 375 | 1400 | Mb/s |
| | 8 | 375 | 1600 | 375 | 1600 | 375 | 1260 | 375 | 1600 | Mb/s |
| LVDS TX SDR (TX_BITSLICE) | 4 | 187.5 | 800 | 187.5 | 800 | 187.5 | 630 | 187.5 | 700 | Mb/s |
| | 8 | 187.5 | 800 | 187.5 | 800 | 187.5 | 630 | 187.5 | 800 | Mb/s |
| LVDS RX DDR (RX_BITSLICE)(3) | 4 | 375 | 1600 | 375 | 1600 | 375 | 1260 | 375 | 1400 | Mb/s |
| | 8 | 375 | 1600 | 375 | 1600 | 375 | 1260 | 375 | 1600 | Mb/s |
| LVDS RX SDR (RX_BITSLICE)(3) | 4 | 187.5 | 800 | 187.5 | 800 | 187.5 | 630 | 187.5 | 700 | Mb/s |
| | 8 | 187.5 | 800 | 187.5 | 800 | 187.5 | 630 | 187.5 | 800 | Mb/s |

**Notes:**

1. Native mode is supported through the High-Speed SelectIO Interface Wizard available with the Vivado Design Suite.
2. PLL settings can restrict the minimum allowable data rate. For example, when using the PLL with CLKOUTPHY_MODE = VCO_HALF the minimum frequency is PLL_FVCOMIN/2.
3. LVDS receivers are typically bounded with certain applications to achieve maximum performance. Package skews are not included and should be removed through PCB routing.

*Table 21:* **MIPI D-PHY Performance**

| Description | Speed Grade and $V_{CCINT}$ Operating Voltages | | | | Units |
|---|---|---|---|---|---|
| | 0.90V | 0.85V | | 0.72V | |
| | -3 | -2 | -1 | -2 | |
| MIPI D-PHY transmitter or receiver. | 1500 | 1500 | 1260 | 1260 | Mb/s |

*Table 24:* **IOB High Performance (HP) Switching Characteristics *(Cont'd)***

| I/O Standards | $T_{INBUF\_DELAY\_PAD\_I}$ | | | | $T_{OUTBUF\_DELAY\_O\_PAD}$ | | | | $T_{OUTBUF\_DELAY\_TD\_PAD}$ | | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 0.90V | 0.85V | | 0.72V | 0.90V | 0.85V | | 0.72V | 0.90V | 0.85V | | 0.72V | |
| | -3 | -2 | -1 | -2 | -3 | -2 | -1 | -2 | -3 | -2 | -1 | -2 | |
| HSLVDCI_18_S | 0.424 | 0.424 | 0.447 | 0.424 | 0.761 | 0.761 | 0.817 | 0.761 | 0.836 | 0.836 | 0.900 | 0.836 | ns |
| HSTL_I_12_F | 0.378 | 0.378 | 0.399 | 0.378 | 0.423 | 0.423 | 0.443 | 0.423 | 0.553 | 0.553 | 0.582 | 0.553 | ns |
| HSTL_I_12_M | 0.378 | 0.378 | 0.399 | 0.378 | 0.551 | 0.551 | 0.582 | 0.551 | 0.642 | 0.642 | 0.679 | 0.642 | ns |
| HSTL_I_12_S | 0.378 | 0.378 | 0.399 | 0.378 | 0.750 | 0.750 | 0.799 | 0.750 | 0.813 | 0.813 | 0.868 | 0.813 | ns |
| HSTL_I_18_F | 0.322 | 0.322 | 0.339 | 0.322 | 0.456 | 0.456 | 0.474 | 0.456 | 0.576 | 0.576 | 0.606 | 0.576 | ns |
| HSTL_I_18_M | 0.322 | 0.322 | 0.339 | 0.322 | 0.569 | 0.569 | 0.602 | 0.569 | 0.653 | 0.653 | 0.692 | 0.653 | ns |
| HSTL_I_18_S | 0.322 | 0.322 | 0.339 | 0.322 | 0.781 | 0.781 | 0.833 | 0.781 | 0.816 | 0.816 | 0.871 | 0.816 | ns |
| HSTL_I_DCI_12_F | 0.378 | 0.378 | 0.399 | 0.378 | 0.406 | 0.406 | 0.429 | 0.406 | 0.534 | 0.534 | 0.564 | 0.534 | ns |
| HSTL_I_DCI_12_M | 0.378 | 0.378 | 0.399 | 0.378 | 0.556 | 0.556 | 0.586 | 0.556 | 0.654 | 0.654 | 0.694 | 0.654 | ns |
| HSTL_I_DCI_12_S | 0.378 | 0.378 | 0.399 | 0.378 | 0.754 | 0.754 | 0.803 | 0.754 | 0.842 | 0.842 | 0.907 | 0.842 | ns |
| HSTL_I_DCI_18_F | 0.321 | 0.321 | 0.339 | 0.321 | 0.445 | 0.445 | 0.461 | 0.445 | 0.566 | 0.566 | 0.595 | 0.566 | ns |
| HSTL_I_DCI_18_M | 0.321 | 0.321 | 0.339 | 0.321 | 0.554 | 0.554 | 0.585 | 0.554 | 0.643 | 0.643 | 0.684 | 0.643 | ns |
| HSTL_I_DCI_18_S | 0.321 | 0.321 | 0.339 | 0.321 | 0.761 | 0.761 | 0.817 | 0.761 | 0.836 | 0.836 | 0.900 | 0.836 | ns |
| HSTL_I_DCI_F | 0.393 | 0.393 | 0.415 | 0.393 | 0.431 | 0.431 | 0.445 | 0.431 | 0.555 | 0.555 | 0.575 | 0.555 | ns |
| HSTL_I_DCI_M | 0.393 | 0.393 | 0.415 | 0.393 | 0.552 | 0.552 | 0.581 | 0.552 | 0.644 | 0.644 | 0.684 | 0.644 | ns |
| HSTL_I_DCI_S | 0.393 | 0.393 | 0.415 | 0.393 | 0.766 | 0.766 | 0.821 | 0.766 | 0.847 | 0.847 | 0.912 | 0.847 | ns |
| HSTL_I_F | 0.378 | 0.378 | 0.399 | 0.378 | 0.423 | 0.423 | 0.443 | 0.423 | 0.549 | 0.549 | 0.581 | 0.549 | ns |
| HSTL_I_M | 0.378 | 0.378 | 0.399 | 0.378 | 0.554 | 0.554 | 0.585 | 0.554 | 0.640 | 0.640 | 0.677 | 0.640 | ns |
| HSTL_I_S | 0.378 | 0.378 | 0.399 | 0.378 | 0.766 | 0.766 | 0.816 | 0.766 | 0.811 | 0.811 | 0.866 | 0.811 | ns |
| HSUL_12_DCI_F | 0.378 | 0.378 | 0.399 | 0.378 | 0.425 | 0.425 | 0.443 | 0.425 | 0.558 | 0.558 | 0.586 | 0.558 | ns |
| HSUL_12_DCI_M | 0.378 | 0.378 | 0.399 | 0.378 | 0.556 | 0.556 | 0.586 | 0.556 | 0.654 | 0.654 | 0.694 | 0.654 | ns |
| HSUL_12_DCI_S | 0.378 | 0.378 | 0.399 | 0.378 | 0.736 | 0.736 | 0.784 | 0.736 | 0.821 | 0.821 | 0.886 | 0.821 | ns |
| HSUL_12_F | 0.378 | 0.378 | 0.399 | 0.378 | 0.412 | 0.412 | 0.430 | 0.412 | 0.538 | 0.538 | 0.566 | 0.538 | ns |
| HSUL_12_M | 0.378 | 0.378 | 0.399 | 0.378 | 0.551 | 0.551 | 0.582 | 0.551 | 0.642 | 0.642 | 0.679 | 0.642 | ns |
| HSUL_12_S | 0.378 | 0.378 | 0.399 | 0.378 | 0.750 | 0.750 | 0.799 | 0.750 | 0.813 | 0.813 | 0.868 | 0.813 | ns |
| LVCMOS12_F_2 | 0.512 | 0.512 | 0.555 | 0.512 | 0.672 | 0.672 | 0.692 | 0.672 | 0.898 | 0.898 | 0.922 | 0.898 | ns |
| LVCMOS12_F_4 | 0.512 | 0.512 | 0.555 | 0.512 | 0.504 | 0.504 | 0.521 | 0.504 | 0.664 | 0.664 | 0.693 | 0.664 | ns |
| LVCMOS12_F_6 | 0.512 | 0.512 | 0.555 | 0.512 | 0.485 | 0.485 | 0.507 | 0.485 | 0.634 | 0.634 | 0.669 | 0.634 | ns |
| LVCMOS12_F_8 | 0.512 | 0.512 | 0.555 | 0.512 | 0.465 | 0.465 | 0.489 | 0.465 | 0.611 | 0.611 | 0.666 | 0.611 | ns |
| LVCMOS12_M_2 | 0.512 | 0.512 | 0.555 | 0.512 | 0.708 | 0.708 | 0.727 | 0.708 | 0.916 | 0.916 | 0.945 | 0.916 | ns |
| LVCMOS12_M_4 | 0.512 | 0.512 | 0.555 | 0.512 | 0.550 | 0.550 | 0.573 | 0.550 | 0.664 | 0.664 | 0.690 | 0.664 | ns |
| LVCMOS12_M_6 | 0.512 | 0.512 | 0.555 | 0.512 | 0.527 | 0.527 | 0.554 | 0.527 | 0.622 | 0.622 | 0.652 | 0.622 | ns |
| LVCMOS12_M_8 | 0.512 | 0.512 | 0.555 | 0.512 | 0.540 | 0.540 | 0.571 | 0.540 | 0.614 | 0.614 | 0.649 | 0.614 | ns |
| LVCMOS12_S_2 | 0.512 | 0.512 | 0.555 | 0.512 | 0.767 | 0.767 | 0.803 | 0.767 | 0.990 | 0.990 | 1.024 | 0.990 | ns |
| LVCMOS12_S_4 | 0.512 | 0.512 | 0.555 | 0.512 | 0.666 | 0.666 | 0.704 | 0.666 | 0.803 | 0.803 | 0.848 | 0.803 | ns |
| LVCMOS12_S_6 | 0.512 | 0.512 | 0.555 | 0.512 | 0.657 | 0.657 | 0.695 | 0.657 | 0.732 | 0.732 | 0.774 | 0.732 | ns |
| LVCMOS12_S_8 | 0.512 | 0.512 | 0.555 | 0.512 | 0.708 | 0.708 | 0.761 | 0.708 | 0.745 | 0.745 | 0.790 | 0.745 | ns |
| LVCMOS15_F_12 | 0.414 | 0.414 | 0.445 | 0.414 | 0.500 | 0.500 | 0.522 | 0.500 | 0.647 | 0.647 | 0.682 | 0.647 | ns |
| LVCMOS15_F_2 | 0.414 | 0.414 | 0.445 | 0.414 | 0.702 | 0.702 | 0.722 | 0.702 | 0.919 | 0.919 | 0.940 | 0.919 | ns |
| LVCMOS15_F_4 | 0.414 | 0.414 | 0.445 | 0.414 | 0.579 | 0.579 | 0.601 | 0.579 | 0.755 | 0.755 | 0.781 | 0.755 | ns |
| LVCMOS15_F_6 | 0.414 | 0.414 | 0.445 | 0.414 | 0.547 | 0.547 | 0.569 | 0.547 | 0.711 | 0.711 | 0.742 | 0.711 | ns |

*Table 26:* **Input Delay Measurement Methodology *(Cont'd)***

| Description | I/O Standard Attribute | $V_L$ (1)(2) | $V_H$ (1)(2) | $V_{MEAS}$ (1)(4)(6) | $V_{REF}$ (1)(3)(5) |
|---|---|---|---|---|---|
| DIFF_HSUL, 1.2V | DIFF_HSUL_12 | 0.6 – 0.25 | 0.6 + 0.25 | 0(6) | – |
| DIFF_SSTL, 1.2V | DIFF_SSTL12 | 0.6 – 0.25 | 0.6 + 0.25 | 0(6) | – |
| DIFF_SSTL135 and DIFF_SSTL135 class II, 1.35V | DIFF_SSTL135, DIFF_SSTL135_II | 0.675 – 0.2875 | 0.675 + 0.2875 | 0(6) | – |
| DIFF_SSTL15 and DIFF_SSTL15 class II, 1.5V | DIFF_SSTL15, DIFF_SSTL15_II | 0.75 – 0.325 | 0.75 + 0.325 | 0(6) | – |
| DIFF_SSTL18_I, DIFF_SSTL18_II, 1.8V | DIFF_SSTL18_I, DIFF_SSTL18_II | 0.9 – 0.4 | 0.9 + 0.4 | 0(6) | – |
| DIFF_POD10, 1.0V | DIFF_POD10 | 0.5 – 0.2 | 0.5 + 0.2 | 0(6) | – |
| DIFF_POD12, 1.2V | DIFF_POD12 | 0.6 – 0.25 | 0.6 + 0.25 | 0(6) | – |
| LVDS (low-voltage differential signaling), 1.8V | LVDS | 0.9 – 0.125 | 0.9 + 0.125 | 0(6) | – |
| SUB_LVDS, 1.8V | SUB_LVDS | 0.9 – 0.125 | 0.9 + 0.125 | 0(6) | – |
| SLVS, 1.8V | SLVS_400_18 | 0.9 – 0.125 | 0.9 + 0.125 | 0(6) | – |
| MIPI D-PHY (high speed) 1.2V | MIPI_DPHY_DCI_HS | 0.2 – 0.125 | 0.2 + 0.125 | 0(6) | – |
| MIPI D-PHY (low power) 1.2V | MIPI_DPHY_DCI_LP | 0.715 – 0.2 | 0.715 + 0.2 | 0(6) | – |

**Notes:**

1. The input delay measurement methodology parameters for LVDCI/HSLVDCI are the same for LVCMOS standards of the same voltage. Parameters for all other DCI standards are the same for the corresponding non-DCI standards.
2. Input waveform switches between $V_L$ and $V_H$.
3. Measurements are made at typical, minimum, and maximum $V_{REF}$ values. Reported delays reflect worst case of these measurements. $V_{REF}$ values listed are typical.
4. Input voltage level from which measurement starts.
5. This is an input voltage reference that bears no relation to the $V_{REF}$/$V_{MEAS}$ parameters found in IBIS models and/or noted in Figure 1.
6. The value given is the differential input voltage.

## Output Delay Measurement Methodology

Output delays are measured with short output traces. Standard termination was used for all testing. The propagation delay of the trace is characterized separately and subtracted from the final measurement, and is therefore not included in the generalized test setups shown in Figure 1 and Figure 2.

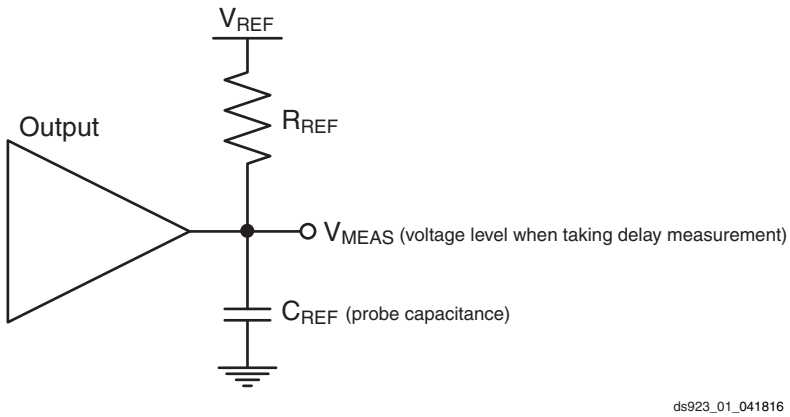


*Figure 1:* **Single-Ended Test Setup**

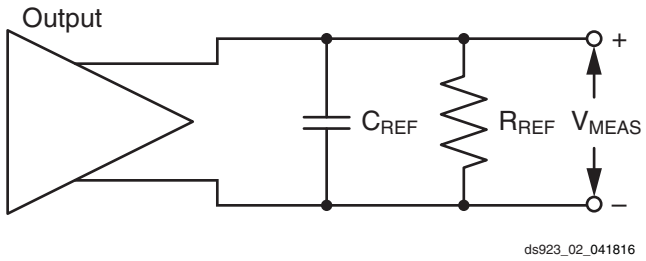


*Figure 2:* **Differential Test Setup**

Parameters $V_{REF}$, $R_{REF}$, $C_{REF}$, and $V_{MEAS}$ fully describe the test conditions for each I/O standard. The most accurate prediction of propagation delay in any given application can be obtained through IBIS simulation, using this method:

1. Simulate the output driver of choice into the generalized test setup using values from Table 27.
2. Record the time to $V_{MEAS}$.
3. Simulate the output driver of choice into the actual PCB trace and load using the appropriate IBIS model or capacitance value to represent the load.
4. Record the time to $V_{MEAS}$.
5. Compare the results of step 2 and step 4. The increase or decrease in delay yields the actual propagation delay of the PCB trace.

*Table 27:* **Output Delay Measurement Methodology**

| Description | I/O Standard Attribute | $R_{REF}$ (Ω) | $C_{REF}$[1] (pF) | $V_{MEAS}$ (V) | $V_{REF}$ (V) |
|---|---|---|---|---|---|
| LVCMOS, 1.2V | LVCMOS12 | 1M | 0 | 0.6 | 0 |
| LVCMOS, 1.5V | LVCMOS15 | 1M | 0 | 0.75 | 0 |
| LVCMOS, 1.8V | LVCMOS18 | 1M | 0 | 0.9 | 0 |
| LVDCI, HSLVDCI, 1.5V | LVDCI_15, HSLVDCI_15 | 50 | 0 | $V_{REF}$ | 0.75 |
| LVDCI, HSLVDCI, 1.8V | LVDCI_15, HSLVDCI_18 | 50 | 0 | $V_{REF}$ | 0.9 |
| HSTL (high-speed transceiver logic), class I, 1.2V | HSTL_I_12 | 50 | 0 | $V_{REF}$ | 0.6 |
| HSTL, class I, 1.5V | HSTL_I | 50 | 0 | $V_{REF}$ | 0.75 |
| HSTL, class I, 1.8V | HSTL_I_18 | 50 | 0 | $V_{REF}$ | 0.9 |
| HSUL (high-speed unterminated logic), 1.2V | HSUL_12 | 50 | 0 | $V_{REF}$ | 0.6 |
| SSTL12 (stub series terminated logic), 1.2V | SSTL12 | 50 | 0 | $V_{REF}$ | 0.6 |
| SSTL135, 1.35V | SSTL135 | 50 | 0 | $V_{REF}$ | 0.675 |
| SSTL15, 1.5V | SSTL15 | 50 | 0 | $V_{REF}$ | 0.75 |
| SSTL18, class I, 1.8V | SSTL18_I | 50 | 0 | $V_{REF}$ | 0.9 |
| POD10, 1.0V | POD10 | 50 | 0 | $V_{REF}$ | 1.0 |
| POD12, 1.2V | POD12 | 50 | 0 | $V_{REF}$ | 1.2 |
| DIFF_HSTL, class I, 1.2V | DIFF_HSTL_I_12 | 50 | 0 | $V_{REF}$ | 0.6 |
| DIFF_HSTL, class I, 1.5V | DIFF_HSTL_I | 50 | 0 | $V_{REF}$ | 0.75 |
| DIFF_HSTL, class I, 1.8V | DIFF_HSTL_I_18 | 50 | 0 | $V_{REF}$ | 0.9 |
| DIFF_HSUL, 1.2V | DIFF_HSUL_12 | 50 | 0 | $V_{REF}$ | 0.6 |
| DIFF_SSTL12, 1.2V | DIFF_SSTL12 | 50 | 0 | $V_{REF}$ | 0.6 |
| DIFF_SSTL135, 1.35V | DIFF_SSTL135 | 50 | 0 | $V_{REF}$ | 0.675 |
| DIFF_SSTL15, 1.5V | DIFF_SSTL15 | 50 | 0 | $V_{REF}$ | 0.75 |
| DIFF_SSTL18, 1.8V | DIFF_SSTL18_I | 50 | 0 | $V_{REF}$ | 0.9 |
| DIFF_POD10, 1.0V | DIFF_POD10 | 50 | 0 | $V_{REF}$ | 1.0 |
| DIFF_POD12, 1.2V | DIFF_POD12 | 50 | 0 | $V_{REF}$ | 1.2 |
| LVDS (low-voltage differential signaling), 1.8V | LVDS | 100 | 0 | 0[2] | 0 |
| SUB_LVDS, 1.8V | SUB_LVDS | 100 | 0 | 0[2] | 0 |
| MIPI D-PHY (high speed) 1.2V | MIPI_DPHY_DCI_HS | 100 | 0 | 0[2] | 0 |
| MIPI D-PHY (low power) 1.2V | MIPI_DPHY_DCI_LP | 1M | 0 | 0.6 | 0 |

**Notes:**

1. $C_{REF}$ is the capacitance of the probe, nominally 0 pF.
2. The value given is the differential output voltage.

# Block RAM and FIFO Switching Characteristics

*Table 28:* **Block RAM and FIFO Switching Characteristics**

| Symbol | Description | Speed Grade and $V_{CCINT}$ Operating Voltages | | | | Units |
|---|---|---|---|---|---|---|
| | | 0.90V | 0.85V | | 0.72V | |
| | | -3 | -2 | -1 | -2 | |
| **Maximum Frequency** | | | | | | |
| $F_{MAX\_WF\_NC}$ | Block RAM (WRITE_FIRST and NO_CHANGE modes). | 825 | 737 | 645 | 585 | MHz |
| $F_{MAX\_RF}$ | Block RAM (READ_FIRST mode). | 718 | 637 | 575 | 510 | MHz |
| $F_{MAX\_FIFO}$ | FIFO in all modes without ECC. | 825 | 737 | 645 | 585 | MHz |
| $F_{MAX\_ECC}$ | Block RAM and FIFO in ECC configuration without PIPELINE. | 718 | 637 | 575 | 510 | MHz |
| | Block RAM and FIFO in ECC configuration with PIPELINE and Block RAM in WRITE_FIRST or NO_CHANGE mode. | 825 | 737 | 645 | 585 | MHz |
| $T_{PW}$[(1)] | Minimum pulse width. | 495 | 542 | 543 | 577 | ps |
| **Block RAM and FIFO Clock-to-Out Delays** | | | | | | |
| $T_{RCKO\_DO}$ | Clock CLK to DOUT output (without output register). | 0.91 | 1.02 | 1.11 | 1.46 | ns, Max |
| $T_{RCKO\_DO\_REG}$ | Clock CLK to DOUT output (with output register). | 0.27 | 0.29 | 0.30 | 0.42 | ns, Max |

**Notes:**

1. The MMCM and PLL DUTY_CYCLE attribute should be set to 50% to meet the pulse-width requirements at the higher frequencies.

# UltraRAM Switching Characteristics

*Table 29:* **UltraRAM Switching Characteristics**

| Symbol | Description | Speed Grade and $V_{CCINT}$ Operating Voltages | | | | Units |
|---|---|---|---|---|---|---|
| | | 0.90V | 0.85V | | 0.72V | |
| | | -3 | -2 | -1 | -2 | |
| **Maximum Frequency** | | | | | | |
| $F_{MAX}$ | UltraRAM maximum frequency with OREG_B = True. | 650 | 600 | 575 | 500 | MHz |
| $F_{MAX\_ECC}$ | UltraRAM maximum frequency OREG_B = False and EN_ECC_RD_B = True. | 450 | 400 | 386 | 325 | MHz |
| $F_{MAX\_NORPIPELINE}$ | UltraRAM maximum frequency with OREG_B = False and EN_ECC_RD_B = False. | 550 | 500 | 478 | 425 | MHz |
| $T_{PW}$[(1)] | Minimum pulse width. | 650 | 700 | 730 | 800 | ps |
| $T_{RSTPW}$ | Asynchronous reset minimum pulse width. One cycle required. | 1 clock cycle | | | | ps |

**Notes:**

1. The MMCM and PLL DUTY_CYCLE attribute should be set to 50% to meet the pulse-width requirements at the higher frequencies.

# Input/Output Delay Switching Characteristics

*Table 30:* **Input/Output Delay Switching Characteristics**

| Symbol | Description | Speed Grade and $V_{CCINT}$ Operating Voltages | | | | Units |
|---|---|---|---|---|---|---|
| | | 0.90V | 0.85V | | 0.72V | |
| | | -3 | -2 | -1 | -2 | |
| $F_{REFCLK}$ | REFCLK frequency for IDELAYCTRL (component mode). | 300 to 800 | | | | MHz |
| | REFCLK frequency for BITSLICE_CONTROL (native mode).(1) | 300 to 2666.67 | 300 to 2666.67 | 300 to 2400 | 300 to 2400 | MHz |
| $T_{MINPER\_CLK}$ | Minimum period for IODELAY clock. | 3.195 | 3.195 | 3.195 | 3.195 | ns |
| $T_{MINPER\_RST}$ | Minimum reset pulse width. | 52.00 | | | | ns |
| $T_{IDELAY\_RESOLUTION}$/ $T_{ODELAY\_RESOLUTION}$ | IDELAY/ODELAY chain resolution. | 2.1 to 12 | | | | ps |

**Notes:**

1. PLL settings could restrict the minimum allowable data rate. For example, when using a PLL with CLKOUTPHY_MODE = VCO_HALF, the minimum frequency is PLL_FVCOMIN/2.

# DSP48 Slice Switching Characteristics

*Table 31:* **DSP48 Slice Switching Characteristics**

| Symbol | Description | Speed Grade and $V_{CCINT}$ Operating Voltages | | | | Units |
|---|---|---|---|---|---|---|
| | | 0.90V | 0.85V | | 0.72V | |
| | | -3 | -2 | -1 | -2 | |
| **Maximum Frequency** | | | | | | |
| $F_{MAX}$ | With all registers used. | 891 | 775 | 645 | 644 | MHz |
| $F_{MAX\_PATDET}$ | With pattern detector. | 794 | 687 | 571 | 562 | MHz |
| $F_{MAX\_MULT\_NOMREG}$ | Two register multiply without MREG. | 635 | 544 | 456 | 440 | MHz |
| $F_{MAX\_MULT\_NOMREG\_PATDET}$ | Two register multiply without MREG with pattern detect. | 577 | 492 | 410 | 395 | MHz |
| $F_{MAX\_PREADD\_NOADREG}$ | Without ADREG. | 655 | 565 | 468 | 453 | MHz |
| $F_{MAX\_NOPIPELINEREG}$ | Without pipeline registers (MREG, ADREG). | 483 | 410 | 338 | 323 | MHz |
| $F_{MAX\_NOPIPELINEREG\_PATDET}$ | Without pipeline registers (MREG, ADREG) with pattern detect. | 448 | 379 | 314 | 299 | MHz |

# MMCM Switching Characteristics

*Table 33:* **MMCM Specification**

| Symbol | Description | Speed Grade and $V_{CCINT}$ Operating Voltages | | | | Units |
|---|---|---|---|---|---|---|
| | | 0.90V | 0.85V | | 0.72V | |
| | | -3 | -2 | -1 | -2 | |
| MMCM_$F_{INMAX}$ | Maximum input clock frequency. | 1066 | 933 | 800 | 933 | MHz |
| MMCM_$F_{INMIN}$ | Minimum input clock frequency. | 10 | 10 | 10 | 10 | MHz |
| MMCM_$F_{INJITTER}$ | Maximum input clock period jitter. | < 20% of clock input period or 1 ns Max | | | | |
| MMCM_$F_{INDUTY}$ | Input duty cycle range: 10–49 MHz. | 25–75 | | | | % |
| | Input duty cycle range: 50–199 MHz. | 30–70 | | | | % |
| | Input duty cycle range: 200–399 MHz. | 35–65 | | | | % |
| | Input duty cycle range: 400–499 MHz. | 40–60 | | | | % |
| | Input duty cycle range: >500 MHz. | 45–55 | | | | % |
| MMCM_$F_{MIN_PSCLK}$ | Minimum dynamic phase shift clock frequency. | 0.01 | 0.01 | 0.01 | 0.01 | MHz |
| MMCM_$F_{MAX_PSCLK}$ | Maximum dynamic phase shift clock frequency. | 550 | 500 | 450 | 500 | MHz |
| MMCM_$F_{VCOMIN}$ | Minimum MMCM VCO frequency. | 800 | 800 | 800 | 800 | MHz |
| MMCM_$F_{VCOMAX}$ | Maximum MMCM VCO frequency. | 1600 | 1600 | 1600 | 1600 | MHz |
| MMCM_$F_{BANDWIDTH}$ | Low MMCM bandwidth at typical.(1) | 1.00 | 1.00 | 1.00 | 1.00 | MHz |
| | High MMCM bandwidth at typical.(1) | 4.00 | 4.00 | 4.00 | 4.00 | MHz |
| MMCM_$T_{STATPHAOFFSET}$ | Static phase offset of the MMCM outputs.(2) | 0.12 | 0.12 | 0.12 | 0.12 | ns |
| MMCM_$T_{OUTJITTER}$ | MMCM output jitter. | Note 3 | | | | |
| MMCM_$T_{OUTDUTY}$ | MMCM output clock duty cycle precision.(4) | 0.165 | 0.20 | 0.20 | 0.20 | ns |
| MMCM_$T_{LOCKMAX}$ | MMCM maximum lock time for MMCM_$F_{PFDMIN}$. | 100 | 100 | 100 | 100 | µs |
| MMCM_$F_{OUTMAX}$ | MMCM maximum output frequency. | 891 | 775 | 667 | 725 | MHz |
| MMCM_$F_{OUTMIN}$ | MMCM minimum output frequency.(4)(5) | 6.25 | 6.25 | 6.25 | 6.25 | MHz |
| MMCM_$T_{EXTFDVAR}$ | External clock feedback variation. | < 20% of clock input period or 1 ns Max | | | | |
| MMCM_$RST_{MINPULSE}$ | Minimum reset pulse width. | 5.00 | 5.00 | 5.00 | 5.00 | ns |
| MMCM_$F_{PFDMAX}$ | Maximum frequency at the phase frequency detector. | 550 | 500 | 450 | 500 | MHz |
| MMCM_$F_{PFDMIN}$ | Minimum frequency at the phase frequency detector. | 10 | 10 | 10 | 10 | MHz |
| MMCM_$T_{FBDELAY}$ | Maximum delay in the feedback path. | 5 ns Max or one clock cycle | | | | |
| MMCM_$F_{DPRCLK_MAX}$ | Maximum DRP clock frequency | 250 | 250 | 250 | 250 | MHz |

**Notes:**

1. The MMCM does not filter typical spread-spectrum input clocks because they are usually far below the bandwidth filter frequencies.
2. The static offset is measured between any MMCM outputs with identical phase.
3. Values for this parameter are available in the Clocking Wizard.
4. Includes global clock buffer.
5. Calculated as $F_{VCO}$/128 assuming output duty cycle is 50%.

# Device Pin-to-Pin Input Parameter Guidelines

The pin-to-pin numbers in Table 38 are based on the clock root placement in the center of the device. The actual pin-to-pin values will vary if the root placement selected is different. Consult the Vivado Design Suite timing report for the actual pin-to-pin values.

*Table 38:* **Global Clock Input Setup and Hold With MMCM**

| Symbol | Description | | Device | Speed Grade and $V_{CCINT}$ Operating Voltages | | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | | | 0.90V | 0.85V | | 0.72V | |
| | | | | -3 | -2 | -1 | -2 | |
| **Input Setup and Hold Time Relative to Global Clock Input Signal using SSTL15 Standard.(1)(2)(3)** | | | | | | | | |
| $T_{PSMMCMCC\_VU3P}$ | Global clock input and input flip-flop (or latch) with MMCM. | Setup | XCVU3P | 1.86 | 1.86 | 1.99 | 2.32 | ns |
| $T_{PHMMCMCC\_VU3P}$ | | Hold | | –0.13 | –0.13 | –0.13 | 0.14 | ns |
| $T_{PSMMCMCC\_VU5P}$ | | Setup | XCVU5P | 1.86 | 1.86 | 1.99 | 2.32 | ns |
| $T_{PHMMCMCC\_VU5P}$ | | Hold | | –0.13 | –0.13 | –0.13 | 0.14 | ns |
| $T_{PSMMCMCC\_VU7P}$ | | Setup | XCVU7P | 1.86 | 1.86 | 1.99 | 2.32 | ns |
| $T_{PHMMCMCC\_VU7P}$ | | Hold | | –0.13 | –0.13 | –0.13 | 0.14 | ns |
| $T_{PSMMCMCC\_VU9P}$ | | Setup | XCVU9P | 1.86 | 1.86 | 1.99 | 2.32 | ns |
| $T_{PHMMCMCC\_VU9P}$ | | Hold | | –0.13 | –0.13 | –0.13 | 0.14 | ns |
| $T_{PSMMCMCC\_VU11P}$ | | Setup | XCVU11P | 1.92 | 1.92 | 2.05 | 2.36 | ns |
| $T_{PHMMCMCC\_VU11P}$ | | Hold | | –0.13 | –0.13 | –0.13 | 0.16 | ns |
| $T_{PSMMCMCC\_VU13P}$ | | Setup | XCVU13P | 1.92 | 1.92 | 2.05 | 2.36 | ns |
| $T_{PHMMCMCC\_VU13P}$ | | Hold | | –0.13 | –0.13 | –0.13 | 0.16 | ns |

**Notes:**

1. Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, slowest temperature, and slowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, fastest temperature, and fastest voltage.
2. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible I/O and CLB flip-flops are clocked by the global clock net in a single SLR.
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

*Table 39:* **Sampling Window**

| Description | Speed Grade and $V_{CCINT}$ Operating Voltages | | | | Units |
|---|---|---|---|---|---|
| | 0.90V | 0.85V | | 0.72V | |
| | -3 | -2 | -1 | -2 | |
| $T_{SAMP\_BUFG}$(1) | 510 | 610 | 610 | 610 | ps |
| $T_{SAMP\_NATIVE\_DPA}$ | 100 | 100 | 125 | 125 | ps |
| $T_{SAMP\_NATIVE\_BISC}$ | 60 | 60 | 85 | 85 | ps |

**Notes:**

1. This parameter indicates the total sampling error of the Virtex UltraScale+ FPGA DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the MMCM to capture the DDR input registers' edges of operation. These measurements include: CLK0 MMCM jitter, MMCM accuracy (phase offset), and MMCM phase shift resolution. These measurements do not include package or clock tree skew.

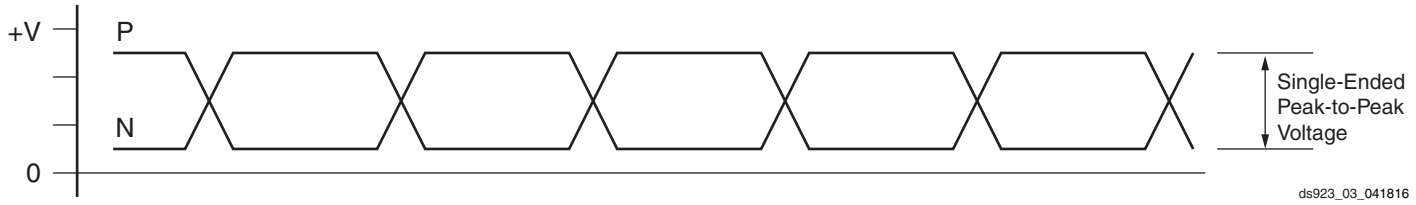


*Figure 3:* **Single-Ended Peak-to-Peak Voltage**

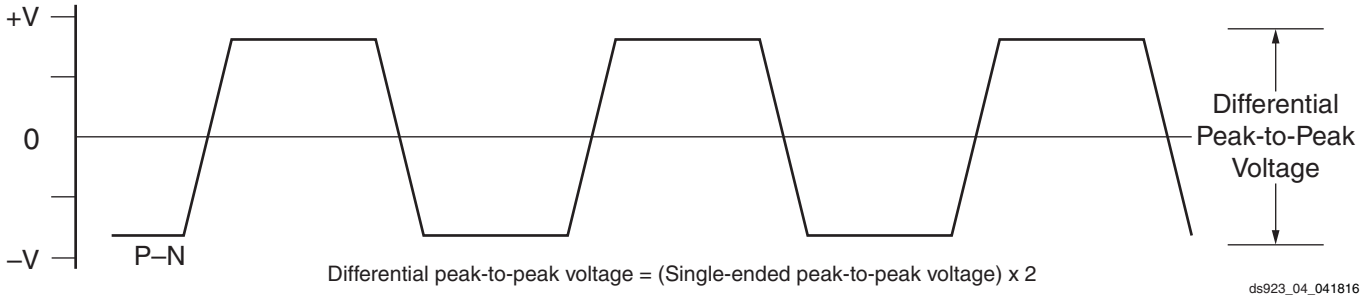


*Figure 4:* **Differential Peak-to-Peak Voltage**

Table 42 and Table 43 summarize the DC specifications of the clock input of the GTY transceivers in Virtex UltraScale+ FPGAs. Consult www.xilinx.com/products/technology/high-speed-serial for further details.

*Table 42:* **GTY Transceiver Clock DC Input Level Specification**

| Symbol | DC Parameter | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| $V_{IDIFF}$ | Differential peak-to-peak input voltage | 250 | – | 2000 | mV |
| $R_{IN}$ | Differential input resistance | – | 100 | – | Ω |
| $C_{EXT}$ | Required external AC coupling capacitor | – | 10 | – | nF |

*Table 43:* **GTY Transceiver Clock Output Level Specification**

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{OL}$ | Output high voltage for P and N | $R_T$ = 100Ω across P and N signals | 100 | – | 330 | mV |
| $V_{OH}$ | Output low voltage for P and N | $R_T$ = 100Ω across P and N signals | 500 | – | 700 | mV |
| $V_{DDOUT}$ | Differential output voltage<br>(P–N), P = High<br>(N–P), N = High | $R_T$ = 100Ω across P and N signals | 300 | – | 430 | mV |
| $V_{CMOUT}$ | Common mode voltage | $R_T$ = 100Ω across P and N signals | 300 | – | 500 | mV |

*Table 48:* **GTY Transceiver PLL/Lock Time Adaptation**

| Symbol | Description | Conditions | All Speed Grades | | | Units |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $T_{LOCK}$ | Initial PLL lock. | | – | – | 1 | ms |
| $T_{DLOCK}$ | Clock recovery phase acquisition and adaptation time for decision feedback equalizer (DFE). | After the PLL is locked to the reference clock, this is the time it takes to lock the clock data recovery (CDR) to the data present at the input. | – | 50,000 | $37 \times 10^6$ | UI |
| | Clock recovery phase acquisition and adaptation time for low-power mode (LPM) when the DFE is disabled. | | – | 50,000 | $2.3 \times 10^6$ | UI |

*Table 49:* **GTY Transceiver User Clock Switching Characteristics(1)**

| Symbol | Description | Data Width Conditions (Bit) | | Speed Grade and $V_{CCINT}$ Operating Voltages | | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | | | 0.90V | 0.85V | | 0.72V | |
| | | Internal Logic | Interconnect Logic | -3 | -2 | -1 | -2 | |
| $F_{TXOUTPMA}$ | TXOUTCLK maximum frequency sourced from OUTCLKPMA | | | 511.719 | 511.719 | 402.833 | 402.833 | MHz |
| $F_{RXOUTPMA}$ | RXOUTCLK maximum frequency sourced from OUTCLKPMA | | | 511.719 | 511.719 | 402.833 | 402.833 | MHz |
| $F_{TXOUTPROGDIV}$ | TXOUTCLK maximum frequency sourced from TXPROGDIVCLK | | | 511.719 | 511.719 | 511.719 | 511.719 | MHz |
| $F_{RXOUTPROGDIV}$ | RXOUTCLK maximum frequency sourced from RXPROGDIVCLK | | | 511.719 | 511.719 | 511.719 | 511.719 | MHz |
| $F_{TXIN}$ | TXUSRCLK(2) maximum frequency | 16 | 16, 32 | 511.719 | 511.719 | 390.625 | 390.625 | MHz |
| | | 32 | 32, 64 | 511.719 | 511.719 | 390.625 | 390.625 | MHz |
| | | 64 | 64, 128 | 511.719 | 440.781 | 402.832 | 402.832 | MHz |
| | | 20 | 20, 40 | 409.375 | 409.375 | 312.500 | 312.500 | MHz |
| | | 40 | 40, 80 | 409.375 | 409.375 | 312.500 | 350.000 | MHz |
| | | 80 | 80, 160 | 409.375 | 352.625 | 322.266 | 352.625 | MHz |
| $F_{RXIN}$ | RXUSRCLK(2) maximum frequency | 16 | 16, 32 | 511.719 | 511.719 | 390.625 | 390.625 | MHz |
| | | 32 | 32, 64 | 511.719 | 511.719 | 390.625 | 390.625 | MHz |
| | | 64 | 64, 128 | 511.719 | 440.781 | 402.832 | 402.832 | MHz |
| | | 20 | 20, 40 | 409.375 | 409.375 | 312.500 | 312.500 | MHz |
| | | 40 | 40, 80 | 409.375 | 409.375 | 312.500 | 350.000 | MHz |
| | | 80 | 80, 160 | 409.375 | 352.625 | 322.266 | 352.625 | MHz |

*Table 51:* **GTY Transceiver Receiver Switching Characteristics**

| Symbol | Description | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $F_{GTYRX}$ | Serial data rate | | 0.500 | – | $F_{GTYMAX}$ | Gb/s |
| $R_{XSST}$ | Receiver spread-spectrum tracking(1) | Modulated at 33 kHz | –5000 | – | 0 | ppm |
| $R_{XRL}$ | Run length (CID) | | – | – | 256 | UI |
| $R_{XPPMTOL}$ | Data/REFCLK PPM offset tolerance | Bit rates ≤ 6.6 Gb/s | –1250 | – | 1250 | ppm |
| | | Bit rates > 6.6 Gb/s and ≤ 8.0 Gb/s | –700 | – | 700 | ppm |
| | | Bit rates > 8.0 Gb/s | –200 | – | 200 | ppm |
| **SJ Jitter Tolerance(2)** | | | | | | |
| $J_{T\_SJ32.75}$ | Sinusoidal jitter (QPLL)(3) | 32.75 Gb/s | 0.25 | – | – | UI |
| $J_{T\_SJ28.21}$ | Sinusoidal jitter (QPLL)(3) | 28.21 Gb/s | 0.30 | – | – | UI |
| $J_{T\_SJ16.375}$ | Sinusoidal jitter (QPLL)(3) | 16.375 Gb/s | 0.30 | – | – | UI |
| $J_{T\_SJ15.0}$ | Sinusoidal jitter (QPLL)(3) | 15.0 Gb/s | 0.30 | – | – | UI |
| $J_{T\_SJ14.1}$ | Sinusoidal jitter (QPLL)(3) | 14.1 Gb/s | 0.30 | – | – | UI |
| $J_{T\_SJ13.1}$ | Sinusoidal jitter (QPLL)(3) | 13.1 Gb/s | 0.30 | – | – | UI |
| $J_{T\_SJ12.5}$ | Sinusoidal jitter (QPLL)(3) | 12.5 Gb/s | 0.30 | – | – | UI |
| $J_{T\_SJ11.3}$ | Sinusoidal jitter (QPLL)(3) | 11.3 Gb/s | 0.30 | – | – | UI |
| $J_{T\_SJ10.32\_QPLL}$ | Sinusoidal jitter (QPLL)(3) | 10.32 Gb/s | 0.30 | – | – | UI |
| $J_{T\_SJ10.32\_CPLL}$ | Sinusoidal jitter (CPLL)(3) | 10.32 Gb/s | 0.30 | – | – | UI |
| $J_{T\_SJ9.953\_QPLL}$ | Sinusoidal jitter (QPLL)(3) | 9.953 Gb/s | 0.30 | – | – | UI |
| $J_{T\_SJ9.953\_CPLL}$ | Sinusoidal jitter (CPLL)(3) | 9.953 Gb/s | 0.30 | – | – | UI |
| $J_{T\_SJ8.0}$ | Sinusoidal jitter (CPLL)(3) | 8.0 Gb/s | 0.42 | – | – | UI |
| $J_{T\_SJ6.6}$ | Sinusoidal jitter (CPLL)(3) | 6.6 Gb/s | 0.44 | – | – | UI |
| $J_{T\_SJ5.0}$ | Sinusoidal jitter (CPLL)(3) | 5.0 Gb/s | 0.44 | – | – | UI |
| $J_{T\_SJ4.25}$ | Sinusoidal jitter (CPLL)(3) | 4.25 Gb/s | 0.44 | – | – | UI |
| $J_{T\_SJ3.2}$ | Sinusoidal jitter (CPLL)(3) | 3.2 Gb/s(4) | 0.45 | – | – | UI |
| $J_{T\_SJ2.5}$ | Sinusoidal jitter (CPLL)(3) | 2.5 Gb/s(5) | 0.30 | – | – | UI |
| $J_{T\_SJ1.25}$ | Sinusoidal jitter (CPLL)(3) | 1.25 Gb/s(6) | 0.30 | – | – | UI |
| $J_{T\_SJ500}$ | Sinusoidal jitter (CPLL)(3) | 500 Mb/s(7) | 0.30 | – | – | UI |
| **SJ Jitter Tolerance with Stressed Eye(2)** | | | | | | |
| $J_{T\_TJSE3.2}$ | Total jitter with stressed eye(8) | 3.2 Gb/s | 0.70 | – | – | UI |
| $J_{T\_TJSE6.6}$ | | 6.6 Gb/s | 0.70 | – | – | UI |
| $J_{T\_SJSE3.2}$ | Sinusoidal jitter with stressed eye(8) | 3.2 Gb/s | 0.10 | – | – | UI |
| $J_{T\_SJSE6.6}$ | | 6.6 Gb/s | 0.10 | – | – | UI |

**Notes:**

1. Using RXOUT_DIV = 1, 2, and 4.
2. All jitter values are based on a bit error ratio of $10^{-12}$.
3. The frequency of the injected sinusoidal jitter is 80 MHz.
4. CPLL frequency at 3.2 GHz and RXOUT_DIV = 2.
5. CPLL frequency at 2.5 GHz and RXOUT_DIV = 2.
6. CPLL frequency at 2.5 GHz and RXOUT_DIV = 4.
7. CPLL frequency at 2.0 GHz and RXOUT_DIV = 8.
8. Composite jitter with RX equalizer enabled. DFE disabled.

# Integrated Interface Block for 100G Ethernet MAC and PCS

More information and documentation on solutions using the integrated 100 Gb/s Ethernet block can be found at UltraScale Integrated 100G Ethernet MAC/PCS. The *UltraScale Architecture and Product Overview* (DS890) lists how many blocks are in each Virtex UltraScale+ FPGA.

*Table 56:* **Maximum Performance for 100G Ethernet Designs**

| Symbol | Description | Speed Grade and $V_{CCINT}$ Operating Voltages | | | | Units |
|---|---|---|---|---|---|---|
| | | 0.90V | 0.85V | | 0.72V | |
| | | -3 | -2(1) | -1 | -2 | |
| $F_{TX\_CLK}$ | Transmit clock | 390.625 | 390.625 | 322.223 | 322.223 | MHz |
| $F_{RX\_CLK}$ | Receive clock | 390.625 | 390.625 | 322.223 | 322.223 | MHz |
| $F_{RX\_SERDES\_CLK}$ | Receive serializer/deserializer clock | 390.625 | 390.625 | 322.223 | 322.223 | MHz |
| $F_{DRP\_CLK}$ | Dynamic reconfiguration port clock | 250.00 | 250.00 | 250.00 | 250.00 | MHz |

**Notes:**

1. The maximum clock frequency of 390.625 MHz only applies to the CAUI-10 interface. The maximum clock frequency for the CAUI-4 interface is 322.223 MHz.

# Integrated Interface Block for PCI Express Designs

More information and documentation on solutions for PCI Express designs can be found at PCI Express. The *UltraScale Architecture and Product Overview* (DS890) lists how many blocks are in each Virtex UltraScale+ FPGA.

*Table 57:* **Maximum Performance for PCI Express Designs(1)(2)**

| Symbol | Description | Speed Grade and $V_{CCINT}$ Operating Voltages | | | | Units |
|---|---|---|---|---|---|---|
| | | 0.90V | 0.85V | | 0.72V | |
| | | -3 | -2 | -1 | -2 | |
| $F_{PIPECLK}$ | Pipe clock maximum frequency. | 250.00 | 250.00 | 250.00 | 250.00 | MHz |
| $F_{CORECLK}$ | Core clock maximum frequency. | 500.00 | 500.00 | 500.00 | 250.00 | MHz |
| $F_{DRPCLK}$ | DRP clock maximum frequency. | 250.00 | 250.00 | 250.00 | 250.00 | MHz |
| $F_{MCAPCLK}$ | MCAP clock maximum frequency. | 125.00 | 125.00 | 125.00 | 125.00 | MHz |

**Notes:**

1. PCI Express Gen4 operation is supported for x1, x2, x4, and x8 widths.
2. PCI Express Gen4 operation is supported in -3E, -2E, and -2I speed grades.

# System Monitor Specifications

*Table 58:* **System Monitor Specifications**

| Parameter | Symbol | Comments/Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{CCADC}$ = 1.8V ±3%, $V_{REFP}$ = 1.25V, $V_{REFN}$ = 0V, ADCCLK = 5.2 MHz, $T_j$ = –40°C to 100°C, typical values at $T_j$ = 40°C | | | | | | |
| **ADC Accuracy**(1) | | | | | | |
| Resolution | | | 10 | – | – | Bits |
| Integral nonlinearity(2) | INL | | – | – | ±1.5 | LSBs |
| Differential nonlinearity | DNL | No missing codes, guaranteed monotonic | – | – | ±1 | LSBs |
| Offset error | | Offset calibration enabled | – | – | ±2 | LSBs |
| Gain error | | | – | – | ±0.4 | % |
| Sample rate | | | – | – | 0.2 | MS/s |
| RMS code noise | | External 1.25V reference | – | – | 1 | LSBs |
| | | On-chip reference | – | 1 | – | LSBs |
| **ADC Accuracy at Extended Temperatures** | | | | | | |
| Resolution | | $T_j$ = –55°C to 125°C | 10 | – | – | Bits |
| Integral nonlinearity | INL | $T_j$ = –55°C to 125°C | – | – | ±1.5 | LSBs |
| Differential nonlinearity | DNL | No missing codes, guaranteed monotonic $T_j$ = –55°C to 125°C | – | – | ±1 | |
| **Analog Inputs**(2) | | | | | | |
| ADC input ranges | | Unipolar operation | 0 | – | 1 | V |
| | | Bipolar operation | –0.5 | – | +0.5 | V |
| | | Unipolar common mode range (FS input) | 0 | – | +0.5 | V |
| | | Bipolar common mode range (FS input) | +0.5 | – | +0.6 | V |
| Maximum external channel input ranges | | Adjacent channels set within these ranges should not corrupt measurements on adjacent channels | –0.1 | – | $V_{CCADC}$ | V |
| **On-Chip Sensor Accuracy** | | | | | | |
| Temperature sensor error(1)(3) | | $T_j$ = –55°C to 125°C (with external REF) | – | – | ±3 | °C |
| | | $T_j$ = –55°C to 110°C (with internal REF) | – | – | ±3.5 | °C |
| | | $T_j$ = 110°C to 125°C (with internal REF) | – | – | ±5 | °C |