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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Active
Number of LABs/CLBs	216000
Number of Logic Elements/Cells	3780000
Total RAM Bits	514867200
Number of I/O	702
Number of Gates	-
Voltage - Supply	0.873V ~ 0.927V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 100°C (TJ)
Package / Case	2104-BBGA, FCBGA
Supplier Device Package	2104-FCBGA (52.5x52.5)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xcvu13p-3fhgb2104e

Recommended Operating Conditions

Table 2: **Recommended Operating Conditions[1][2]**

Symbol	Description	Min	Typ	Max	Units
FPGA Logic					
V_{CCINT}	Internal supply voltage.	0.825	0.850	0.876	V
	For -2LE (V_{CCINT} = 0.72V) devices: internal supply voltage.	0.698	0.720	0.742	V
	For -3E devices: internal supply voltage.	0.873	0.900	0.927	V
V_{CCINT_IO}[3]	Internal supply voltage for the I/O banks.	0.825	0.850	0.876	V
	For -2LE devices (V_{CCINT} = 0.85V): internal supply voltage for the I/O banks.	0.825	0.850	0.876	V
	For -3E devices: internal supply voltage for the I/O banks.	0.873	0.900	0.927	V
V_{CCBRAM}	Block RAM supply voltage.	0.825	0.850	0.876	V
	For -3E devices: block RAM supply voltage.	0.873	0.900	0.927	V
V_{CCAUX}	Auxiliary supply voltage.	1.746	1.800	1.854	V
V_{CCO}[4][5]	Supply voltage for I/O banks.	0.950	–	1.900	V
V_{CCAUX_IO}[6]	Auxiliary I/O supply voltage.	1.746	1.800	1.854	V
V_{IN}[7]	I/O input voltage.	–0.200	–	V_{CCO} + 0.200	V
I_{IN}[8]	Maximum current through any pin in a powered or unpowered bank when forward biasing the clamp diode.	–	–	10	mA
V_{BATT}[9]	Battery voltage.	1.000	–	1.890	V
GTY Transceiver					
$V_{MGTAVCC}$[10]	Analog supply voltage for the GTY transceiver.	0.873	0.900	0.927	V
$V_{MGTAVTT}$[10]	Analog supply voltage for the GTY transmitter and receiver termination circuits.	1.164	1.20	1.236	V
$V_{MGTVCCAUX}$[10]	Auxiliary analog QPLL voltage supply for the transceivers.	1.746	1.80	1.854	V
$V_{MGTAVTTRCAL}$[10]	Analog supply voltage for the resistor calibration circuit of the GTY transceiver column.	1.164	1.20	1.236	V

DC Input and Output Levels

Values for V_{IL} and V_{IH} are recommended input voltages. Values for I_{OL} and I_{OH} are guaranteed over the recommended operating conditions at the V_{OL} and V_{OH} test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at a minimum V_{CCO} with the respective V_{OL} and V_{OH} voltage levels shown. Other standards are sample tested.

Table 8: **SelectIO DC Input and Output Levels for the I/O Banks**[(1)(2)(3)]

I/O Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
HSTL_I	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	5.8	–5.8
HSTL_I_12	–0.300	V_{REF} – 0.080	V_{REF} + 0.080	V_{CCO} + 0.300	25% V_{CCO}	75% V_{CCO}	4.1	–4.1
HSTL_I_18	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	6.2	–6.2
HSUL_12	–0.300	V_{REF} – 0.130	V_{REF} + 0.130	V_{CCO} + 0.300	20% V_{CCO}	80% V_{CCO}	0.1	–0.1
LVCMOS12	–0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	Note 4	Note 4
LVCMOS15	–0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	0.450	V_{CCO} – 0.450	Note 5	Note 5
LVCMOS18	–0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	0.450	V_{CCO} – 0.450	Note 5	Note 5
LVDCI_15	–0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	0.450	V_{CCO} – 0.450	7.0	–7.0
LVDCI_18	–0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	0.450	V_{CCO} – 0.450	7.0	–7.0
SSTL12	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	V_{CCO}/2 – 0.150	V_{CCO}/2 + 0.150	8.0	–8.0
SSTL135	–0.300	V_{REF} – 0.090	V_{REF} + 0.090	V_{CCO} + 0.300	V_{CCO}/2 – 0.150	V_{CCO}/2 + 0.150	9.0	–9.0
SSTL15	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	V_{CCO}/2 – 0.175	V_{CCO}/2 + 0.175	10.0	–10.0
SSTL18_I	–0.300	V_{REF} – 0.125	V_{REF} + 0.125	V_{CCO} + 0.300	V_{CCO}/2 – 0.470	V_{CCO}/2 + 0.470	7.0	–7.0
MIPI_DPHY_DCI_LP[(6)]	–0.300	0.550	0.880	V_{CCO} + 0.300	0.050	1.100	0.01	–0.01

Notes:
1. Tested according to relevant specifications.
2. Standards specified using the default I/O standard configuration. For details, see the *UltraScale Architecture SelectIO Resources User Guide* (UG571).
3. POD10 and POD12 DC input and output levels are shown in Table 9, Table 13, and Table 14.
4. Supported drive strengths of 2, 4, 6, or 8 mA in the I/O banks.
5. Supported drive strengths of 2, 4, 6, 8, or 12 mA in the I/O banks.
6. Low-power option for MIPI_DPHY_DCI.

Table 9: **DC Input Levels for Single-ended POD10 and POD12 I/O Standards**[(1)(2)]

I/O Standard	V_{IL}		V_{IH}	
	V, Min	V, Max	V, Min	V, Max
POD10	–0.300	V_{REF} – 0.068	V_{REF} + 0.068	V_{CCO} + 0.300
POD12	–0.300	V_{REF} – 0.068	V_{REF} + 0.068	V_{CCO} + 0.300

Notes:
1. Tested according to relevant specifications.
2. Standards specified using the default I/O standard configuration. For details, see the *UltraScale Architecture SelectIO Resources User Guide* (UG571).

Speed Grade Designations

Since individual family members are produced at different times, the migration from one category to another depends completely on the status of the fabrication process for each device. Table 16 correlates the current status of the Virtex UltraScale+ FPGA on a per speed grade basis.

Table 17: **Speed Grade Designations by Device**

Device	Speed Grade, Temperature Ranges, and V_{CCINT} Operating Voltages		
	Advance	Preliminary	Production
XCVU3P	-3E (V_{CCINT} = 0.90V) -2LE (V_{CCINT} = 0.85V) -2LE (V_{CCINT} = 0.72V)(1)		-2I (V_{CCINT} = 0.85V) -1E (V_{CCINT} = 0.85V) -1I (V_{CCINT} = 0.85V)
XCVU5P	-3E (V_{CCINT} = 0.90V) -2I (V_{CCINT} = 0.85V), -2LE (V_{CCINT} = 0.85V) -1E (V_{CCINT} = 0.85V), -1I (V_{CCINT} = 0.85V) -2LE (V_{CCINT} = 0.72V)(1)		
XCVU7P	-3E (V_{CCINT} = 0.90V) -2I (V_{CCINT} = 0.85V), -2LE (V_{CCINT} = 0.85V) -1E (V_{CCINT} = 0.85V), -1I (V_{CCINT} = 0.85V) -2LE (V_{CCINT} = 0.72V)(1)		
XCVU9P	-3E (V_{CCINT} = 0.90V) -2I (V_{CCINT} = 0.85V), -2LE (V_{CCINT} = 0.85V) -1E (V_{CCINT} = 0.85V), -1I (V_{CCINT} = 0.85V) -2LE (V_{CCINT} = 0.72V)(1)		
XCVU11P	-3E (V_{CCINT} = 0.90V) -2I (V_{CCINT} = 0.85V), -2LE (V_{CCINT} = 0.85V) -1E (V_{CCINT} = 0.85V), -1I (V_{CCINT} = 0.85V), -2LE (V_{CCINT} = 0.72V)(1)		
XCVU13P	-3E (V_{CCINT} = 0.90V) -2I (V_{CCINT} = 0.85V), -2LE (V_{CCINT} = 0.85V) -1E (V_{CCINT} = 0.85V), -1I (V_{CCINT} = 0.85V) -2LE (V_{CCINT} = 0.72V)(1)		

Notes:

1. The lowest power -2L devices, where V_{CCINT} = 0.72V, are listed in the Vivado Design Suite as -2LV.

Table 24: **IOB High Performance (HP) Switching Characteristics *(Cont'd)***

I/O Standards	$T_{INBUF\_DELAY\_PAD\_I}$				$T_{OUTBUF\_DELAY\_O\_PAD}$				$T_{OUTBUF\_DELAY\_TD\_PAD}$				Units
	0.90V	0.85V		0.72V	0.90V	0.85V		0.72V	0.90V	0.85V		0.72V	
	-3	-2	-1	-2	-3	-2	-1	-2	-3	-2	-1	-2	
LVCMOS15_F_8	0.414	0.414	0.445	0.414	0.518	0.518	0.538	0.518	0.686	0.686	0.703	0.686	ns
LVCMOS15_M_12	0.414	0.414	0.445	0.414	0.607	0.607	0.644	0.607	0.637	0.637	0.676	0.637	ns
LVCMOS15_M_2	0.414	0.414	0.445	0.414	0.741	0.741	0.770	0.741	0.938	0.938	0.962	0.938	ns
LVCMOS15_M_4	0.414	0.414	0.445	0.414	0.625	0.625	0.651	0.625	0.754	0.754	0.786	0.754	ns
LVCMOS15_M_6	0.414	0.414	0.445	0.414	0.576	0.576	0.604	0.576	0.674	0.674	0.710	0.674	ns
LVCMOS15_M_8	0.414	0.414	0.445	0.414	0.568	0.568	0.601	0.568	0.639	0.639	0.681	0.639	ns
LVCMOS15_S_12	0.414	0.414	0.445	0.414	0.788	0.788	0.855	0.788	0.695	0.695	0.733	0.695	ns
LVCMOS15_S_2	0.414	0.414	0.445	0.414	0.829	0.829	0.864	0.829	1.039	1.039	1.079	1.039	ns
LVCMOS15_S_4	0.414	0.414	0.445	0.414	0.687	0.687	0.725	0.687	0.813	0.813	0.851	0.813	ns
LVCMOS15_S_6	0.414	0.414	0.445	0.414	0.671	0.671	0.710	0.671	0.726	0.726	0.763	0.726	ns
LVCMOS15_S_8	0.414	0.414	0.445	0.414	0.704	0.704	0.755	0.704	0.721	0.721	0.758	0.721	ns
LVCMOS18_F_12	0.418	0.418	0.445	0.418	0.573	0.573	0.601	0.573	0.731	0.731	0.769	0.731	ns
LVCMOS18_F_2	0.418	0.418	0.445	0.418	0.739	0.739	0.760	0.739	0.945	0.945	0.971	0.945	ns
LVCMOS18_F_4	0.418	0.418	0.445	0.418	0.609	0.609	0.630	0.609	0.778	0.778	0.802	0.778	ns
LVCMOS18_F_6	0.418	0.418	0.445	0.418	0.603	0.603	0.633	0.603	0.781	0.781	0.808	0.781	ns
LVCMOS18_F_8	0.418	0.418	0.445	0.418	0.573	0.573	0.600	0.573	0.733	0.733	0.767	0.733	ns
LVCMOS18_M_12	0.418	0.418	0.445	0.418	0.640	0.640	0.678	0.640	0.670	0.670	0.709	0.670	ns
LVCMOS18_M_2	0.418	0.418	0.445	0.418	0.798	0.798	0.822	0.798	0.991	0.991	1.016	0.991	ns
LVCMOS18_M_4	0.418	0.418	0.445	0.418	0.664	0.664	0.693	0.664	0.798	0.798	0.836	0.798	ns
LVCMOS18_M_6	0.418	0.418	0.445	0.418	0.629	0.629	0.663	0.629	0.735	0.735	0.775	0.735	ns
LVCMOS18_M_8	0.418	0.418	0.445	0.418	0.626	0.626	0.661	0.626	0.705	0.705	0.746	0.705	ns
LVCMOS18_S_12	0.418	0.418	0.445	0.418	0.795	0.795	0.861	0.795	0.683	0.683	0.721	0.683	ns
LVCMOS18_S_2	0.418	0.418	0.445	0.418	0.862	0.862	0.897	0.862	1.076	1.076	1.098	1.076	ns
LVCMOS18_S_4	0.418	0.418	0.445	0.418	0.716	0.716	0.758	0.716	0.829	0.829	0.872	0.829	ns
LVCMOS18_S_6	0.418	0.418	0.445	0.418	0.682	0.682	0.724	0.682	0.724	0.724	0.762	0.724	ns
LVCMOS18_S_8	0.418	0.418	0.445	0.418	0.707	0.707	0.760	0.707	0.709	0.709	0.745	0.709	ns
LVDCI_15_F	0.425	0.425	0.462	0.425	0.426	0.426	0.443	0.426	0.548	0.548	0.581	0.548	ns
LVDCI_15_M	0.425	0.425	0.462	0.425	0.553	0.553	0.582	0.553	0.645	0.645	0.685	0.645	ns
LVDCI_15_S	0.425	0.425	0.462	0.425	0.749	0.749	0.803	0.749	0.821	0.821	0.890	0.821	ns
LVDCI_18_F	0.414	0.414	0.447	0.414	0.441	0.441	0.459	0.441	0.560	0.560	0.589	0.560	ns
LVDCI_18_M	0.414	0.414	0.447	0.414	0.554	0.554	0.585	0.554	0.644	0.644	0.683	0.644	ns
LVDCI_18_S	0.414	0.414	0.447	0.414	0.760	0.760	0.818	0.760	0.837	0.837	0.899	0.837	ns
LVDS	0.539	0.539	0.620	0.539	0.626	0.626	0.662	0.626	960.447	960.447	960.447	960.447	ns
MIPI_DPHY_DCI_HS	0.386	0.386	0.415	0.386	0.502	0.502	0.522	0.502	N/A	N/A	N/A	N/A	ns
MIPI_DPHY_DCI_LP	8.438	8.438	8.792	8.438	0.914	0.914	0.937	0.914	N/A	N/A	N/A	N/A	ns
POD10_DCI_F	0.408	0.408	0.430	0.408	0.425	0.425	0.444	0.425	0.555	0.555	0.584	0.555	ns
POD10_DCI_M	0.408	0.408	0.430	0.408	0.542	0.542	0.571	0.542	0.640	0.640	0.681	0.640	ns
POD10_DCI_S	0.408	0.408	0.430	0.408	0.754	0.754	0.815	0.754	0.850	0.850	0.917	0.850	ns
POD10_F	0.407	0.407	0.430	0.407	0.438	0.438	0.459	0.438	0.569	0.569	0.601	0.569	ns
POD10_M	0.407	0.407	0.430	0.407	0.538	0.538	0.568	0.538	0.630	0.630	0.667	0.630	ns
POD10_S	0.407	0.407	0.430	0.407	0.766	0.766	0.821	0.766	0.836	0.836	0.894	0.836	ns

Table 24: **IOB High Performance (HP) Switching Characteristics *(Cont'd)***

I/O Standards	$T_{INBUF\_DELAY\_PAD\_I}$				$T_{OUTBUF\_DELAY\_O\_PAD}$				$T_{OUTBUF\_DELAY\_TD\_PAD}$				Units
	0.90V	0.85V		0.72V	0.90V	0.85V		0.72V	0.90V	0.85V		0.72V	
	-3	-2	-1	-2	-3	-2	-1	-2	-3	-2	-1	-2	
POD12_DCI_F	0.409	0.409	0.431	0.409	0.425	0.425	0.443	0.425	0.558	0.558	0.586	0.558	ns
POD12_DCI_M	0.409	0.409	0.431	0.409	0.543	0.543	0.572	0.543	0.638	0.638	0.678	0.638	ns
POD12_DCI_S	0.409	0.409	0.431	0.409	0.772	0.772	0.822	0.772	0.862	0.862	0.929	0.862	ns
POD12_F	0.409	0.409	0.431	0.409	0.455	0.455	0.476	0.455	0.595	0.595	0.626	0.595	ns
POD12_M	0.409	0.409	0.431	0.409	0.551	0.551	0.582	0.551	0.641	0.641	0.679	0.641	ns
POD12_S	0.409	0.409	0.431	0.409	0.767	0.767	0.817	0.767	0.832	0.832	0.889	0.832	ns
SLVS_400_18	0.539	0.539	0.620	0.539	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	ns
SSTL12_DCI_F	0.381	0.381	0.399	0.381	0.425	0.425	0.443	0.425	0.558	0.558	0.586	0.558	ns
SSTL12_DCI_M	0.381	0.381	0.399	0.381	0.557	0.557	0.587	0.557	0.654	0.654	0.694	0.654	ns
SSTL12_DCI_S	0.381	0.381	0.399	0.381	0.754	0.754	0.803	0.754	0.842	0.842	0.908	0.842	ns
SSTL12_F	0.403	0.403	0.403	0.403	0.412	0.412	0.430	0.412	0.538	0.538	0.566	0.538	ns
SSTL12_M	0.403	0.403	0.403	0.403	0.553	0.553	0.584	0.553	0.641	0.641	0.676	0.641	ns
SSTL12_S	0.403	0.403	0.403	0.403	0.758	0.758	0.808	0.758	0.823	0.823	0.879	0.823	ns
SSTL135_DCI_F	0.366	0.366	0.399	0.366	0.411	0.411	0.428	0.411	0.537	0.537	0.565	0.537	ns
SSTL135_DCI_M	0.366	0.366	0.399	0.366	0.551	0.551	0.582	0.551	0.645	0.645	0.685	0.645	ns
SSTL135_DCI_S	0.366	0.366	0.399	0.366	0.746	0.746	0.799	0.746	0.829	0.829	0.893	0.829	ns
SSTL135_F	0.378	0.378	0.399	0.378	0.408	0.408	0.428	0.408	0.528	0.528	0.561	0.528	ns
SSTL135_M	0.378	0.378	0.399	0.378	0.555	0.555	0.585	0.555	0.641	0.641	0.679	0.641	ns
SSTL135_S	0.378	0.378	0.399	0.378	0.772	0.772	0.823	0.772	0.827	0.827	0.878	0.827	ns
SSTL15_DCI_F	0.402	0.402	0.417	0.402	0.412	0.412	0.429	0.412	0.531	0.531	0.563	0.531	ns
SSTL15_DCI_M	0.402	0.402	0.417	0.402	0.553	0.553	0.583	0.553	0.645	0.645	0.685	0.645	ns
SSTL15_DCI_S	0.402	0.402	0.417	0.402	0.768	0.768	0.822	0.768	0.847	0.847	0.912	0.847	ns
SSTL15_F	0.371	0.371	0.400	0.371	0.408	0.408	0.428	0.408	0.530	0.530	0.556	0.530	ns
SSTL15_M	0.371	0.371	0.400	0.371	0.554	0.554	0.585	0.554	0.639	0.639	0.677	0.639	ns
SSTL15_S	0.371	0.371	0.400	0.371	0.767	0.767	0.817	0.767	0.813	0.813	0.867	0.813	ns
SSTL18_I_DCI_F	0.329	0.329	0.336	0.329	0.445	0.445	0.461	0.445	0.566	0.566	0.595	0.566	ns
SSTL18_I_DCI_M	0.329	0.329	0.336	0.329	0.554	0.554	0.585	0.554	0.644	0.644	0.683	0.644	ns
SSTL18_I_DCI_S	0.329	0.329	0.336	0.329	0.762	0.762	0.818	0.762	0.837	0.837	0.899	0.837	ns
SSTL18_I_F	0.316	0.316	0.337	0.316	0.454	0.454	0.476	0.454	0.578	0.578	0.608	0.578	ns
SSTL18_I_M	0.316	0.316	0.337	0.316	0.571	0.571	0.603	0.571	0.652	0.652	0.692	0.652	ns
SSTL18_I_S	0.316	0.316	0.337	0.316	0.782	0.782	0.835	0.782	0.816	0.816	0.870	0.816	ns
SUB_LVDS	0.539	0.539	0.620	0.539	0.660	0.660	0.692	0.660	969.863	969.863	969.863	969.863	ns

Output Delay Measurement Methodology

Output delays are measured with short output traces. Standard termination was used for all testing. The propagation delay of the trace is characterized separately and subtracted from the final measurement, and is therefore not included in the generalized test setups shown in Figure 1 and Figure 2.

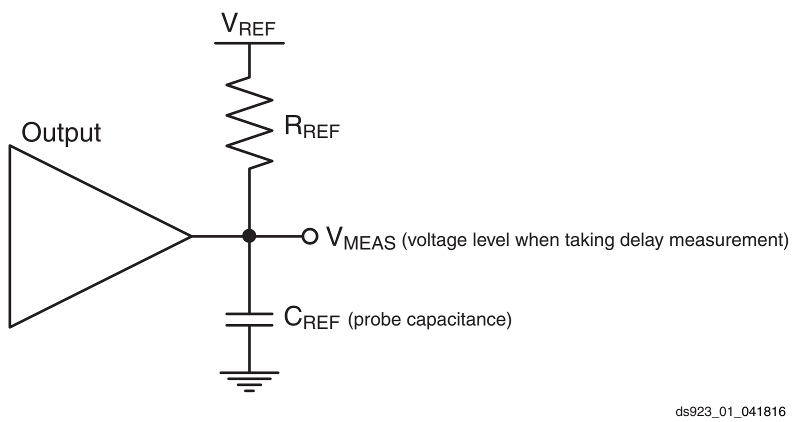

Figure 1: **Single-Ended Test Setup**

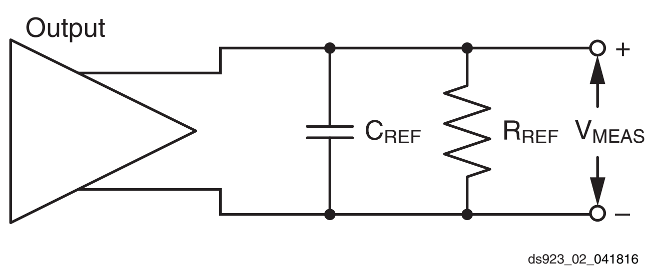

Figure 2: **Differential Test Setup**

Parameters V_{REF}, R_{REF}, C_{REF}, and V_{MEAS} fully describe the test conditions for each I/O standard. The most accurate prediction of propagation delay in any given application can be obtained through IBIS simulation, using this method:

1. Simulate the output driver of choice into the generalized test setup using values from Table 27.
2. Record the time to V_{MEAS}.
3. Simulate the output driver of choice into the actual PCB trace and load using the appropriate IBIS model or capacitance value to represent the load.
4. Record the time to V_{MEAS}.
5. Compare the results of step 2 and step 4. The increase or decrease in delay yields the actual propagation delay of the PCB trace.

Table 27: **Output Delay Measurement Methodology**

Description	I/O Standard Attribute	R_{REF} (Ω)	C_{REF}[(1)] (pF)	V_{MEAS} (V)	V_{REF} (V)
LVCMOS, 1.2V	LVCMOS12	1M	0	0.6	0
LVCMOS, 1.5V	LVCMOS15	1M	0	0.75	0
LVCMOS, 1.8V	LVCMOS18	1M	0	0.9	0
LVDCI, HSLVDCI, 1.5V	LVDCI_15, HSLVDCI_15	50	0	V_{REF}	0.75
LVDCI, HSLVDCI, 1.8V	LVDCI_15, HSLVDCI_18	50	0	V_{REF}	0.9
HSTL (high-speed transceiver logic), class I, 1.2V	HSTL_I_12	50	0	V_{REF}	0.6
HSTL, class I, 1.5V	HSTL_I	50	0	V_{REF}	0.75
HSTL, class I, 1.8V	HSTL_I_18	50	0	V_{REF}	0.9
HSUL (high-speed unterminated logic), 1.2V	HSUL_12	50	0	V_{REF}	0.6
SSTL12 (stub series terminated logic), 1.2V	SSTL12	50	0	V_{REF}	0.6
SSTL135, 1.35V	SSTL135	50	0	V_{REF}	0.675
SSTL15, 1.5V	SSTL15	50	0	V_{REF}	0.75
SSTL18, class I, 1.8V	SSTL18_I	50	0	V_{REF}	0.9
POD10, 1.0V	POD10	50	0	V_{REF}	1.0
POD12, 1.2V	POD12	50	0	V_{REF}	1.2
DIFF_HSTL, class I, 1.2V	DIFF_HSTL_I_12	50	0	V_{REF}	0.6
DIFF_HSTL, class I, 1.5V	DIFF_HSTL_I	50	0	V_{REF}	0.75
DIFF_HSTL, class I, 1.8V	DIFF_HSTL_I_18	50	0	V_{REF}	0.9
DIFF_HSUL, 1.2V	DIFF_HSUL_12	50	0	V_{REF}	0.6
DIFF_SSTL12, 1.2V	DIFF_SSTL12	50	0	V_{REF}	0.6
DIFF_SSTL135, 1.35V	DIFF_SSTL135	50	0	V_{REF}	0.675
DIFF_SSTL15, 1.5V	DIFF_SSTL15	50	0	V_{REF}	0.75
DIFF_SSTL18, 1.8V	DIFF_SSTL18_I	50	0	V_{REF}	0.9
DIFF_POD10, 1.0V	DIFF_POD10	50	0	V_{REF}	1.0
DIFF_POD12, 1.2V	DIFF_POD12	50	0	V_{REF}	1.2
LVDS (low-voltage differential signaling), 1.8V	LVDS	100	0	0[(2)]	0
SUB_LVDS, 1.8V	SUB_LVDS	100	0	0[(2)]	0
MIPI D-PHY (high speed) 1.2V	MIPI_DPHY_DCI_HS	100	0	0[(2)]	0
MIPI D-PHY (low power) 1.2V	MIPI_DPHY_DCI_LP	1M	0	0.6	0

Notes:

1. C_{REF} is the capacitance of the probe, nominally 0 pF.
2. The value given is the differential output voltage.

Clock Buffers and Networks

Table 32: **Clock Buffers Switching Characteristics**

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages				Units
		0.90V	0.85V		0.72V	
		-3	-2	-1	-2	
Global Clock Switching Characteristics (Including BUFGCTRL)						
F_{MAX}	Maximum frequency of a global clock tree (BUFG).	891	775	667	725	MHz
Global Clock Buffer with Input Divide Capability (BUFGCE_DIV)						
F_{MAX}	Maximum frequency of a global clock buffer with input divide capability (BUFGCE_DIV).	891	775	667	725	MHz
Global Clock Buffer with Clock Enable (BUFGCE)						
F_{MAX}	Maximum frequency of a global clock buffer with clock enable (BUFGCE).	891	775	667	725	MHz
Leaf Clock Buffer with Clock Enable (BUFCE_LEAF)						
F_{MAX}	Maximum frequency of a leaf clock buffer with clock enable (BUFCE_LEAF).	891	775	667	725	MHz
GTY Clock Buffer with Clock Enable and Clock Input Divide Capability (BUFG_GT)						
F_{MAX}	Maximum frequency of a serial transceiver clock buffer with clock enable and clock input divide capability.	512	512	512	512	MHz

Table 37: **Global Clock Input to Output Delay With MMCM**

Symbol	Description	Device	Speed Grade and V_{CCINT} Operating Voltages				Units
			0.90V	0.85V		0.72V	
			-3	-2	-1	-2	
SSTL15 Global Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, with MMCM.							
$T_{ICKOFMMCMCC}$	Global clock input and output flip-flop *with* MMCM.	XCVU3P	1.80	1.80	1.94	2.34	ns
		XCVU5P	1.80	1.80	1.94	2.34	ns
		XCVU7P	1.80	1.80	1.94	2.34	ns
		XCVU9P	1.80	1.80	1.94	2.34	ns
		XCVU11P	1.56	1.56	1.68	2.07	ns
		XCVU13P	1.56	1.56	1.68	2.07	ns

Notes:

1. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible I/O and CLB flip-flops are clocked by the global clock net in a single SLR.
2. MMCM output jitter is already included in the timing calculation.

Device Pin-to-Pin Input Parameter Guidelines

The pin-to-pin numbers in Table 38 are based on the clock root placement in the center of the device. The actual pin-to-pin values will vary if the root placement selected is different. Consult the Vivado Design Suite timing report for the actual pin-to-pin values.

Table 38: **Global Clock Input Setup and Hold With MMCM**

Symbol	Description		Device	Speed Grade and V_{CCINT} Operating Voltages				Units
				0.90V	0.85V		0.72V	
				-3	-2	-1	-2	
Input Setup and Hold Time Relative to Global Clock Input Signal using SSTL15 Standard.[1][2][3]								
$T_{PSMMCMCC\_VU3P}$	Global clock input and input flip-flop (or latch) with MMCM.	Setup	XCVU3P	1.86	1.86	1.99	2.32	ns
$T_{PHMMCMCC\_VU3P}$		Hold		–0.13	–0.13	–0.13	0.14	ns
$T_{PSMMCMCC\_VU5P}$		Setup	XCVU5P	1.86	1.86	1.99	2.32	ns
$T_{PHMMCMCC\_VU5P}$		Hold		–0.13	–0.13	–0.13	0.14	ns
$T_{PSMMCMCC\_VU7P}$		Setup	XCVU7P	1.86	1.86	1.99	2.32	ns
$T_{PHMMCMCC\_VU7P}$		Hold		–0.13	–0.13	–0.13	0.14	ns
$T_{PSMMCMCC\_VU9P}$		Setup	XCVU9P	1.86	1.86	1.99	2.32	ns
$T_{PHMMCMCC\_VU9P}$		Hold		–0.13	–0.13	–0.13	0.14	ns
$T_{PSMMCMCC\_VU11P}$		Setup	XCVU11P	1.92	1.92	2.05	2.36	ns
$T_{PHMMCMCC\_VU11P}$		Hold		–0.13	–0.13	–0.13	0.16	ns
$T_{PSMMCMCC\_VU13P}$		Setup	XCVU13P	1.92	1.92	2.05	2.36	ns
$T_{PHMMCMCC\_VU13P}$		Hold		–0.13	–0.13	–0.13	0.16	ns

Notes:

1. Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, slowest temperature, and slowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, fastest temperature, and fastest voltage.
2. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible I/O and CLB flip-flops are clocked by the global clock net in a single SLR.
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 39: **Sampling Window**

Description	Speed Grade and V_{CCINT} Operating Voltages				Units
	0.90V	0.85V		0.72V	
	-3	-2	-1	-2	
T_{SAMP_BUFG}[1]	510	610	610	610	ps
$T_{SAMP\_NATIVE\_DPA}$	100	100	125	125	ps
$T_{SAMP\_NATIVE\_BISC}$	60	60	85	85	ps

Notes:

1. This parameter indicates the total sampling error of the Virtex UltraScale+ FPGA DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the MMCM to capture the DDR input registers' edges of operation. These measurements include: CLK0 MMCM jitter, MMCM accuracy (phase offset), and MMCM phase shift resolution. These measurements do not include package or clock tree skew.

GTY Transceiver Specifications

The *UltraScale Architecture and Product Overview* (DS890) lists the Virtex UltraScale+ FPGAs that include the GTY transceivers.

GTY Transceiver DC Input and Output Levels

Table 41 summarizes the DC specifications of the GTY transceivers in Virtex UltraScale+ FPGAs. Consult the *UltraScale Architecture GTY Transceiver User Guide* (UG578) for further information.

Table 41: **GTY Transceiver DC Specifications**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
DV_{PPIN}	Differential peak-to-peak input voltage (external AC coupled)	>10.3125 Gb/s	150	–	1250	mV
		6.6 Gb/s to 10.3125 Gb/s	150	–	1250	mV
		≤ 6.6 Gb/s	150	–	2000	mV
V_{IN}	Single-ended input voltage. Voltage measured at the pin referenced to GND.	DC coupled $V_{MGTAVTT}$ = 1.2V	–400	–	$V_{MGTAVTT}$	mV
V_{CMIN}	Common mode input voltage	DC coupled $V_{MGTAVTT}$ = 1.2V	–	2/3 $V_{MGTAVTT}$	–	mV
D_{VPPOUT}	Differential peak-to-peak output voltage[1]	Transmitter output swing is set to 1010	800	–	–	mV
$V_{CMOUTDC}$	Common mode output voltage: DC coupled (equation based)	When remote RX is terminated to GND	$V_{MGTAVTT}/2 - D_{VPPOUT}/4$			mV
		When remote RX termination is floating	$V_{MGTAVTT} - D_{VPPOUT}/2$			mV
		When remote RX is terminated to V_{RX_TERM}[2]	$V_{MGTAVTT} - \frac{D_{VPPOUT}}{4} - \left(\frac{V_{MGTAVTT} - V_{RX\_TERM}}{2}\right)$			mV
$V_{CMOUTAC}$	Common mode output voltage: AC coupled	Equation based	$V_{MGTAVTT} - D_{VPPOUT}/2$			mV
R_{IN}	Differential input resistance		–	100	–	Ω
R_{OUT}	Differential output resistance		–	100	–	Ω
T_{OSKEW}	Transmitter output pair (TXP and TXN) intra-pair skew		–	–	10	ps
C_{EXT}	Recommended external AC coupling capacitor[3]		–	100	–	nF

Notes:

1. The output swing and pre-emphasis levels are programmable using the GTY transceiver attributes discussed in the *UltraScale Architecture GTY Transceiver User Guide* (UG578) and can result in values lower than reported in this table.
2. V_{RX_TERM} is the remote RX termination voltage.
3. Other values can be used as appropriate to conform to specific protocols and standards.

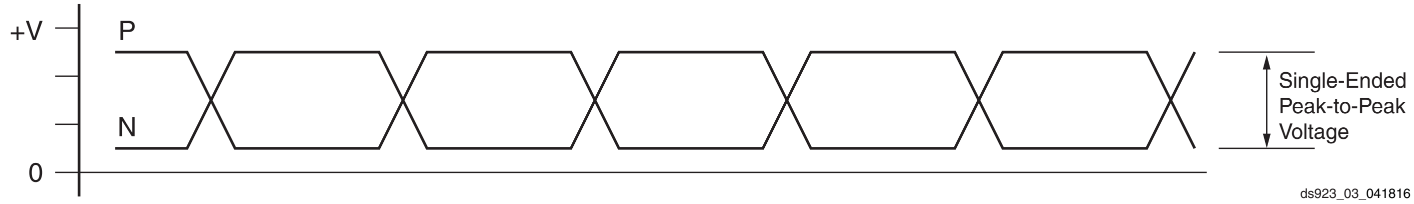

Figure 3: **Single-Ended Peak-to-Peak Voltage**

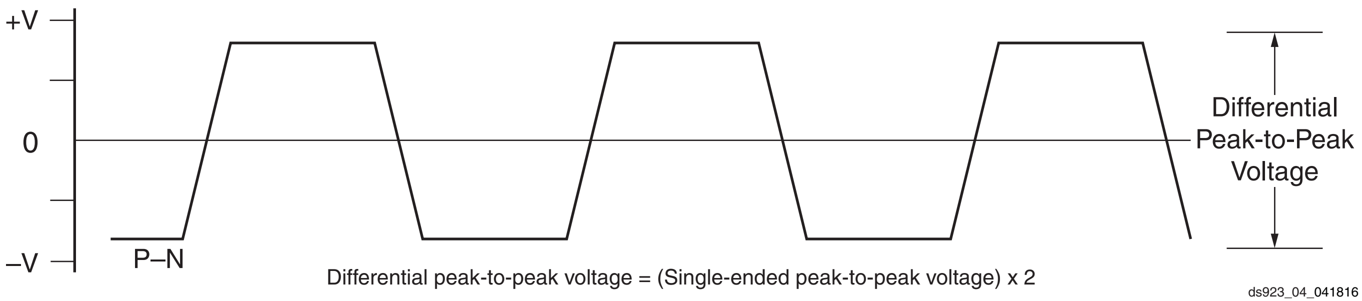

Figure 4: **Differential Peak-to-Peak Voltage**

Table 42 and Table 43 summarize the DC specifications of the clock input of the GTY transceivers in Virtex UltraScale+ FPGAs. Consult www.xilinx.com/products/technology/high-speed-serial for further details.

Table 42: **GTY Transceiver Clock DC Input Level Specification**

Symbol	DC Parameter	Min	Typ	Max	Units
V_{IDIFF}	Differential peak-to-peak input voltage	250	–	2000	mV
R_{IN}	Differential input resistance	–	100	–	Ω
C_{EXT}	Required external AC coupling capacitor	–	10	–	nF

Table 43: **GTY Transceiver Clock Output Level Specification**

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{OL}	Output high voltage for P and N	R_T = 100Ω across P and N signals	100	–	330	mV
V_{OH}	Output low voltage for P and N	R_T = 100Ω across P and N signals	500	–	700	mV
V_{DDOUT}	Differential output voltage (P–N), P = High (N–P), N = High	R_T = 100Ω across P and N signals	300	–	430	mV
V_{CMOUT}	Common mode voltage	R_T = 100Ω across P and N signals	300	–	500	mV

GTY Transceiver Switching Characteristics

Consult www.xilinx.com/products/technology/high-speed-serial for further information.

Table 44: **GTY Transceiver Performance**

Symbol	Description	Output Divider	Speed Grade and V_{CCINT} Operating Voltages								Units
			0.90V		0.85V				0.72V		
			-3		-2		-1		-2		
F_{GTYMAX}	GTY maximum line rate		32.75[1]		28.21[1]		25.7813[1]		28.21[1]		Gb/s
F_{GTYMIN}	GTY minimum line rate		0.5		0.5		0.5		0.5		Gb/s
			Min	Max	Min	Max	Min	Max	Min	Max	
$F_{GTYCRANGE}$	CPLL line rate range[2]	1	4.0	12.5	4.0	12.5	4.0	8.5	4.0	12.5	Gb/s
		2	2.0	6.25	2.0	6.25	2.0	4.25	2.0	6.25	Gb/s
		4	1.0	3.125	1.0	3.125	1.0	2.125	1.0	3.125	Gb/s
		8	0.5	1.5625	0.5	1.5625	0.5	1.0625	0.5	1.5625	Gb/s
		16	N/A								Gb/s
		32	N/A								Gb/s
			Min	Max	Min	Max	Min	Max	Min	Max	
$F_{GTYQRANGE1}$	QPLL0 line rate range[3]	1	19.6	32.75	19.6	28.21	19.6	25.7813	19.6	28.21	Gb/s
		1	9.8	16.375	9.8	16.375	9.8	12.5	9.8	16.375	Gb/s
		2	4.9	8.1875	4.9	8.1875	4.9	8.1875	4.9	8.1875	Gb/s
		4	2.45	4.09375	2.45	4.09375	2.45	4.09375	2.45	4.09375	Gb/s
		8	1.225	2.04688	1.225	2.04688	1.225	2.04688	1.225	2.04688	Gb/s
		16	0.6125	1.02344	0.6125	1.02344	0.6125	1.02344	0.6125	1.02344	Gb/s
			Min	Max	Min	Max	Min	Max	Min	Max	
$F_{GTYQRANGE2}$	QPLL1 line rate range[4]	1	16.0	26.0	16.0	26.0	19.6	25.7813	16.0	26.0	Gb/s
		1	8.0	13.0	8.0	13.0	8.0	12.5	8.0	13.0	Gb/s
		2	4.0	6.5	4.0	6.5	4.0	6.5	4.0	6.5	Gb/s
		4	2.0	3.25	2.0	3.25	2.0	3.25	2.0	3.25	Gb/s
		8	1.0	1.625	1.0	1.625	1.0	1.625	1.0	1.625	Gb/s
		16	0.5	0.8125	0.5	0.8125	0.5	0.8125	0.5	0.8125	Gb/s
			Min	Max	Min	Max	Min	Max	Min	Max	
$F_{CPLLRANGE}$	CPLL frequency range		2.0	6.25	2.0	6.25	2.0	4.25	2.0	6.25	GHz
$F_{QPLL0RANGE}$	QPLL0 frequency range		9.8	16.375	9.8	16.375	9.8	16.375	9.8	16.375	GHz
$F_{QPLL1RANGE}$	QPLL1 frequency range		8.0	13.0	8.0	13.0	8.0	13.0	8.0	13.0	GHz

Notes:

1. XCVU11P devices in the FLGF1924 package have a maximum GTY transceiver line rate of 16.3 Gb/s.
2. The values listed are the rounded results of the calculated equation (2 x CPLL_Frequency)/Output_Divider.
3. The values listed are the rounded results of the calculated equation (2 x QPLL0_Frequency)/Output_Divider.
4. The values listed are the rounded results of the calculated equation (2 x QPLL1_Frequency)/Output_Divider.

Table 45: **GTY Transceiver Dynamic Reconfiguration Port (DRP) Switching Characteristics**

Symbol	Description	All Speed Grades	Units
$F_{GTYDRPCLK}$	GTYDRPCLK maximum frequency.	250	MHz

Table 46: **GTY Transceiver Reference Clock Switching Characteristics**

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
F_{GCLK}	Reference clock frequency range.		60	–	820	MHz
T_{RCLK}	Reference clock rise time.	20% – 80%	–	200	–	ps
T_{FCLK}	Reference clock fall time.	80% – 20%	–	200	–	ps
T_{DCREF}	Reference clock duty cycle.	Transceiver PLL only	40	50	60	%

Table 47: **GTY Transceiver Reference Clock Oscillator Selection Phase Noise Mask**[1]

Symbol	Description	Offset Frequency	Min	Typ	Max	Units
$QPLL_{REFCLKMASK}$	QPLL0/QPLL1 reference clock select phase noise mask at REFCLK frequency = 156.25 MHz.	10 kHz	–	–	–112	dBc/Hz
		100 kHz	–	–	–128	
		1 MHz	–	–	–145	
	QPLL0/QPLL1 reference clock select phase noise mask at REFCLK frequency = 312.5 MHz.	10 kHz	–	–	–103	dBc/Hz
		100 kHz	–	–	–123	
		1 MHz	–	–	–143	
	QPLL0/QPLL1 reference clock select phase noise mask at REFCLK frequency =625 MHz.	10 kHz	–	–	–98	dBc/Hz
		100 kHz	–	–	–117	
		1 MHz	–	–	–140	
$CPLL_{REFCLKMASK}$	CPLL reference clock select phase noise mask at REFCLK frequency = 156.25 MHz.	10 kHz	–	–	–112	dBc/Hz
		100 kHz	–	–	–128	
		1 MHz	–	–	–145	
		50 MHz	–	–	–145	
	CPLL reference clock select phase noise mask at REFCLK frequency = 312.5 MHz.	10 kHz	–	–	–103	dBc/Hz
		100 kHz	–	–	–123	
		1 MHz	–	–	–143	
		50 MHz	–	–	–145	
	CPLL reference clock select phase noise mask at REFCLK frequency = 625 MHz.	10 kHz	–	–	–98	dBc/Hz
		100 kHz	–	–	–117	
		1 MHz	–	–	–140	
		50 MHz	–	–	–144	

Notes:

1. For reference clock frequencies not in this table, use the phase-noise mask for the nearest reference clock frequency.

Table 50: **GTY Transceiver Transmitter Switching Characteristics**

Symbol	Description	Condition	Min	Typ	Max	Units
F_{GTYTX}	Serial data rate range		0.500	–	F_{GTYMAX}	Gb/s
T_{RTX}	TX rise time	20%–80%	–	21	–	ps
T_{FTX}	TX fall time	80%–20%	–	21	–	ps
T_{LLSKEW}	TX lane-to-lane skew(1)		–	–	500.00	ps
$T_{J32.75}$	Total jitter(2)(4)	32.75 Gb/s	–	–	0.35	UI
$D_{J32.75}$	Deterministic jitter(2)(4)		–	–	0.19	UI
$T_{J28.21}$	Total jitter(2)(4)	28.21 Gb/s	–	–	0.28	UI
$D_{J28.21}$	Deterministic jitter(2)(4)		–	–	0.17	UI
$T_{J16.375}$	Total jitter(2)(4)	16.375 Gb/s	–	–	0.28	UI
$D_{J16.375}$	Deterministic jitter(2)(4)		–	–	0.17	UI
$T_{J15.0}$	Total jitter(2)(4)	15.0 Gb/s	–	–	0.28	UI
$D_{J15.0}$	Deterministic jitter(2)(4)		–	–	0.17	UI
$T_{J14.1}$	Total jitter(2)(4)	14.1 Gb/s	–	–	0.28	UI
$D_{J14.1}$	Deterministic jitter(2)(4)		–	–	0.17	UI
$T_{J14.1}$	Total jitter(2)(4)	14.025 Gb/s	–	–	0.28	UI
$D_{J14.1}$	Deterministic jitter(2)(4)		–	–	0.17	UI
$T_{J13.1}$	Total jitter(2)(4)	13.1 Gb/s	–	–	0.28	UI
$D_{J13.1}$	Deterministic jitter(2)(4)		–	–	0.17	UI
$T_{J12.5\_QPLL}$	Total jitter(2)(4)	12.5 Gb/s	–	–	0.28	UI
$D_{J12.5\_QPLL}$	Deterministic jitter(2)(4)		–	–	0.17	UI
$T_{J12.5\_CPLL}$	Total jitter(3)(4)	12.5 Gb/s	–	–	0.33	UI
$D_{J12.5\_CPLL}$	Deterministic jitter(3)(4)		–	–	0.17	UI
$T_{J11.3}$	Total jitter(2)(4)	11.3 Gb/s	–	–	0.28	UI
$D_{J11.3}$	Deterministic jitter(2)(4)		–	–	0.17	UI
$T_{J10.3125\_QPLL}$	Total jitter(2)(4)	10.3125 Gb/s	–	–	0.28	UI
$D_{J10.3125\_QPLL}$	Deterministic jitter(2)(4)		–	–	0.17	UI
$T_{J10.3125\_CPLL}$	Total jitter(3)(4)	10.3125 Gb/s	–	–	0.33	UI
$D_{J10.3125\_CPLL}$	Deterministic jitter(3)(4)		–	–	0.17	UI
$T_{J9.953\_QPLL}$	Total jitter(2)(4)	9.953 Gb/s	–	–	0.28	UI
$D_{J9.953\_QPLL}$	Deterministic jitter(2)(4)		–	–	0.17	UI
$T_{J9.953\_CPLL}$	Total jitter(3)(4)	9.953 Gb/s	–	–	0.33	UI
$D_{J9.953\_CPLL}$	Deterministic jitter(3)(4)		–	–	0.17	UI
$T_{J8.0}$	Total jitter(3)(4)	8.0 Gb/s	–	–	0.32	UI
$D_{J8.0}$	Deterministic jitter(3)(4)		–	–	0.17	UI
$T_{J6.6}$	Total jitter(3)(4)	6.6 Gb/s	–	–	0.30	UI
$D_{J6.6}$	Deterministic jitter(3)(4)		–	–	0.15	UI
$T_{J5.0}$	Total jitter(3)(4)	5.0 Gb/s	–	–	0.30	UI
$D_{J5.0}$	Deterministic jitter(3)(4)		–	–	0.15	UI
$T_{J4.25}$	Total jitter(3)(4)	4.25 Gb/s	–	–	0.30	UI
$D_{J4.25}$	Deterministic jitter(3)(4)		–	–	0.15	UI

Table 52: **GTY Transceiver Protocol List *(Cont'd)***

Protocol	Specification	Serial Rate (Gb/s)	Electrical Compliance
Serial RapidIO	RapidIO specification 3.1	1.25–10.3125	Compliant
DisplayPort (source only)	DP 1.2B CTS	1.62–5.4	Compliant[(3)]
Fibre channel	FC-PI-4	1.0625–14.025	Compliant
SATA Gen1, 2, 3	Serial ATA revision 3.0 specification	1.5, 3.0, and 6.0	Compliant
SAS Gen1, 2, 3	T10/BSR INCITS 519	3.0, 6.0, and 12.0	Compliant
SFI-5	OIF-SFI5-01.0	0.625 - 12.5	Compliant
Aurora	CEI-6G, CEI-11G-LR	All rates	Compliant

Notes:

1. 25 dB loss at Nyquist without FEC.
2. The transition time of the transmitter is faster than the IEEE Std 802.3-2012 specification.
3. This protocol requires external circuitry to achieve compliance.

Integrated Interface Block for Interlaken

More information and documentation on solutions using the integrated interface block for Interlaken can be found at UltraScale Interlaken. The *UltraScale Architecture and Product Overview* (DS890) lists how many blocks are in each Virtex UltraScale+ FPGA. This section describes the following Interlaken configurations.

- 12 x 12.5 Gb/s protocol and lane logic mode (Table 53).
- 6 x 25.78125 Gb/s and 6 x 28.21 Gb/s protocol and lane logic mode (Table 54).
- 12 x 25.78125 Gb/s lane logic only mode (Table 55).

XCVU11P devices in the FLVF1924 package are only supported using the 12 x 12.5 Gb/s Interlaken configuration. See Table 44 for the F_{GTYMAX} description.

Table 53: **Maximum Performance for Interlaken 12 x 12.5 Gb/s Protocol and Lane Logic Mode Designs**

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages										Units
		0.90V		0.85V				0.72V				
		-3		-2		-1		-2		-1		
$F_{RX\_SERDES\_CLK}$	Receive serializer/ deserializer clock	195.32		195.32		195.32		195.32		195.32		MHz
$F_{TX\_SERDES\_CLK}$	Transmit serializer/ deserializer clock	195.32		195.32		195.32		195.32		195.32		MHz
F_{DRP_CLK}	Dynamic reconfiguration port clock	250.00		250.00		250.00		250.00		250.00		MHz
		Min(1)	Max	Min(1)	Max	Min(1)	Max	Min(1)	Max	Min(1)	Max	
F_{CORE_CLK}	Interlaken core clock	300.00	322.27	300.00	322.27	300.00	322.27	300.00	322.27	300.00	322.27	MHz
F_{LBUS_CLK}	Interlaken local bus clock	300.00	322.27	300.00	322.27	300.00	322.27	300.00	322.27	300.00	322.27	MHz

Notes:

1. These are the minimum clock frequencies at the maximum lane performance.

Table 54: **Maximum Performance for Interlaken 6 x 25.78125 Gb/s and 6 x 28.21 Gb/s Protocol and Lane Logic Mode Designs**

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages										Units
		0.90V		0.85V				0.72V				
		-3[1]		-2[1]		-1		-2		-1		
$F_{RX\_SERDES\_CLK}$	Receive serializer/ deserializer clock	440.79		440.79		N/A		402.84		N/A		MHz
$F_{TX\_SERDES\_CLK}$	Transmit serializer/ deserializer clock	440.79		440.79		N/A		402.84		N/A		MHz
F_{DRP_CLK}	Dynamic reconfiguration port clock	250.00		250.00		N/A		250.00		N/A		MHz
		Min[2]	Max	Min[2]	Max	Min	Max	Min[2]	Max	Min	Max	
F_{CORE_CLK}	Interlaken core clock	412.50[3]	479.20	412.50[3]	479.20	N/A		412.50	429.69	N/A		MHz
F_{LBUS_CLK}	Interlaken local bus clock	300.00[4]	349.52	300.00[4]	349.52	N/A		300.00	349.52	N/A		MHz

Notes:

1. 6 x 28.21 mode is only supported in the -2 (V_{CCINT}=0.85V) and -3 (V_{CCINT}=0.90V) speed grades.
2. These are the minimum clock frequencies at the maximum lane performance.
3. The minimum value for CORE_CLK is 451.36 MHz for the 6 x 28.21 Gb/s protocol.
4. The minimum value for LBUS_CLK is 330.00 MHz for the 6 x 28.21 Gb/s protocol.

Table 55: **Maximum Performance for Interlaken 12 x 25.78125 Gb/s Lane Logic Only Mode Designs**

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages					Units
		0.90V	0.85V		0.72V		
		-3	-2	-1	-2	-1	
$F_{RX\_SERDES\_CLK}$	Receive serializer/ deserializer clock	402.84	402.84	N/A	N/A	N/A	MHz
$F_{TX\_SERDES\_CLK}$	Transmit serializer/ deserializer clock	402.84	402.84	N/A	N/A	N/A	MHz
F_{DRP_CLK}	Dynamic reconfiguration port clock	250.00	250.00	N/A	N/A	N/A	MHz
F_{CORE_CLK}	Interlaken core clock	412.50	412.50	N/A	N/A	N/A	MHz
F_{LBUS_CLK}	Interlaken local bus clock	349.52	349.52	N/A	N/A	N/A	MHz

Table 58: **System Monitor Specifications *(Cont'd)***

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
Supply sensor error[4]		Supply voltages 0.72V to 1.2V, T_j = –40°C to 100°C (with external REF)	–	–	±0.5	%
		Supply voltages 0.72V to 1.2V, T_j = –55°C to 125°C (with external REF)	–	–	±1.0	%
		All other supply voltages, T_j = –40°C to 100°C (with external REF)	–	–	±1.0	%
		All other supply voltages, T_j = –55°C to 125°C (with external REF)	–	–	±2.0	%
		Supply voltages 0.72V to 1.2V, T_j = –40°C to 100°C (with internal REF)	–	–	±1.0	%
		Supply voltages 0.72V to 1.2V, T_j = –55°C to 125°C (with internal REF)	–	–	±2.0	%
		All other supply voltages, T_j = –40°C to 100°C (with internal REF)	–	–	±1.5	%
		All other supply voltages, T_j = –55°C to 125°C (with internal REF)	–	–	±2.5	%
Conversion Rate[5]						
Conversion time—continuous	t_{CONV}	Number of ADCCLK cycles	26	–	32	Cycles
Conversion time—event	t_{CONV}	Number of ADCCLK cycles	–	–	21	Cycles
DRP clock frequency	DCLK	DRP clock frequency	8	–	250	MHz
ADC clock frequency	ADCCLK	Derived from DCLK	1	–	5.2	MHz
DCLK duty cycle			40	–	60	%
SYSMON Reference[6]						
External reference	V_{REFP}	Externally supplied reference voltage	1.20	1.25	1.30	V
On-chip reference		Ground V_{REFP} pin to AGND, T_j = –40°C to 100°C	1.2375	1.25	1.2625	V
		Ground V_{REFP} pin to AGND, T_j = –55°C to 125°C	1.225	1.25	1.275	V

Notes:

1. ADC offset errors are removed by enabling the ADC automatic offset calibration feature. The values are specified for when this feature is enabled.
2. See the *Analog Input* section in the *UltraScale Architecture System Monitor User Guide* (UG580).
3. When reading temperature values directly from the PMBus interface, the SYSMON has a +4°C offset due to the transfer function used by the PMBus application. For example, the external REF temperature sensor error's range of ±3°C becomes +1°C to +7°C when the temperature is read through the PMBus interface.
4. Supply sensor offset and gain errors are removed by enabling the automatic offset and gain calibration feature. The values are specified for when this feature is enabled.
5. See the *Adjusting the Acquisition Settling Time* section in the *UltraScale Architecture System Monitor User Guide* (UG580).
6. Any variation in the reference voltage from the nominal V_{REFP} = 1.25V and V_{REFN} = 0V will result in a deviation from the ideal transfer function. This also impacts the accuracy of the internal sensor measurements (i.e., temperature and power supply). However, for external ratiometric type applications allowing reference to vary by ±4% is permitted.

Configuration Switching Characteristics

Table 61: **Configuration Switching Characteristics**

Symbol	Description		Speed Grade and V_{CCINT} Operating Voltages 0.90V -3	0.85V -2	0.85V -1	0.72V -2	Units
Power-up Timing Characteristics							
T_{PL}	Program latency.		8.5	8.5	8.5	8.5	ms, Max
T_{POR}	Power-on reset (40 ms maximum ramp rate).		65	65	65	65	ms, Max
			0	0	0	0	ms, Min
	Power-on reset with POR override (2 ms maximum ramp rate).		15	15	15	15	ms, Max
			5	5	5	5	ms, Min
$T_{PROGRAM}$	Program pulse width.		250	250	250	250	ns, Min
CCLK Output (Master Mode)							
T_{ICCK}	Master CCLK output delay from INIT_B.		150	150	150	150	ns, Min
T_{MCCKL}[1]	Master CCLK clock Low time duty cycle.		40/60	40/60	40/60	40/60	%, Min/Max
T_{MCCKH}	Master CCLK clock High time duty cycle.		40/60	40/60	40/60	40/60	%, Min/Max
F_{MCCK}	Master SPI/BPI CCLK frequency.		125	125	125	100	MHz, Max
F_{MCCK_START}	Master CCLK frequency at start of configuration.		2.70	2.70	2.70	2.70	MHz, Typ
$F_{MCCKTOL}$	Frequency tolerance, master mode with respect to nominal CCLK.		±15	±15	±15	±15	%, Max
CCLK Input (Slave Mode)							
T_{SCCKL}	Slave CCLK clock minimum Low time.		2.5	2.5	2.5	2.5	ns, Min
T_{SCCKH}	Slave CCLK clock minimum High time.		2.5	2.5	2.5	2.5	ns, Min
F_{SCCK}	Slave serial SelectMap CCLK frequency.	XCVU3P, XCVU5P, XCVU7P, XCVU9P	125	125	125	100	MHz, Max
		XCVU11P, XCVU13P	125	125	125	66	MHz, Max
EMCCLK Input (Master Mode)							
T_{EMCCKL}	External master CCLK Low time.		2.5	2.5	2.5	2.5	ns, Min
T_{EMCCKH}	External master CCLK High time.		2.5	2.5	2.5	2.5	ns, Min
F_{EMCCK}	External master CCLK frequency.		125	125	125	100	MHz, Max
Internal Configuration Access Port							
F_{ICAPCK}	Internal configuration access port (ICAPE3).	XCVU3P	200	200	200	150	MHz, Max
	Master SLR ICAPE3 accessing entire device.	XCVU5P, XCVU7P, XCVU9P, XCVU11P, XCVU13P	125	125	125	100	MHz, Max
	SLR ICAPE3 accessing local SLR.	XCVU5P, XCVU7P, XCVU9P, XCVU11P, XCVU13P	200	200	200	150	MHz, Max
Slave Serial Mode Programming Switching							
T_{DCCK}/T_{CCKD}	D_{IN} setup/hold.		3.0/0	3.0/0	3.0/0	4.0/0	ns, Min
T_{CCO}	D_{OUT} clock to out.		8.0	8.0	8.0	9.0	ns, Max