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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	216000
Number of Logic Elements/Cells	3780000
Total RAM Bits	514867200
Number of I/O	448
Number of Gates	-
Voltage - Supply	0.873V ~ 0.927V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 100°C (TJ)
Package / Case	2577-BBGA, FCBGA
Supplier Device Package	2577-FCBGA (52.5x52.5)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xcvu13p-3flga2577e

Recommended Operating Conditions

Table 2: **Recommended Operating Conditions(1)(2)**

Symbol	Description	Min	Typ	Max	Units
FPGA Logic					
V_{CCINT}	Internal supply voltage.	0.825	0.850	0.876	V
	For -2LE (V_{CCINT} = 0.72V) devices: internal supply voltage.	0.698	0.720	0.742	V
	For -3E devices: internal supply voltage.	0.873	0.900	0.927	V
V_{CCINT_IO}(3)	Internal supply voltage for the I/O banks.	0.825	0.850	0.876	V
	For -2LE devices (V_{CCINT} = 0.85V): internal supply voltage for the I/O banks.	0.825	0.850	0.876	V
	For -3E devices: internal supply voltage for the I/O banks.	0.873	0.900	0.927	V
V_{CCBRAM}	Block RAM supply voltage.	0.825	0.850	0.876	V
	For -3E devices: block RAM supply voltage.	0.873	0.900	0.927	V
V_{CCAUX}	Auxiliary supply voltage.	1.746	1.800	1.854	V
V_{CCO}(4)(5)	Supply voltage for I/O banks.	0.950	–	1.900	V
V_{CCAUX_IO}(6)	Auxiliary I/O supply voltage.	1.746	1.800	1.854	V
V_{IN}(7)	I/O input voltage.	–0.200	–	V_{CCO} + 0.200	V
I_{IN}(8)	Maximum current through any pin in a powered or unpowered bank when forward biasing the clamp diode.	–	–	10	mA
V_{BATT}(9)	Battery voltage.	1.000	–	1.890	V
GTY Transceiver					
$V_{MGTAVCC}$(10)	Analog supply voltage for the GTY transceiver.	0.873	0.900	0.927	V
$V_{MGTAVTT}$(10)	Analog supply voltage for the GTY transmitter and receiver termination circuits.	1.164	1.20	1.236	V
$V_{MGTVCCAUX}$(10)	Auxiliary analog QPLL voltage supply for the transceivers.	1.746	1.80	1.854	V
$V_{MGTAVTTRCAL}$(10)	Analog supply voltage for the resistor calibration circuit of the GTY transceiver column.	1.164	1.20	1.236	V

Table 2: **Recommended Operating Conditions(1)(2) *(Cont'd)***

Symbol	Description	Min	Typ	Max	Units
SYSMON					
V_{CCADC}	SYSMON supply relative to GNDADC.	1.746	1.800	1.854	V
V_{REFP}	SYSMON externally supplied reference voltage relative to GNDADC.	1.200	1.250	1.300	V
Temperature					
T_j(11)	Junction temperature operating range for extended (E) temperature devices.(12)	0	–	100	°C
	Junction temperature operating range for industrial (I) temperature devices.	–40	–	100	°C
	Junction temperature operating range for eFUSE programming.(13)	–40	–	125	°C

Notes:

1. All voltages are relative to GND.
2. For the design of the power distribution system consult *UltraScale Architecture PCB Design Guide* (UG583).
3. V_{CCINT_IO} must be connected to V_{CCBRAM}.
4. For V_{CCO_0}, the minimum recommended operating voltage for power on and during configuration is 1.425V. After configuration, data is retained even if V_{CCO} drops to 0V.
5. Includes V_{CCO} of 1.0V, 1.2V, 1.35V, 1.5V, and 1.8V.
6. V_{CCAUX_IO} must be connected to V_{CCAUX}.
7. The lower absolute voltage specification always applies.
8. A total of 200 mA per bank should not be exceeded.
9. If battery is not used, connect V_{BATT} to either GND or V_{CCAUX}.
10. Each voltage listed requires filtering as described in the *UltraScale Architecture GTY Transceiver User Guide* (UG578).
11. Xilinx recommends measuring the Tj of a device using the system monitor as described in the *UltraScale Architecture System Monitor User Guide* (UG580). The SYSMON temperature measurement errors (that are described in Table 58) must be accounted for in your design. For example, by using an external reference of 1.25V, when SYSMON reports 97°C, there is a measurement error ±3°C. A reading of 97°C is considered the maximum adjusted Tj (100°C – 3°C = 97°C).
12. Devices labeled with the speed/temperature grade of -2LE can operate for a limited time at a junction temperature of 110°C. Timing parameters adhere to the same speed file at 110°C as they do below 110°C, regardless of operating voltage (nominal voltage of 0.85V or a low-voltage of 0.72V). Operation at Tj = 110°C is limited to 1% of the device lifetime and can occur sequentially or at regular intervals as long as the total time does not exceed 1% of the device lifetime.
13. Do not program eFUSE during device configuration (e.g., during configuration, during configuration readback, or when readback CRC is active).

Table 5: **Typical Quiescent Supply Current(1)(2)(3) *(Cont'd)***

Symbol	Description	Device	Speed Grade and V_{CCINT} Operating Voltages				Units
			0.90V	0.85V		0.72V	
			-3	-2	-1	-2	
I_{CCAUX_IOQ}	Quiescent V_{CCAUX_IO} supply current.	XCVU3P	62	62	62	62	mA
		XCVU5P	124	124	124	124	mA
		XCVU7P	124	124	124	124	mA
		XCVU9P	187	187	187	187	mA
		XCVU11P	79	79	79	79	mA
		XCVU13P	105	105	105	105	mA
$I_{CCBRAMQ}$	Quiescent V_{CCBRAM} supply current.	XCVU3P	45	43	43	43	mA
		XCVU5P	90	85	85	85	mA
		XCVU7P	90	85	85	85	mA
		XCVU9P	134	128	128	128	mA
		XCVU11P	130	124	124	124	mA
		XCVU13P	174	165	165	165	mA

Notes:

1. Typical values are specified at nominal voltage, 85°C junction temperatures (T_j) with single-ended SelectIO™ resources.
2. Typical values are for blank configured devices with no output current loads, no active input pull-up resistors, all I/O pins are 3-state and floating.
3. Use the Xilinx Power Estimator (XPE) spreadsheet tool (download at www.xilinx.com/power) to estimate static power consumption for conditions other than those specified.

Power-On/Off Power Supply Sequencing

The recommended power-on sequence is V_{CCINT}, V_{CCINT_IO}/V_{CCBRAM}, V_{CCAUX}/V_{CCAUX_IO}, and V_{CCO} to achieve minimum current draw and ensure that the I/Os are 3-stated at power-on. The recommended power-off sequence is the reverse of the power-on sequence. If V_{CCINT} and V_{CCINT_IO}/V_{CCBRAM} have the same recommended voltage levels, they can be powered by the same supply and ramped simultaneously. V_{CCINT_IO} must be connected to V_{CCBRAM}. If V_{CCAUX}/V_{CCAUX_IO} and V_{CCO} have the same recommended voltage levels, they can be powered by the same supply and ramped simultaneously. V_{CCAUX} and V_{CCAUX_IO} must be connected together. V_{CCADC} and V_{REF} can be powered at any time and have no power-up sequencing requirements.

The recommended power-on sequence to achieve minimum current draw for the GTY transceivers are V_{CCINT}, $V_{MGTAVCC}$, $V_{MGTAVTT}$ OR $V_{MGTAVCC}$, V_{CCINT}, $V_{MGTAVTT}$. There is no recommended sequencing for $V_{MGTVCCAUX}$. Both $V_{MGTAVCC}$ and V_{CCINT} can be ramped simultaneously. The recommended power-off sequence is the reverse of the power-on sequence to achieve minimum current draw.

If these recommended sequences are not met, current drawn from $V_{MGTAVTT}$ can be higher than specifications during power-up and power-down.

Table 13: **DC Output Levels for Single-ended and Differential POD10 and POD12 Standards(1)(2)**

Symbol	Description	V_{OUT}	Min	Typ	Max	Units
R_{OL}	Pull-down resistance.	V_{OM_DC} (as described in Table 14)	36	40	44	Ω
R_{OH}	Pull-up resistance.	V_{OM_DC} (as described in Table 14)	36	40	44	Ω

Notes:

1. Tested according to relevant specifications.
2. Standards specified using the default I/O standard configuration. For details, see the *UltraScale Architecture SelectIO Resources User Guide* (UG571).

Table 14: **Table 13 Definitions for DC Output Levels for POD Standards**

Symbol	Description	All Speed Grades	Units
V_{OM_DC}	DC output Mid measurement level (for IV curve linearity).	0.8 x V_{CCO}	V

LVDS DC Specifications (LVDS)

Table 15: **LVDS DC Specifications**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{CCO}(1)	Supply voltage.		1.710	1.800	1.890	V
V_{ODIFF}(2)	Differential output voltage: ($\underline{Q}$ – $\overline{Q}$), $\underline{Q}$ = High ($\underline{Q}$ – $\overline{Q}$), $\overline{Q}$ = High	R_T = 100Ω across Q and $\overline{Q}$ signals	247	350	454	mV
V_{OCM}(2)	Output common-mode voltage.	R_T = 100 Ω across Q and $\overline{Q}$ signals	1.000	1.250	1.425	V
V_{IDIFF}	Differential input voltage: ($\underline{Q}$ – $\overline{Q}$), $\underline{Q}$ = High ($\underline{Q}$ – $\overline{Q}$), $\overline{Q}$ = High		100	350	600(3)	mV
V_{ICM_DC}(4)	Input common-mode voltage (DC coupling).		0.300	1.200	1.425	V
V_{ICM_AC}(5)	Input common-mode voltage (AC coupling).		0.600	–	1.100	V

Notes:

1. In I/O banks, when LVDS is used with input-only functionality, it can be placed in a bank where the V_{CCO} levels are different from the specified level only if internal differential termination is not used. In this scenario, V_{CCO} must be chosen to ensure the input pin voltage levels do not violate the *Recommended Operating Condition* (Table 2) specification for the V_{IN} I/O pin voltage.
2. V_{OCM} and V_{ODIFF} values are for LVDS_PRE_EMPHASIS = FALSE.
3. Maximum V_{IDIFF} value is specified for the maximum V_{ICM} specification. With a lower V_{ICM}, a higher V_{DIFF} is tolerated only when the recommended operating conditions and overshoot/undershoot V_{IN} specifications are maintained.
4. Input common mode voltage for DC coupled configurations. EQUALIZATION = EQ_NONE (Default).
5. External input common mode voltage specification for AC coupled configurations. EQUALIZATION = EQ_LEVEL0, EQ_LEVEL1, EQ_LEVEL2, EQ_LEVEL3, EQ_LEVEL4.

Production Silicon and Software Status

In some cases, a particular family member (and speed grade) is released to production before a speed specification is released with the correct label (Advance, Preliminary, Production). Any labeling discrepancies are corrected in subsequent speed specification releases.

Table 18 lists the production released Virtex UltraScale+ FPGA, speed grade, and the minimum corresponding supported speed specification version and Vivado software revisions. The Vivado software and speed specifications listed are the minimum releases required for production. All subsequent releases of software and speed specifications are valid.

Table 18: **Virtex UltraScale+ FPGA Device Production Software and Speed Specification Release**

Device	Speed Grade and V_{CCINT} Operating Voltages				
	0.90V	0.85V			0.72V
	-3	-2	-1	-2L	-2L
XCVU3P		Vivado tools 2017.1 v1.10			
XCVU5P					
XCVU7P					
XCVU9P					
XCVU11P					
XCVU13P					

Notes:

1. Blank entries indicate a device and/or speed grade in Advance or Preliminary status.

Table 24: **IOB High Performance (HP) Switching Characteristics *(Cont'd)***

I/O Standards	$T_{INBUF\_DELAY\_PAD\_I}$				$T_{OUTBUF\_DELAY\_O\_PAD}$				$T_{OUTBUF\_DELAY\_TD\_PAD}$				Units
	0.90V	0.85V		0.72V	0.90V	0.85V		0.72V	0.90V	0.85V		0.72V	
	-3	-2	-1	-2	-3	-2	-1	-2	-3	-2	-1	-2	
HSLVDCI_18_S	0.424	0.424	0.447	0.424	0.761	0.761	0.817	0.761	0.836	0.836	0.900	0.836	ns
HSTL_I_12_F	0.378	0.378	0.399	0.378	0.423	0.423	0.443	0.423	0.553	0.553	0.582	0.553	ns
HSTL_I_12_M	0.378	0.378	0.399	0.378	0.551	0.551	0.582	0.551	0.642	0.642	0.679	0.642	ns
HSTL_I_12_S	0.378	0.378	0.399	0.378	0.750	0.750	0.799	0.750	0.813	0.813	0.868	0.813	ns
HSTL_I_18_F	0.322	0.322	0.339	0.322	0.456	0.456	0.474	0.456	0.576	0.576	0.606	0.576	ns
HSTL_I_18_M	0.322	0.322	0.339	0.322	0.569	0.569	0.602	0.569	0.653	0.653	0.692	0.653	ns
HSTL_I_18_S	0.322	0.322	0.339	0.322	0.781	0.781	0.833	0.781	0.816	0.816	0.871	0.816	ns
HSTL_I_DCI_12_F	0.378	0.378	0.399	0.378	0.406	0.406	0.429	0.406	0.534	0.534	0.564	0.534	ns
HSTL_I_DCI_12_M	0.378	0.378	0.399	0.378	0.556	0.556	0.586	0.556	0.654	0.654	0.694	0.654	ns
HSTL_I_DCI_12_S	0.378	0.378	0.399	0.378	0.754	0.754	0.803	0.754	0.842	0.842	0.907	0.842	ns
HSTL_I_DCI_18_F	0.321	0.321	0.339	0.321	0.445	0.445	0.461	0.445	0.566	0.566	0.595	0.566	ns
HSTL_I_DCI_18_M	0.321	0.321	0.339	0.321	0.554	0.554	0.585	0.554	0.643	0.643	0.684	0.643	ns
HSTL_I_DCI_18_S	0.321	0.321	0.339	0.321	0.761	0.761	0.817	0.761	0.836	0.836	0.900	0.836	ns
HSTL_I_DCI_F	0.393	0.393	0.415	0.393	0.431	0.431	0.445	0.431	0.555	0.555	0.575	0.555	ns
HSTL_I_DCI_M	0.393	0.393	0.415	0.393	0.552	0.552	0.581	0.552	0.644	0.644	0.684	0.644	ns
HSTL_I_DCI_S	0.393	0.393	0.415	0.393	0.766	0.766	0.821	0.766	0.847	0.847	0.912	0.847	ns
HSTL_I_F	0.378	0.378	0.399	0.378	0.423	0.423	0.443	0.423	0.549	0.549	0.581	0.549	ns
HSTL_I_M	0.378	0.378	0.399	0.378	0.554	0.554	0.585	0.554	0.640	0.640	0.677	0.640	ns
HSTL_I_S	0.378	0.378	0.399	0.378	0.766	0.766	0.816	0.766	0.811	0.811	0.866	0.811	ns
HSUL_12_DCI_F	0.378	0.378	0.399	0.378	0.425	0.425	0.443	0.425	0.558	0.558	0.586	0.558	ns
HSUL_12_DCI_M	0.378	0.378	0.399	0.378	0.556	0.556	0.586	0.556	0.654	0.654	0.694	0.654	ns
HSUL_12_DCI_S	0.378	0.378	0.399	0.378	0.736	0.736	0.784	0.736	0.821	0.821	0.886	0.821	ns
HSUL_12_F	0.378	0.378	0.399	0.378	0.412	0.412	0.430	0.412	0.538	0.538	0.566	0.538	ns
HSUL_12_M	0.378	0.378	0.399	0.378	0.551	0.551	0.582	0.551	0.642	0.642	0.679	0.642	ns
HSUL_12_S	0.378	0.378	0.399	0.378	0.750	0.750	0.799	0.750	0.813	0.813	0.868	0.813	ns
LVCMOS12_F_2	0.512	0.512	0.555	0.512	0.672	0.672	0.692	0.672	0.898	0.898	0.922	0.898	ns
LVCMOS12_F_4	0.512	0.512	0.555	0.512	0.504	0.504	0.521	0.504	0.664	0.664	0.693	0.664	ns
LVCMOS12_F_6	0.512	0.512	0.555	0.512	0.485	0.485	0.507	0.485	0.634	0.634	0.669	0.634	ns
LVCMOS12_F_8	0.512	0.512	0.555	0.512	0.465	0.465	0.489	0.465	0.611	0.611	0.666	0.611	ns
LVCMOS12_M_2	0.512	0.512	0.555	0.512	0.708	0.708	0.727	0.708	0.916	0.916	0.945	0.916	ns
LVCMOS12_M_4	0.512	0.512	0.555	0.512	0.550	0.550	0.573	0.550	0.664	0.664	0.690	0.664	ns
LVCMOS12_M_6	0.512	0.512	0.555	0.512	0.527	0.527	0.554	0.527	0.622	0.622	0.652	0.622	ns
LVCMOS12_M_8	0.512	0.512	0.555	0.512	0.540	0.540	0.571	0.540	0.614	0.614	0.649	0.614	ns
LVCMOS12_S_2	0.512	0.512	0.555	0.512	0.767	0.767	0.803	0.767	0.990	0.990	1.024	0.990	ns
LVCMOS12_S_4	0.512	0.512	0.555	0.512	0.666	0.666	0.704	0.666	0.803	0.803	0.848	0.803	ns
LVCMOS12_S_6	0.512	0.512	0.555	0.512	0.657	0.657	0.695	0.657	0.732	0.732	0.774	0.732	ns
LVCMOS12_S_8	0.512	0.512	0.555	0.512	0.708	0.708	0.761	0.708	0.745	0.745	0.790	0.745	ns
LVCMOS15_F_12	0.414	0.414	0.445	0.414	0.500	0.500	0.522	0.500	0.647	0.647	0.682	0.647	ns
LVCMOS15_F_2	0.414	0.414	0.445	0.414	0.702	0.702	0.722	0.702	0.919	0.919	0.940	0.919	ns
LVCMOS15_F_4	0.414	0.414	0.445	0.414	0.579	0.579	0.601	0.579	0.755	0.755	0.781	0.755	ns
LVCMOS15_F_6	0.414	0.414	0.445	0.414	0.547	0.547	0.569	0.547	0.711	0.711	0.742	0.711	ns

Table 24: **IOB High Performance (HP) Switching Characteristics *(Cont'd)***

I/O Standards	$T_{INBUF\_DELAY\_PAD\_I}$				$T_{OUTBUF\_DELAY\_O\_PAD}$				$T_{OUTBUF\_DELAY\_TD\_PAD}$				Units
	0.90V	0.85V		0.72V	0.90V	0.85V		0.72V	0.90V	0.85V		0.72V	
	-3	-2	-1	-2	-3	-2	-1	-2	-3	-2	-1	-2	
POD12_DCI_F	0.409	0.409	0.431	0.409	0.425	0.425	0.443	0.425	0.558	0.558	0.586	0.558	ns
POD12_DCI_M	0.409	0.409	0.431	0.409	0.543	0.543	0.572	0.543	0.638	0.638	0.678	0.638	ns
POD12_DCI_S	0.409	0.409	0.431	0.409	0.772	0.772	0.822	0.772	0.862	0.862	0.929	0.862	ns
POD12_F	0.409	0.409	0.431	0.409	0.455	0.455	0.476	0.455	0.595	0.595	0.626	0.595	ns
POD12_M	0.409	0.409	0.431	0.409	0.551	0.551	0.582	0.551	0.641	0.641	0.679	0.641	ns
POD12_S	0.409	0.409	0.431	0.409	0.767	0.767	0.817	0.767	0.832	0.832	0.889	0.832	ns
SLVS_400_18	0.539	0.539	0.620	0.539	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	ns
SSTL12_DCI_F	0.381	0.381	0.399	0.381	0.425	0.425	0.443	0.425	0.558	0.558	0.586	0.558	ns
SSTL12_DCI_M	0.381	0.381	0.399	0.381	0.557	0.557	0.587	0.557	0.654	0.654	0.694	0.654	ns
SSTL12_DCI_S	0.381	0.381	0.399	0.381	0.754	0.754	0.803	0.754	0.842	0.842	0.908	0.842	ns
SSTL12_F	0.403	0.403	0.403	0.403	0.412	0.412	0.430	0.412	0.538	0.538	0.566	0.538	ns
SSTL12_M	0.403	0.403	0.403	0.403	0.553	0.553	0.584	0.553	0.641	0.641	0.676	0.641	ns
SSTL12_S	0.403	0.403	0.403	0.403	0.758	0.758	0.808	0.758	0.823	0.823	0.879	0.823	ns
SSTL135_DCI_F	0.366	0.366	0.399	0.366	0.411	0.411	0.428	0.411	0.537	0.537	0.565	0.537	ns
SSTL135_DCI_M	0.366	0.366	0.399	0.366	0.551	0.551	0.582	0.551	0.645	0.645	0.685	0.645	ns
SSTL135_DCI_S	0.366	0.366	0.399	0.366	0.746	0.746	0.799	0.746	0.829	0.829	0.893	0.829	ns
SSTL135_F	0.378	0.378	0.399	0.378	0.408	0.408	0.428	0.408	0.528	0.528	0.561	0.528	ns
SSTL135_M	0.378	0.378	0.399	0.378	0.555	0.555	0.585	0.555	0.641	0.641	0.679	0.641	ns
SSTL135_S	0.378	0.378	0.399	0.378	0.772	0.772	0.823	0.772	0.827	0.827	0.878	0.827	ns
SSTL15_DCI_F	0.402	0.402	0.417	0.402	0.412	0.412	0.429	0.412	0.531	0.531	0.563	0.531	ns
SSTL15_DCI_M	0.402	0.402	0.417	0.402	0.553	0.553	0.583	0.553	0.645	0.645	0.685	0.645	ns
SSTL15_DCI_S	0.402	0.402	0.417	0.402	0.768	0.768	0.822	0.768	0.847	0.847	0.912	0.847	ns
SSTL15_F	0.371	0.371	0.400	0.371	0.408	0.408	0.428	0.408	0.530	0.530	0.556	0.530	ns
SSTL15_M	0.371	0.371	0.400	0.371	0.554	0.554	0.585	0.554	0.639	0.639	0.677	0.639	ns
SSTL15_S	0.371	0.371	0.400	0.371	0.767	0.767	0.817	0.767	0.813	0.813	0.867	0.813	ns
SSTL18_I_DCI_F	0.329	0.329	0.336	0.329	0.445	0.445	0.461	0.445	0.566	0.566	0.595	0.566	ns
SSTL18_I_DCI_M	0.329	0.329	0.336	0.329	0.554	0.554	0.585	0.554	0.644	0.644	0.683	0.644	ns
SSTL18_I_DCI_S	0.329	0.329	0.336	0.329	0.762	0.762	0.818	0.762	0.837	0.837	0.899	0.837	ns
SSTL18_I_F	0.316	0.316	0.337	0.316	0.454	0.454	0.476	0.454	0.578	0.578	0.608	0.578	ns
SSTL18_I_M	0.316	0.316	0.337	0.316	0.571	0.571	0.603	0.571	0.652	0.652	0.692	0.652	ns
SSTL18_I_S	0.316	0.316	0.337	0.316	0.782	0.782	0.835	0.782	0.816	0.816	0.870	0.816	ns
SUB_LVDS	0.539	0.539	0.620	0.539	0.660	0.660	0.692	0.660	969.863	969.863	969.863	969.863	ns

MMCM Switching Characteristics

Table 33: **MMCM Specification**

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages				Units
		0.90V	0.85V		0.72V	
		-3	-2	-1	-2	
MMCM_F_{INMAX}	Maximum input clock frequency.	1066	933	800	933	MHz
MMCM_F_{INMIN}	Minimum input clock frequency.	10	10	10	10	MHz
MMCM_$F_{INJITTER}$	Maximum input clock period jitter.	< 20% of clock input period or 1 ns Max				
MMCM_F_{INDUTY}	Input duty cycle range: 10–49 MHz.	25–75				%
	Input duty cycle range: 50–199 MHz.	30–70				%
	Input duty cycle range: 200–399 MHz.	35–65				%
	Input duty cycle range: 400–499 MHz.	40–60				%
	Input duty cycle range: >500 MHz.	45–55				%
MMCM_F_{MIN_PSCLK}	Minimum dynamic phase shift clock frequency.	0.01	0.01	0.01	0.01	MHz
MMCM_F_{MAX_PSCLK}	Maximum dynamic phase shift clock frequency.	550	500	450	500	MHz
MMCM_F_{VCOMIN}	Minimum MMCM VCO frequency.	800	800	800	800	MHz
MMCM_F_{VCOMAX}	Maximum MMCM VCO frequency.	1600	1600	1600	1600	MHz
MMCM_$F_{BANDWIDTH}$	Low MMCM bandwidth at typical.(1)	1.00	1.00	1.00	1.00	MHz
	High MMCM bandwidth at typical.(1)	4.00	4.00	4.00	4.00	MHz
MMCM_$T_{STATPHAOFFSET}$	Static phase offset of the MMCM outputs.(2)	0.12	0.12	0.12	0.12	ns
MMCM_$T_{OUTJITTER}$	MMCM output jitter.	Note 3				
MMCM_$T_{OUTDUTY}$	MMCM output clock duty cycle precision.(4)	0.165	0.20	0.20	0.20	ns
MMCM_$T_{LOCKMAX}$	MMCM maximum lock time for MMCM_F_{PFDMIN}.	100	100	100	100	µs
MMCM_F_{OUTMAX}	MMCM maximum output frequency.	891	775	667	725	MHz
MMCM_F_{OUTMIN}	MMCM minimum output frequency.(4)(5)	6.25	6.25	6.25	6.25	MHz
MMCM_$T_{EXTFDVAR}$	External clock feedback variation.	< 20% of clock input period or 1 ns Max				
MMCM_$RST_{MINPULSE}$	Minimum reset pulse width.	5.00	5.00	5.00	5.00	ns
MMCM_F_{PFDMAX}	Maximum frequency at the phase frequency detector.	550	500	450	500	MHz
MMCM_F_{PFDMIN}	Minimum frequency at the phase frequency detector.	10	10	10	10	MHz
MMCM_$T_{FBDELAY}$	Maximum delay in the feedback path.	5 ns Max or one clock cycle				
MMCM_F_{DPRCLK_MAX}	Maximum DRP clock frequency	250	250	250	250	MHz

Notes:

1. The MMCM does not filter typical spread-spectrum input clocks because they are usually far below the bandwidth filter frequencies.
2. The static offset is measured between any MMCM outputs with identical phase.
3. Values for this parameter are available in the Clocking Wizard.
4. Includes global clock buffer.
5. Calculated as F_{VCO}/128 assuming output duty cycle is 50%.

Device Pin-to-Pin Output Parameter Guidelines

The pin-to-pin numbers in Table 35 through Table 37 are based on the clock root placement in the center of the device. The actual pin-to-pin values will vary if the root placement selected is different. Consult the Vivado Design Suite timing report for the actual pin-to-pin values.

Table 35: **Global Clock Input to Output Delay Without MMCM (Near Clock Region)**

Symbol	Description	Device	Speed Grade and V_{CCINT} Operating Voltages				Units
			0.90V	0.85V		0.72V	
			-3	-2	-1	-2	
SSTL15 Global Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, *without* MMCM.							
T_{ICKOF}	Global clock input and output flip-flop *without* MMCM (near clock region).	XCVU3P	4.08	4.77	5.09	5.28	ns
		XCVU5P	4.08	4.77	5.09	5.28	ns
		XCVU7P	4.08	4.77	5.09	5.28	ns
		XCVU9P	4.08	4.77	5.09	5.28	ns
		XCVU11P	3.93	4.59	4.90	5.07	ns
		XCVU13P	3.93	4.59	4.90	5.07	ns

Notes:

1. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible I/O and CLB flip-flops are clocked by the global clock net in a single SLR.

Table 36: **Global Clock Input to Output Delay Without MMCM (Far Clock Region)**

Symbol	Description	Device	Speed Grade and V_{CCINT} Operating Voltages				Units
			0.90V	0.85V		0.72V	
			-3	-2	-1	-2	
SSTL15 Global Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, *without* MMCM.							
T_{ICKOF_FAR}	Global clock input and output flip-flop *without* MMCM (far clock region).	XCVU3P	4.53	5.33	5.69	5.92	ns
		XCVU5P	4.53	5.33	5.69	5.92	ns
		XCVU7P	4.53	5.33	5.69	5.92	ns
		XCVU9P	4.53	5.33	5.69	5.92	ns
		XCVU11P	4.10	4.79	5.11	5.28	ns
		XCVU13P	4.10	4.79	5.11	5.28	ns

Notes:

1. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible I/O and CLB flip-flops are clocked by the global clock net in a single SLR.

Table 37: **Global Clock Input to Output Delay With MMCM**

Symbol	Description	Device	Speed Grade and V_{CCINT} Operating Voltages				Units
			0.90V	0.85V		0.72V	
			-3	-2	-1	-2	
SSTL15 Global Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, with MMCM.							
$T_{ICKOFMMCMCC}$	Global clock input and output flip-flop *with* MMCM.	XCVU3P	1.80	1.80	1.94	2.34	ns
		XCVU5P	1.80	1.80	1.94	2.34	ns
		XCVU7P	1.80	1.80	1.94	2.34	ns
		XCVU9P	1.80	1.80	1.94	2.34	ns
		XCVU11P	1.56	1.56	1.68	2.07	ns
		XCVU13P	1.56	1.56	1.68	2.07	ns

Notes:

1. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible I/O and CLB flip-flops are clocked by the global clock net in a single SLR.
2. MMCM output jitter is already included in the timing calculation.

Package Parameter Guidelines

The parameters in this section provide the necessary values for calculating timing budgets for clock transmitter and receiver data-valid windows.

Table 40: **Package Skew**

Symbol	Description	Device	Package	Value	Units
PKGSKEW	Package Skew	XCVU3P	FFVC1517	197	ps
		XCVU5P	FLVA2104	175	ps
			FLVB2104	225	ps
			FLVC2104	216	ps
		XCVU7P	FLVA2104	175	ps
			FLVB2104	225	ps
			FLVC2104	216	ps
		XCVU9P	FLGA2104	217	ps
			FLGB2104	275	ps
			FLGC2104	299	ps
			FSGD2104	229	ps
			FLGA2577	149	ps
		XCVU11P	FLGF1924	180	ps
			FLGB2104	216	ps
			FLGC2104		ps
			FSGD2104		ps
			FLGA2577	154	ps
		XCVU13P	FHGA2104		ps
			FHGB2104	259	ps
			FHGC2104	182	ps
			FIGD2104		ps
			FLGA2577	140	ps

Notes:

1. These values represent the worst-case skew between any two SelectIO resources in the package: shortest delay to longest delay from die pad to ball.
2. Package delay information is available for these device/package combinations. This information can be used to deskew the package.

GTY Transceiver Specifications

The *UltraScale Architecture and Product Overview* (DS890) lists the Virtex UltraScale+ FPGAs that include the GTY transceivers.

GTY Transceiver DC Input and Output Levels

Table 41 summarizes the DC specifications of the GTY transceivers in Virtex UltraScale+ FPGAs. Consult the *UltraScale Architecture GTY Transceiver User Guide* (UG578) for further information.

Table 41: **GTY Transceiver DC Specifications**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
DV_{PPIN}	Differential peak-to-peak input voltage (external AC coupled)	>10.3125 Gb/s	150	–	1250	mV
		6.6 Gb/s to 10.3125 Gb/s	150	–	1250	mV
		≤ 6.6 Gb/s	150	–	2000	mV
V_{IN}	Single-ended input voltage. Voltage measured at the pin referenced to GND.	DC coupled $V_{MGTAVTT}$ = 1.2V	–400	–	$V_{MGTAVTT}$	mV
V_{CMIN}	Common mode input voltage	DC coupled $V_{MGTAVTT}$ = 1.2V	–	2/3 $V_{MGTAVTT}$	–	mV
D_{VPPOUT}	Differential peak-to-peak output voltage(1)	Transmitter output swing is set to 1010	800	–	–	mV
$V_{CMOUTDC}$	Common mode output voltage: DC coupled (equation based)	When remote RX is terminated to GND	$V_{MGTAVTT}/2 - D_{VPPOUT}/4$			mV
		When remote RX termination is floating	$V_{MGTAVTT} - D_{VPPOUT}/2$			mV
		When remote RX is terminated to V_{RX_TERM}(2)	$V_{MGTAVTT} - \frac{D_{VPPOUT}}{4} - \left(\frac{V_{MGTAVTT} - V_{RX\_TERM}}{2}\right)$			mV
$V_{CMOUTAC}$	Common mode output voltage: AC coupled	Equation based	$V_{MGTAVTT} - D_{VPPOUT}/2$			mV
R_{IN}	Differential input resistance		–	100	–	Ω
R_{OUT}	Differential output resistance		–	100	–	Ω
T_{OSKEW}	Transmitter output pair (TXP and TXN) intra-pair skew		–	–	10	ps
C_{EXT}	Recommended external AC coupling capacitor(3)		–	100	–	nF

Notes:

1. The output swing and pre-emphasis levels are programmable using the GTY transceiver attributes discussed in the *UltraScale Architecture GTY Transceiver User Guide* (UG578) and can result in values lower than reported in this table.
2. V_{RX_TERM} is the remote RX termination voltage.
3. Other values can be used as appropriate to conform to specific protocols and standards.

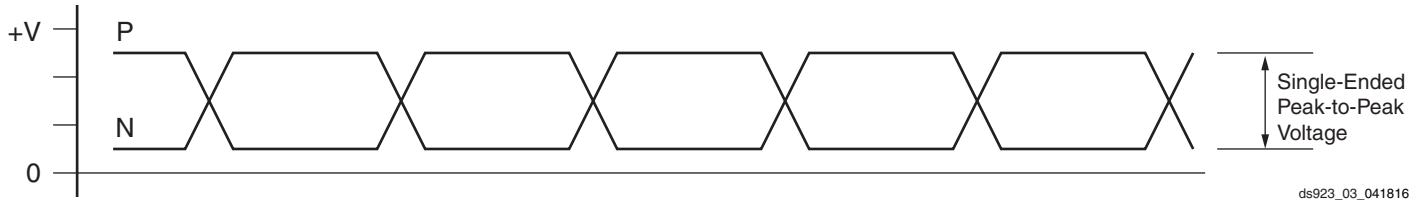

Figure 3: **Single-Ended Peak-to-Peak Voltage**

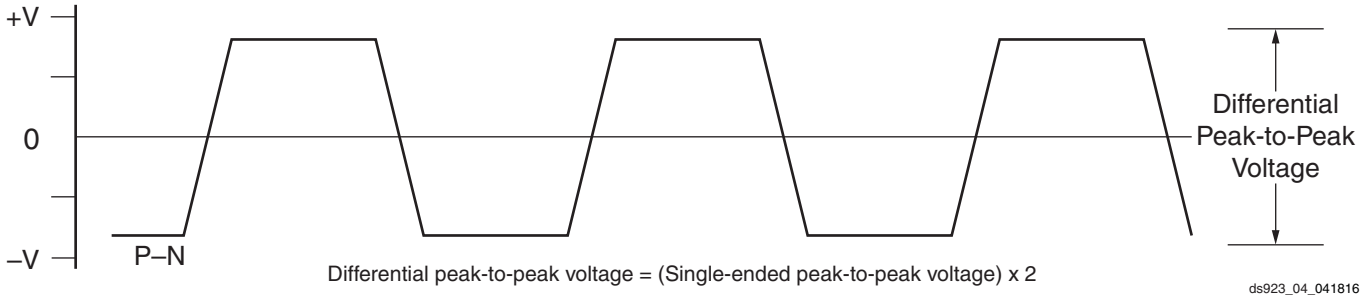

Figure 4: **Differential Peak-to-Peak Voltage**

Table 42 and Table 43 summarize the DC specifications of the clock input of the GTY transceivers in Virtex UltraScale+ FPGAs. Consult www.xilinx.com/products/technology/high-speed-serial for further details.

Table 42: **GTY Transceiver Clock DC Input Level Specification**

Symbol	DC Parameter	Min	Typ	Max	Units
V_{IDIFF}	Differential peak-to-peak input voltage	250	–	2000	mV
R_{IN}	Differential input resistance	–	100	–	Ω
C_{EXT}	Required external AC coupling capacitor	–	10	–	nF

Table 43: **GTY Transceiver Clock Output Level Specification**

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{OL}	Output high voltage for P and N	R_T = 100Ω across P and N signals	100	–	330	mV
V_{OH}	Output low voltage for P and N	R_T = 100Ω across P and N signals	500	–	700	mV
V_{DDOUT}	Differential output voltage (P–N), P = High (N–P), N = High	R_T = 100Ω across P and N signals	300	–	430	mV
V_{CMOUT}	Common mode voltage	R_T = 100Ω across P and N signals	300	–	500	mV

GTY Transceiver Switching Characteristics

Consult www.xilinx.com/products/technology/high-speed-serial for further information.

Table 44: **GTY Transceiver Performance**

Symbol	Description	Output Divider	Speed Grade and V_{CCINT} Operating Voltages								Units
			0.90V		0.85V				0.72V		
			-3		-2		-1		-2		
F_{GTYMAX}	GTY maximum line rate		32.75(1)		28.21(1)		25.7813(1)		28.21(1)		Gb/s
F_{GTYMIN}	GTY minimum line rate		0.5		0.5		0.5		0.5		Gb/s
			Min	Max	Min	Max	Min	Max	Min	Max	
$F_{GTYCRANGE}$	CPLL line rate range(2)	1	4.0	12.5	4.0	12.5	4.0	8.5	4.0	12.5	Gb/s
		2	2.0	6.25	2.0	6.25	2.0	4.25	2.0	6.25	Gb/s
		4	1.0	3.125	1.0	3.125	1.0	2.125	1.0	3.125	Gb/s
		8	0.5	1.5625	0.5	1.5625	0.5	1.0625	0.5	1.5625	Gb/s
		16	N/A								Gb/s
		32	N/A								Gb/s
			Min	Max	Min	Max	Min	Max	Min	Max	
$F_{GTYQRANGE1}$	QPLL0 line rate range(3)	1	19.6	32.75	19.6	28.21	19.6	25.7813	19.6	28.21	Gb/s
		1	9.8	16.375	9.8	16.375	9.8	12.5	9.8	16.375	Gb/s
		2	4.9	8.1875	4.9	8.1875	4.9	8.1875	4.9	8.1875	Gb/s
		4	2.45	4.09375	2.45	4.09375	2.45	4.09375	2.45	4.09375	Gb/s
		8	1.225	2.04688	1.225	2.04688	1.225	2.04688	1.225	2.04688	Gb/s
		16	0.6125	1.02344	0.6125	1.02344	0.6125	1.02344	0.6125	1.02344	Gb/s
			Min	Max	Min	Max	Min	Max	Min	Max	
$F_{GTYQRANGE2}$	QPLL1 line rate range(4)	1	16.0	26.0	16.0	26.0	19.6	25.7813	16.0	26.0	Gb/s
		1	8.0	13.0	8.0	13.0	8.0	12.5	8.0	13.0	Gb/s
		2	4.0	6.5	4.0	6.5	4.0	6.5	4.0	6.5	Gb/s
		4	2.0	3.25	2.0	3.25	2.0	3.25	2.0	3.25	Gb/s
		8	1.0	1.625	1.0	1.625	1.0	1.625	1.0	1.625	Gb/s
		16	0.5	0.8125	0.5	0.8125	0.5	0.8125	0.5	0.8125	Gb/s
			Min	Max	Min	Max	Min	Max	Min	Max	
$F_{CPLLRANGE}$	CPLL frequency range		2.0	6.25	2.0	6.25	2.0	4.25	2.0	6.25	GHz
$F_{QPLL0RANGE}$	QPLL0 frequency range		9.8	16.375	9.8	16.375	9.8	16.375	9.8	16.375	GHz
$F_{QPLL1RANGE}$	QPLL1 frequency range		8.0	13.0	8.0	13.0	8.0	13.0	8.0	13.0	GHz

Notes:

1. XCVU11P devices in the FLGF1924 package have a maximum GTY transceiver line rate of 16.3 Gb/s.
2. The values listed are the rounded results of the calculated equation (2 x CPLL_Frequency)/Output_Divider.
3. The values listed are the rounded results of the calculated equation (2 x QPLL0_Frequency)/Output_Divider.
4. The values listed are the rounded results of the calculated equation (2 x QPLL1_Frequency)/Output_Divider.

Table 50: **GTY Transceiver Transmitter Switching Characteristics *(Cont'd)***

Symbol	Description	Condition	Min	Typ	Max	Units
$T_{J3.20}$	Total jitter(3)(4)	3.20 Gb/s(5)	–	–	0.20	UI
$D_{J3.20}$	Deterministic jitter(3)(4)		–	–	0.10	UI
$T_{J2.5}$	Total jitter(3)(4)	2.5 Gb/s(6)	–	–	0.20	UI
$D_{J2.5}$	Deterministic jitter(3)(4)		–	–	0.10	UI
$T_{J1.25}$	Total jitter(3)(4)	1.25 Gb/s(7)	–	–	0.15	UI
$D_{J1.25}$	Deterministic jitter(3)(4)		–	–	0.06	UI
T_{J500}	Total jitter(3)(4)	500 Mb/s(8)	–	–	0.10	UI
D_{J500}	Deterministic jitter(3)(4)		–	–	0.03	UI

Notes:

1. Using same REFCLK input with TX phase alignment enabled for up to four consecutive transmitters (one fully populated GTY Quad) at maximum line rate.
2. Using QPLL_FBDIV = 40, 20-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
3. Using CPLL_FBDIV = 2, 20-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
4. All jitter values are based on a bit-error ratio of 10^{-12}.
5. CPLL frequency at 3.2 GHz and TXOUT_DIV = 2.
6. CPLL frequency at 2.5 GHz and TXOUT_DIV = 2.
7. CPLL frequency at 2.5 GHz and TXOUT_DIV = 4.
8. CPLL frequency at 2.0 GHz and TXOUT_DIV = 8.

Table 51: **GTY Transceiver Receiver Switching Characteristics**

Symbol	Description	Condition	Min	Typ	Max	Units
F_{GTYRX}	Serial data rate		0.500	–	F_{GTYMAX}	Gb/s
R_{XSST}	Receiver spread-spectrum tracking(1)	Modulated at 33 kHz	–5000	–	0	ppm
R_{XRL}	Run length (CID)		–	–	256	UI
$R_{XPPMTOL}$	Data/REFCLK PPM offset tolerance	Bit rates ≤ 6.6 Gb/s	–1250	–	1250	ppm
		Bit rates > 6.6 Gb/s and ≤ 8.0 Gb/s	–700	–	700	ppm
		Bit rates > 8.0 Gb/s	–200	–	200	ppm
SJ Jitter Tolerance(2)						
$J_{T\_SJ32.75}$	Sinusoidal jitter (QPLL)(3)	32.75 Gb/s	0.25	–	–	UI
$J_{T\_SJ28.21}$	Sinusoidal jitter (QPLL)(3)	28.21 Gb/s	0.30	–	–	UI
$J_{T\_SJ16.375}$	Sinusoidal jitter (QPLL)(3)	16.375 Gb/s	0.30	–	–	UI
$J_{T\_SJ15.0}$	Sinusoidal jitter (QPLL)(3)	15.0 Gb/s	0.30	–	–	UI
$J_{T\_SJ14.1}$	Sinusoidal jitter (QPLL)(3)	14.1 Gb/s	0.30	–	–	UI
$J_{T\_SJ13.1}$	Sinusoidal jitter (QPLL)(3)	13.1 Gb/s	0.30	–	–	UI
$J_{T\_SJ12.5}$	Sinusoidal jitter (QPLL)(3)	12.5 Gb/s	0.30	–	–	UI
$J_{T\_SJ11.3}$	Sinusoidal jitter (QPLL)(3)	11.3 Gb/s	0.30	–	–	UI
$J_{T\_SJ10.32\_QPLL}$	Sinusoidal jitter (QPLL)(3)	10.32 Gb/s	0.30	–	–	UI
$J_{T\_SJ10.32\_CPLL}$	Sinusoidal jitter (CPLL)(3)	10.32 Gb/s	0.30	–	–	UI
$J_{T\_SJ9.953\_QPLL}$	Sinusoidal jitter (QPLL)(3)	9.953 Gb/s	0.30	–	–	UI
$J_{T\_SJ9.953\_CPLL}$	Sinusoidal jitter (CPLL)(3)	9.953 Gb/s	0.30	–	–	UI
$J_{T\_SJ8.0}$	Sinusoidal jitter (CPLL)(3)	8.0 Gb/s	0.42	–	–	UI
$J_{T\_SJ6.6}$	Sinusoidal jitter (CPLL)(3)	6.6 Gb/s	0.44	–	–	UI
$J_{T\_SJ5.0}$	Sinusoidal jitter (CPLL)(3)	5.0 Gb/s	0.44	–	–	UI
$J_{T\_SJ4.25}$	Sinusoidal jitter (CPLL)(3)	4.25 Gb/s	0.44	–	–	UI
$J_{T\_SJ3.2}$	Sinusoidal jitter (CPLL)(3)	3.2 Gb/s(4)	0.45	–	–	UI
$J_{T\_SJ2.5}$	Sinusoidal jitter (CPLL)(3)	2.5 Gb/s(5)	0.30	–	–	UI
$J_{T\_SJ1.25}$	Sinusoidal jitter (CPLL)(3)	1.25 Gb/s(6)	0.30	–	–	UI
J_{T_SJ500}	Sinusoidal jitter (CPLL)(3)	500 Mb/s(7)	0.30	–	–	UI
SJ Jitter Tolerance with Stressed Eye(2)						
$J_{T\_TJSE3.2}$	Total jitter with stressed eye(8)	3.2 Gb/s	0.70	–	–	UI
$J_{T\_TJSE6.6}$		6.6 Gb/s	0.70	–	–	UI
$J_{T\_SJSE3.2}$	Sinusoidal jitter with stressed eye(8)	3.2 Gb/s	0.10	–	–	UI
$J_{T\_SJSE6.6}$		6.6 Gb/s	0.10	–	–	UI

Notes:

1. Using RXOUT_DIV = 1, 2, and 4.
2. All jitter values are based on a bit error ratio of 10^{-12}.
3. The frequency of the injected sinusoidal jitter is 80 MHz.
4. CPLL frequency at 3.2 GHz and RXOUT_DIV = 2.
5. CPLL frequency at 2.5 GHz and RXOUT_DIV = 2.
6. CPLL frequency at 2.5 GHz and RXOUT_DIV = 4.
7. CPLL frequency at 2.0 GHz and RXOUT_DIV = 8.
8. Composite jitter with RX equalizer enabled. DFE disabled.

GTY Transceiver Electrical Compliance

The *UltraScale Architecture GTY Transceiver User Guide* (UG578) contains recommended use modes that ensure compliance for the protocols listed in Table 52. The transceiver wizard provides the recommended settings for those use cases and for protocol specific characteristics.

Table 52: **GTY Transceiver Protocol List**

Protocol	Specification	Serial Rate (Gb/s)	Electrical Compliance
CAUI-4	IEEE 802.3-2012	25.78125	Compliant
28 Gb/s backplane	CEI-25G-LR	25–28.05	Compliant
Interlaken	OIF-CEI-6G, OIF-CEI-11GSR, OIF-CEI-28G-MR	4.25–25.78125	Compliant
100GBASE-KR4	IEEE 802.3bj-2014, CEI-25G-LR	25.78125	Compliant(1)
100GBASE-CR4	IEEE 802.3bj-2014, CEI-25G-LR	25.78125	Compliant(1)
50GBASE-KR4	IEEE 802.3by-2014, CEI-25G-LR	25.78125	Compliant(1)
50GBASE-CR4	IEEE 802.3by-2014, CEI-25G-LR	25.78125	Compliant(1)
25GBASE-KR4	IEEE 802.3by-2014, CEI-25G-LR	25.78125	Compliant(1)
25GBASE-CR4	IEEE 802.3by-2014, CEI-25G-LR	25.78125	Compliant(1)
OTU4 (OTL4.4) CFP2	OIF-CEI-28G-VSR	27.952493-32.75	Compliant
OTU4 (OTL4.4) CFP	OIF-CEI-11G-MR	11.18–13.1	Compliant
CAUI-10	IEEE 802.3-2012	10.3125	Compliant
nPPI	IEEE 802.3-2012	10.3125	Compliant
10GBASE-KR(2)	IEEE 802.3-2012	10.3125	Compliant
SFP+	SFF-8431 (SR and LR)	9.95328–11.10	Compliant
XFP	INF-8077i, revision 4.5	10.3125	Compliant
RXAUI	CEI-6G-SR	6.25	Compliant
XAUI	IEEE 802.3-2012	3.125	Compliant
1000BASE-X	IEEE 802.3-2012	1.25	Compliant
5.0G Ethernet	IEEE 802.3bx (PAR)	5	Compliant
2.5G Ethernet	IEEE 802.3bx (PAR)	2.5	Compliant
HiGig, HiGig+, HiGig2	IEEE 802.3-2012	3.74, 6.6	Compliant
QSGMII	QSGMII v1.2 (Cisco System, ENG-46158)	5	Compliant
OTU2	ITU G.8251	10.709225	Compliant
OTU4 (OTL4.10)	OIF-CEI-11G-SR	11.180997	Compliant
OC-3/12/48/192	GR-253-CORE	0.1555–9.956	Compliant
PCIe Gen1, 2, 3	PCI Express base 3.0	2.5, 5.0, and 8.0	Compliant
SDI(3)	SMPTE 424M-2006	0.27–2.97	Compliant
UHD-SDI(3)	SMPTE ST-2081 6G, SMPTE ST-2082 12G	6 and 12	Compliant
Hybrid memory cube (HMC)	HMC-15G-SR	10, 12.5, and 15.0	Compliant
MoSys bandwidth engine	CEI-11-SR and CEI-11-SR (overclocked)	10.3125, 15.5	Compliant
CPRI	CPRI_v_6_1_2014-07-01	0.6144–12.165	Compliant
Passive optical network (PON)	10G-EPON, 1G-EPON, NG-PON2, XG-PON, and 2.5G-PON	0.155–10.3125	Compliant
JESD204a/b	OIF-CEI-6G, OIF-CEI-11G	3.125–12.5	Compliant

Table 52: **GTY Transceiver Protocol List *(Cont'd)***

Protocol	Specification	Serial Rate (Gb/s)	Electrical Compliance
Serial RapidIO	RapidIO specification 3.1	1.25–10.3125	Compliant
DisplayPort (source only)	DP 1.2B CTS	1.62–5.4	Compliant(3)
Fibre channel	FC-PI-4	1.0625–14.025	Compliant
SATA Gen1, 2, 3	Serial ATA revision 3.0 specification	1.5, 3.0, and 6.0	Compliant
SAS Gen1, 2, 3	T10/BSR INCITS 519	3.0, 6.0, and 12.0	Compliant
SFI-5	OIF-SFI5-01.0	0.625 - 12.5	Compliant
Aurora	CEI-6G, CEI-11G-LR	All rates	Compliant

Notes:

1. 25 dB loss at Nyquist without FEC.
2. The transition time of the transmitter is faster than the IEEE Std 802.3-2012 specification.
3. This protocol requires external circuitry to achieve compliance.

Table 54: **Maximum Performance for Interlaken 6 x 25.78125 Gb/s and 6 x 28.21 Gb/s Protocol and Lane Logic Mode Designs**

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages										Units
		0.90V		0.85V				0.72V				
		-3(1)		-2(1)		-1		-2		-1		
$F_{RX\_SERDES\_CLK}$	Receive serializer/ deserializer clock	440.79		440.79		N/A		402.84		N/A		MHz
$F_{TX\_SERDES\_CLK}$	Transmit serializer/ deserializer clock	440.79		440.79		N/A		402.84		N/A		MHz
F_{DRP_CLK}	Dynamic reconfiguration port clock	250.00		250.00		N/A		250.00		N/A		MHz
		Min(2)	Max	Min(2)	Max	Min	Max	Min(2)	Max	Min	Max	
F_{CORE_CLK}	Interlaken core clock	412.50(3)	479.20	412.50(3)	479.20	N/A		412.50	429.69	N/A		MHz
F_{LBUS_CLK}	Interlaken local bus clock	300.00(4)	349.52	300.00(4)	349.52	N/A		300.00	349.52	N/A		MHz

Notes:

1. 6 x 28.21 mode is only supported in the -2 (V_{CCINT}=0.85V) and -3 (V_{CCINT}=0.90V) speed grades.
2. These are the minimum clock frequencies at the maximum lane performance.
3. The minimum value for CORE_CLK is 451.36 MHz for the 6 x 28.21 Gb/s protocol.
4. The minimum value for LBUS_CLK is 330.00 MHz for the 6 x 28.21 Gb/s protocol.

Table 55: **Maximum Performance for Interlaken 12 x 25.78125 Gb/s Lane Logic Only Mode Designs**

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages					Units
		0.90V	0.85V		0.72V		
		-3	-2	-1	-2	-1	
$F_{RX\_SERDES\_CLK}$	Receive serializer/ deserializer clock	402.84	402.84	N/A	N/A	N/A	MHz
$F_{TX\_SERDES\_CLK}$	Transmit serializer/ deserializer clock	402.84	402.84	N/A	N/A	N/A	MHz
F_{DRP_CLK}	Dynamic reconfiguration port clock	250.00	250.00	N/A	N/A	N/A	MHz
F_{CORE_CLK}	Interlaken core clock	412.50	412.50	N/A	N/A	N/A	MHz
F_{LBUS_CLK}	Interlaken local bus clock	349.52	349.52	N/A	N/A	N/A	MHz

Table 61: **Configuration Switching Characteristics *(Cont'd)***

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages				Units
		0.90V	0.85V		0.72V	
		-3	-2	-1	-2	
DNA Port Switching						
F_{DNACK}	DNA port frequency.	200	200	200	175	MHz, Max
STARTUPE3 Ports						
$T_{USRCCLKO}$	STARTUPE3 USRCCLKO input port to CCLK pin output delay.	0.25/ 6.00	0.25/ 6.50	0.25/ 7.50	0.25/ 9.00	ns, Min/Max
T_{DO}	DO[3:0] ports to D03-D00 pins output delay.	0.25/ 6.70	0.25/ 7.70	0.25/ 8.40	0.25/ 10.00	ns, Min/Max
T_{DTS}	DTS[3:0] ports to D03-D00 pins 3-state delays.	0.25/ 6.70	0.25/ 7.70	0.25/ 8.40	0.25/ 10.00	ns, Min/Max
T_{FCSBO}	FCSBO port to FCS_B pin output delay.	0.25/ 6.90	0.25/ 7.50	0.25/ 8.40	0.25/ 9.80	ns, Min/Max
T_{FCSBTS}	FCSBTS port to FCS_B pin 3-state delay.	0.25/ 6.90	0.25/ 7.50	0.25/ 8.40	0.25/ 9.80	ns, Min/Max
$T_{USRDONEO}$	USRDONEO port to DONE pin output delay.	0.25/ 8.60	0.25/ 9.40	0.25/ 10.50	0.25/ 12.10	ns, Min/Max
$T_{USRDONETS}$	USRDONETS port to DONE pin 3-state delay.	0.25/ 8.60	0.25/ 9.40	0.25/ 10.50	0.25/ 12.10	ns, Min/Max
T_{DI}	D03-D00 pins to DI[3:0] ports input delay.	0.5/ 2.6	0.5/ 3.1	0.5/ 3.5	0.5/ 4.0	ns, Min/Max
$F_{CFGMCLK}$	STARTUPE3 CFGMCLK output frequency.	50	50	50	50	MHz, Typ
$F_{CFGMCLKTOL}$	STARTUPE3 CFGMCLK output frequency tolerance.	±15	±15	±15	±15	%, Max
T_{DCI_MATCH}	Specifies a stall in the startup cycle until the digitally controlled impedance (DCI) match signals are asserted.	4	4	4	4	ms, Max

Notes:

1. When the CCLK is sourced from the EMCCLK pin with a divide-by-one setting, the external EMCCLK must meet this duty-cycle requirement.