Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	49260
Number of Logic Elements/Cells	862050
Total RAM Bits	118067200
Number of I/O	520
Number of Gates	-
Voltage - Supply	0.873V ~ 0.927V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 100°C (TJ)
Package / Case	1517-BBGA, FCBGA
Supplier Device Package	1517-FCBGA (40x40)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xcvu3p-3ffvc1517e

Recommended Operating Conditions

Table 2: **Recommended Operating Conditions(1)(2)**

Symbol	Description	Min	Typ	Max	Units
FPGA Logic					
V_{CCINT}	Internal supply voltage.	0.825	0.850	0.876	V
	For -2LE (V_{CCINT} = 0.72V) devices: internal supply voltage.	0.698	0.720	0.742	V
	For -3E devices: internal supply voltage.	0.873	0.900	0.927	V
V_{CCINT_IO}(3)	Internal supply voltage for the I/O banks.	0.825	0.850	0.876	V
	For -2LE devices (V_{CCINT} = 0.85V): internal supply voltage for the I/O banks.	0.825	0.850	0.876	V
	For -3E devices: internal supply voltage for the I/O banks.	0.873	0.900	0.927	V
V_{CCBRAM}	Block RAM supply voltage.	0.825	0.850	0.876	V
	For -3E devices: block RAM supply voltage.	0.873	0.900	0.927	V
V_{CCAUX}	Auxiliary supply voltage.	1.746	1.800	1.854	V
V_{CCO}(4)(5)	Supply voltage for I/O banks.	0.950	–	1.900	V
V_{CCAUX_IO}(6)	Auxiliary I/O supply voltage.	1.746	1.800	1.854	V
V_{IN}(7)	I/O input voltage.	–0.200	–	V_{CCO} + 0.200	V
I_{IN}(8)	Maximum current through any pin in a powered or unpowered bank when forward biasing the clamp diode.	–	–	10	mA
V_{BATT}(9)	Battery voltage.	1.000	–	1.890	V
GTY Transceiver					
$V_{MGTAVCC}$(10)	Analog supply voltage for the GTY transceiver.	0.873	0.900	0.927	V
$V_{MGTAVTT}$(10)	Analog supply voltage for the GTY transmitter and receiver termination circuits.	1.164	1.20	1.236	V
$V_{MGTVCCAUX}$(10)	Auxiliary analog QPLL voltage supply for the transceivers.	1.746	1.80	1.854	V
$V_{MGTAVTTRCAL}$(10)	Analog supply voltage for the resistor calibration circuit of the GTY transceiver column.	1.164	1.20	1.236	V

Table 3: **DC Characteristics Over Recommended Operating Conditions *(Cont'd)***

Symbol	Description	Min	Typ(1)	Max	Units
Uncalibrated programmable on-die termination in I/O banks (measured per JEDEC specification)					
$R^{(9)}$	Thevenin equivalent resistance of programmable input termination to $V_{CCO}/2$ where ODT = RTT_40.	–50%	40	+50%	Ω
	Thevenin equivalent resistance of programmable input termination to $V_{CCO}/2$ where ODT = RTT_48.	–50%	48	+50%	Ω
	Thevenin equivalent resistance of programmable input termination to $V_{CCO}/2$ where ODT = RTT_60.	–50%	60	+50%	Ω
	Programmable input termination to V_{CCO} where ODT = RTT_40.	–50%	40	+50%	Ω
	Programmable input termination to V_{CCO} where ODT = RTT_48.	–50%	48	+50%	Ω
	Programmable input termination to V_{CCO} where ODT = RTT_60.	–50%	60	+50%	Ω
	Programmable input termination to V_{CCO} where ODT = RTT_120.	–50%	120	+50%	Ω
	Programmable input termination to V_{CCO} where ODT = RTT_240.	–50%	240	+50%	Ω
Internal V_{REF}	50% V_{CCO}	V_{CCO} x 0.49	V_{CCO} x 0.50	V_{CCO} x 0.51	V
	70% V_{CCO}	V_{CCO} x 0.69	V_{CCO} x 0.70	V_{CCO} x 0.71	V
Differential termination	Programmable differential termination (TERM_100) for the I/O banks.	–35%	100	+35%	Ω
n	Temperature diode ideality factor.	–	1.026	–	–
r	Temperature diode series resistance.	–	2	–	Ω

Notes:

1. Typical values are specified at nominal voltage, 25°C.
2. For the I/O banks with a V_{CCO} of 1.8V and separated V_{CCO} and V_{CCAUX_IO} power supplies, the I_L maximum current is 70 µA.
3. This measurement represents the die capacitance at the pad, not including the package.
4. Maximum value specified for worst case process at 25°C.
5. I_{BATT} is measured when the battery-backed RAM (BBRAM) is enabled.
6. Do not program eFUSE during device configuration (e.g., during configuration, during configuration readback, or when readback CRC is active).
7. If VRP resides at a different bank (DCI cascade), the range increases to ±15%.
8. VRP resistor tolerance is (240Ω ±1%)
9. On-die input termination resistance, for more information see the *UltraScale Architecture SelectIO Resources User Guide* (UG571).

Table 5: **Typical Quiescent Supply Current(1)(2)(3) *(Cont'd)***

Symbol	Description	Device	Speed Grade and V_{CCINT} Operating Voltages				Units
			0.90V	0.85V		0.72V	
			-3	-2	-1	-2	
I_{CCAUX_IOQ}	Quiescent V_{CCAUX_IO} supply current.	XCVU3P	62	62	62	62	mA
		XCVU5P	124	124	124	124	mA
		XCVU7P	124	124	124	124	mA
		XCVU9P	187	187	187	187	mA
		XCVU11P	79	79	79	79	mA
		XCVU13P	105	105	105	105	mA
$I_{CCBRAMQ}$	Quiescent V_{CCBRAM} supply current.	XCVU3P	45	43	43	43	mA
		XCVU5P	90	85	85	85	mA
		XCVU7P	90	85	85	85	mA
		XCVU9P	134	128	128	128	mA
		XCVU11P	130	124	124	124	mA
		XCVU13P	174	165	165	165	mA

Notes:

1. Typical values are specified at nominal voltage, 85°C junction temperatures (T_j) with single-ended SelectIO™ resources.
2. Typical values are for blank configured devices with no output current loads, no active input pull-up resistors, all I/O pins are 3-state and floating.
3. Use the Xilinx Power Estimator (XPE) spreadsheet tool (download at www.xilinx.com/power) to estimate static power consumption for conditions other than those specified.

Power-On/Off Power Supply Sequencing

The recommended power-on sequence is V_{CCINT}, V_{CCINT_IO}/V_{CCBRAM}, V_{CCAUX}/V_{CCAUX_IO}, and V_{CCO} to achieve minimum current draw and ensure that the I/Os are 3-stated at power-on. The recommended power-off sequence is the reverse of the power-on sequence. If V_{CCINT} and V_{CCINT_IO}/V_{CCBRAM} have the same recommended voltage levels, they can be powered by the same supply and ramped simultaneously. V_{CCINT_IO} must be connected to V_{CCBRAM}. If V_{CCAUX}/V_{CCAUX_IO} and V_{CCO} have the same recommended voltage levels, they can be powered by the same supply and ramped simultaneously. V_{CCAUX} and V_{CCAUX_IO} must be connected together. V_{CCADC} and V_{REF} can be powered at any time and have no power-up sequencing requirements.

The recommended power-on sequence to achieve minimum current draw for the GTY transceivers are V_{CCINT}, $V_{MGTAVCC}$, $V_{MGTAVTT}$ OR $V_{MGTAVCC}$, V_{CCINT}, $V_{MGTAVTT}$. There is no recommended sequencing for $V_{MGTVCCAUX}$. Both $V_{MGTAVCC}$ and V_{CCINT} can be ramped simultaneously. The recommended power-off sequence is the reverse of the power-on sequence to achieve minimum current draw.

If these recommended sequences are not met, current drawn from $V_{MGTAVTT}$ can be higher than specifications during power-up and power-down.

Table 10: **Differential SelectIO DC Input and Output Levels**

I/O Standard	V_{ICM} (V)(1)			V_{ID}(V)(2)			V_{ILHS}(3)	V_{IHHS}(3)	V_{OCM}(V)(4)			V_{OD}(V)(5)		
	Min	Typ	Max	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Typ	Max
SUB_LVDS	0.500	0.900	1.300	0.070	–	–	–	–	0.700	0.900	1.100	0.100	0.150	0.200
SLVS_400_18	0.070	0.200	0.330	0.140	–	0.450	–	–	–	–	–	–	–	–
MIPI_DPHY_DCI_HS(7)	0.070	–	0.330	0.070	–	–	–0.040	0.460	0.150	0.200	0.250	0.140	0.200	0.270

Notes:

1. V_{ICM} is the input common mode voltage.
2. V_{ID} is the input differential voltage (Q – $\overline{Q}$).
3. V_{IHHS} and V_{ILHS} are the single-ended input high and low voltages, respectively.
4. V_{OCM} is the output common mode voltage.
5. V_{OD} is the output differential voltage (Q – $\overline{Q}$).
6. LVDS is specified in Table 15.
7. High-speed option for MIPI_DPHY_DCI. The V_{ID} maximum is aligned with the standard's specification. A higher V_{ID} is acceptable as long as the V_{IN} specification is also met.

Table 11: **Complementary Differential SelectIO DC Input and Output Levels for the I/O Banks(1)**

I/O Standard	V_{ICM} (V)(2)			V_{ID} (V)(3)		V_{OL} (V)(4)	V_{OH} (V)(5)	I_{OL}	I_{OH}
	Min	Typ	Max	Min	Max	Max	Min	mA	mA
DIFF_HSTL_I	0.680	V_{CCO}/2	(V_{CCO}/2) + 0.150	0.100	–	0.400	V_{CCO} – 0.400	5.8	–5.8
DIFF_HSTL_I_12	0.400 x V_{CCO}	V_{CCO}/2	0.600 x V_{CCO}	0.100	–	0.250 x V_{CCO}	0.750 x V_{CCO}	4.1	–4.1
DIFF_HSTL_I_18	(V_{CCO}/2) – 0.175	V_{CCO}/2	(V_{CCO}/2) + 0.175	0.100	–	0.400	V_{CCO} – 0.400	6.2	–6.2
DIFF_HSUL_12	(V_{CCO}/2) – 0.120	V_{CCO}/2	(V_{CCO}/2) + 0.120	0.100	–	20% V_{CCO}	80% V_{CCO}	0.1	–0.1
DIFF_SSTL12	(V_{CCO}/2) – 0.150	V_{CCO}/2	(V_{CCO}/2) + 0.150	0.100	–	(V_{CCO}/2) – 0.150	(V_{CCO}/2) + 0.150	8.0	–8.0
DIFF_SSTL135	(V_{CCO}/2) – 0.150	V_{CCO}/2	(V_{CCO}/2) + 0.150	0.100	–	(V_{CCO}/2) – 0.150	(V_{CCO}/2) + 0.150	9.0	–9.0
DIFF_SSTL15	(V_{CCO}/2) – 0.175	V_{CCO}/2	(V_{CCO}/2) + 0.175	0.100	–	(V_{CCO}/2) – 0.175	(V_{CCO}/2) + 0.175	10.0	–10.0
DIFF_SSTL18_I	(V_{CCO}/2) – 0.175	V_{CCO}/2	(V_{CCO}/2) + 0.175	0.100	–	(V_{CCO}/2) – 0.470	(V_{CCO}/2) + 0.470	7.0	–7.0

Notes:

1. DIFF_POD10 and DIFF_POD12 HP I/O bank specifications are shown in Table 12, Table 13, and Table 14.
2. V_{ICM} is the input common mode voltage.
3. V_{ID} is the input differential voltage.
4. V_{OL} is the single-ended low-output voltage.
5. V_{OH} is the single-ended high-output voltage.

Table 12: **DC Input Levels for Differential POD10 and POD12 I/O Standards(1)(2)**

I/O Standard	V_{ICM} (V)			V_{ID} (V)	
	Min	Typ	Max	Min	Max
DIFF_POD10	0.63	0.70	0.77	0.14	–
DIFF_POD12	0.76	0.84	0.92	0.16	–

Notes:

1. Tested according to relevant specifications.
2. Standards specified using the default I/O standard configuration. For details, see the *UltraScale Architecture SelectIO Resources User Guide* (UG571).

Production Silicon and Software Status

In some cases, a particular family member (and speed grade) is released to production before a speed specification is released with the correct label (Advance, Preliminary, Production). Any labeling discrepancies are corrected in subsequent speed specification releases.

Table 18 lists the production released Virtex UltraScale+ FPGA, speed grade, and the minimum corresponding supported speed specification version and Vivado software revisions. The Vivado software and speed specifications listed are the minimum releases required for production. All subsequent releases of software and speed specifications are valid.

Table 18: **Virtex UltraScale+ FPGA Device Production Software and Speed Specification Release**

Device	Speed Grade and V_{CCINT} Operating Voltages				
	0.90V	0.85V			0.72V
	-3	-2	-1	-2L	-2L
XCVU3P		Vivado tools 2017.1 v1.10			
XCVU5P					
XCVU7P					
XCVU9P					
XCVU11P					
XCVU13P					

Notes:

1. Blank entries indicate a device and/or speed grade in Advance or Preliminary status.

FPGA Logic Performance Characteristics

This section provides the performance characteristics of some common functions and designs implemented in Virtex UltraScale+ FPGAs. These values are subject to the same guidelines as the AC Switching Characteristics, page 13.

Table 19: **LVDS Component Mode Performance**

Description	Speed Grade and V_{CCINT} Operating Voltages								Units
	0.90V		0.85V				0.72V		
	-3		-2		-1		-2		
	Min	Max	Min	Max	Min	Max	Min	Max	
LVDS TX DDR (OSERDES 4:1, 8:1)	0	1250	0	1250	0	1250	0	1250	Mb/s
LVDS TX SDR (OSERDES 2:1, 4:1)	0	625	0	625	0	625	0	625	Mb/s
LVDS RX DDR (ISERDES 1:4, 1:8)(1)	0	1250	0	1250	0	1250	0	1250	Mb/s
LVDS RX SDR (ISERDES 1:2, 1:4)(1)	0	625	0	625	0	625	0	625	Mb/s

Notes:

1. LVDS receivers are typically bounded with certain applications to achieve maximum performance. Package skews are not included and should be removed through PCB routing.

Table 20: **LVDS Native Mode Performance(1)(2)**

Description	DATA_WIDTH	Speed Grade and V_{CCINT} Operating Voltages								Units
		0.90V		0.85V				0.72V		
		-3		-2		-1		-2		
		Min	Max	Min	Max	Min	Max	Min	Max	
LVDS TX DDR (TX_BITSLICE)	4	375	1600	375	1600	375	1260	375	1400	Mb/s
	8	375	1600	375	1600	375	1260	375	1600	Mb/s
LVDS TX SDR (TX_BITSLICE)	4	187.5	800	187.5	800	187.5	630	187.5	700	Mb/s
	8	187.5	800	187.5	800	187.5	630	187.5	800	Mb/s
LVDS RX DDR (RX_BITSLICE)(3)	4	375	1600	375	1600	375	1260	375	1400	Mb/s
	8	375	1600	375	1600	375	1260	375	1600	Mb/s
LVDS RX SDR (RX_BITSLICE)(3)	4	187.5	800	187.5	800	187.5	630	187.5	700	Mb/s
	8	187.5	800	187.5	800	187.5	630	187.5	800	Mb/s

Notes:

1. Native mode is supported through the High-Speed SelectIO Interface Wizard available with the Vivado Design Suite.
2. PLL settings can restrict the minimum allowable data rate. For example, when using the PLL with CLKOUTPHY_MODE = VCO_HALF the minimum frequency is PLL_FVCOMIN/2.
3. LVDS receivers are typically bounded with certain applications to achieve maximum performance. Package skews are not included and should be removed through PCB routing.

Table 21: **MIPI D-PHY Performance**

Description	Speed Grade and V_{CCINT} Operating Voltages				Units
	0.90V	0.85V		0.72V	
	-3	-2	-1	-2	
MIPI D-PHY transmitter or receiver.	1500	1500	1260	1260	Mb/s

Table 22: **LVDS Native-Mode 1000BASE-X Support(1)**

Description	Speed Grade and V_{CCINT} Operating Voltages			
	0.90V	0.85V		0.72V
	-3	-2	-1	-2
1000BASE-X	Yes			

Notes:
1. 1000BASE-X support is based on the *IEEE Standard for CSMA/CD Access Method and Physical Layer Specifications* (IEEE Std 802.3-2008).

Table 23 provides the maximum data rates for applicable memory standards using the Virtex UltraScale+ FPGA memory PHY. Refer to Memory Interfaces for the complete list of memory interface standards supported and detailed specifications. The final performance of the memory interface is determined through a complete design implemented in the Vivado Design Suite, following guidelines in the *UltraScale Architecture PCB Design Guide* (UG583), electrical analysis, and characterization of the system.

Table 23: **Maximum Physical Interface (PHY) Rate for Memory Interfaces**

Memory Standard	DRAM Type	Speed Grade and V_{CCINT} Operating Voltages				Units
		0.90V	0.85V		0.72V	
		-3	-2	-1	-2	
DDR4	Single rank component	2666	2666	2400	2400	Mb/s
	1 rank DIMM(1)(2)	2400	2400	2133	2133	Mb/s
	2 rank DIMM(1)(3)	2133	2133	1866	1866	Mb/s
	4 rank DIMM(1)(4)	1600	1600	1333	1333	Mb/s
DDR3	Single rank component	2133	2133	2133	2133	Mb/s
	1 rank DIMM(1)(2)	1866	1866	1866	1866	Mb/s
	2 rank DIMM(1)(3)	1600	1600	1600	1600	Mb/s
	4 rank DIMM(1)(4)	1066	1066	1066	1066	Mb/s
DDR3L	Single rank component	1866	1866	1866	1866	Mb/s
	1 rank DIMM(1)(2)	1600	1600	1600	1600	Mb/s
	2 rank DIMM(1)(3)	1333	1333	1333	1333	Mb/s
	4 rank DIMM(1)(4)	800	800	800	800	Mb/s
QDR II+	Single rank component(5)	633	633	600	600	MHz
RLDRAM 3	Single rank component	1200	1200	1066	1066	MHz
QDR IV XP	Single rank component	1066	1066	1066	933	MHz
LPDDR3	Single rank component	1600	1600	1600	1600	Mb/s

Notes:
1. Dual in-line memory module (DIMM) includes RDIMM, SODIMM, UDIMM, and LRDIMM.
2. Includes: 1 rank 1 slot, DDP 2 rank, LRDIMM 2 or 4 rank 1 slot.
3. Includes: 2 rank 1 slot, 1 rank 2 slot, LRDIMM 2 rank 2 slot.
4. Includes: 2 rank 2 slot, 4 rank 1 slot.
5. The QDRII+ performance specifications are for burst-length 4 (BL = 4) implementations.

FPGA Logic Switching Characteristics

Table 24, high-performance IOB (HP), summarizes the values of standard-specific data input delay adjustments, output delays terminating at pads (based on standard) and 3-state delays.

- $T_{INBUF\_DELAY\_PAD\_I}$ is the delay from IOB pad through the input buffer to the I-pin of an IOB pad. The delay varies depending on the capability of the SelectIO input buffer.
- $T_{OUTBUF\_DELAY\_O\_PAD}$ is the delay from the O pin to the IOB pad through the output buffer of an IOB pad. The delay varies depending on the capability of the SelectIO output buffer.
- $T_{OUTBUF\_DELAY\_TD\_PAD}$ is the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is disabled. The delay varies depending on the SelectIO capability of the output buffer. In HP I/O banks, the internal DCI termination turn-on time is always faster than $T_{OUTBUF\_DELAY\_TD\_PAD}$ when the DCITERMDISABLE pin is used.

IOB High Performance (HP) Switching Characteristics

Table 24: **IOB High Performance (HP) Switching Characteristics**

I/O Standards	$T_{INBUF\_DELAY\_PAD\_I}$				$T_{OUTBUF\_DELAY\_O\_PAD}$				$T_{OUTBUF\_DELAY\_TD\_PAD}$				Units
	0.90V	0.85V		0.72V	0.90V	0.85V		0.72V	0.90V	0.85V		0.72V	
	-3	-2	-1	-2	-3	-2	-1	-2	-3	-2	-1	-2	
DIFF_HSTL_I_12_F	0.394	0.394	0.402	0.394	0.423	0.423	0.443	0.423	0.553	0.553	0.582	0.553	ns
DIFF_HSTL_I_12_M	0.394	0.394	0.402	0.394	0.552	0.552	0.583	0.552	0.641	0.641	0.679	0.641	ns
DIFF_HSTL_I_12_S	0.394	0.394	0.402	0.394	0.752	0.752	0.800	0.752	0.813	0.813	0.868	0.813	ns
DIFF_HSTL_I_18_F	0.319	0.319	0.339	0.319	0.456	0.456	0.474	0.456	0.576	0.576	0.606	0.576	ns
DIFF_HSTL_I_18_M	0.319	0.319	0.339	0.319	0.570	0.570	0.603	0.570	0.653	0.653	0.692	0.653	ns
DIFF_HSTL_I_18_S	0.319	0.319	0.339	0.319	0.782	0.782	0.834	0.782	0.816	0.816	0.871	0.816	ns
DIFF_HSTL_I_DCI_12_F	0.394	0.394	0.402	0.394	0.406	0.406	0.429	0.406	0.534	0.534	0.564	0.534	ns
DIFF_HSTL_I_DCI_12_M	0.394	0.394	0.402	0.394	0.557	0.557	0.587	0.557	0.653	0.653	0.694	0.653	ns
DIFF_HSTL_I_DCI_12_S	0.394	0.394	0.402	0.394	0.755	0.755	0.806	0.755	0.842	0.842	0.907	0.842	ns
DIFF_HSTL_I_DCI_18_F	0.323	0.323	0.339	0.323	0.445	0.445	0.461	0.445	0.566	0.566	0.595	0.566	ns
DIFF_HSTL_I_DCI_18_M	0.323	0.323	0.339	0.323	0.555	0.555	0.586	0.555	0.643	0.643	0.684	0.643	ns
DIFF_HSTL_I_DCI_18_S	0.323	0.323	0.339	0.323	0.762	0.762	0.818	0.762	0.836	0.836	0.900	0.836	ns
DIFF_HSTL_I_DCI_F	0.397	0.397	0.417	0.397	0.431	0.431	0.445	0.431	0.555	0.555	0.575	0.555	ns
DIFF_HSTL_I_DCI_M	0.397	0.397	0.417	0.397	0.553	0.553	0.583	0.553	0.644	0.644	0.684	0.644	ns
DIFF_HSTL_I_DCI_S	0.397	0.397	0.417	0.397	0.767	0.767	0.823	0.767	0.848	0.848	0.912	0.848	ns
DIFF_HSTL_I_F	0.404	0.404	0.417	0.404	0.423	0.423	0.443	0.423	0.549	0.549	0.581	0.549	ns
DIFF_HSTL_I_M	0.404	0.404	0.417	0.404	0.555	0.555	0.586	0.555	0.640	0.640	0.677	0.640	ns
DIFF_HSTL_I_S	0.404	0.404	0.417	0.404	0.767	0.767	0.818	0.767	0.811	0.811	0.866	0.811	ns
DIFF_HSUL_12_DCI_F	0.381	0.381	0.400	0.381	0.425	0.425	0.443	0.425	0.558	0.558	0.586	0.558	ns
DIFF_HSUL_12_DCI_M	0.381	0.381	0.400	0.381	0.557	0.557	0.587	0.557	0.653	0.653	0.694	0.653	ns
DIFF_HSUL_12_DCI_S	0.381	0.381	0.400	0.381	0.737	0.737	0.787	0.737	0.822	0.822	0.885	0.822	ns
DIFF_HSUL_12_F	0.394	0.394	0.402	0.394	0.412	0.412	0.430	0.412	0.538	0.538	0.566	0.538	ns
DIFF_HSUL_12_M	0.394	0.394	0.402	0.394	0.552	0.552	0.583	0.552	0.641	0.641	0.679	0.641	ns
DIFF_HSUL_12_S	0.394	0.394	0.402	0.394	0.752	0.752	0.800	0.752	0.813	0.813	0.868	0.813	ns

Table 24: **IOB High Performance (HP) Switching Characteristics *(Cont'd)***

I/O Standards	$T_{INBUF\_DELAY\_PAD\_I}$				$T_{OUTBUF\_DELAY\_O\_PAD}$				$T_{OUTBUF\_DELAY\_TD\_PAD}$				Units
	0.90V	0.85V		0.72V	0.90V	0.85V		0.72V	0.90V	0.85V		0.72V	
	-3	-2	-1	-2	-3	-2	-1	-2	-3	-2	-1	-2	
HSLVDCI_18_S	0.424	0.424	0.447	0.424	0.761	0.761	0.817	0.761	0.836	0.836	0.900	0.836	ns
HSTL_I_12_F	0.378	0.378	0.399	0.378	0.423	0.423	0.443	0.423	0.553	0.553	0.582	0.553	ns
HSTL_I_12_M	0.378	0.378	0.399	0.378	0.551	0.551	0.582	0.551	0.642	0.642	0.679	0.642	ns
HSTL_I_12_S	0.378	0.378	0.399	0.378	0.750	0.750	0.799	0.750	0.813	0.813	0.868	0.813	ns
HSTL_I_18_F	0.322	0.322	0.339	0.322	0.456	0.456	0.474	0.456	0.576	0.576	0.606	0.576	ns
HSTL_I_18_M	0.322	0.322	0.339	0.322	0.569	0.569	0.602	0.569	0.653	0.653	0.692	0.653	ns
HSTL_I_18_S	0.322	0.322	0.339	0.322	0.781	0.781	0.833	0.781	0.816	0.816	0.871	0.816	ns
HSTL_I_DCI_12_F	0.378	0.378	0.399	0.378	0.406	0.406	0.429	0.406	0.534	0.534	0.564	0.534	ns
HSTL_I_DCI_12_M	0.378	0.378	0.399	0.378	0.556	0.556	0.586	0.556	0.654	0.654	0.694	0.654	ns
HSTL_I_DCI_12_S	0.378	0.378	0.399	0.378	0.754	0.754	0.803	0.754	0.842	0.842	0.907	0.842	ns
HSTL_I_DCI_18_F	0.321	0.321	0.339	0.321	0.445	0.445	0.461	0.445	0.566	0.566	0.595	0.566	ns
HSTL_I_DCI_18_M	0.321	0.321	0.339	0.321	0.554	0.554	0.585	0.554	0.643	0.643	0.684	0.643	ns
HSTL_I_DCI_18_S	0.321	0.321	0.339	0.321	0.761	0.761	0.817	0.761	0.836	0.836	0.900	0.836	ns
HSTL_I_DCI_F	0.393	0.393	0.415	0.393	0.431	0.431	0.445	0.431	0.555	0.555	0.575	0.555	ns
HSTL_I_DCI_M	0.393	0.393	0.415	0.393	0.552	0.552	0.581	0.552	0.644	0.644	0.684	0.644	ns
HSTL_I_DCI_S	0.393	0.393	0.415	0.393	0.766	0.766	0.821	0.766	0.847	0.847	0.912	0.847	ns
HSTL_I_F	0.378	0.378	0.399	0.378	0.423	0.423	0.443	0.423	0.549	0.549	0.581	0.549	ns
HSTL_I_M	0.378	0.378	0.399	0.378	0.554	0.554	0.585	0.554	0.640	0.640	0.677	0.640	ns
HSTL_I_S	0.378	0.378	0.399	0.378	0.766	0.766	0.816	0.766	0.811	0.811	0.866	0.811	ns
HSUL_12_DCI_F	0.378	0.378	0.399	0.378	0.425	0.425	0.443	0.425	0.558	0.558	0.586	0.558	ns
HSUL_12_DCI_M	0.378	0.378	0.399	0.378	0.556	0.556	0.586	0.556	0.654	0.654	0.694	0.654	ns
HSUL_12_DCI_S	0.378	0.378	0.399	0.378	0.736	0.736	0.784	0.736	0.821	0.821	0.886	0.821	ns
HSUL_12_F	0.378	0.378	0.399	0.378	0.412	0.412	0.430	0.412	0.538	0.538	0.566	0.538	ns
HSUL_12_M	0.378	0.378	0.399	0.378	0.551	0.551	0.582	0.551	0.642	0.642	0.679	0.642	ns
HSUL_12_S	0.378	0.378	0.399	0.378	0.750	0.750	0.799	0.750	0.813	0.813	0.868	0.813	ns
LVCMOS12_F_2	0.512	0.512	0.555	0.512	0.672	0.672	0.692	0.672	0.898	0.898	0.922	0.898	ns
LVCMOS12_F_4	0.512	0.512	0.555	0.512	0.504	0.504	0.521	0.504	0.664	0.664	0.693	0.664	ns
LVCMOS12_F_6	0.512	0.512	0.555	0.512	0.485	0.485	0.507	0.485	0.634	0.634	0.669	0.634	ns
LVCMOS12_F_8	0.512	0.512	0.555	0.512	0.465	0.465	0.489	0.465	0.611	0.611	0.666	0.611	ns
LVCMOS12_M_2	0.512	0.512	0.555	0.512	0.708	0.708	0.727	0.708	0.916	0.916	0.945	0.916	ns
LVCMOS12_M_4	0.512	0.512	0.555	0.512	0.550	0.550	0.573	0.550	0.664	0.664	0.690	0.664	ns
LVCMOS12_M_6	0.512	0.512	0.555	0.512	0.527	0.527	0.554	0.527	0.622	0.622	0.652	0.622	ns
LVCMOS12_M_8	0.512	0.512	0.555	0.512	0.540	0.540	0.571	0.540	0.614	0.614	0.649	0.614	ns
LVCMOS12_S_2	0.512	0.512	0.555	0.512	0.767	0.767	0.803	0.767	0.990	0.990	1.024	0.990	ns
LVCMOS12_S_4	0.512	0.512	0.555	0.512	0.666	0.666	0.704	0.666	0.803	0.803	0.848	0.803	ns
LVCMOS12_S_6	0.512	0.512	0.555	0.512	0.657	0.657	0.695	0.657	0.732	0.732	0.774	0.732	ns
LVCMOS12_S_8	0.512	0.512	0.555	0.512	0.708	0.708	0.761	0.708	0.745	0.745	0.790	0.745	ns
LVCMOS15_F_12	0.414	0.414	0.445	0.414	0.500	0.500	0.522	0.500	0.647	0.647	0.682	0.647	ns
LVCMOS15_F_2	0.414	0.414	0.445	0.414	0.702	0.702	0.722	0.702	0.919	0.919	0.940	0.919	ns
LVCMOS15_F_4	0.414	0.414	0.445	0.414	0.579	0.579	0.601	0.579	0.755	0.755	0.781	0.755	ns
LVCMOS15_F_6	0.414	0.414	0.445	0.414	0.547	0.547	0.569	0.547	0.711	0.711	0.742	0.711	ns

Output Delay Measurement Methodology

Output delays are measured with short output traces. Standard termination was used for all testing. The propagation delay of the trace is characterized separately and subtracted from the final measurement, and is therefore not included in the generalized test setups shown in Figure 1 and Figure 2.

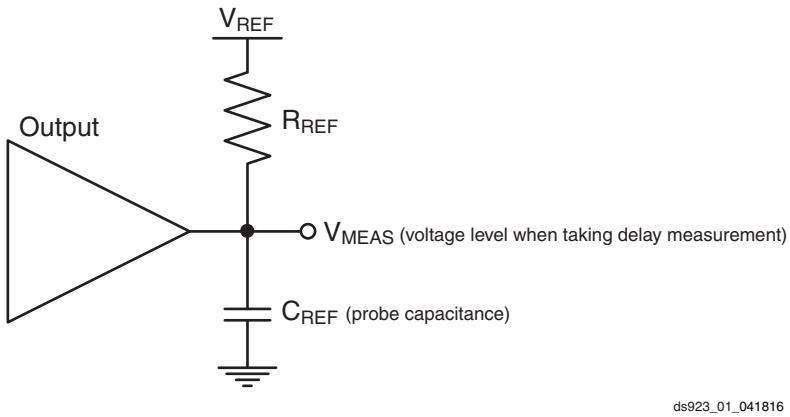

Figure 1: **Single-Ended Test Setup**

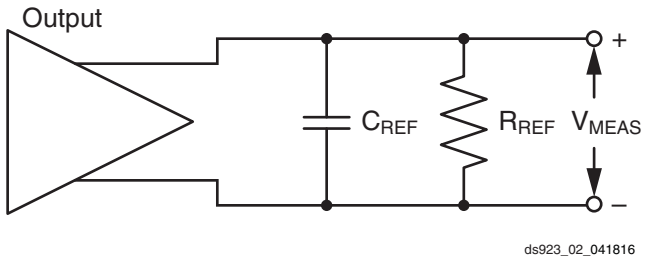

Figure 2: **Differential Test Setup**

Parameters V_{REF}, R_{REF}, C_{REF}, and V_{MEAS} fully describe the test conditions for each I/O standard. The most accurate prediction of propagation delay in any given application can be obtained through IBIS simulation, using this method:

1. Simulate the output driver of choice into the generalized test setup using values from Table 27.
2. Record the time to V_{MEAS}.
3. Simulate the output driver of choice into the actual PCB trace and load using the appropriate IBIS model or capacitance value to represent the load.
4. Record the time to V_{MEAS}.
5. Compare the results of step 2 and step 4. The increase or decrease in delay yields the actual propagation delay of the PCB trace.

Block RAM and FIFO Switching Characteristics

Table 28: **Block RAM and FIFO Switching Characteristics**

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages				Units
		0.90V	0.85V		0.72V	
		-3	-2	-1	-2	
Maximum Frequency						
$F_{MAX\_WF\_NC}$	Block RAM (WRITE_FIRST and NO_CHANGE modes).	825	737	645	585	MHz
F_{MAX_RF}	Block RAM (READ_FIRST mode).	718	637	575	510	MHz
F_{MAX_FIFO}	FIFO in all modes without ECC.	825	737	645	585	MHz
F_{MAX_ECC}	Block RAM and FIFO in ECC configuration without PIPELINE.	718	637	575	510	MHz
	Block RAM and FIFO in ECC configuration with PIPELINE and Block RAM in WRITE_FIRST or NO_CHANGE mode.	825	737	645	585	MHz
T_{PW}[(1)]	Minimum pulse width.	495	542	543	577	ps
Block RAM and FIFO Clock-to-Out Delays						
T_{RCKO_DO}	Clock CLK to DOUT output (without output register).	0.91	1.02	1.11	1.46	ns, Max
$T_{RCKO\_DO\_REG}$	Clock CLK to DOUT output (with output register).	0.27	0.29	0.30	0.42	ns, Max

Notes:

1. The MMCM and PLL DUTY_CYCLE attribute should be set to 50% to meet the pulse-width requirements at the higher frequencies.

UltraRAM Switching Characteristics

Table 29: **UltraRAM Switching Characteristics**

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages				Units
		0.90V	0.85V		0.72V	
		-3	-2	-1	-2	
Maximum Frequency						
F_{MAX}	UltraRAM maximum frequency with OREG_B = True.	650	600	575	500	MHz
F_{MAX_ECC}	UltraRAM maximum frequency OREG_B = False and EN_ECC_RD_B = True.	450	400	386	325	MHz
$F_{MAX\_NORPIPELINE}$	UltraRAM maximum frequency with OREG_B = False and EN_ECC_RD_B = False.	550	500	478	425	MHz
T_{PW}[(1)]	Minimum pulse width.	650	700	730	800	ps
T_{RSTPW}	Asynchronous reset minimum pulse width. One cycle required.	1 clock cycle				ps

Notes:

1. The MMCM and PLL DUTY_CYCLE attribute should be set to 50% to meet the pulse-width requirements at the higher frequencies.

Clock Buffers and Networks

Table 32: **Clock Buffers Switching Characteristics**

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages				Units
		0.90V	0.85V		0.72V	
		-3	-2	-1	-2	
Global Clock Switching Characteristics (Including BUFGCTRL)						
F_{MAX}	Maximum frequency of a global clock tree (BUFG).	891	775	667	725	MHz
Global Clock Buffer with Input Divide Capability (BUFGCE_DIV)						
F_{MAX}	Maximum frequency of a global clock buffer with input divide capability (BUFGCE_DIV).	891	775	667	725	MHz
Global Clock Buffer with Clock Enable (BUFGCE)						
F_{MAX}	Maximum frequency of a global clock buffer with clock enable (BUFGCE).	891	775	667	725	MHz
Leaf Clock Buffer with Clock Enable (BUFCE_LEAF)						
F_{MAX}	Maximum frequency of a leaf clock buffer with clock enable (BUFCE_LEAF).	891	775	667	725	MHz
GTY Clock Buffer with Clock Enable and Clock Input Divide Capability (BUFG_GT)						
F_{MAX}	Maximum frequency of a serial transceiver clock buffer with clock enable and clock input divide capability.	512	512	512	512	MHz

MMCM Switching Characteristics

Table 33: **MMCM Specification**

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages				Units
		0.90V	0.85V		0.72V	
		-3	-2	-1	-2	
MMCM_F_{INMAX}	Maximum input clock frequency.	1066	933	800	933	MHz
MMCM_F_{INMIN}	Minimum input clock frequency.	10	10	10	10	MHz
MMCM_$F_{INJITTER}$	Maximum input clock period jitter.	< 20% of clock input period or 1 ns Max				
MMCM_F_{INDUTY}	Input duty cycle range: 10–49 MHz.	25–75				%
	Input duty cycle range: 50–199 MHz.	30–70				%
	Input duty cycle range: 200–399 MHz.	35–65				%
	Input duty cycle range: 400–499 MHz.	40–60				%
	Input duty cycle range: >500 MHz.	45–55				%
MMCM_F_{MIN_PSCLK}	Minimum dynamic phase shift clock frequency.	0.01	0.01	0.01	0.01	MHz
MMCM_F_{MAX_PSCLK}	Maximum dynamic phase shift clock frequency.	550	500	450	500	MHz
MMCM_F_{VCOMIN}	Minimum MMCM VCO frequency.	800	800	800	800	MHz
MMCM_F_{VCOMAX}	Maximum MMCM VCO frequency.	1600	1600	1600	1600	MHz
MMCM_$F_{BANDWIDTH}$	Low MMCM bandwidth at typical.(1)	1.00	1.00	1.00	1.00	MHz
	High MMCM bandwidth at typical.(1)	4.00	4.00	4.00	4.00	MHz
MMCM_$T_{STATPHAOFFSET}$	Static phase offset of the MMCM outputs.(2)	0.12	0.12	0.12	0.12	ns
MMCM_$T_{OUTJITTER}$	MMCM output jitter.	Note 3				
MMCM_$T_{OUTDUTY}$	MMCM output clock duty cycle precision.(4)	0.165	0.20	0.20	0.20	ns
MMCM_$T_{LOCKMAX}$	MMCM maximum lock time for MMCM_F_{PFDMIN}.	100	100	100	100	µs
MMCM_F_{OUTMAX}	MMCM maximum output frequency.	891	775	667	725	MHz
MMCM_F_{OUTMIN}	MMCM minimum output frequency.(4)(5)	6.25	6.25	6.25	6.25	MHz
MMCM_$T_{EXTFDVAR}$	External clock feedback variation.	< 20% of clock input period or 1 ns Max				
MMCM_$RST_{MINPULSE}$	Minimum reset pulse width.	5.00	5.00	5.00	5.00	ns
MMCM_F_{PFDMAX}	Maximum frequency at the phase frequency detector.	550	500	450	500	MHz
MMCM_F_{PFDMIN}	Minimum frequency at the phase frequency detector.	10	10	10	10	MHz
MMCM_$T_{FBDELAY}$	Maximum delay in the feedback path.	5 ns Max or one clock cycle				
MMCM_F_{DPRCLK_MAX}	Maximum DRP clock frequency	250	250	250	250	MHz

Notes:

1. The MMCM does not filter typical spread-spectrum input clocks because they are usually far below the bandwidth filter frequencies.
2. The static offset is measured between any MMCM outputs with identical phase.
3. Values for this parameter are available in the Clocking Wizard.
4. Includes global clock buffer.
5. Calculated as F_{VCO}/128 assuming output duty cycle is 50%.

Device Pin-to-Pin Input Parameter Guidelines

The pin-to-pin numbers in Table 38 are based on the clock root placement in the center of the device. The actual pin-to-pin values will vary if the root placement selected is different. Consult the Vivado Design Suite timing report for the actual pin-to-pin values.

Table 38: **Global Clock Input Setup and Hold With MMCM**

Symbol	Description		Device	Speed Grade and V_{CCINT} Operating Voltages				Units
				0.90V	0.85V		0.72V	
				-3	-2	-1	-2	
Input Setup and Hold Time Relative to Global Clock Input Signal using SSTL15 Standard.(1)(2)(3)								
$T_{PSMMCMCC\_VU3P}$	Global clock input and input flip-flop (or latch) with MMCM.	Setup	XCVU3P	1.86	1.86	1.99	2.32	ns
$T_{PHMMCMCC\_VU3P}$		Hold		–0.13	–0.13	–0.13	0.14	ns
$T_{PSMMCMCC\_VU5P}$		Setup	XCVU5P	1.86	1.86	1.99	2.32	ns
$T_{PHMMCMCC\_VU5P}$		Hold		–0.13	–0.13	–0.13	0.14	ns
$T_{PSMMCMCC\_VU7P}$		Setup	XCVU7P	1.86	1.86	1.99	2.32	ns
$T_{PHMMCMCC\_VU7P}$		Hold		–0.13	–0.13	–0.13	0.14	ns
$T_{PSMMCMCC\_VU9P}$		Setup	XCVU9P	1.86	1.86	1.99	2.32	ns
$T_{PHMMCMCC\_VU9P}$		Hold		–0.13	–0.13	–0.13	0.14	ns
$T_{PSMMCMCC\_VU11P}$		Setup	XCVU11P	1.92	1.92	2.05	2.36	ns
$T_{PHMMCMCC\_VU11P}$		Hold		–0.13	–0.13	–0.13	0.16	ns
$T_{PSMMCMCC\_VU13P}$		Setup	XCVU13P	1.92	1.92	2.05	2.36	ns
$T_{PHMMCMCC\_VU13P}$		Hold		–0.13	–0.13	–0.13	0.16	ns

Notes:

1. Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, slowest temperature, and slowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, fastest temperature, and fastest voltage.
2. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible I/O and CLB flip-flops are clocked by the global clock net in a single SLR.
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 39: **Sampling Window**

Description	Speed Grade and V_{CCINT} Operating Voltages				Units
	0.90V	0.85V		0.72V	
	-3	-2	-1	-2	
T_{SAMP_BUFG}(1)	510	610	610	610	ps
$T_{SAMP\_NATIVE\_DPA}$	100	100	125	125	ps
$T_{SAMP\_NATIVE\_BISC}$	60	60	85	85	ps

Notes:

1. This parameter indicates the total sampling error of the Virtex UltraScale+ FPGA DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the MMCM to capture the DDR input registers' edges of operation. These measurements include: CLK0 MMCM jitter, MMCM accuracy (phase offset), and MMCM phase shift resolution. These measurements do not include package or clock tree skew.

Package Parameter Guidelines

The parameters in this section provide the necessary values for calculating timing budgets for clock transmitter and receiver data-valid windows.

Table 40: **Package Skew**

Symbol	Description	Device	Package	Value	Units
PKGSKEW	Package Skew	XCVU3P	FFVC1517	197	ps
		XCVU5P	FLVA2104	175	ps
			FLVB2104	225	ps
			FLVC2104	216	ps
		XCVU7P	FLVA2104	175	ps
			FLVB2104	225	ps
			FLVC2104	216	ps
		XCVU9P	FLGA2104	217	ps
			FLGB2104	275	ps
			FLGC2104	299	ps
			FSGD2104	229	ps
			FLGA2577	149	ps
		XCVU11P	FLGF1924	180	ps
			FLGB2104	216	ps
			FLGC2104		ps
			FSGD2104		ps
			FLGA2577	154	ps
		XCVU13P	FHGA2104		ps
			FHGB2104	259	ps
			FHGC2104	182	ps
			FIGD2104		ps
			FLGA2577	140	ps

Notes:

1. These values represent the worst-case skew between any two SelectIO resources in the package: shortest delay to longest delay from die pad to ball.
2. Package delay information is available for these device/package combinations. This information can be used to deskew the package.

Table 45: **GTY Transceiver Dynamic Reconfiguration Port (DRP) Switching Characteristics**

Symbol	Description	All Speed Grades	Units
$F_{GTYDRPCLK}$	GTYDRPCLK maximum frequency.	250	MHz

Table 46: **GTY Transceiver Reference Clock Switching Characteristics**

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
F_{GCLK}	Reference clock frequency range.		60	–	820	MHz
T_{RCLK}	Reference clock rise time.	20% – 80%	–	200	–	ps
T_{FCLK}	Reference clock fall time.	80% – 20%	–	200	–	ps
T_{DCREF}	Reference clock duty cycle.	Transceiver PLL only	40	50	60	%

Table 47: **GTY Transceiver Reference Clock Oscillator Selection Phase Noise Mask(1)**

Symbol	Description	Offset Frequency	Min	Typ	Max	Units
$QPLL_{REFCLKMASK}$	QPLL0/QPLL1 reference clock select phase noise mask at REFCLK frequency = 156.25 MHz.	10 kHz	–	–	–112	dBc/Hz
		100 kHz	–	–	–128	
		1 MHz	–	–	–145	
	QPLL0/QPLL1 reference clock select phase noise mask at REFCLK frequency = 312.5 MHz.	10 kHz	–	–	–103	dBc/Hz
		100 kHz	–	–	–123	
		1 MHz	–	–	–143	
	QPLL0/QPLL1 reference clock select phase noise mask at REFCLK frequency =625 MHz.	10 kHz	–	–	–98	dBc/Hz
		100 kHz	–	–	–117	
		1 MHz	–	–	–140	
$CPLL_{REFCLKMASK}$	CPLL reference clock select phase noise mask at REFCLK frequency = 156.25 MHz.	10 kHz	–	–	–112	dBc/Hz
		100 kHz	–	–	–128	
		1 MHz	–	–	–145	
		50 MHz	–	–	–145	
	CPLL reference clock select phase noise mask at REFCLK frequency = 312.5 MHz.	10 kHz	–	–	–103	dBc/Hz
		100 kHz	–	–	–123	
		1 MHz	–	–	–143	
		50 MHz	–	–	–145	
	CPLL reference clock select phase noise mask at REFCLK frequency = 625 MHz.	10 kHz	–	–	–98	dBc/Hz
		100 kHz	–	–	–117	
		1 MHz	–	–	–140	
		50 MHz	–	–	–144	

Notes:

1. For reference clock frequencies not in this table, use the phase-noise mask for the nearest reference clock frequency.

Table 50: **GTY Transceiver Transmitter Switching Characteristics**

Symbol	Description	Condition	Min	Typ	Max	Units
F_{GTYTX}	Serial data rate range		0.500	–	F_{GTYMAX}	Gb/s
T_{RTX}	TX rise time	20%–80%	–	21	–	ps
T_{FTX}	TX fall time	80%–20%	–	21	–	ps
T_{LLSKEW}	TX lane-to-lane skew(1)		–	–	500.00	ps
$T_{J32.75}$	Total jitter(2)(4)	32.75 Gb/s	–	–	0.35	UI
$D_{J32.75}$	Deterministic jitter(2)(4)		–	–	0.19	UI
$T_{J28.21}$	Total jitter(2)(4)	28.21 Gb/s	–	–	0.28	UI
$D_{J28.21}$	Deterministic jitter(2)(4)		–	–	0.17	UI
$T_{J16.375}$	Total jitter(2)(4)	16.375 Gb/s	–	–	0.28	UI
$D_{J16.375}$	Deterministic jitter(2)(4)		–	–	0.17	UI
$T_{J15.0}$	Total jitter(2)(4)	15.0 Gb/s	–	–	0.28	UI
$D_{J15.0}$	Deterministic jitter(2)(4)		–	–	0.17	UI
$T_{J14.1}$	Total jitter(2)(4)	14.1 Gb/s	–	–	0.28	UI
$D_{J14.1}$	Deterministic jitter(2)(4)		–	–	0.17	UI
$T_{J14.1}$	Total jitter(2)(4)	14.025 Gb/s	–	–	0.28	UI
$D_{J14.1}$	Deterministic jitter(2)(4)		–	–	0.17	UI
$T_{J13.1}$	Total jitter(2)(4)	13.1 Gb/s	–	–	0.28	UI
$D_{J13.1}$	Deterministic jitter(2)(4)		–	–	0.17	UI
$T_{J12.5\_QPLL}$	Total jitter(2)(4)	12.5 Gb/s	–	–	0.28	UI
$D_{J12.5\_QPLL}$	Deterministic jitter(2)(4)		–	–	0.17	UI
$T_{J12.5\_CPLL}$	Total jitter(3)(4)	12.5 Gb/s	–	–	0.33	UI
$D_{J12.5\_CPLL}$	Deterministic jitter(3)(4)		–	–	0.17	UI
$T_{J11.3}$	Total jitter(2)(4)	11.3 Gb/s	–	–	0.28	UI
$D_{J11.3}$	Deterministic jitter(2)(4)		–	–	0.17	UI
$T_{J10.3125\_QPLL}$	Total jitter(2)(4)	10.3125 Gb/s	–	–	0.28	UI
$D_{J10.3125\_QPLL}$	Deterministic jitter(2)(4)		–	–	0.17	UI
$T_{J10.3125\_CPLL}$	Total jitter(3)(4)	10.3125 Gb/s	–	–	0.33	UI
$D_{J10.3125\_CPLL}$	Deterministic jitter(3)(4)		–	–	0.17	UI
$T_{J9.953\_QPLL}$	Total jitter(2)(4)	9.953 Gb/s	–	–	0.28	UI
$D_{J9.953\_QPLL}$	Deterministic jitter(2)(4)		–	–	0.17	UI
$T_{J9.953\_CPLL}$	Total jitter(3)(4)	9.953 Gb/s	–	–	0.33	UI
$D_{J9.953\_CPLL}$	Deterministic jitter(3)(4)		–	–	0.17	UI
$T_{J8.0}$	Total jitter(3)(4)	8.0 Gb/s	–	–	0.32	UI
$D_{J8.0}$	Deterministic jitter(3)(4)		–	–	0.17	UI
$T_{J6.6}$	Total jitter(3)(4)	6.6 Gb/s	–	–	0.30	UI
$D_{J6.6}$	Deterministic jitter(3)(4)		–	–	0.15	UI
$T_{J5.0}$	Total jitter(3)(4)	5.0 Gb/s	–	–	0.30	UI
$D_{J5.0}$	Deterministic jitter(3)(4)		–	–	0.15	UI
$T_{J4.25}$	Total jitter(3)(4)	4.25 Gb/s	–	–	0.30	UI
$D_{J4.25}$	Deterministic jitter(3)(4)		–	–	0.15	UI

Integrated Interface Block for 100G Ethernet MAC and PCS

More information and documentation on solutions using the integrated 100 Gb/s Ethernet block can be found at UltraScale Integrated 100G Ethernet MAC/PCS. The *UltraScale Architecture and Product Overview* (DS890) lists how many blocks are in each Virtex UltraScale+ FPGA.

Table 56: **Maximum Performance for 100G Ethernet Designs**

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages				Units
		0.90V	0.85V		0.72V	
		-3	-2(1)	-1	-2	
F_{TX_CLK}	Transmit clock	390.625	390.625	322.223	322.223	MHz
F_{RX_CLK}	Receive clock	390.625	390.625	322.223	322.223	MHz
$F_{RX\_SERDES\_CLK}$	Receive serializer/deserializer clock	390.625	390.625	322.223	322.223	MHz
F_{DRP_CLK}	Dynamic reconfiguration port clock	250.00	250.00	250.00	250.00	MHz

Notes:

1. The maximum clock frequency of 390.625 MHz only applies to the CAUI-10 interface. The maximum clock frequency for the CAUI-4 interface is 322.223 MHz.

Integrated Interface Block for PCI Express Designs

More information and documentation on solutions for PCI Express designs can be found at PCI Express. The *UltraScale Architecture and Product Overview* (DS890) lists how many blocks are in each Virtex UltraScale+ FPGA.

Table 57: **Maximum Performance for PCI Express Designs(1)(2)**

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages				Units
		0.90V	0.85V		0.72V	
		-3	-2	-1	-2	
$F_{PIPECLK}$	Pipe clock maximum frequency.	250.00	250.00	250.00	250.00	MHz
$F_{CORECLK}$	Core clock maximum frequency.	500.00	500.00	500.00	250.00	MHz
F_{DRPCLK}	DRP clock maximum frequency.	250.00	250.00	250.00	250.00	MHz
$F_{MCAPCLK}$	MCAP clock maximum frequency.	125.00	125.00	125.00	125.00	MHz

Notes:

1. PCI Express Gen4 operation is supported for x1, x2, x4, and x8 widths.
2. PCI Express Gen4 operation is supported in -3E, -2E, and -2I speed grades.

Table 58: **System Monitor Specifications *(Cont'd)***

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
Supply sensor error(4)		Supply voltages 0.72V to 1.2V, T_j = –40°C to 100°C (with external REF)	–	–	±0.5	%
		Supply voltages 0.72V to 1.2V, T_j = –55°C to 125°C (with external REF)	–	–	±1.0	%
		All other supply voltages, T_j = –40°C to 100°C (with external REF)	–	–	±1.0	%
		All other supply voltages, T_j = –55°C to 125°C (with external REF)	–	–	±2.0	%
		Supply voltages 0.72V to 1.2V, T_j = –40°C to 100°C (with internal REF)	–	–	±1.0	%
		Supply voltages 0.72V to 1.2V, T_j = –55°C to 125°C (with internal REF)	–	–	±2.0	%
		All other supply voltages, T_j = –40°C to 100°C (with internal REF)	–	–	±1.5	%
		All other supply voltages, T_j = –55°C to 125°C (with internal REF)	–	–	±2.5	%
Conversion Rate(5)						
Conversion time—continuous	t_{CONV}	Number of ADCCLK cycles	26	–	32	Cycles
Conversion time—event	t_{CONV}	Number of ADCCLK cycles	–	–	21	Cycles
DRP clock frequency	DCLK	DRP clock frequency	8	–	250	MHz
ADC clock frequency	ADCCLK	Derived from DCLK	1	–	5.2	MHz
DCLK duty cycle			40	–	60	%
SYSMON Reference(6)						
External reference	V_{REFP}	Externally supplied reference voltage	1.20	1.25	1.30	V
On-chip reference		Ground V_{REFP} pin to AGND, T_j = –40°C to 100°C	1.2375	1.25	1.2625	V
		Ground V_{REFP} pin to AGND, T_j = –55°C to 125°C	1.225	1.25	1.275	V

Notes:

1. ADC offset errors are removed by enabling the ADC automatic offset calibration feature. The values are specified for when this feature is enabled.
2. See the *Analog Input* section in the *UltraScale Architecture System Monitor User Guide* (UG580).
3. When reading temperature values directly from the PMBus interface, the SYSMON has a +4°C offset due to the transfer function used by the PMBus application. For example, the external REF temperature sensor error's range of ±3°C becomes +1°C to +7°C when the temperature is read through the PMBus interface.
4. Supply sensor offset and gain errors are removed by enabling the automatic offset and gain calibration feature. The values are specified for when this feature is enabled.
5. See the *Adjusting the Acquisition Settling Time* section in the *UltraScale Architecture System Monitor User Guide* (UG580).
6. Any variation in the reference voltage from the nominal V_{REFP} = 1.25V and V_{REFN} = 0V will result in a deviation from the ideal transfer function. This also impacts the accuracy of the internal sensor measurements (i.e., temperature and power supply). However, for external ratiometric type applications allowing reference to vary by ±4% is permitted.

Table 61: **Configuration Switching Characteristics *(Cont'd)***

Symbol	Description		Speed Grade and V_{CCINT} Operating Voltages				Units
			0.90V	0.85V		0.72V	
			-3	-2	-1	-2	
SelectMAP Mode Programming Switching							
T_{SMDCCK}/T_{SMCCKD}	D[31:00] setup/hold.	XCVU3P, XCVU5P, XCVU7P, XCVU9P	4.0/0	4.0/0	4.0/0	5.0/0	ns, Min
		XCVU11P, XCVU13P	4.5/0	4.5/0	4.5/0	7.5/0	ns, Min
$T_{SMCSCCK}/T_{SMCCKCS}$	CSI_B setup/hold.	XCVU3P, XCVU5P, XCVU7P, XCVU9P	4.0/0	4.0/0	4.0/0	5.0/0	ns, Min
		XCVU11P, XCVU13P	4.5/0	4.5/0	4.5/0	7.5/0	ns, Min
T_{SMWCCK}/T_{SMCCKW}	RDWR_B setup/hold.	XCVU3P, XCVU5P, XCVU7P, XCVU9P	10.0/0	10.0/0	10.0/0	11.0/0	ns, Min
		XCVU11P, XCVU13P	11.0/0	11.0/0	11.0/0	17.0/0	ns, Min
$T_{SMCKCSO}$	CSO_B clock to out (330Ω pull-up resistor required).		7.0	7.0	7.0	7.0	ns, Max
T_{SMCO}	D[31:00] clock to out in readback.		8.0	8.0	8.0	8.0	ns, Max
F_{RBCCK}	Readback frequency.	XCVU3P, XCVU5P, XCVU7P, XCVU9P	125	125	125	100	MHz, Max
		XCVU11P, XCVU13P	125	125	125	66	MHz, Max
Boundary-Scan Port Timing Specifications							
T_{TAPTCK}/T_{TCKTAP}	TMS and TDI setup/hold.	XCVU3P	3.0/ 2.0	3.0/ 2.0	3.0/ 2.0	3.0/ 2.0	ns, Min
		XCVU5P, XCVU7P, XCVU9P, XCVU11P, XCVU13P	8.5/ 2.0	8.5/ 2.0	8.5/ 2.0	8.5/ 2.0	ns, Min
T_{TCKTDO}	TCK falling edge to TDO output.	XCVU3P	7.0	7.0	7.0	7.0	ns, Max
		XCVU5P, XCVU7P, XCVU9P, XCVU11P, XCVU13P	15.0	15.0	15.0	15.0	ns, Max
F_{TCK}	TCK frequency.	XCVU3P	66	66	66	66	MHz, Max
		XCVU5P, XCVU7P, XCVU9P, XCVU11P, XCVU13P	20	20	20	20	MHz, Max
BPI Master Flash Mode Programming Switching							
T_{BPICCO}	A[28:00], RS[1:0], FCS_B, FOE_B, FWE_B, ADV_B clock to out.		10	10	10	10	ns, Max
T_{BPIDCC}/T_{BPICCD}	D[15:00] setup/hold.	XCVU3P, XCVU5P, XCVU7P, XCVU9P	4.0/0	4.0/0	4.0/0	5.0/0	ns, Min
		XCVU11P, XCVU13P	4.5/0	4.5/0	4.5/0	7.5/0	ns, Min
SPI Master Flash Mode Programming Switching							
T_{SPIDCC}/T_{SPICCD}	D[03:00] setup/hold.		3.0/0	3.0/0	3.0/0	4.0/0	ns, Min
T_{SPIDCC}/T_{SPICCD}	D[07:04] setup/hold.	XCVU3P, XCVU5P, XCVU7P, XCVU9P	4.0/0	4.0/0	4.0/0	5.0/0	ns, Min
		XCVU11P, XCVU13P	4.5/0	4.5/0	4.5/0	7.5/0	ns, Min
T_{SPICCM}	MOSI clock to out.		8.0	8.0	8.0	8.0	ns, Max
$T_{SPICCFC}$	FCS_B clock to out.		8.0	8.0	8.0	8.0	ns, Max