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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	75072
Number of Logic Elements/Cells	1313763
Total RAM Bits	190976000
Number of I/O	832
Number of Gates	-
Voltage - Supply	0.873V ~ 0.927V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 100°C (TJ)
Package / Case	2104-BBGA, FCBGA
Supplier Device Package	2104-FCBGA (47.5x47.5)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xcvu5p-3flva2104e

Recommended Operating Conditions

Table 2: **Recommended Operating Conditions(1)(2)**

Symbol	Description	Min	Typ	Max	Units
FPGA Logic					
V_{CCINT}	Internal supply voltage.	0.825	0.850	0.876	V
	For -2LE (V_{CCINT} = 0.72V) devices: internal supply voltage.	0.698	0.720	0.742	V
	For -3E devices: internal supply voltage.	0.873	0.900	0.927	V
V_{CCINT_IO}(3)	Internal supply voltage for the I/O banks.	0.825	0.850	0.876	V
	For -2LE devices (V_{CCINT} = 0.85V): internal supply voltage for the I/O banks.	0.825	0.850	0.876	V
	For -3E devices: internal supply voltage for the I/O banks.	0.873	0.900	0.927	V
V_{CCBRAM}	Block RAM supply voltage.	0.825	0.850	0.876	V
	For -3E devices: block RAM supply voltage.	0.873	0.900	0.927	V
V_{CCAUX}	Auxiliary supply voltage.	1.746	1.800	1.854	V
V_{CCO}(4)(5)	Supply voltage for I/O banks.	0.950	–	1.900	V
V_{CCAUX_IO}(6)	Auxiliary I/O supply voltage.	1.746	1.800	1.854	V
V_{IN}(7)	I/O input voltage.	–0.200	–	V_{CCO} + 0.200	V
I_{IN}(8)	Maximum current through any pin in a powered or unpowered bank when forward biasing the clamp diode.	–	–	10	mA
V_{BATT}(9)	Battery voltage.	1.000	–	1.890	V
GTY Transceiver					
$V_{MGTAVCC}$(10)	Analog supply voltage for the GTY transceiver.	0.873	0.900	0.927	V
$V_{MGTAVTT}$(10)	Analog supply voltage for the GTY transmitter and receiver termination circuits.	1.164	1.20	1.236	V
$V_{MGTVCCAUX}$(10)	Auxiliary analog QPLL voltage supply for the transceivers.	1.746	1.80	1.854	V
$V_{MGTAVTTRCAL}$(10)	Analog supply voltage for the resistor calibration circuit of the GTY transceiver column.	1.164	1.20	1.236	V

Table 2: **Recommended Operating Conditions(1)(2) *(Cont'd)***

Symbol	Description	Min	Typ	Max	Units
SYSMON					
V_{CCADC}	SYSMON supply relative to GNDADC.	1.746	1.800	1.854	V
V_{REFP}	SYSMON externally supplied reference voltage relative to GNDADC.	1.200	1.250	1.300	V
Temperature					
T_j(11)	Junction temperature operating range for extended (E) temperature devices.(12)	0	–	100	°C
	Junction temperature operating range for industrial (I) temperature devices.	–40	–	100	°C
	Junction temperature operating range for eFUSE programming.(13)	–40	–	125	°C

Notes:

1. All voltages are relative to GND.
2. For the design of the power distribution system consult *UltraScale Architecture PCB Design Guide* (UG583).
3. V_{CCINT_IO} must be connected to V_{CCBRAM}.
4. For V_{CCO_0}, the minimum recommended operating voltage for power on and during configuration is 1.425V. After configuration, data is retained even if V_{CCO} drops to 0V.
5. Includes V_{CCO} of 1.0V, 1.2V, 1.35V, 1.5V, and 1.8V.
6. V_{CCAUX_IO} must be connected to V_{CCAUX}.
7. The lower absolute voltage specification always applies.
8. A total of 200 mA per bank should not be exceeded.
9. If battery is not used, connect V_{BATT} to either GND or V_{CCAUX}.
10. Each voltage listed requires filtering as described in the *UltraScale Architecture GTY Transceiver User Guide* (UG578).
11. Xilinx recommends measuring the Tj of a device using the system monitor as described in the *UltraScale Architecture System Monitor User Guide* (UG580). The SYSMON temperature measurement errors (that are described in Table 58) must be accounted for in your design. For example, by using an external reference of 1.25V, when SYSMON reports 97°C, there is a measurement error ±3°C. A reading of 97°C is considered the maximum adjusted Tj (100°C – 3°C = 97°C).
12. Devices labeled with the speed/temperature grade of -2LE can operate for a limited time at a junction temperature of 110°C. Timing parameters adhere to the same speed file at 110°C as they do below 110°C, regardless of operating voltage (nominal voltage of 0.85V or a low-voltage of 0.72V). Operation at Tj = 110°C is limited to 1% of the device lifetime and can occur sequentially or at regular intervals as long as the total time does not exceed 1% of the device lifetime.
13. Do not program eFUSE during device configuration (e.g., during configuration, during configuration readback, or when readback CRC is active).

DC Characteristics Over Recommended Operating Conditions

Table 3: **DC Characteristics Over Recommended Operating Conditions**

Symbol	Description	Min	Typ(1)	Max	Units
V_{DRINT}	Data retention V_{CCINT} voltage (below which configuration data might be lost).	0.68	–	–	V
V_{DRAUX}	Data retention V_{CCAUX} voltage (below which configuration data might be lost).	1.5	–	–	V
I_{REF}	V_{REF} leakage current per pin.	–	–	15	µA
I_L	Input or output leakage current per pin (sample-tested).(2)	–	–	15	µA
C_{IN}(3)	Die input capacitance at the pad.	–	–	3.1	pF
I_{RPU}	Pad pull-up (when selected) at V_{IN} = 0V, V_{CCO} = 3.3V.	75	–	190	µA
	Pad pull-up (when selected) at V_{IN} = 0V, V_{CCO} = 2.5V.	50	–	169	µA
	Pad pull-up (when selected) at V_{IN} = 0V, V_{CCO} = 1.8V.	60	–	120	µA
	Pad pull-up (when selected) at V_{IN} = 0V, V_{CCO} = 1.5V.	30	–	120	µA
	Pad pull-up (when selected) at V_{IN} = 0V, V_{CCO} = 1.2V.	10	–	100	µA
I_{RPD}	Pad pull-down (when selected) at V_{IN} = 3.3V.	60	–	200	µA
	Pad pull-down (when selected) at V_{IN} = 1.8V.	29	–	120	µA
$I_{CCADCON}$	Analog supply current for the SYSMON circuits in the power-up state.	–	–	8	mA
$I_{CCADCOFF}$	Analog supply current for the SYSMON circuits in the power-down state.	–	–	1.5	mA
I_{BATT}(4)(5)	Battery supply current at V_{BATT} = 1.89V.	–	–	650	nA
	Battery supply current at V_{BATT} = 1.20V.	–	–	150	nA
I_{PFS}(6)	V_{CCAUX} additional supply current during eFUSE programming.	–	–	115	mA
Calibrated programmable on-die termination (DCI) in I/O banks(8) (measured per JEDEC specification)					
R(9)	Thevenin equivalent resistance of programmable input termination to V_{CCO}/2 where ODT = RTT_40.	–10%(8)	40	+10%(8)	Ω
	Thevenin equivalent resistance of programmable input termination to V_{CCO}/2 where ODT = RTT_48.	–10%(8)	48	+10%(8)	Ω
	Thevenin equivalent resistance of programmable input termination to V_{CCO}/2 where ODT = RTT_60.	–10%(8)	60	+10%(8)	Ω
	Programmable input termination to V_{CCO} where ODT = RTT_40.	–10%(8)	40	+10%(8)	Ω
	Programmable input termination to V_{CCO} where ODT = RTT_48.	–10%(8)	48	+10%(8)	Ω
	Programmable input termination to V_{CCO} where ODT = RTT_60.	–10%(8)	60	+10%(8)	Ω
	Programmable input termination to V_{CCO} where ODT = RTT_120.	–10%(8)	120	+10%(8)	Ω
	Programmable input termination to V_{CCO} where ODT = RTT_240.	–10%(8)	240	+10%(8)	Ω

V_{IN} Maximum Allowed AC Voltage Overshoot and Undershoot

Table 4: **V_{IN} Maximum Allowed AC Voltage Overshoot and Undershoot for HP I/O Banks(1)(2)**

AC Voltage Overshoot	% of UI at –40°C to 100°C	AC Voltage Undershoot	% of UI at –40°C to 100°C
V_{CCO} + 0.30	100%	–0.30	100%
V_{CCO} + 0.35	100%	–0.35	90%
V_{CCO} + 0.40	92%	–0.40	92%
V_{CCO} + 0.45	50%	–0.45	50%
V_{CCO} + 0.50	20%	–0.50	20%
V_{CCO} + 0.55	10%	–0.55	10%
V_{CCO} + 0.60	6%	–0.60	6%
V_{CCO} + 0.65	2%	–0.65	2%
V_{CCO} + 0.70	2%	–0.70	2%

Notes:
1. A total of 200 mA per bank should not be exceeded.
2. For UI smaller than 20 µs.

Quiescent Supply Current

Table 5: **Typical Quiescent Supply Current(1)(2)(3)**

Symbol	Description	Device	Speed Grade and V_{CCINT} Operating Voltages				Units
			0.90V	0.85V		0.72V	
			-3	-2	-1	-2	
I_{CCINTQ}	Quiescent V_{CCINT} supply current.	XCVU3P	2384	2276	2276	2017	mA
		XCVU5P	4769	4552	4552	4034	mA
		XCVU7P	4769	4552	4552	4034	mA
		XCVU9P	7153	6828	6828	6050	mA
		XCVU11P	7567	7202	7202	6332	mA
		XCVU13P	10090	9602	9602	8442	mA
I_{CCINT_IOQ}	Quiescent current for V_{CCINT_IO} supply.	XCVU3P	149	144	144	144	mA
		XCVU5P	298	287	287	287	mA
		XCVU7P	298	287	287	287	mA
		XCVU9P	447	431	431	431	mA
		XCVU11P	182	176	176	176	mA
		XCVU13P	243	234	234	234	mA
I_{CCOQ}	Quiescent V_{CCO} supply current.	All devices	1	1	1	1	mA
I_{CCAUXQ}	Quiescent V_{CCAUX} supply current.	XCVU3P	268	268	268	268	mA
		XCVU5P	535	535	535	535	mA
		XCVU7P	535	535	535	535	mA
		XCVU9P	1015	1015	1015	1015	mA
		XCVU11P	819	819	819	819	mA
		XCVU13P	1091	1091	1091	1091	mA

Power Supply Requirements

Table 6 shows the minimum current, in addition to I_{CCQ} maximum, required by each Virtex UltraScale+ FPGA for proper power-on and configuration. If the current minimums shown in Table 6 are met, the device powers on after all supplies have passed through their power-on reset threshold voltages. The device must not be configured until after V_{CCINT} is applied. Once initialized and configured, use the Xilinx Power Estimator (XPE) tools to estimate current drain on these supplies.

Table 6: **Power-on Current by Device(1)**

Device	$I_{CCINTMIN}$	$I_{CCINT\_IOMIN} + I_{CCBRAMMIN}$	I_{CCOMIN}	$I_{CCAUXMIN} + I_{CCAUX\_IOMIN}$	Units
XCVU3P	I_{CCINTQ} + 2000	$I_{CCBRAMQ} + I_{CCINT\_IOQ}$ + 950	I_{CCOQ} + 50	$I_{CCAUXQ} + I_{CCAUX\_IOQ}$ + 350	mA
XCVU5P	I_{CCINTQ} + 4000	$I_{CCBRAMQ} + I_{CCINT\_IOQ}$ + 1900	I_{CCOQ} + 100	$I_{CCAUXQ} + I_{CCAUX\_IOQ}$ + 700	mA
XCVU7P	I_{CCINTQ} + 4000	$I_{CCBRAMQ} + I_{CCINT\_IOQ}$ + 1900	I_{CCOQ} + 100	$I_{CCAUXQ} + I_{CCAUX\_IOQ}$ + 700	mA
XCVU9P	I_{CCINTQ} + 6000	$I_{CCBRAMQ} + I_{CCINT\_IOQ}$ + 2850	I_{CCOQ} + 150	$I_{CCAUXQ} + I_{CCAUX\_IOQ}$ + 1050	mA
XCVU11P	I_{CCINTQ} + 6549	$I_{CCBRAMQ} + I_{CCINT\_IOQ}$ + 3111	I_{CCOQ} + 164	$I_{CCAUXQ} + I_{CCAUX\_IOQ}$ + 1146	mA
XCVU13P	I_{CCINTQ} + 8731	$I_{CCBRAMQ} + I_{CCINT\_IOQ}$ + 4148	I_{CCOQ} + 219	$I_{CCAUXQ} + I_{CCAUX\_IOQ}$ + 1528	mA

Notes:

1. Use the Xilinx Power Estimator (XPE) spreadsheet tool (download at www.xilinx.com/power) to estimate power-on current for all supplies.

Table 7 shows the power supply ramp time.

Table 7: **Power Supply Ramp Time**

Symbol	Description	Min	Max	Units
T_{VCCINT}	Ramp time from GND to 95% of V_{CCINT}.	0.2	40	ms
T_{VCCINT_IO}	Ramp time from GND to 95% of V_{CCINT_IO}.	0.2	40	ms
T_{VCCO}	Ramp time from GND to 95% of V_{CCO}.	0.2	40	ms
T_{VCCAUX}	Ramp time from GND to 95% of V_{CCAUX}.	0.2	40	ms
$T_{VCCBRAM}$	Ramp time from GND to 95% of V_{CCBRAM}.	0.2	40	ms
$T_{MGTAVCC}$	Ramp time from GND to 95% of $V_{MGTAVCC}$.	0.2	40	ms
$T_{MGTAVTT}$	Ramp time from GND to 95% of $V_{MGTAVTT}$.	0.2	40	ms
$T_{MGTVCCAUX}$	Ramp time from GND to 95% of $V_{MGTVCCAUX}$.	0.2	40	ms

AC Switching Characteristics

All values represented in this data sheet are based on the speed specifications in the Vivado® Design Suite as outlined in Table 16.

Table 16: **Speed Specification Version By Device**

2017.1	Device
1.10	XCVU3P, XCVU7P, XCVU9P, XCVU5P, XCVU11P, XCVU13P

Switching characteristics are specified on a per-speed-grade basis and can be designated as Advance, Preliminary, or Production. Each designation is defined as follows:

Advance Product Specification

These specifications are based on simulations only and are typically available soon after device design specifications are frozen. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

Preliminary Product Specification

These specifications are based on complete ES (engineering sample) silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting delays is greatly reduced as compared to Advance data.

Product Specification

These specifications are released once enough production silicon of a particular device family member has been characterized to provide full correlation between specifications and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to production before faster speed grades.

Testing of AC Switching Characteristics

Internal timing parameters are derived from measuring internal test patterns. All AC switching characteristics are representative of worst-case supply voltage and junction temperature conditions.

For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer and back-annotate to the simulation net list. Unless otherwise noted, values apply to all Virtex UltraScale+ FPGAs.

FPGA Logic Performance Characteristics

This section provides the performance characteristics of some common functions and designs implemented in Virtex UltraScale+ FPGAs. These values are subject to the same guidelines as the AC Switching Characteristics, page 13.

Table 19: **LVDS Component Mode Performance**

Description	Speed Grade and V_{CCINT} Operating Voltages								Units
	0.90V		0.85V				0.72V		
	-3		-2		-1		-2		
	Min	Max	Min	Max	Min	Max	Min	Max	
LVDS TX DDR (OSERDES 4:1, 8:1)	0	1250	0	1250	0	1250	0	1250	Mb/s
LVDS TX SDR (OSERDES 2:1, 4:1)	0	625	0	625	0	625	0	625	Mb/s
LVDS RX DDR (ISERDES 1:4, 1:8)(1)	0	1250	0	1250	0	1250	0	1250	Mb/s
LVDS RX SDR (ISERDES 1:2, 1:4)(1)	0	625	0	625	0	625	0	625	Mb/s

Notes:

1. LVDS receivers are typically bounded with certain applications to achieve maximum performance. Package skews are not included and should be removed through PCB routing.

Table 20: **LVDS Native Mode Performance(1)(2)**

Description	DATA_WIDTH	Speed Grade and V_{CCINT} Operating Voltages								Units
		0.90V		0.85V				0.72V		
		-3		-2		-1		-2		
		Min	Max	Min	Max	Min	Max	Min	Max	
LVDS TX DDR (TX_BITSLICE)	4	375	1600	375	1600	375	1260	375	1400	Mb/s
	8	375	1600	375	1600	375	1260	375	1600	Mb/s
LVDS TX SDR (TX_BITSLICE)	4	187.5	800	187.5	800	187.5	630	187.5	700	Mb/s
	8	187.5	800	187.5	800	187.5	630	187.5	800	Mb/s
LVDS RX DDR (RX_BITSLICE)(3)	4	375	1600	375	1600	375	1260	375	1400	Mb/s
	8	375	1600	375	1600	375	1260	375	1600	Mb/s
LVDS RX SDR (RX_BITSLICE)(3)	4	187.5	800	187.5	800	187.5	630	187.5	700	Mb/s
	8	187.5	800	187.5	800	187.5	630	187.5	800	Mb/s

Notes:

1. Native mode is supported through the High-Speed SelectIO Interface Wizard available with the Vivado Design Suite.
2. PLL settings can restrict the minimum allowable data rate. For example, when using the PLL with CLKOUTPHY_MODE = VCO_HALF the minimum frequency is PLL_FVCOMIN/2.
3. LVDS receivers are typically bounded with certain applications to achieve maximum performance. Package skews are not included and should be removed through PCB routing.

Table 21: **MIPI D-PHY Performance**

Description	Speed Grade and V_{CCINT} Operating Voltages				Units
	0.90V	0.85V		0.72V	
	-3	-2	-1	-2	
MIPI D-PHY transmitter or receiver.	1500	1500	1260	1260	Mb/s

Table 24: **IOB High Performance (HP) Switching Characteristics *(Cont'd)***

I/O Standards	$T_{INBUF\_DELAY\_PAD\_I}$				$T_{OUTBUF\_DELAY\_O\_PAD}$				$T_{OUTBUF\_DELAY\_TD\_PAD}$				Units
	0.90V	0.85V		0.72V	0.90V	0.85V		0.72V	0.90V	0.85V		0.72V	
	-3	-2	-1	-2	-3	-2	-1	-2	-3	-2	-1	-2	
DIFF_POD10_DCI_F	0.411	0.411	0.430	0.411	0.425	0.425	0.444	0.425	0.555	0.555	0.584	0.555	ns
DIFF_POD10_DCI_M	0.411	0.411	0.430	0.411	0.542	0.542	0.571	0.542	0.640	0.640	0.681	0.640	ns
DIFF_POD10_DCI_S	0.411	0.411	0.430	0.411	0.754	0.754	0.815	0.754	0.850	0.850	0.917	0.850	ns
DIFF_POD10_F	0.411	0.411	0.433	0.411	0.438	0.438	0.459	0.438	0.569	0.569	0.601	0.569	ns
DIFF_POD10_M	0.411	0.411	0.433	0.411	0.538	0.538	0.568	0.538	0.630	0.630	0.667	0.630	ns
DIFF_POD10_S	0.411	0.411	0.433	0.411	0.766	0.766	0.821	0.766	0.836	0.836	0.894	0.836	ns
DIFF_POD12_DCI_F	0.407	0.407	0.432	0.407	0.425	0.425	0.443	0.425	0.558	0.558	0.586	0.558	ns
DIFF_POD12_DCI_M	0.407	0.407	0.432	0.407	0.543	0.543	0.572	0.543	0.638	0.638	0.678	0.638	ns
DIFF_POD12_DCI_S	0.407	0.407	0.432	0.407	0.772	0.772	0.822	0.772	0.862	0.862	0.929	0.862	ns
DIFF_POD12_F	0.409	0.409	0.430	0.409	0.455	0.455	0.476	0.455	0.595	0.595	0.626	0.595	ns
DIFF_POD12_M	0.409	0.409	0.430	0.409	0.551	0.551	0.582	0.551	0.641	0.641	0.679	0.641	ns
DIFF_POD12_S	0.409	0.409	0.430	0.409	0.767	0.767	0.817	0.767	0.832	0.832	0.889	0.832	ns
DIFF_SSTL12_DCI_F	0.381	0.381	0.400	0.381	0.425	0.425	0.443	0.425	0.558	0.558	0.586	0.558	ns
DIFF_SSTL12_DCI_M	0.381	0.381	0.400	0.381	0.557	0.557	0.587	0.557	0.654	0.654	0.694	0.654	ns
DIFF_SSTL12_DCI_S	0.381	0.381	0.400	0.381	0.754	0.754	0.803	0.754	0.842	0.842	0.908	0.842	ns
DIFF_SSTL12_F	0.394	0.394	0.402	0.394	0.412	0.412	0.430	0.412	0.538	0.538	0.566	0.538	ns
DIFF_SSTL12_M	0.394	0.394	0.402	0.394	0.553	0.553	0.584	0.553	0.641	0.641	0.676	0.641	ns
DIFF_SSTL12_S	0.394	0.394	0.402	0.394	0.758	0.758	0.808	0.758	0.823	0.823	0.879	0.823	ns
DIFF_SSTL135_DCI_F	0.371	0.371	0.402	0.371	0.411	0.411	0.428	0.411	0.537	0.537	0.565	0.537	ns
DIFF_SSTL135_DCI_M	0.371	0.371	0.402	0.371	0.551	0.551	0.582	0.551	0.645	0.645	0.685	0.645	ns
DIFF_SSTL135_DCI_S	0.371	0.371	0.402	0.371	0.746	0.746	0.799	0.746	0.829	0.829	0.893	0.829	ns
DIFF_SSTL135_F	0.375	0.375	0.402	0.375	0.408	0.408	0.428	0.408	0.528	0.528	0.561	0.528	ns
DIFF_SSTL135_M	0.375	0.375	0.402	0.375	0.555	0.555	0.585	0.555	0.641	0.641	0.679	0.641	ns
DIFF_SSTL135_S	0.375	0.375	0.402	0.375	0.772	0.772	0.823	0.772	0.827	0.827	0.878	0.827	ns
DIFF_SSTL15_DCI_F	0.397	0.397	0.417	0.397	0.412	0.412	0.429	0.412	0.531	0.531	0.563	0.531	ns
DIFF_SSTL15_DCI_M	0.397	0.397	0.417	0.397	0.553	0.553	0.583	0.553	0.645	0.645	0.685	0.645	ns
DIFF_SSTL15_DCI_S	0.397	0.397	0.417	0.397	0.768	0.768	0.822	0.768	0.847	0.847	0.912	0.847	ns
DIFF_SSTL15_F	0.404	0.404	0.417	0.404	0.424	0.424	0.445	0.424	0.551	0.551	0.577	0.551	ns
DIFF_SSTL15_M	0.404	0.404	0.417	0.404	0.554	0.554	0.585	0.554	0.639	0.639	0.677	0.639	ns
DIFF_SSTL15_S	0.404	0.404	0.417	0.404	0.767	0.767	0.817	0.767	0.813	0.813	0.867	0.813	ns
DIFF_SSTL18_I_DCI_F	0.320	0.320	0.336	0.320	0.445	0.445	0.461	0.445	0.566	0.566	0.595	0.566	ns
DIFF_SSTL18_I_DCI_M	0.320	0.320	0.336	0.320	0.554	0.554	0.585	0.554	0.644	0.644	0.683	0.644	ns
DIFF_SSTL18_I_DCI_S	0.320	0.320	0.336	0.320	0.762	0.762	0.818	0.762	0.837	0.837	0.899	0.837	ns
DIFF_SSTL18_I_F	0.316	0.316	0.336	0.316	0.454	0.454	0.476	0.454	0.578	0.578	0.608	0.578	ns
DIFF_SSTL18_I_M	0.316	0.316	0.336	0.316	0.571	0.571	0.603	0.571	0.652	0.652	0.692	0.652	ns
DIFF_SSTL18_I_S	0.316	0.316	0.336	0.316	0.782	0.782	0.835	0.782	0.816	0.816	0.870	0.816	ns
HSLVDCI_15_F	0.393	0.393	0.415	0.393	0.425	0.425	0.443	0.425	0.548	0.548	0.579	0.548	ns
HSLVDCI_15_M	0.393	0.393	0.415	0.393	0.552	0.552	0.581	0.552	0.644	0.644	0.684	0.644	ns
HSLVDCI_15_S	0.393	0.393	0.415	0.393	0.748	0.748	0.802	0.748	0.827	0.827	0.890	0.827	ns
HSLVDCI_18_F	0.424	0.424	0.447	0.424	0.445	0.445	0.461	0.445	0.566	0.566	0.595	0.566	ns
HSLVDCI_18_M	0.424	0.424	0.447	0.424	0.567	0.567	0.598	0.567	0.658	0.658	0.699	0.658	ns

Table 24: **IOB High Performance (HP) Switching Characteristics *(Cont'd)***

I/O Standards	$T_{INBUF\_DELAY\_PAD\_I}$				$T_{OUTBUF\_DELAY\_O\_PAD}$				$T_{OUTBUF\_DELAY\_TD\_PAD}$				Units
	0.90V	0.85V		0.72V	0.90V	0.85V		0.72V	0.90V	0.85V		0.72V	
	-3	-2	-1	-2	-3	-2	-1	-2	-3	-2	-1	-2	
POD12_DCI_F	0.409	0.409	0.431	0.409	0.425	0.425	0.443	0.425	0.558	0.558	0.586	0.558	ns
POD12_DCI_M	0.409	0.409	0.431	0.409	0.543	0.543	0.572	0.543	0.638	0.638	0.678	0.638	ns
POD12_DCI_S	0.409	0.409	0.431	0.409	0.772	0.772	0.822	0.772	0.862	0.862	0.929	0.862	ns
POD12_F	0.409	0.409	0.431	0.409	0.455	0.455	0.476	0.455	0.595	0.595	0.626	0.595	ns
POD12_M	0.409	0.409	0.431	0.409	0.551	0.551	0.582	0.551	0.641	0.641	0.679	0.641	ns
POD12_S	0.409	0.409	0.431	0.409	0.767	0.767	0.817	0.767	0.832	0.832	0.889	0.832	ns
SLVS_400_18	0.539	0.539	0.620	0.539	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	ns
SSTL12_DCI_F	0.381	0.381	0.399	0.381	0.425	0.425	0.443	0.425	0.558	0.558	0.586	0.558	ns
SSTL12_DCI_M	0.381	0.381	0.399	0.381	0.557	0.557	0.587	0.557	0.654	0.654	0.694	0.654	ns
SSTL12_DCI_S	0.381	0.381	0.399	0.381	0.754	0.754	0.803	0.754	0.842	0.842	0.908	0.842	ns
SSTL12_F	0.403	0.403	0.403	0.403	0.412	0.412	0.430	0.412	0.538	0.538	0.566	0.538	ns
SSTL12_M	0.403	0.403	0.403	0.403	0.553	0.553	0.584	0.553	0.641	0.641	0.676	0.641	ns
SSTL12_S	0.403	0.403	0.403	0.403	0.758	0.758	0.808	0.758	0.823	0.823	0.879	0.823	ns
SSTL135_DCI_F	0.366	0.366	0.399	0.366	0.411	0.411	0.428	0.411	0.537	0.537	0.565	0.537	ns
SSTL135_DCI_M	0.366	0.366	0.399	0.366	0.551	0.551	0.582	0.551	0.645	0.645	0.685	0.645	ns
SSTL135_DCI_S	0.366	0.366	0.399	0.366	0.746	0.746	0.799	0.746	0.829	0.829	0.893	0.829	ns
SSTL135_F	0.378	0.378	0.399	0.378	0.408	0.408	0.428	0.408	0.528	0.528	0.561	0.528	ns
SSTL135_M	0.378	0.378	0.399	0.378	0.555	0.555	0.585	0.555	0.641	0.641	0.679	0.641	ns
SSTL135_S	0.378	0.378	0.399	0.378	0.772	0.772	0.823	0.772	0.827	0.827	0.878	0.827	ns
SSTL15_DCI_F	0.402	0.402	0.417	0.402	0.412	0.412	0.429	0.412	0.531	0.531	0.563	0.531	ns
SSTL15_DCI_M	0.402	0.402	0.417	0.402	0.553	0.553	0.583	0.553	0.645	0.645	0.685	0.645	ns
SSTL15_DCI_S	0.402	0.402	0.417	0.402	0.768	0.768	0.822	0.768	0.847	0.847	0.912	0.847	ns
SSTL15_F	0.371	0.371	0.400	0.371	0.408	0.408	0.428	0.408	0.530	0.530	0.556	0.530	ns
SSTL15_M	0.371	0.371	0.400	0.371	0.554	0.554	0.585	0.554	0.639	0.639	0.677	0.639	ns
SSTL15_S	0.371	0.371	0.400	0.371	0.767	0.767	0.817	0.767	0.813	0.813	0.867	0.813	ns
SSTL18_I_DCI_F	0.329	0.329	0.336	0.329	0.445	0.445	0.461	0.445	0.566	0.566	0.595	0.566	ns
SSTL18_I_DCI_M	0.329	0.329	0.336	0.329	0.554	0.554	0.585	0.554	0.644	0.644	0.683	0.644	ns
SSTL18_I_DCI_S	0.329	0.329	0.336	0.329	0.762	0.762	0.818	0.762	0.837	0.837	0.899	0.837	ns
SSTL18_I_F	0.316	0.316	0.337	0.316	0.454	0.454	0.476	0.454	0.578	0.578	0.608	0.578	ns
SSTL18_I_M	0.316	0.316	0.337	0.316	0.571	0.571	0.603	0.571	0.652	0.652	0.692	0.652	ns
SSTL18_I_S	0.316	0.316	0.337	0.316	0.782	0.782	0.835	0.782	0.816	0.816	0.870	0.816	ns
SUB_LVDS	0.539	0.539	0.620	0.539	0.660	0.660	0.692	0.660	969.863	969.863	969.863	969.863	ns

Table 26: **Input Delay Measurement Methodology *(Cont'd)***

Description	I/O Standard Attribute	V_L (1)(2)	V_H (1)(2)	V_{MEAS} (1)(4)(6)	V_{REF} (1)(3)(5)
DIFF_HSUL, 1.2V	DIFF_HSUL_12	0.6 – 0.25	0.6 + 0.25	0(6)	–
DIFF_SSTL, 1.2V	DIFF_SSTL12	0.6 – 0.25	0.6 + 0.25	0(6)	–
DIFF_SSTL135 and DIFF_SSTL135 class II, 1.35V	DIFF_SSTL135, DIFF_SSTL135_II	0.675 – 0.2875	0.675 + 0.2875	0(6)	–
DIFF_SSTL15 and DIFF_SSTL15 class II, 1.5V	DIFF_SSTL15, DIFF_SSTL15_II	0.75 – 0.325	0.75 + 0.325	0(6)	–
DIFF_SSTL18_I, DIFF_SSTL18_II, 1.8V	DIFF_SSTL18_I, DIFF_SSTL18_II	0.9 – 0.4	0.9 + 0.4	0(6)	–
DIFF_POD10, 1.0V	DIFF_POD10	0.5 – 0.2	0.5 + 0.2	0(6)	–
DIFF_POD12, 1.2V	DIFF_POD12	0.6 – 0.25	0.6 + 0.25	0(6)	–
LVDS (low-voltage differential signaling), 1.8V	LVDS	0.9 – 0.125	0.9 + 0.125	0(6)	–
SUB_LVDS, 1.8V	SUB_LVDS	0.9 – 0.125	0.9 + 0.125	0(6)	–
SLVS, 1.8V	SLVS_400_18	0.9 – 0.125	0.9 + 0.125	0(6)	–
MIPI D-PHY (high speed) 1.2V	MIPI_DPHY_DCI_HS	0.2 – 0.125	0.2 + 0.125	0(6)	–
MIPI D-PHY (low power) 1.2V	MIPI_DPHY_DCI_LP	0.715 – 0.2	0.715 + 0.2	0(6)	–

Notes:

1. The input delay measurement methodology parameters for LVDCI/HSLVDCI are the same for LVCMOS standards of the same voltage. Parameters for all other DCI standards are the same for the corresponding non-DCI standards.
2. Input waveform switches between V_L and V_H.
3. Measurements are made at typical, minimum, and maximum V_{REF} values. Reported delays reflect worst case of these measurements. V_{REF} values listed are typical.
4. Input voltage level from which measurement starts.
5. This is an input voltage reference that bears no relation to the V_{REF}/V_{MEAS} parameters found in IBIS models and/or noted in Figure 1.
6. The value given is the differential input voltage.

Block RAM and FIFO Switching Characteristics

Table 28: **Block RAM and FIFO Switching Characteristics**

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages				Units
		0.90V	0.85V		0.72V	
		-3	-2	-1	-2	
Maximum Frequency						
$F_{MAX\_WF\_NC}$	Block RAM (WRITE_FIRST and NO_CHANGE modes).	825	737	645	585	MHz
F_{MAX_RF}	Block RAM (READ_FIRST mode).	718	637	575	510	MHz
F_{MAX_FIFO}	FIFO in all modes without ECC.	825	737	645	585	MHz
F_{MAX_ECC}	Block RAM and FIFO in ECC configuration without PIPELINE.	718	637	575	510	MHz
	Block RAM and FIFO in ECC configuration with PIPELINE and Block RAM in WRITE_FIRST or NO_CHANGE mode.	825	737	645	585	MHz
T_{PW}[(1)]	Minimum pulse width.	495	542	543	577	ps
Block RAM and FIFO Clock-to-Out Delays						
T_{RCKO_DO}	Clock CLK to DOUT output (without output register).	0.91	1.02	1.11	1.46	ns, Max
$T_{RCKO\_DO\_REG}$	Clock CLK to DOUT output (with output register).	0.27	0.29	0.30	0.42	ns, Max

Notes:

1. The MMCM and PLL DUTY_CYCLE attribute should be set to 50% to meet the pulse-width requirements at the higher frequencies.

UltraRAM Switching Characteristics

Table 29: **UltraRAM Switching Characteristics**

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages				Units
		0.90V	0.85V		0.72V	
		-3	-2	-1	-2	
Maximum Frequency						
F_{MAX}	UltraRAM maximum frequency with OREG_B = True.	650	600	575	500	MHz
F_{MAX_ECC}	UltraRAM maximum frequency OREG_B = False and EN_ECC_RD_B = True.	450	400	386	325	MHz
$F_{MAX\_NORPIPELINE}$	UltraRAM maximum frequency with OREG_B = False and EN_ECC_RD_B = False.	550	500	478	425	MHz
T_{PW}[(1)]	Minimum pulse width.	650	700	730	800	ps
T_{RSTPW}	Asynchronous reset minimum pulse width. One cycle required.	1 clock cycle				ps

Notes:

1. The MMCM and PLL DUTY_CYCLE attribute should be set to 50% to meet the pulse-width requirements at the higher frequencies.

PLL Switching Characteristics

Table 34: **PLL Specification(1)**

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages				Units
		0.90V	0.85V		0.72V	
		-3	-2	-1	-2	
PLL_F_{INMAX}	Maximum input clock frequency.	1066	933	800	933	MHz
PLL_F_{INMIN}	Minimum input clock frequency.	70	70	70	70	MHz
PLL_$F_{INJITTER}$	Maximum input clock period jitter.	< 20% of clock input period or 1 ns Max				
PLL_F_{INDUTY}	Input duty cycle range: 70–399 MHz.	35–65				%
	Input duty cycle range: 400–499 MHz.	40–60				%
	Input duty cycle range: >500 MHz.	45–55				%
PLL_F_{VCOMIN}	Minimum PLL VCO frequency.	750	750	750	750	MHz
PLL_F_{VCOMAX}	Maximum PLL VCO frequency.	1500	1500	1500	1500	MHz
PLL_$T_{STATPHAOFFSET}$	Static phase offset of the PLL outputs.(2)	0.12	0.12	0.12	0.12	ns
PLL_$T_{OUTJITTER}$	PLL output jitter.	Note 3				
PLL_$T_{OUTDUTY}$	PLL CLKOUT0, CLKOUT0B, CLKOUT1, CLKOUT1B duty-cycle precision.(4)	0.165	0.20	0.20	0.20	ns
PLL_$T_{LOCKMAX}$	PLL maximum lock time.	100				µs
PLL_F_{OUTMAX}	PLL maximum output frequency at CLKOUT0, CLKOUT0B, CLKOUT1, CLKOUT1B.	891	775	667	725	MHz
	PLL maximum output frequency at CLKOUTPHY.	2667	2667	2400	2400	MHz
PLL_F_{OUTMIN}	PLL minimum output frequency at CLKOUT0, CLKOUT0B, CLKOUT1, CLKOUT1B.(5)	5.86	5.86	5.86	5.86	MHz
	PLL minimum output frequency at CLKOUTPHY.	2 x VCO mode: 1500 1 x VCO mode: 750 0.5 x VCO mode: 375				MHz
PLL_$RST_{MINPULSE}$	Minimum reset pulse width.	5.00	5.00	5.00	5.00	ns
PLL_F_{PFDMAX}	Maximum frequency at the phase frequency detector.	667.5	667.5	667.5	667.5	MHz
PLL_F_{PFDMIN}	Minimum frequency at the phase frequency detector.	70	70	70	70	MHz
PLL_$F_{BANDWIDTH}$	PLL bandwidth at typical.	14	14	14	14	MHz
PLL_F_{DPRCLK_MAX}	Maximum DRP clock frequency	250	250	250	250	MHz

Notes:

1. The PLL does not filter typical spread-spectrum input clocks because they are usually far below the loop filter frequencies.
2. The static offset is measured between any PLL outputs with identical phase.
3. Values for this parameter are available in the Clocking Wizard.
4. Includes global clock buffer.
5. Calculated as $F_{VCO}/128$ assuming output duty cycle is 50%.

Table 37: **Global Clock Input to Output Delay With MMCM**

Symbol	Description	Device	Speed Grade and V_{CCINT} Operating Voltages				Units
			0.90V	0.85V		0.72V	
			-3	-2	-1	-2	
SSTL15 Global Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, with MMCM.							
$T_{ICKOFMMCMCC}$	Global clock input and output flip-flop *with* MMCM.	XCVU3P	1.80	1.80	1.94	2.34	ns
		XCVU5P	1.80	1.80	1.94	2.34	ns
		XCVU7P	1.80	1.80	1.94	2.34	ns
		XCVU9P	1.80	1.80	1.94	2.34	ns
		XCVU11P	1.56	1.56	1.68	2.07	ns
		XCVU13P	1.56	1.56	1.68	2.07	ns

Notes:

1. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible I/O and CLB flip-flops are clocked by the global clock net in a single SLR.
2. MMCM output jitter is already included in the timing calculation.

Device Pin-to-Pin Input Parameter Guidelines

The pin-to-pin numbers in Table 38 are based on the clock root placement in the center of the device. The actual pin-to-pin values will vary if the root placement selected is different. Consult the Vivado Design Suite timing report for the actual pin-to-pin values.

Table 38: **Global Clock Input Setup and Hold With MMCM**

Symbol	Description		Device	Speed Grade and V_{CCINT} Operating Voltages				Units
				0.90V	0.85V		0.72V	
				-3	-2	-1	-2	
Input Setup and Hold Time Relative to Global Clock Input Signal using SSTL15 Standard.(1)(2)(3)								
$T_{PSMMCMCC\_VU3P}$	Global clock input and input flip-flop (or latch) with MMCM.	Setup	XCVU3P	1.86	1.86	1.99	2.32	ns
$T_{PHMMCMCC\_VU3P}$		Hold		–0.13	–0.13	–0.13	0.14	ns
$T_{PSMMCMCC\_VU5P}$		Setup	XCVU5P	1.86	1.86	1.99	2.32	ns
$T_{PHMMCMCC\_VU5P}$		Hold		–0.13	–0.13	–0.13	0.14	ns
$T_{PSMMCMCC\_VU7P}$		Setup	XCVU7P	1.86	1.86	1.99	2.32	ns
$T_{PHMMCMCC\_VU7P}$		Hold		–0.13	–0.13	–0.13	0.14	ns
$T_{PSMMCMCC\_VU9P}$		Setup	XCVU9P	1.86	1.86	1.99	2.32	ns
$T_{PHMMCMCC\_VU9P}$		Hold		–0.13	–0.13	–0.13	0.14	ns
$T_{PSMMCMCC\_VU11P}$		Setup	XCVU11P	1.92	1.92	2.05	2.36	ns
$T_{PHMMCMCC\_VU11P}$		Hold		–0.13	–0.13	–0.13	0.16	ns
$T_{PSMMCMCC\_VU13P}$		Setup	XCVU13P	1.92	1.92	2.05	2.36	ns
$T_{PHMMCMCC\_VU13P}$		Hold		–0.13	–0.13	–0.13	0.16	ns

Notes:

1. Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, slowest temperature, and slowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, fastest temperature, and fastest voltage.
2. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible I/O and CLB flip-flops are clocked by the global clock net in a single SLR.
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 39: **Sampling Window**

Description	Speed Grade and V_{CCINT} Operating Voltages				Units
	0.90V	0.85V		0.72V	
	-3	-2	-1	-2	
T_{SAMP_BUFG}(1)	510	610	610	610	ps
$T_{SAMP\_NATIVE\_DPA}$	100	100	125	125	ps
$T_{SAMP\_NATIVE\_BISC}$	60	60	85	85	ps

Notes:

1. This parameter indicates the total sampling error of the Virtex UltraScale+ FPGA DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the MMCM to capture the DDR input registers' edges of operation. These measurements include: CLK0 MMCM jitter, MMCM accuracy (phase offset), and MMCM phase shift resolution. These measurements do not include package or clock tree skew.

Table 48: **GTY Transceiver PLL/Lock Time Adaptation**

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
T_{LOCK}	Initial PLL lock.		–	–	1	ms
T_{DLOCK}	Clock recovery phase acquisition and adaptation time for decision feedback equalizer (DFE).	After the PLL is locked to the reference clock, this is the time it takes to lock the clock data recovery (CDR) to the data present at the input.	–	50,000	37×10^6	UI
	Clock recovery phase acquisition and adaptation time for low-power mode (LPM) when the DFE is disabled.		–	50,000	2.3×10^6	UI

Table 49: **GTY Transceiver User Clock Switching Characteristics(1)**

Symbol	Description	Data Width Conditions (Bit)		Speed Grade and V_{CCINT} Operating Voltages				Units
				0.90V	0.85V		0.72V	
		Internal Logic	Interconnect Logic	-3	-2	-1	-2	
$F_{TXOUTPMA}$	TXOUTCLK maximum frequency sourced from OUTCLKPMA			511.719	511.719	402.833	402.833	MHz
$F_{RXOUTPMA}$	RXOUTCLK maximum frequency sourced from OUTCLKPMA			511.719	511.719	402.833	402.833	MHz
$F_{TXOUTPROGDIV}$	TXOUTCLK maximum frequency sourced from TXPROGDIVCLK			511.719	511.719	511.719	511.719	MHz
$F_{RXOUTPROGDIV}$	RXOUTCLK maximum frequency sourced from RXPROGDIVCLK			511.719	511.719	511.719	511.719	MHz
F_{TXIN}	TXUSRCLK(2) maximum frequency	16	16, 32	511.719	511.719	390.625	390.625	MHz
		32	32, 64	511.719	511.719	390.625	390.625	MHz
		64	64, 128	511.719	440.781	402.832	402.832	MHz
		20	20, 40	409.375	409.375	312.500	312.500	MHz
		40	40, 80	409.375	409.375	312.500	350.000	MHz
		80	80, 160	409.375	352.625	322.266	352.625	MHz
F_{RXIN}	RXUSRCLK(2) maximum frequency	16	16, 32	511.719	511.719	390.625	390.625	MHz
		32	32, 64	511.719	511.719	390.625	390.625	MHz
		64	64, 128	511.719	440.781	402.832	402.832	MHz
		20	20, 40	409.375	409.375	312.500	312.500	MHz
		40	40, 80	409.375	409.375	312.500	350.000	MHz
		80	80, 160	409.375	352.625	322.266	352.625	MHz

Table 49: **GTY Transceiver User Clock Switching Characteristics(1) *(Cont'd)***

Symbol	Description	Data Width Conditions (Bit)		Speed Grade and V_{CCINT} Operating Voltages				Units
				0.90V	0.85V		0.72V	
		Internal Logic	Interconnect Logic	-3	-2	-1	-2	
F_{TXIN2}	TXUSRCLK2(2) maximum frequency	16	16	511.719	511.719	390.625	390.625	MHz
		16	32	255.859	255.859	195.313	195.313	MHz
		32	32	511.719	511.719	390.625	390.625	MHz
		32	64	255.859	255.859	195.313	195.313	MHz
		64	64	511.719	440.781	402.832	402.832	MHz
		64	128	255.859	220.391	201.416	201.416	MHz
		20	20	409.375	409.375	312.500	312.500	MHz
		20	40	204.688	204.688	156.250	156.250	MHz
		40	40	409.375	409.375	312.500	350.000	MHz
		40	80	204.688	204.688	156.250	175.000	MHz
		80	80	409.375	352.625	322.266	352.625	MHz
		80	160	204.688	176.313	161.133	176.313	MHz
F_{RXIN2}	RXUSRCLK2(2) maximum frequency	16	16	511.719	511.719	390.625	390.625	MHz
		16	32	255.859	255.859	195.313	195.313	MHz
		32	32	511.719	511.719	390.625	390.625	MHz
		32	64	255.859	255.859	195.313	195.313	MHz
		64	64	511.719	440.781	402.832	402.832	MHz
		64	128	255.859	220.391	201.416	201.416	MHz
		20	20	409.375	409.375	312.500	312.500	MHz
		20	40	204.688	204.688	156.250	156.250	MHz
		40	40	409.375	409.375	312.500	350.000	MHz
		40	80	204.688	204.688	156.250	175.000	MHz
		80	80	409.375	352.625	322.266	352.625	MHz
		80	160	204.688	176.313	161.133	176.313	MHz

Notes:

1. Clocking must be implemented as described in the *UltraScale Architecture GTY Transceiver User Guide* (UG578).
2. When the gearbox is used, these maximums refer to the XCLK. For more information, see the *Valid Data Width Combinations for TX Asynchronous Gearbox* table in the *UltraScale Architecture GTY Transceiver User Guide* (UG578).

Table 50: **GTY Transceiver Transmitter Switching Characteristics *(Cont'd)***

Symbol	Description	Condition	Min	Typ	Max	Units
$T_{J3.20}$	Total jitter(3)(4)	3.20 Gb/s(5)	–	–	0.20	UI
$D_{J3.20}$	Deterministic jitter(3)(4)		–	–	0.10	UI
$T_{J2.5}$	Total jitter(3)(4)	2.5 Gb/s(6)	–	–	0.20	UI
$D_{J2.5}$	Deterministic jitter(3)(4)		–	–	0.10	UI
$T_{J1.25}$	Total jitter(3)(4)	1.25 Gb/s(7)	–	–	0.15	UI
$D_{J1.25}$	Deterministic jitter(3)(4)		–	–	0.06	UI
T_{J500}	Total jitter(3)(4)	500 Mb/s(8)	–	–	0.10	UI
D_{J500}	Deterministic jitter(3)(4)		–	–	0.03	UI

Notes:

1. Using same REFCLK input with TX phase alignment enabled for up to four consecutive transmitters (one fully populated GTY Quad) at maximum line rate.
2. Using QPLL_FBDIV = 40, 20-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
3. Using CPLL_FBDIV = 2, 20-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
4. All jitter values are based on a bit-error ratio of 10^{-12}.
5. CPLL frequency at 3.2 GHz and TXOUT_DIV = 2.
6. CPLL frequency at 2.5 GHz and TXOUT_DIV = 2.
7. CPLL frequency at 2.5 GHz and TXOUT_DIV = 4.
8. CPLL frequency at 2.0 GHz and TXOUT_DIV = 8.

Integrated Interface Block for Interlaken

More information and documentation on solutions using the integrated interface block for Interlaken can be found at UltraScale Interlaken. The *UltraScale Architecture and Product Overview* (DS890) lists how many blocks are in each Virtex UltraScale+ FPGA. This section describes the following Interlaken configurations.

- 12 x 12.5 Gb/s protocol and lane logic mode (Table 53).
- 6 x 25.78125 Gb/s and 6 x 28.21 Gb/s protocol and lane logic mode (Table 54).
- 12 x 25.78125 Gb/s lane logic only mode (Table 55).

XCVU11P devices in the FLVF1924 package are only supported using the 12 x 12.5 Gb/s Interlaken configuration. See Table 44 for the F_{GTYMAX} description.

Table 53: **Maximum Performance for Interlaken 12 x 12.5 Gb/s Protocol and Lane Logic Mode Designs**

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages										Units
		0.90V		0.85V				0.72V				
		-3		-2		-1		-2		-1		
$F_{RX\_SERDES\_CLK}$	Receive serializer/ deserializer clock	195.32		195.32		195.32		195.32		195.32		MHz
$F_{TX\_SERDES\_CLK}$	Transmit serializer/ deserializer clock	195.32		195.32		195.32		195.32		195.32		MHz
F_{DRP_CLK}	Dynamic reconfiguration port clock	250.00		250.00		250.00		250.00		250.00		MHz
		Min(1)	Max	Min(1)	Max	Min(1)	Max	Min(1)	Max	Min(1)	Max	
F_{CORE_CLK}	Interlaken core clock	300.00	322.27	300.00	322.27	300.00	322.27	300.00	322.27	300.00	322.27	MHz
F_{LBUS_CLK}	Interlaken local bus clock	300.00	322.27	300.00	322.27	300.00	322.27	300.00	322.27	300.00	322.27	MHz

Notes:

1. These are the minimum clock frequencies at the maximum lane performance.

System Monitor Specifications

Table 58: **System Monitor Specifications**

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
V_{CCADC} = 1.8V ±3%, V_{REFP} = 1.25V, V_{REFN} = 0V, ADCCLK = 5.2 MHz, T_j = –40°C to 100°C, typical values at T_j = 40°C						
ADC Accuracy(1)						
Resolution			10	–	–	Bits
Integral nonlinearity(2)	INL		–	–	±1.5	LSBs
Differential nonlinearity	DNL	No missing codes, guaranteed monotonic	–	–	±1	LSBs
Offset error		Offset calibration enabled	–	–	±2	LSBs
Gain error			–	–	±0.4	%
Sample rate			–	–	0.2	MS/s
RMS code noise		External 1.25V reference	–	–	1	LSBs
		On-chip reference	–	1	–	LSBs
ADC Accuracy at Extended Temperatures						
Resolution		T_j = –55°C to 125°C	10	–	–	Bits
Integral nonlinearity	INL	T_j = –55°C to 125°C	–	–	±1.5	LSBs
Differential nonlinearity	DNL	No missing codes, guaranteed monotonic T_j = –55°C to 125°C	–	–	±1	
Analog Inputs(2)						
ADC input ranges		Unipolar operation	0	–	1	V
		Bipolar operation	–0.5	–	+0.5	V
		Unipolar common mode range (FS input)	0	–	+0.5	V
		Bipolar common mode range (FS input)	+0.5	–	+0.6	V
Maximum external channel input ranges		Adjacent channels set within these ranges should not corrupt measurements on adjacent channels	–0.1	–	V_{CCADC}	V
On-Chip Sensor Accuracy						
Temperature sensor error(1)(3)		T_j = –55°C to 125°C (with external REF)	–	–	±3	°C
		T_j = –55°C to 110°C (with internal REF)	–	–	±3.5	°C
		T_j = 110°C to 125°C (with internal REF)	–	–	±5	°C

Configuration Switching Characteristics

Table 61: **Configuration Switching Characteristics**

Symbol	Description		Speed Grade and V_{CCINT} Operating Voltages				Units
			0.90V	0.85V		0.72V	
			-3	-2	-1	-2	
Power-up Timing Characteristics							
T_{PL}	Program latency.		8.5	8.5	8.5	8.5	ms, Max
T_{POR}	Power-on reset (40 ms maximum ramp rate).		65	65	65	65	ms, Max
			0	0	0	0	ms, Min
	Power-on reset with POR override (2 ms maximum ramp rate).		15	15	15	15	ms, Max
			5	5	5	5	ms, Min
$T_{PROGRAM}$	Program pulse width.		250	250	250	250	ns, Min
CCLK Output (Master Mode)							
T_{ICCK}	Master CCLK output delay from INIT_B.		150	150	150	150	ns, Min
T_{MCCKL} (1)	Master CCLK clock Low time duty cycle.		40/60	40/60	40/60	40/60	%, Min/Max
T_{MCCKH}	Master CCLK clock High time duty cycle.		40/60	40/60	40/60	40/60	%, Min/Max
F_{MCCK}	Master SPI/BPI CCLK frequency.		125	125	125	100	MHz, Max
F_{MCCK_START}	Master CCLK frequency at start of configuration.		2.70	2.70	2.70	2.70	MHz, Typ
$F_{MCCKTOL}$	Frequency tolerance, master mode with respect to nominal CCLK.		±15	±15	±15	±15	%, Max
CCLK Input (Slave Mode)							
T_{SCCKL}	Slave CCLK clock minimum Low time.		2.5	2.5	2.5	2.5	ns, Min
T_{SCCKH}	Slave CCLK clock minimum High time.		2.5	2.5	2.5	2.5	ns, Min
F_{SCCK}	Slave serial SelectMap CCLK frequency.	XCVU3P, XCVU5P, XCVU7P, XCVU9P	125	125	125	100	MHz, Max
		XCVU11P, XCVU13P	125	125	125	66	MHz, Max
EMCCLK Input (Master Mode)							
T_{EMCCKL}	External master CCLK Low time.		2.5	2.5	2.5	2.5	ns, Min
T_{EMCCKH}	External master CCLK High time.		2.5	2.5	2.5	2.5	ns, Min
F_{EMCCK}	External master CCLK frequency.		125	125	125	100	MHz, Max
Internal Configuration Access Port							
F_{ICAPCK}	Internal configuration access port (ICAPE3).	XCVU3P	200	200	200	150	MHz, Max
	Master SLR ICAPE3 accessing entire device.	XCVU5P, XCVU7P, XCVU9P, XCVU11P, XCVU13P	125	125	125	100	MHz, Max
	SLR ICAPE3 accessing local SLR.	XCVU5P, XCVU7P, XCVU9P, XCVU11P, XCVU13P	200	200	200	150	MHz, Max
Slave Serial Mode Programming Switching							
T_{DCCK}/T_{CCKD}	D_{IN} setup/hold.		3.0/0	3.0/0	3.0/0	4.0/0	ns, Min
T_{CCO}	D_{OUT} clock to out.		8.0	8.0	8.0	9.0	ns, Max