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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	98520
Number of Logic Elements/Cells	1724100
Total RAM Bits	260812800
Number of I/O	416
Number of Gates	-
Voltage - Supply	0.873V ~ 0.927V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 100°C (TJ)
Package / Case	2104-BBGA, FCBGA
Supplier Device Package	2104-FCBGA (47.5x47.5)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xcvu7p-3flvc2104e

Table 1: **Absolute Maximum Ratings(1) *(Cont'd)***

Symbol	Description	Min	Max	Units
I_{RMS}	Available RMS output current at the pad.	–20	20	mA
GTY Transceivers				
$V_{MGTAVCC}$	Analog supply voltage for transceiver circuits.	–0.500	1.000	V
$V_{MGTAVTT}$	Analog supply voltage for transceiver termination circuits.	–0.500	1.300	V
$V_{MGTVCCAUX}$	Auxiliary analog Quad PLL (QPLL) voltage supply for transceivers.	–0.500	1.900	V
$V_{MGTREFCLK}$	Transceiver reference clock absolute input voltage.	–0.500	1.300	V
$V_{MGTAVTTRCAL}$	Analog supply voltage for the resistor calibration circuit of the transceiver column.	–0.500	1.300	V
V_{IN}	Receiver (RXP/RXN) and transmitter (TXP/TXN) absolute input voltage.	–0.500	1.200	V
$I_{DCIN-FLOAT}$	DC input current for receiver input pins DC coupled RX termination = floating.(7)	–	10	mA
$I_{DCIN-MGTAVTT}$	DC input current for receiver input pins DC coupled RX termination = $V_{MGTAVTT}$.	–	10	mA
$I_{DCIN-GND}$	DC input current for receiver input pins DC coupled RX termination = GND.(8)	–	0	mA
$I_{DCIN-PROG}$	DC input current for receiver input pins DC coupled RX termination = programmable.(9)	–	0	mA
$I_{DCOUT-FLOAT}$	DC output current for transmitter pins DC coupled RX termination = floating.	–	6	mA
$I_{DCOUT-MGTAVTT}$	DC output current for transmitter pins DC coupled RX termination = $V_{MGTAVTT}$.	–	6	mA
System Monitor				
V_{CCADC}	System Monitor supply relative to GNDADC.	0.500	2.000	V
V_{REFP}	System Monitor reference input relative to GNDADC.	0.500	2.000	V
Temperature				
T_{STG}	Storage temperature (ambient).	–65	150	°C
T_{SOL}	Maximum soldering temperature.(11)	–	260	°C
T_j	Maximum junction temperature.(11)	–	125	°C

Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.
2. V_{CCINT_IO} must be connected to V_{CCBRAM}.
3. V_{CCAUX_IO} must be connected to V_{CCAUX}.
4. The lower absolute voltage specification always applies.
5. For I/O operation, see the *UltraScale Architecture SelectIO Resources User Guide* (UG571).
6. When operating outside of the recommended operating conditions, refer to Table 4 for maximum overshoot and undershoot specifications.
7. AC coupled operation is not supported for RX termination = floating.
8. For GTY transceivers, DC coupled operation is not supported for RX termination = GND.
9. DC coupled operation is not supported for RX termination = programmable.
10. For more information on supported GTY transceiver terminations see the or *UltraScale Architecture GTY Transceiver User Guide* (UG578)
11. For soldering guidelines and thermal considerations, see the *UltraScale and UltraScale+ FPGA Packaging and Pinout Specifications* (UG575).

Table 2: **Recommended Operating Conditions(1)(2) *(Cont'd)***

Symbol	Description	Min	Typ	Max	Units
SYSMON					
V_{CCADC}	SYSMON supply relative to GNDADC.	1.746	1.800	1.854	V
V_{REFP}	SYSMON externally supplied reference voltage relative to GNDADC.	1.200	1.250	1.300	V
Temperature					
T_j(11)	Junction temperature operating range for extended (E) temperature devices.(12)	0	–	100	°C
	Junction temperature operating range for industrial (I) temperature devices.	–40	–	100	°C
	Junction temperature operating range for eFUSE programming.(13)	–40	–	125	°C

Notes:

1. All voltages are relative to GND.
2. For the design of the power distribution system consult *UltraScale Architecture PCB Design Guide* (UG583).
3. V_{CCINT_IO} must be connected to V_{CCBRAM}.
4. For V_{CCO_0}, the minimum recommended operating voltage for power on and during configuration is 1.425V. After configuration, data is retained even if V_{CCO} drops to 0V.
5. Includes V_{CCO} of 1.0V, 1.2V, 1.35V, 1.5V, and 1.8V.
6. V_{CCAUX_IO} must be connected to V_{CCAUX}.
7. The lower absolute voltage specification always applies.
8. A total of 200 mA per bank should not be exceeded.
9. If battery is not used, connect V_{BATT} to either GND or V_{CCAUX}.
10. Each voltage listed requires filtering as described in the *UltraScale Architecture GTY Transceiver User Guide* (UG578).
11. Xilinx recommends measuring the Tj of a device using the system monitor as described in the *UltraScale Architecture System Monitor User Guide* (UG580). The SYSMON temperature measurement errors (that are described in Table 58) must be accounted for in your design. For example, by using an external reference of 1.25V, when SYSMON reports 97°C, there is a measurement error ±3°C. A reading of 97°C is considered the maximum adjusted Tj (100°C – 3°C = 97°C).
12. Devices labeled with the speed/temperature grade of -2LE can operate for a limited time at a junction temperature of 110°C. Timing parameters adhere to the same speed file at 110°C as they do below 110°C, regardless of operating voltage (nominal voltage of 0.85V or a low-voltage of 0.72V). Operation at Tj = 110°C is limited to 1% of the device lifetime and can occur sequentially or at regular intervals as long as the total time does not exceed 1% of the device lifetime.
13. Do not program eFUSE during device configuration (e.g., during configuration, during configuration readback, or when readback CRC is active).

Table 13: **DC Output Levels for Single-ended and Differential POD10 and POD12 Standards(1)(2)**

Symbol	Description	V_{OUT}	Min	Typ	Max	Units
R_{OL}	Pull-down resistance.	V_{OM_DC} (as described in Table 14)	36	40	44	Ω
R_{OH}	Pull-up resistance.	V_{OM_DC} (as described in Table 14)	36	40	44	Ω

Notes:

1. Tested according to relevant specifications.
2. Standards specified using the default I/O standard configuration. For details, see the *UltraScale Architecture SelectIO Resources User Guide* (UG571).

Table 14: **Table 13 Definitions for DC Output Levels for POD Standards**

Symbol	Description	All Speed Grades	Units
V_{OM_DC}	DC output Mid measurement level (for IV curve linearity).	0.8 x V_{CCO}	V

LVDS DC Specifications (LVDS)

Table 15: **LVDS DC Specifications**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{CCO}(1)	Supply voltage.		1.710	1.800	1.890	V
V_{ODIFF}(2)	Differential output voltage: ($\underline{Q}$ – $\overline{Q}$), $\underline{Q}$ = High ($\underline{Q}$ – $\overline{Q}$), $\overline{Q}$ = High	R_T = 100Ω across Q and $\overline{Q}$ signals	247	350	454	mV
V_{OCM}(2)	Output common-mode voltage.	R_T = 100 Ω across Q and $\overline{Q}$ signals	1.000	1.250	1.425	V
V_{IDIFF}	Differential input voltage: ($\underline{Q}$ – $\overline{Q}$), $\underline{Q}$ = High ($\underline{Q}$ – $\overline{Q}$), $\overline{Q}$ = High		100	350	600(3)	mV
V_{ICM_DC}(4)	Input common-mode voltage (DC coupling).		0.300	1.200	1.425	V
V_{ICM_AC}(5)	Input common-mode voltage (AC coupling).		0.600	–	1.100	V

Notes:

1. In I/O banks, when LVDS is used with input-only functionality, it can be placed in a bank where the V_{CCO} levels are different from the specified level only if internal differential termination is not used. In this scenario, V_{CCO} must be chosen to ensure the input pin voltage levels do not violate the *Recommended Operating Condition* (Table 2) specification for the V_{IN} I/O pin voltage.
2. V_{OCM} and V_{ODIFF} values are for LVDS_PRE_EMPHASIS = FALSE.
3. Maximum V_{IDIFF} value is specified for the maximum V_{ICM} specification. With a lower V_{ICM}, a higher V_{DIFF} is tolerated only when the recommended operating conditions and overshoot/undershoot V_{IN} specifications are maintained.
4. Input common mode voltage for DC coupled configurations. EQUALIZATION = EQ_NONE (Default).
5. External input common mode voltage specification for AC coupled configurations. EQUALIZATION = EQ_LEVEL0, EQ_LEVEL1, EQ_LEVEL2, EQ_LEVEL3, EQ_LEVEL4.

AC Switching Characteristics

All values represented in this data sheet are based on the speed specifications in the Vivado® Design Suite as outlined in Table 16.

Table 16: **Speed Specification Version By Device**

2017.1	Device
1.10	XCVU3P, XCVU7P, XCVU9P, XCVU5P, XCVU11P, XCVU13P

Switching characteristics are specified on a per-speed-grade basis and can be designated as Advance, Preliminary, or Production. Each designation is defined as follows:

Advance Product Specification

These specifications are based on simulations only and are typically available soon after device design specifications are frozen. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

Preliminary Product Specification

These specifications are based on complete ES (engineering sample) silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting delays is greatly reduced as compared to Advance data.

Product Specification

These specifications are released once enough production silicon of a particular device family member has been characterized to provide full correlation between specifications and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to production before faster speed grades.

Testing of AC Switching Characteristics

Internal timing parameters are derived from measuring internal test patterns. All AC switching characteristics are representative of worst-case supply voltage and junction temperature conditions.

For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer and back-annotate to the simulation net list. Unless otherwise noted, values apply to all Virtex UltraScale+ FPGAs.

Production Silicon and Software Status

In some cases, a particular family member (and speed grade) is released to production before a speed specification is released with the correct label (Advance, Preliminary, Production). Any labeling discrepancies are corrected in subsequent speed specification releases.

Table 18 lists the production released Virtex UltraScale+ FPGA, speed grade, and the minimum corresponding supported speed specification version and Vivado software revisions. The Vivado software and speed specifications listed are the minimum releases required for production. All subsequent releases of software and speed specifications are valid.

Table 18: **Virtex UltraScale+ FPGA Device Production Software and Speed Specification Release**

Device	Speed Grade and V_{CCINT} Operating Voltages				
	0.90V	0.85V			0.72V
	-3	-2	-1	-2L	-2L
XCVU3P		Vivado tools 2017.1 v1.10			
XCVU5P					
XCVU7P					
XCVU9P					
XCVU11P					
XCVU13P					

Notes:

1. Blank entries indicate a device and/or speed grade in Advance or Preliminary status.

FPGA Logic Performance Characteristics

This section provides the performance characteristics of some common functions and designs implemented in Virtex UltraScale+ FPGAs. These values are subject to the same guidelines as the AC Switching Characteristics, page 13.

Table 19: **LVDS Component Mode Performance**

Description	Speed Grade and V_{CCINT} Operating Voltages								Units
	0.90V		0.85V				0.72V		
	-3		-2		-1		-2		
	Min	Max	Min	Max	Min	Max	Min	Max	
LVDS TX DDR (OSERDES 4:1, 8:1)	0	1250	0	1250	0	1250	0	1250	Mb/s
LVDS TX SDR (OSERDES 2:1, 4:1)	0	625	0	625	0	625	0	625	Mb/s
LVDS RX DDR (ISERDES 1:4, 1:8)(1)	0	1250	0	1250	0	1250	0	1250	Mb/s
LVDS RX SDR (ISERDES 1:2, 1:4)(1)	0	625	0	625	0	625	0	625	Mb/s

Notes:

1. LVDS receivers are typically bounded with certain applications to achieve maximum performance. Package skews are not included and should be removed through PCB routing.

Table 20: **LVDS Native Mode Performance(1)(2)**

Description	DATA_WIDTH	Speed Grade and V_{CCINT} Operating Voltages								Units
		0.90V		0.85V				0.72V		
		-3		-2		-1		-2		
		Min	Max	Min	Max	Min	Max	Min	Max	
LVDS TX DDR (TX_BITSLICE)	4	375	1600	375	1600	375	1260	375	1400	Mb/s
	8	375	1600	375	1600	375	1260	375	1600	Mb/s
LVDS TX SDR (TX_BITSLICE)	4	187.5	800	187.5	800	187.5	630	187.5	700	Mb/s
	8	187.5	800	187.5	800	187.5	630	187.5	800	Mb/s
LVDS RX DDR (RX_BITSLICE)(3)	4	375	1600	375	1600	375	1260	375	1400	Mb/s
	8	375	1600	375	1600	375	1260	375	1600	Mb/s
LVDS RX SDR (RX_BITSLICE)(3)	4	187.5	800	187.5	800	187.5	630	187.5	700	Mb/s
	8	187.5	800	187.5	800	187.5	630	187.5	800	Mb/s

Notes:

1. Native mode is supported through the High-Speed SelectIO Interface Wizard available with the Vivado Design Suite.
2. PLL settings can restrict the minimum allowable data rate. For example, when using the PLL with CLKOUTPHY_MODE = VCO_HALF the minimum frequency is PLL_FVCOMIN/2.
3. LVDS receivers are typically bounded with certain applications to achieve maximum performance. Package skews are not included and should be removed through PCB routing.

Table 21: **MIPI D-PHY Performance**

Description	Speed Grade and V_{CCINT} Operating Voltages				Units
	0.90V	0.85V		0.72V	
	-3	-2	-1	-2	
MIPI D-PHY transmitter or receiver.	1500	1500	1260	1260	Mb/s

Table 24: **IOB High Performance (HP) Switching Characteristics *(Cont'd)***

I/O Standards	$T_{INBUF\_DELAY\_PAD\_I}$				$T_{OUTBUF\_DELAY\_O\_PAD}$				$T_{OUTBUF\_DELAY\_TD\_PAD}$				Units
	0.90V	0.85V		0.72V	0.90V	0.85V		0.72V	0.90V	0.85V		0.72V	
	-3	-2	-1	-2	-3	-2	-1	-2	-3	-2	-1	-2	
LVCMOS15_F_8	0.414	0.414	0.445	0.414	0.518	0.518	0.538	0.518	0.686	0.686	0.703	0.686	ns
LVCMOS15_M_12	0.414	0.414	0.445	0.414	0.607	0.607	0.644	0.607	0.637	0.637	0.676	0.637	ns
LVCMOS15_M_2	0.414	0.414	0.445	0.414	0.741	0.741	0.770	0.741	0.938	0.938	0.962	0.938	ns
LVCMOS15_M_4	0.414	0.414	0.445	0.414	0.625	0.625	0.651	0.625	0.754	0.754	0.786	0.754	ns
LVCMOS15_M_6	0.414	0.414	0.445	0.414	0.576	0.576	0.604	0.576	0.674	0.674	0.710	0.674	ns
LVCMOS15_M_8	0.414	0.414	0.445	0.414	0.568	0.568	0.601	0.568	0.639	0.639	0.681	0.639	ns
LVCMOS15_S_12	0.414	0.414	0.445	0.414	0.788	0.788	0.855	0.788	0.695	0.695	0.733	0.695	ns
LVCMOS15_S_2	0.414	0.414	0.445	0.414	0.829	0.829	0.864	0.829	1.039	1.039	1.079	1.039	ns
LVCMOS15_S_4	0.414	0.414	0.445	0.414	0.687	0.687	0.725	0.687	0.813	0.813	0.851	0.813	ns
LVCMOS15_S_6	0.414	0.414	0.445	0.414	0.671	0.671	0.710	0.671	0.726	0.726	0.763	0.726	ns
LVCMOS15_S_8	0.414	0.414	0.445	0.414	0.704	0.704	0.755	0.704	0.721	0.721	0.758	0.721	ns
LVCMOS18_F_12	0.418	0.418	0.445	0.418	0.573	0.573	0.601	0.573	0.731	0.731	0.769	0.731	ns
LVCMOS18_F_2	0.418	0.418	0.445	0.418	0.739	0.739	0.760	0.739	0.945	0.945	0.971	0.945	ns
LVCMOS18_F_4	0.418	0.418	0.445	0.418	0.609	0.609	0.630	0.609	0.778	0.778	0.802	0.778	ns
LVCMOS18_F_6	0.418	0.418	0.445	0.418	0.603	0.603	0.633	0.603	0.781	0.781	0.808	0.781	ns
LVCMOS18_F_8	0.418	0.418	0.445	0.418	0.573	0.573	0.600	0.573	0.733	0.733	0.767	0.733	ns
LVCMOS18_M_12	0.418	0.418	0.445	0.418	0.640	0.640	0.678	0.640	0.670	0.670	0.709	0.670	ns
LVCMOS18_M_2	0.418	0.418	0.445	0.418	0.798	0.798	0.822	0.798	0.991	0.991	1.016	0.991	ns
LVCMOS18_M_4	0.418	0.418	0.445	0.418	0.664	0.664	0.693	0.664	0.798	0.798	0.836	0.798	ns
LVCMOS18_M_6	0.418	0.418	0.445	0.418	0.629	0.629	0.663	0.629	0.735	0.735	0.775	0.735	ns
LVCMOS18_M_8	0.418	0.418	0.445	0.418	0.626	0.626	0.661	0.626	0.705	0.705	0.746	0.705	ns
LVCMOS18_S_12	0.418	0.418	0.445	0.418	0.795	0.795	0.861	0.795	0.683	0.683	0.721	0.683	ns
LVCMOS18_S_2	0.418	0.418	0.445	0.418	0.862	0.862	0.897	0.862	1.076	1.076	1.098	1.076	ns
LVCMOS18_S_4	0.418	0.418	0.445	0.418	0.716	0.716	0.758	0.716	0.829	0.829	0.872	0.829	ns
LVCMOS18_S_6	0.418	0.418	0.445	0.418	0.682	0.682	0.724	0.682	0.724	0.724	0.762	0.724	ns
LVCMOS18_S_8	0.418	0.418	0.445	0.418	0.707	0.707	0.760	0.707	0.709	0.709	0.745	0.709	ns
LVDCI_15_F	0.425	0.425	0.462	0.425	0.426	0.426	0.443	0.426	0.548	0.548	0.581	0.548	ns
LVDCI_15_M	0.425	0.425	0.462	0.425	0.553	0.553	0.582	0.553	0.645	0.645	0.685	0.645	ns
LVDCI_15_S	0.425	0.425	0.462	0.425	0.749	0.749	0.803	0.749	0.821	0.821	0.890	0.821	ns
LVDCI_18_F	0.414	0.414	0.447	0.414	0.441	0.441	0.459	0.441	0.560	0.560	0.589	0.560	ns
LVDCI_18_M	0.414	0.414	0.447	0.414	0.554	0.554	0.585	0.554	0.644	0.644	0.683	0.644	ns
LVDCI_18_S	0.414	0.414	0.447	0.414	0.760	0.760	0.818	0.760	0.837	0.837	0.899	0.837	ns
LVDS	0.539	0.539	0.620	0.539	0.626	0.626	0.662	0.626	960.447	960.447	960.447	960.447	ns
MIPI_DPHY_DCI_HS	0.386	0.386	0.415	0.386	0.502	0.502	0.522	0.502	N/A	N/A	N/A	N/A	ns
MIPI_DPHY_DCI_LP	8.438	8.438	8.792	8.438	0.914	0.914	0.937	0.914	N/A	N/A	N/A	N/A	ns
POD10_DCI_F	0.408	0.408	0.430	0.408	0.425	0.425	0.444	0.425	0.555	0.555	0.584	0.555	ns
POD10_DCI_M	0.408	0.408	0.430	0.408	0.542	0.542	0.571	0.542	0.640	0.640	0.681	0.640	ns
POD10_DCI_S	0.408	0.408	0.430	0.408	0.754	0.754	0.815	0.754	0.850	0.850	0.917	0.850	ns
POD10_F	0.407	0.407	0.430	0.407	0.438	0.438	0.459	0.438	0.569	0.569	0.601	0.569	ns
POD10_M	0.407	0.407	0.430	0.407	0.538	0.538	0.568	0.538	0.630	0.630	0.667	0.630	ns
POD10_S	0.407	0.407	0.430	0.407	0.766	0.766	0.821	0.766	0.836	0.836	0.894	0.836	ns

Table 24: **IOB High Performance (HP) Switching Characteristics *(Cont'd)***

I/O Standards	$T_{INBUF\_DELAY\_PAD\_I}$				$T_{OUTBUF\_DELAY\_O\_PAD}$				$T_{OUTBUF\_DELAY\_TD\_PAD}$				Units
	0.90V	0.85V		0.72V	0.90V	0.85V		0.72V	0.90V	0.85V		0.72V	
	-3	-2	-1	-2	-3	-2	-1	-2	-3	-2	-1	-2	
POD12_DCI_F	0.409	0.409	0.431	0.409	0.425	0.425	0.443	0.425	0.558	0.558	0.586	0.558	ns
POD12_DCI_M	0.409	0.409	0.431	0.409	0.543	0.543	0.572	0.543	0.638	0.638	0.678	0.638	ns
POD12_DCI_S	0.409	0.409	0.431	0.409	0.772	0.772	0.822	0.772	0.862	0.862	0.929	0.862	ns
POD12_F	0.409	0.409	0.431	0.409	0.455	0.455	0.476	0.455	0.595	0.595	0.626	0.595	ns
POD12_M	0.409	0.409	0.431	0.409	0.551	0.551	0.582	0.551	0.641	0.641	0.679	0.641	ns
POD12_S	0.409	0.409	0.431	0.409	0.767	0.767	0.817	0.767	0.832	0.832	0.889	0.832	ns
SLVS_400_18	0.539	0.539	0.620	0.539	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	ns
SSTL12_DCI_F	0.381	0.381	0.399	0.381	0.425	0.425	0.443	0.425	0.558	0.558	0.586	0.558	ns
SSTL12_DCI_M	0.381	0.381	0.399	0.381	0.557	0.557	0.587	0.557	0.654	0.654	0.694	0.654	ns
SSTL12_DCI_S	0.381	0.381	0.399	0.381	0.754	0.754	0.803	0.754	0.842	0.842	0.908	0.842	ns
SSTL12_F	0.403	0.403	0.403	0.403	0.412	0.412	0.430	0.412	0.538	0.538	0.566	0.538	ns
SSTL12_M	0.403	0.403	0.403	0.403	0.553	0.553	0.584	0.553	0.641	0.641	0.676	0.641	ns
SSTL12_S	0.403	0.403	0.403	0.403	0.758	0.758	0.808	0.758	0.823	0.823	0.879	0.823	ns
SSTL135_DCI_F	0.366	0.366	0.399	0.366	0.411	0.411	0.428	0.411	0.537	0.537	0.565	0.537	ns
SSTL135_DCI_M	0.366	0.366	0.399	0.366	0.551	0.551	0.582	0.551	0.645	0.645	0.685	0.645	ns
SSTL135_DCI_S	0.366	0.366	0.399	0.366	0.746	0.746	0.799	0.746	0.829	0.829	0.893	0.829	ns
SSTL135_F	0.378	0.378	0.399	0.378	0.408	0.408	0.428	0.408	0.528	0.528	0.561	0.528	ns
SSTL135_M	0.378	0.378	0.399	0.378	0.555	0.555	0.585	0.555	0.641	0.641	0.679	0.641	ns
SSTL135_S	0.378	0.378	0.399	0.378	0.772	0.772	0.823	0.772	0.827	0.827	0.878	0.827	ns
SSTL15_DCI_F	0.402	0.402	0.417	0.402	0.412	0.412	0.429	0.412	0.531	0.531	0.563	0.531	ns
SSTL15_DCI_M	0.402	0.402	0.417	0.402	0.553	0.553	0.583	0.553	0.645	0.645	0.685	0.645	ns
SSTL15_DCI_S	0.402	0.402	0.417	0.402	0.768	0.768	0.822	0.768	0.847	0.847	0.912	0.847	ns
SSTL15_F	0.371	0.371	0.400	0.371	0.408	0.408	0.428	0.408	0.530	0.530	0.556	0.530	ns
SSTL15_M	0.371	0.371	0.400	0.371	0.554	0.554	0.585	0.554	0.639	0.639	0.677	0.639	ns
SSTL15_S	0.371	0.371	0.400	0.371	0.767	0.767	0.817	0.767	0.813	0.813	0.867	0.813	ns
SSTL18_I_DCI_F	0.329	0.329	0.336	0.329	0.445	0.445	0.461	0.445	0.566	0.566	0.595	0.566	ns
SSTL18_I_DCI_M	0.329	0.329	0.336	0.329	0.554	0.554	0.585	0.554	0.644	0.644	0.683	0.644	ns
SSTL18_I_DCI_S	0.329	0.329	0.336	0.329	0.762	0.762	0.818	0.762	0.837	0.837	0.899	0.837	ns
SSTL18_I_F	0.316	0.316	0.337	0.316	0.454	0.454	0.476	0.454	0.578	0.578	0.608	0.578	ns
SSTL18_I_M	0.316	0.316	0.337	0.316	0.571	0.571	0.603	0.571	0.652	0.652	0.692	0.652	ns
SSTL18_I_S	0.316	0.316	0.337	0.316	0.782	0.782	0.835	0.782	0.816	0.816	0.870	0.816	ns
SUB_LVDS	0.539	0.539	0.620	0.539	0.660	0.660	0.692	0.660	969.863	969.863	969.863	969.863	ns

Table 26: **Input Delay Measurement Methodology *(Cont'd)***

Description	I/O Standard Attribute	V_L (1)(2)	V_H (1)(2)	V_{MEAS} (1)(4)(6)	V_{REF} (1)(3)(5)
DIFF_HSUL, 1.2V	DIFF_HSUL_12	0.6 – 0.25	0.6 + 0.25	0(6)	–
DIFF_SSTL, 1.2V	DIFF_SSTL12	0.6 – 0.25	0.6 + 0.25	0(6)	–
DIFF_SSTL135 and DIFF_SSTL135 class II, 1.35V	DIFF_SSTL135, DIFF_SSTL135_II	0.675 – 0.2875	0.675 + 0.2875	0(6)	–
DIFF_SSTL15 and DIFF_SSTL15 class II, 1.5V	DIFF_SSTL15, DIFF_SSTL15_II	0.75 – 0.325	0.75 + 0.325	0(6)	–
DIFF_SSTL18_I, DIFF_SSTL18_II, 1.8V	DIFF_SSTL18_I, DIFF_SSTL18_II	0.9 – 0.4	0.9 + 0.4	0(6)	–
DIFF_POD10, 1.0V	DIFF_POD10	0.5 – 0.2	0.5 + 0.2	0(6)	–
DIFF_POD12, 1.2V	DIFF_POD12	0.6 – 0.25	0.6 + 0.25	0(6)	–
LVDS (low-voltage differential signaling), 1.8V	LVDS	0.9 – 0.125	0.9 + 0.125	0(6)	–
SUB_LVDS, 1.8V	SUB_LVDS	0.9 – 0.125	0.9 + 0.125	0(6)	–
SLVS, 1.8V	SLVS_400_18	0.9 – 0.125	0.9 + 0.125	0(6)	–
MIPI D-PHY (high speed) 1.2V	MIPI_DPHY_DCI_HS	0.2 – 0.125	0.2 + 0.125	0(6)	–
MIPI D-PHY (low power) 1.2V	MIPI_DPHY_DCI_LP	0.715 – 0.2	0.715 + 0.2	0(6)	–

Notes:

1. The input delay measurement methodology parameters for LVDCI/HSLVDCI are the same for LVCMOS standards of the same voltage. Parameters for all other DCI standards are the same for the corresponding non-DCI standards.
2. Input waveform switches between V_L and V_H.
3. Measurements are made at typical, minimum, and maximum V_{REF} values. Reported delays reflect worst case of these measurements. V_{REF} values listed are typical.
4. Input voltage level from which measurement starts.
5. This is an input voltage reference that bears no relation to the V_{REF}/V_{MEAS} parameters found in IBIS models and/or noted in Figure 1.
6. The value given is the differential input voltage.

Block RAM and FIFO Switching Characteristics

Table 28: **Block RAM and FIFO Switching Characteristics**

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages				Units
		0.90V	0.85V		0.72V	
		-3	-2	-1	-2	
Maximum Frequency						
$F_{MAX\_WF\_NC}$	Block RAM (WRITE_FIRST and NO_CHANGE modes).	825	737	645	585	MHz
F_{MAX_RF}	Block RAM (READ_FIRST mode).	718	637	575	510	MHz
F_{MAX_FIFO}	FIFO in all modes without ECC.	825	737	645	585	MHz
F_{MAX_ECC}	Block RAM and FIFO in ECC configuration without PIPELINE.	718	637	575	510	MHz
	Block RAM and FIFO in ECC configuration with PIPELINE and Block RAM in WRITE_FIRST or NO_CHANGE mode.	825	737	645	585	MHz
T_{PW}[(1)]	Minimum pulse width.	495	542	543	577	ps
Block RAM and FIFO Clock-to-Out Delays						
T_{RCKO_DO}	Clock CLK to DOUT output (without output register).	0.91	1.02	1.11	1.46	ns, Max
$T_{RCKO\_DO\_REG}$	Clock CLK to DOUT output (with output register).	0.27	0.29	0.30	0.42	ns, Max

Notes:

1. The MMCM and PLL DUTY_CYCLE attribute should be set to 50% to meet the pulse-width requirements at the higher frequencies.

UltraRAM Switching Characteristics

Table 29: **UltraRAM Switching Characteristics**

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages				Units
		0.90V	0.85V		0.72V	
		-3	-2	-1	-2	
Maximum Frequency						
F_{MAX}	UltraRAM maximum frequency with OREG_B = True.	650	600	575	500	MHz
F_{MAX_ECC}	UltraRAM maximum frequency OREG_B = False and EN_ECC_RD_B = True.	450	400	386	325	MHz
$F_{MAX\_NORPIPELINE}$	UltraRAM maximum frequency with OREG_B = False and EN_ECC_RD_B = False.	550	500	478	425	MHz
T_{PW}[(1)]	Minimum pulse width.	650	700	730	800	ps
T_{RSTPW}	Asynchronous reset minimum pulse width. One cycle required.	1 clock cycle				ps

Notes:

1. The MMCM and PLL DUTY_CYCLE attribute should be set to 50% to meet the pulse-width requirements at the higher frequencies.

MMCM Switching Characteristics

Table 33: **MMCM Specification**

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages				Units
		0.90V	0.85V		0.72V	
		-3	-2	-1	-2	
MMCM_F_{INMAX}	Maximum input clock frequency.	1066	933	800	933	MHz
MMCM_F_{INMIN}	Minimum input clock frequency.	10	10	10	10	MHz
MMCM_$F_{INJITTER}$	Maximum input clock period jitter.	< 20% of clock input period or 1 ns Max				
MMCM_F_{INDUTY}	Input duty cycle range: 10–49 MHz.	25–75				%
	Input duty cycle range: 50–199 MHz.	30–70				%
	Input duty cycle range: 200–399 MHz.	35–65				%
	Input duty cycle range: 400–499 MHz.	40–60				%
	Input duty cycle range: >500 MHz.	45–55				%
MMCM_F_{MIN_PSCLK}	Minimum dynamic phase shift clock frequency.	0.01	0.01	0.01	0.01	MHz
MMCM_F_{MAX_PSCLK}	Maximum dynamic phase shift clock frequency.	550	500	450	500	MHz
MMCM_F_{VCOMIN}	Minimum MMCM VCO frequency.	800	800	800	800	MHz
MMCM_F_{VCOMAX}	Maximum MMCM VCO frequency.	1600	1600	1600	1600	MHz
MMCM_$F_{BANDWIDTH}$	Low MMCM bandwidth at typical.(1)	1.00	1.00	1.00	1.00	MHz
	High MMCM bandwidth at typical.(1)	4.00	4.00	4.00	4.00	MHz
MMCM_$T_{STATPHAOFFSET}$	Static phase offset of the MMCM outputs.(2)	0.12	0.12	0.12	0.12	ns
MMCM_$T_{OUTJITTER}$	MMCM output jitter.	Note 3				
MMCM_$T_{OUTDUTY}$	MMCM output clock duty cycle precision.(4)	0.165	0.20	0.20	0.20	ns
MMCM_$T_{LOCKMAX}$	MMCM maximum lock time for MMCM_F_{PFDMIN}.	100	100	100	100	µs
MMCM_F_{OUTMAX}	MMCM maximum output frequency.	891	775	667	725	MHz
MMCM_F_{OUTMIN}	MMCM minimum output frequency.(4)(5)	6.25	6.25	6.25	6.25	MHz
MMCM_$T_{EXTFDVAR}$	External clock feedback variation.	< 20% of clock input period or 1 ns Max				
MMCM_$RST_{MINPULSE}$	Minimum reset pulse width.	5.00	5.00	5.00	5.00	ns
MMCM_F_{PFDMAX}	Maximum frequency at the phase frequency detector.	550	500	450	500	MHz
MMCM_F_{PFDMIN}	Minimum frequency at the phase frequency detector.	10	10	10	10	MHz
MMCM_$T_{FBDELAY}$	Maximum delay in the feedback path.	5 ns Max or one clock cycle				
MMCM_F_{DPRCLK_MAX}	Maximum DRP clock frequency	250	250	250	250	MHz

Notes:

1. The MMCM does not filter typical spread-spectrum input clocks because they are usually far below the bandwidth filter frequencies.
2. The static offset is measured between any MMCM outputs with identical phase.
3. Values for this parameter are available in the Clocking Wizard.
4. Includes global clock buffer.
5. Calculated as F_{VCO}/128 assuming output duty cycle is 50%.

PLL Switching Characteristics

Table 34: **PLL Specification(1)**

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages				Units
		0.90V	0.85V		0.72V	
		-3	-2	-1	-2	
PLL_F_{INMAX}	Maximum input clock frequency.	1066	933	800	933	MHz
PLL_F_{INMIN}	Minimum input clock frequency.	70	70	70	70	MHz
PLL_$F_{INJITTER}$	Maximum input clock period jitter.	< 20% of clock input period or 1 ns Max				
PLL_F_{INDUTY}	Input duty cycle range: 70–399 MHz.	35–65				%
	Input duty cycle range: 400–499 MHz.	40–60				%
	Input duty cycle range: >500 MHz.	45–55				%
PLL_F_{VCOMIN}	Minimum PLL VCO frequency.	750	750	750	750	MHz
PLL_F_{VCOMAX}	Maximum PLL VCO frequency.	1500	1500	1500	1500	MHz
PLL_$T_{STATPHAOFFSET}$	Static phase offset of the PLL outputs.(2)	0.12	0.12	0.12	0.12	ns
PLL_$T_{OUTJITTER}$	PLL output jitter.	Note 3				
PLL_$T_{OUTDUTY}$	PLL CLKOUT0, CLKOUT0B, CLKOUT1, CLKOUT1B duty-cycle precision.(4)	0.165	0.20	0.20	0.20	ns
PLL_$T_{LOCKMAX}$	PLL maximum lock time.	100				µs
PLL_F_{OUTMAX}	PLL maximum output frequency at CLKOUT0, CLKOUT0B, CLKOUT1, CLKOUT1B.	891	775	667	725	MHz
	PLL maximum output frequency at CLKOUTPHY.	2667	2667	2400	2400	MHz
PLL_F_{OUTMIN}	PLL minimum output frequency at CLKOUT0, CLKOUT0B, CLKOUT1, CLKOUT1B.(5)	5.86	5.86	5.86	5.86	MHz
	PLL minimum output frequency at CLKOUTPHY.	2 x VCO mode: 1500 1 x VCO mode: 750 0.5 x VCO mode: 375				MHz
PLL_$RST_{MINPULSE}$	Minimum reset pulse width.	5.00	5.00	5.00	5.00	ns
PLL_F_{PFDMAX}	Maximum frequency at the phase frequency detector.	667.5	667.5	667.5	667.5	MHz
PLL_F_{PFDMIN}	Minimum frequency at the phase frequency detector.	70	70	70	70	MHz
PLL_$F_{BANDWIDTH}$	PLL bandwidth at typical.	14	14	14	14	MHz
PLL_F_{DPRCLK_MAX}	Maximum DRP clock frequency	250	250	250	250	MHz

Notes:

1. The PLL does not filter typical spread-spectrum input clocks because they are usually far below the loop filter frequencies.
2. The static offset is measured between any PLL outputs with identical phase.
3. Values for this parameter are available in the Clocking Wizard.
4. Includes global clock buffer.
5. Calculated as $F_{VCO}/128$ assuming output duty cycle is 50%.

Device Pin-to-Pin Output Parameter Guidelines

The pin-to-pin numbers in Table 35 through Table 37 are based on the clock root placement in the center of the device. The actual pin-to-pin values will vary if the root placement selected is different. Consult the Vivado Design Suite timing report for the actual pin-to-pin values.

Table 35: **Global Clock Input to Output Delay Without MMCM (Near Clock Region)**

Symbol	Description	Device	Speed Grade and V_{CCINT} Operating Voltages				Units
			0.90V	0.85V		0.72V	
			-3	-2	-1	-2	
SSTL15 Global Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, *without* MMCM.							
T_{ICKOF}	Global clock input and output flip-flop *without* MMCM (near clock region).	XCVU3P	4.08	4.77	5.09	5.28	ns
		XCVU5P	4.08	4.77	5.09	5.28	ns
		XCVU7P	4.08	4.77	5.09	5.28	ns
		XCVU9P	4.08	4.77	5.09	5.28	ns
		XCVU11P	3.93	4.59	4.90	5.07	ns
		XCVU13P	3.93	4.59	4.90	5.07	ns

Notes:

1. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible I/O and CLB flip-flops are clocked by the global clock net in a single SLR.

Table 36: **Global Clock Input to Output Delay Without MMCM (Far Clock Region)**

Symbol	Description	Device	Speed Grade and V_{CCINT} Operating Voltages				Units
			0.90V	0.85V		0.72V	
			-3	-2	-1	-2	
SSTL15 Global Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, *without* MMCM.							
T_{ICKOF_FAR}	Global clock input and output flip-flop *without* MMCM (far clock region).	XCVU3P	4.53	5.33	5.69	5.92	ns
		XCVU5P	4.53	5.33	5.69	5.92	ns
		XCVU7P	4.53	5.33	5.69	5.92	ns
		XCVU9P	4.53	5.33	5.69	5.92	ns
		XCVU11P	4.10	4.79	5.11	5.28	ns
		XCVU13P	4.10	4.79	5.11	5.28	ns

Notes:

1. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible I/O and CLB flip-flops are clocked by the global clock net in a single SLR.

GTY Transceiver Specifications

The *UltraScale Architecture and Product Overview* (DS890) lists the Virtex UltraScale+ FPGAs that include the GTY transceivers.

GTY Transceiver DC Input and Output Levels

Table 41 summarizes the DC specifications of the GTY transceivers in Virtex UltraScale+ FPGAs. Consult the *UltraScale Architecture GTY Transceiver User Guide* (UG578) for further information.

Table 41: **GTY Transceiver DC Specifications**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
DV_{PPIN}	Differential peak-to-peak input voltage (external AC coupled)	>10.3125 Gb/s	150	–	1250	mV
		6.6 Gb/s to 10.3125 Gb/s	150	–	1250	mV
		≤ 6.6 Gb/s	150	–	2000	mV
V_{IN}	Single-ended input voltage. Voltage measured at the pin referenced to GND.	DC coupled $V_{MGTAVTT}$ = 1.2V	–400	–	$V_{MGTAVTT}$	mV
V_{CMIN}	Common mode input voltage	DC coupled $V_{MGTAVTT}$ = 1.2V	–	2/3 $V_{MGTAVTT}$	–	mV
D_{VPPOUT}	Differential peak-to-peak output voltage(1)	Transmitter output swing is set to 1010	800	–	–	mV
$V_{CMOUTDC}$	Common mode output voltage: DC coupled (equation based)	When remote RX is terminated to GND	$V_{MGTAVTT}/2 - D_{VPPOUT}/4$			mV
		When remote RX termination is floating	$V_{MGTAVTT} - D_{VPPOUT}/2$			mV
		When remote RX is terminated to V_{RX_TERM}(2)	$V_{MGTAVTT} - \frac{D_{VPPOUT}}{4} - \left(\frac{V_{MGTAVTT} - V_{RX\_TERM}}{2}\right)$			mV
$V_{CMOUTAC}$	Common mode output voltage: AC coupled	Equation based	$V_{MGTAVTT} - D_{VPPOUT}/2$			mV
R_{IN}	Differential input resistance		–	100	–	Ω
R_{OUT}	Differential output resistance		–	100	–	Ω
T_{OSKEW}	Transmitter output pair (TXP and TXN) intra-pair skew		–	–	10	ps
C_{EXT}	Recommended external AC coupling capacitor(3)		–	100	–	nF

Notes:

1. The output swing and pre-emphasis levels are programmable using the GTY transceiver attributes discussed in the *UltraScale Architecture GTY Transceiver User Guide* (UG578) and can result in values lower than reported in this table.
2. V_{RX_TERM} is the remote RX termination voltage.
3. Other values can be used as appropriate to conform to specific protocols and standards.

Table 51: **GTY Transceiver Receiver Switching Characteristics**

Symbol	Description	Condition	Min	Typ	Max	Units
F_{GTYRX}	Serial data rate		0.500	–	F_{GTYMAX}	Gb/s
R_{XSST}	Receiver spread-spectrum tracking(1)	Modulated at 33 kHz	–5000	–	0	ppm
R_{XRL}	Run length (CID)		–	–	256	UI
$R_{XPPMTOL}$	Data/REFCLK PPM offset tolerance	Bit rates ≤ 6.6 Gb/s	–1250	–	1250	ppm
		Bit rates > 6.6 Gb/s and ≤ 8.0 Gb/s	–700	–	700	ppm
		Bit rates > 8.0 Gb/s	–200	–	200	ppm
SJ Jitter Tolerance(2)						
$J_{T\_SJ32.75}$	Sinusoidal jitter (QPLL)(3)	32.75 Gb/s	0.25	–	–	UI
$J_{T\_SJ28.21}$	Sinusoidal jitter (QPLL)(3)	28.21 Gb/s	0.30	–	–	UI
$J_{T\_SJ16.375}$	Sinusoidal jitter (QPLL)(3)	16.375 Gb/s	0.30	–	–	UI
$J_{T\_SJ15.0}$	Sinusoidal jitter (QPLL)(3)	15.0 Gb/s	0.30	–	–	UI
$J_{T\_SJ14.1}$	Sinusoidal jitter (QPLL)(3)	14.1 Gb/s	0.30	–	–	UI
$J_{T\_SJ13.1}$	Sinusoidal jitter (QPLL)(3)	13.1 Gb/s	0.30	–	–	UI
$J_{T\_SJ12.5}$	Sinusoidal jitter (QPLL)(3)	12.5 Gb/s	0.30	–	–	UI
$J_{T\_SJ11.3}$	Sinusoidal jitter (QPLL)(3)	11.3 Gb/s	0.30	–	–	UI
$J_{T\_SJ10.32\_QPLL}$	Sinusoidal jitter (QPLL)(3)	10.32 Gb/s	0.30	–	–	UI
$J_{T\_SJ10.32\_CPLL}$	Sinusoidal jitter (CPLL)(3)	10.32 Gb/s	0.30	–	–	UI
$J_{T\_SJ9.953\_QPLL}$	Sinusoidal jitter (QPLL)(3)	9.953 Gb/s	0.30	–	–	UI
$J_{T\_SJ9.953\_CPLL}$	Sinusoidal jitter (CPLL)(3)	9.953 Gb/s	0.30	–	–	UI
$J_{T\_SJ8.0}$	Sinusoidal jitter (CPLL)(3)	8.0 Gb/s	0.42	–	–	UI
$J_{T\_SJ6.6}$	Sinusoidal jitter (CPLL)(3)	6.6 Gb/s	0.44	–	–	UI
$J_{T\_SJ5.0}$	Sinusoidal jitter (CPLL)(3)	5.0 Gb/s	0.44	–	–	UI
$J_{T\_SJ4.25}$	Sinusoidal jitter (CPLL)(3)	4.25 Gb/s	0.44	–	–	UI
$J_{T\_SJ3.2}$	Sinusoidal jitter (CPLL)(3)	3.2 Gb/s(4)	0.45	–	–	UI
$J_{T\_SJ2.5}$	Sinusoidal jitter (CPLL)(3)	2.5 Gb/s(5)	0.30	–	–	UI
$J_{T\_SJ1.25}$	Sinusoidal jitter (CPLL)(3)	1.25 Gb/s(6)	0.30	–	–	UI
J_{T_SJ500}	Sinusoidal jitter (CPLL)(3)	500 Mb/s(7)	0.30	–	–	UI
SJ Jitter Tolerance with Stressed Eye(2)						
$J_{T\_TJSE3.2}$	Total jitter with stressed eye(8)	3.2 Gb/s	0.70	–	–	UI
$J_{T\_TJSE6.6}$		6.6 Gb/s	0.70	–	–	UI
$J_{T\_SJSE3.2}$	Sinusoidal jitter with stressed eye(8)	3.2 Gb/s	0.10	–	–	UI
$J_{T\_SJSE6.6}$		6.6 Gb/s	0.10	–	–	UI

Notes:

1. Using RXOUT_DIV = 1, 2, and 4.
2. All jitter values are based on a bit error ratio of 10^{-12}.
3. The frequency of the injected sinusoidal jitter is 80 MHz.
4. CPLL frequency at 3.2 GHz and RXOUT_DIV = 2.
5. CPLL frequency at 2.5 GHz and RXOUT_DIV = 2.
6. CPLL frequency at 2.5 GHz and RXOUT_DIV = 4.
7. CPLL frequency at 2.0 GHz and RXOUT_DIV = 8.
8. Composite jitter with RX equalizer enabled. DFE disabled.

Table 52: **GTY Transceiver Protocol List *(Cont'd)***

Protocol	Specification	Serial Rate (Gb/s)	Electrical Compliance
Serial RapidIO	RapidIO specification 3.1	1.25–10.3125	Compliant
DisplayPort (source only)	DP 1.2B CTS	1.62–5.4	Compliant(3)
Fibre channel	FC-PI-4	1.0625–14.025	Compliant
SATA Gen1, 2, 3	Serial ATA revision 3.0 specification	1.5, 3.0, and 6.0	Compliant
SAS Gen1, 2, 3	T10/BSR INCITS 519	3.0, 6.0, and 12.0	Compliant
SFI-5	OIF-SFI5-01.0	0.625 - 12.5	Compliant
Aurora	CEI-6G, CEI-11G-LR	All rates	Compliant

Notes:

1. 25 dB loss at Nyquist without FEC.
2. The transition time of the transmitter is faster than the IEEE Std 802.3-2012 specification.
3. This protocol requires external circuitry to achieve compliance.

Table 54: **Maximum Performance for Interlaken 6 x 25.78125 Gb/s and 6 x 28.21 Gb/s Protocol and Lane Logic Mode Designs**

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages										Units
		0.90V		0.85V				0.72V				
		-3(1)		-2(1)		-1		-2		-1		
$F_{RX\_SERDES\_CLK}$	Receive serializer/ deserializer clock	440.79		440.79		N/A		402.84		N/A		MHz
$F_{TX\_SERDES\_CLK}$	Transmit serializer/ deserializer clock	440.79		440.79		N/A		402.84		N/A		MHz
F_{DRP_CLK}	Dynamic reconfiguration port clock	250.00		250.00		N/A		250.00		N/A		MHz
		Min(2)	Max	Min(2)	Max	Min	Max	Min(2)	Max	Min	Max	
F_{CORE_CLK}	Interlaken core clock	412.50(3)	479.20	412.50(3)	479.20	N/A		412.50	429.69	N/A		MHz
F_{LBUS_CLK}	Interlaken local bus clock	300.00(4)	349.52	300.00(4)	349.52	N/A		300.00	349.52	N/A		MHz

Notes:

1. 6 x 28.21 mode is only supported in the -2 (V_{CCINT}=0.85V) and -3 (V_{CCINT}=0.90V) speed grades.
2. These are the minimum clock frequencies at the maximum lane performance.
3. The minimum value for CORE_CLK is 451.36 MHz for the 6 x 28.21 Gb/s protocol.
4. The minimum value for LBUS_CLK is 330.00 MHz for the 6 x 28.21 Gb/s protocol.

Table 55: **Maximum Performance for Interlaken 12 x 25.78125 Gb/s Lane Logic Only Mode Designs**

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages					Units
		0.90V	0.85V		0.72V		
		-3	-2	-1	-2	-1	
$F_{RX\_SERDES\_CLK}$	Receive serializer/ deserializer clock	402.84	402.84	N/A	N/A	N/A	MHz
$F_{TX\_SERDES\_CLK}$	Transmit serializer/ deserializer clock	402.84	402.84	N/A	N/A	N/A	MHz
F_{DRP_CLK}	Dynamic reconfiguration port clock	250.00	250.00	N/A	N/A	N/A	MHz
F_{CORE_CLK}	Interlaken core clock	412.50	412.50	N/A	N/A	N/A	MHz
F_{LBUS_CLK}	Interlaken local bus clock	349.52	349.52	N/A	N/A	N/A	MHz

Integrated Interface Block for 100G Ethernet MAC and PCS

More information and documentation on solutions using the integrated 100 Gb/s Ethernet block can be found at UltraScale Integrated 100G Ethernet MAC/PCS. The *UltraScale Architecture and Product Overview* (DS890) lists how many blocks are in each Virtex UltraScale+ FPGA.

Table 56: **Maximum Performance for 100G Ethernet Designs**

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages				Units
		0.90V	0.85V		0.72V	
		-3	-2(1)	-1	-2	
F_{TX_CLK}	Transmit clock	390.625	390.625	322.223	322.223	MHz
F_{RX_CLK}	Receive clock	390.625	390.625	322.223	322.223	MHz
$F_{RX\_SERDES\_CLK}$	Receive serializer/deserializer clock	390.625	390.625	322.223	322.223	MHz
F_{DRP_CLK}	Dynamic reconfiguration port clock	250.00	250.00	250.00	250.00	MHz

Notes:

1. The maximum clock frequency of 390.625 MHz only applies to the CAUI-10 interface. The maximum clock frequency for the CAUI-4 interface is 322.223 MHz.

Integrated Interface Block for PCI Express Designs

More information and documentation on solutions for PCI Express designs can be found at PCI Express. The *UltraScale Architecture and Product Overview* (DS890) lists how many blocks are in each Virtex UltraScale+ FPGA.

Table 57: **Maximum Performance for PCI Express Designs(1)(2)**

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages				Units
		0.90V	0.85V		0.72V	
		-3	-2	-1	-2	
$F_{PIPECLK}$	Pipe clock maximum frequency.	250.00	250.00	250.00	250.00	MHz
$F_{CORECLK}$	Core clock maximum frequency.	500.00	500.00	500.00	250.00	MHz
F_{DRPCLK}	DRP clock maximum frequency.	250.00	250.00	250.00	250.00	MHz
$F_{MCAPCLK}$	MCAP clock maximum frequency.	125.00	125.00	125.00	125.00	MHz

Notes:

1. PCI Express Gen4 operation is supported for x1, x2, x4, and x8 widths.
2. PCI Express Gen4 operation is supported in -3E, -2E, and -2I speed grades.

Table 61: **Configuration Switching Characteristics *(Cont'd)***

Symbol	Description		Speed Grade and V_{CCINT} Operating Voltages				Units
			0.90V	0.85V		0.72V	
			-3	-2	-1	-2	
SelectMAP Mode Programming Switching							
T_{SMDCCK}/T_{SMCCKD}	D[31:00] setup/hold.	XCVU3P, XCVU5P, XCVU7P, XCVU9P	4.0/0	4.0/0	4.0/0	5.0/0	ns, Min
		XCVU11P, XCVU13P	4.5/0	4.5/0	4.5/0	7.5/0	ns, Min
$T_{SMCSCCK}/T_{SMCCKCS}$	CSI_B setup/hold.	XCVU3P, XCVU5P, XCVU7P, XCVU9P	4.0/0	4.0/0	4.0/0	5.0/0	ns, Min
		XCVU11P, XCVU13P	4.5/0	4.5/0	4.5/0	7.5/0	ns, Min
T_{SMWCCK}/T_{SMCCKW}	RDWR_B setup/hold.	XCVU3P, XCVU5P, XCVU7P, XCVU9P	10.0/0	10.0/0	10.0/0	11.0/0	ns, Min
		XCVU11P, XCVU13P	11.0/0	11.0/0	11.0/0	17.0/0	ns, Min
$T_{SMCKCSO}$	CSO_B clock to out (330Ω pull-up resistor required).		7.0	7.0	7.0	7.0	ns, Max
T_{SMCO}	D[31:00] clock to out in readback.		8.0	8.0	8.0	8.0	ns, Max
F_{RBCCK}	Readback frequency.	XCVU3P, XCVU5P, XCVU7P, XCVU9P	125	125	125	100	MHz, Max
		XCVU11P, XCVU13P	125	125	125	66	MHz, Max
Boundary-Scan Port Timing Specifications							
T_{TAPTCK}/T_{TCKTAP}	TMS and TDI setup/hold.	XCVU3P	3.0/ 2.0	3.0/ 2.0	3.0/ 2.0	3.0/ 2.0	ns, Min
		XCVU5P, XCVU7P, XCVU9P, XCVU11P, XCVU13P	8.5/ 2.0	8.5/ 2.0	8.5/ 2.0	8.5/ 2.0	ns, Min
T_{TCKTDO}	TCK falling edge to TDO output.	XCVU3P	7.0	7.0	7.0	7.0	ns, Max
		XCVU5P, XCVU7P, XCVU9P, XCVU11P, XCVU13P	15.0	15.0	15.0	15.0	ns, Max
F_{TCK}	TCK frequency.	XCVU3P	66	66	66	66	MHz, Max
		XCVU5P, XCVU7P, XCVU9P, XCVU11P, XCVU13P	20	20	20	20	MHz, Max
BPI Master Flash Mode Programming Switching							
T_{BPICCO}	A[28:00], RS[1:0], FCS_B, FOE_B, FWE_B, ADV_B clock to out.		10	10	10	10	ns, Max
T_{BPIDCC}/T_{BPICCD}	D[15:00] setup/hold.	XCVU3P, XCVU5P, XCVU7P, XCVU9P	4.0/0	4.0/0	4.0/0	5.0/0	ns, Min
		XCVU11P, XCVU13P	4.5/0	4.5/0	4.5/0	7.5/0	ns, Min
SPI Master Flash Mode Programming Switching							
T_{SPIDCC}/T_{SPICCD}	D[03:00] setup/hold.		3.0/0	3.0/0	3.0/0	4.0/0	ns, Min
T_{SPIDCC}/T_{SPICCD}	D[07:04] setup/hold.	XCVU3P, XCVU5P, XCVU7P, XCVU9P	4.0/0	4.0/0	4.0/0	5.0/0	ns, Min
		XCVU11P, XCVU13P	4.5/0	4.5/0	4.5/0	7.5/0	ns, Min
T_{SPICCM}	MOSI clock to out.		8.0	8.0	8.0	8.0	ns, Max
$T_{SPICCFC}$	FCS_B clock to out.		8.0	8.0	8.0	8.0	ns, Max

Revision History

The following table shows the revision history for this document.

Date	Version	Description of Revisions
04/19/2017	1.1	Updated the Summary description. In Table 1, updated Note 6, added data, and added Note 7, Note 8, and Note 9. Updated and added data to Table 2 though Table 6. Removed the -1LI speed grade. Updated Table 16, Table 17, and Table 18 to production release in Vivado Design Suite 2017.1 for the XCVU3P: -2E, -2I, -1E, -1I. Updated Table 15. Added Note 1 to Table 17. Updated Table 19, Table 20, Table 24, Table 25, Table 26, Table 28, Table 29, and Table 30. Added Table 21. Added MMCM_F_{DPRCLK_MAX} to Table 33 and PLL_F_{DPRCLK_MAX} to Table 34. Updated to Vivado Design Suite 2017.1 Table 35, Table 36, Table 37, and Table 38. Added data to Table 39 and Table 40. Updated the GTY Transceiver Specifications section. Revised the Integrated Interface Block for Interlaken section. Updated the System Monitor Specifications section adding notes to the tables. Updated the Configuration Switching Characteristics section. Removed the *eFUSE Programming Conditions* table and added the specifications to Table 2 and Table 3. Updated the Automotive Applications Disclaimer.
04/20/2016	1.0	Initial Xilinx release.

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