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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	147780
Number of Logic Elements/Cells	2586150
Total RAM Bits	391168000
Number of I/O	448
Number of Gates	-
Voltage - Supply	0.873V ~ 0.927V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 100°C (TJ)
Package / Case	2577-BBGA, FCBGA
Supplier Device Package	2577-FCBGA (52.5x52.5)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xcvu9p-3flga2577e

Table 2: **Recommended Operating Conditions(1)(2) *(Cont'd)***

Symbol	Description	Min	Typ	Max	Units
SYSMON					
V_{CCADC}	SYSMON supply relative to GNDADC.	1.746	1.800	1.854	V
V_{REFP}	SYSMON externally supplied reference voltage relative to GNDADC.	1.200	1.250	1.300	V
Temperature					
T_j(11)	Junction temperature operating range for extended (E) temperature devices.(12)	0	–	100	°C
	Junction temperature operating range for industrial (I) temperature devices.	–40	–	100	°C
	Junction temperature operating range for eFUSE programming.(13)	–40	–	125	°C

Notes:

1. All voltages are relative to GND.
2. For the design of the power distribution system consult *UltraScale Architecture PCB Design Guide* (UG583).
3. V_{CCINT_IO} must be connected to V_{CCBRAM}.
4. For V_{CCO_0}, the minimum recommended operating voltage for power on and during configuration is 1.425V. After configuration, data is retained even if V_{CCO} drops to 0V.
5. Includes V_{CCO} of 1.0V, 1.2V, 1.35V, 1.5V, and 1.8V.
6. V_{CCAUX_IO} must be connected to V_{CCAUX}.
7. The lower absolute voltage specification always applies.
8. A total of 200 mA per bank should not be exceeded.
9. If battery is not used, connect V_{BATT} to either GND or V_{CCAUX}.
10. Each voltage listed requires filtering as described in the *UltraScale Architecture GTY Transceiver User Guide* (UG578).
11. Xilinx recommends measuring the Tj of a device using the system monitor as described in the *UltraScale Architecture System Monitor User Guide* (UG580). The SYSMON temperature measurement errors (that are described in Table 58) must be accounted for in your design. For example, by using an external reference of 1.25V, when SYSMON reports 97°C, there is a measurement error ±3°C. A reading of 97°C is considered the maximum adjusted Tj (100°C – 3°C = 97°C).
12. Devices labeled with the speed/temperature grade of -2LE can operate for a limited time at a junction temperature of 110°C. Timing parameters adhere to the same speed file at 110°C as they do below 110°C, regardless of operating voltage (nominal voltage of 0.85V or a low-voltage of 0.72V). Operation at Tj = 110°C is limited to 1% of the device lifetime and can occur sequentially or at regular intervals as long as the total time does not exceed 1% of the device lifetime.
13. Do not program eFUSE during device configuration (e.g., during configuration, during configuration readback, or when readback CRC is active).

DC Characteristics Over Recommended Operating Conditions

Table 3: **DC Characteristics Over Recommended Operating Conditions**

Symbol	Description	Min	Typ(1)	Max	Units
V_{DRINT}	Data retention V_{CCINT} voltage (below which configuration data might be lost).	0.68	–	–	V
V_{DRAUX}	Data retention V_{CCAUX} voltage (below which configuration data might be lost).	1.5	–	–	V
I_{REF}	V_{REF} leakage current per pin.	–	–	15	µA
I_L	Input or output leakage current per pin (sample-tested).(2)	–	–	15	µA
C_{IN}(3)	Die input capacitance at the pad.	–	–	3.1	pF
I_{RPU}	Pad pull-up (when selected) at V_{IN} = 0V, V_{CCO} = 3.3V.	75	–	190	µA
	Pad pull-up (when selected) at V_{IN} = 0V, V_{CCO} = 2.5V.	50	–	169	µA
	Pad pull-up (when selected) at V_{IN} = 0V, V_{CCO} = 1.8V.	60	–	120	µA
	Pad pull-up (when selected) at V_{IN} = 0V, V_{CCO} = 1.5V.	30	–	120	µA
	Pad pull-up (when selected) at V_{IN} = 0V, V_{CCO} = 1.2V.	10	–	100	µA
I_{RPD}	Pad pull-down (when selected) at V_{IN} = 3.3V.	60	–	200	µA
	Pad pull-down (when selected) at V_{IN} = 1.8V.	29	–	120	µA
$I_{CCADCON}$	Analog supply current for the SYSMON circuits in the power-up state.	–	–	8	mA
$I_{CCADCOFF}$	Analog supply current for the SYSMON circuits in the power-down state.	–	–	1.5	mA
I_{BATT}(4)(5)	Battery supply current at V_{BATT} = 1.89V.	–	–	650	nA
	Battery supply current at V_{BATT} = 1.20V.	–	–	150	nA
I_{PFS}(6)	V_{CCAUX} additional supply current during eFUSE programming.	–	–	115	mA
Calibrated programmable on-die termination (DCI) in I/O banks(8) (measured per JEDEC specification)					
R(9)	Thevenin equivalent resistance of programmable input termination to V_{CCO}/2 where ODT = RTT_40.	–10%(8)	40	+10%(8)	Ω
	Thevenin equivalent resistance of programmable input termination to V_{CCO}/2 where ODT = RTT_48.	–10%(8)	48	+10%(8)	Ω
	Thevenin equivalent resistance of programmable input termination to V_{CCO}/2 where ODT = RTT_60.	–10%(8)	60	+10%(8)	Ω
	Programmable input termination to V_{CCO} where ODT = RTT_40.	–10%(8)	40	+10%(8)	Ω
	Programmable input termination to V_{CCO} where ODT = RTT_48.	–10%(8)	48	+10%(8)	Ω
	Programmable input termination to V_{CCO} where ODT = RTT_60.	–10%(8)	60	+10%(8)	Ω
	Programmable input termination to V_{CCO} where ODT = RTT_120.	–10%(8)	120	+10%(8)	Ω
	Programmable input termination to V_{CCO} where ODT = RTT_240.	–10%(8)	240	+10%(8)	Ω

Power Supply Requirements

Table 6 shows the minimum current, in addition to I_{CCQ} maximum, required by each Virtex UltraScale+ FPGA for proper power-on and configuration. If the current minimums shown in Table 6 are met, the device powers on after all supplies have passed through their power-on reset threshold voltages. The device must not be configured until after V_{CCINT} is applied. Once initialized and configured, use the Xilinx Power Estimator (XPE) tools to estimate current drain on these supplies.

Table 6: **Power-on Current by Device(1)**

Device	$I_{CCINTMIN}$	$I_{CCINT\_IOMIN} + I_{CCBRAMMIN}$	I_{CCOMIN}	$I_{CCAUXMIN} + I_{CCAUX\_IOMIN}$	Units
XCVU3P	I_{CCINTQ} + 2000	$I_{CCBRAMQ} + I_{CCINT\_IOQ}$ + 950	I_{CCOQ} + 50	$I_{CCAUXQ} + I_{CCAUX\_IOQ}$ + 350	mA
XCVU5P	I_{CCINTQ} + 4000	$I_{CCBRAMQ} + I_{CCINT\_IOQ}$ + 1900	I_{CCOQ} + 100	$I_{CCAUXQ} + I_{CCAUX\_IOQ}$ + 700	mA
XCVU7P	I_{CCINTQ} + 4000	$I_{CCBRAMQ} + I_{CCINT\_IOQ}$ + 1900	I_{CCOQ} + 100	$I_{CCAUXQ} + I_{CCAUX\_IOQ}$ + 700	mA
XCVU9P	I_{CCINTQ} + 6000	$I_{CCBRAMQ} + I_{CCINT\_IOQ}$ + 2850	I_{CCOQ} + 150	$I_{CCAUXQ} + I_{CCAUX\_IOQ}$ + 1050	mA
XCVU11P	I_{CCINTQ} + 6549	$I_{CCBRAMQ} + I_{CCINT\_IOQ}$ + 3111	I_{CCOQ} + 164	$I_{CCAUXQ} + I_{CCAUX\_IOQ}$ + 1146	mA
XCVU13P	I_{CCINTQ} + 8731	$I_{CCBRAMQ} + I_{CCINT\_IOQ}$ + 4148	I_{CCOQ} + 219	$I_{CCAUXQ} + I_{CCAUX\_IOQ}$ + 1528	mA

Notes:

1. Use the Xilinx Power Estimator (XPE) spreadsheet tool (download at www.xilinx.com/power) to estimate power-on current for all supplies.

Table 7 shows the power supply ramp time.

Table 7: **Power Supply Ramp Time**

Symbol	Description	Min	Max	Units
T_{VCCINT}	Ramp time from GND to 95% of V_{CCINT}.	0.2	40	ms
T_{VCCINT_IO}	Ramp time from GND to 95% of V_{CCINT_IO}.	0.2	40	ms
T_{VCCO}	Ramp time from GND to 95% of V_{CCO}.	0.2	40	ms
T_{VCCAUX}	Ramp time from GND to 95% of V_{CCAUX}.	0.2	40	ms
$T_{VCCBRAM}$	Ramp time from GND to 95% of V_{CCBRAM}.	0.2	40	ms
$T_{MGTAVCC}$	Ramp time from GND to 95% of $V_{MGTAVCC}$.	0.2	40	ms
$T_{MGTAVTT}$	Ramp time from GND to 95% of $V_{MGTAVTT}$.	0.2	40	ms
$T_{MGTVCCAUX}$	Ramp time from GND to 95% of $V_{MGTVCCAUX}$.	0.2	40	ms

DC Input and Output Levels

Values for V_{IL} and V_{IH} are recommended input voltages. Values for I_{OL} and I_{OH} are guaranteed over the recommended operating conditions at the V_{OL} and V_{OH} test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at a minimum V_{CCO} with the respective V_{OL} and V_{OH} voltage levels shown. Other standards are sample tested.

Table 8: **SelectIO DC Input and Output Levels for the I/O Banks(1)(2)(3)**

I/O Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
HSTL_I	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	5.8	–5.8
HSTL_I_12	–0.300	V_{REF} – 0.080	V_{REF} + 0.080	V_{CCO} + 0.300	25% V_{CCO}	75% V_{CCO}	4.1	–4.1
HSTL_I_18	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	6.2	–6.2
HSUL_12	–0.300	V_{REF} – 0.130	V_{REF} + 0.130	V_{CCO} + 0.300	20% V_{CCO}	80% V_{CCO}	0.1	–0.1
LVCMOS12	–0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	Note 4	Note 4
LVCMOS15	–0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	0.450	V_{CCO} – 0.450	Note 5	Note 5
LVCMOS18	–0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	0.450	V_{CCO} – 0.450	Note 5	Note 5
LVDCI_15	–0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	0.450	V_{CCO} – 0.450	7.0	–7.0
LVDCI_18	–0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	0.450	V_{CCO} – 0.450	7.0	–7.0
SSTL12	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	V_{CCO}/2 – 0.150	V_{CCO}/2 + 0.150	8.0	–8.0
SSTL135	–0.300	V_{REF} – 0.090	V_{REF} + 0.090	V_{CCO} + 0.300	V_{CCO}/2 – 0.150	V_{CCO}/2 + 0.150	9.0	–9.0
SSTL15	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	V_{CCO}/2 – 0.175	V_{CCO}/2 + 0.175	10.0	–10.0
SSTL18_I	–0.300	V_{REF} – 0.125	V_{REF} + 0.125	V_{CCO} + 0.300	V_{CCO}/2 – 0.470	V_{CCO}/2 + 0.470	7.0	–7.0
MIPI_DPHY_DCI_LP(6)	–0.300	0.550	0.880	V_{CCO} + 0.300	0.050	1.100	0.01	–0.01

Notes:

1. Tested according to relevant specifications.
2. Standards specified using the default I/O standard configuration. For details, see the *UltraScale Architecture SelectIO Resources User Guide* (UG571).
3. POD10 and POD12 DC input and output levels are shown in Table 9, Table 13, and Table 14.
4. Supported drive strengths of 2, 4, 6, or 8 mA in the I/O banks.
5. Supported drive strengths of 2, 4, 6, 8, or 12 mA in the I/O banks.
6. Low-power option for MIPI_DPHY_DCI.

Table 9: **DC Input Levels for Single-ended POD10 and POD12 I/O Standards(1)(2)**

I/O Standard	V_{IL}		V_{IH}	
	V, Min	V, Max	V, Min	V, Max
POD10	–0.300	V_{REF} – 0.068	V_{REF} + 0.068	V_{CCO} + 0.300
POD12	–0.300	V_{REF} – 0.068	V_{REF} + 0.068	V_{CCO} + 0.300

Notes:

1. Tested according to relevant specifications.
2. Standards specified using the default I/O standard configuration. For details, see the *UltraScale Architecture SelectIO Resources User Guide* (UG571).

Table 13: **DC Output Levels for Single-ended and Differential POD10 and POD12 Standards(1)(2)**

Symbol	Description	V_{OUT}	Min	Typ	Max	Units
R_{OL}	Pull-down resistance.	V_{OM_DC} (as described in Table 14)	36	40	44	Ω
R_{OH}	Pull-up resistance.	V_{OM_DC} (as described in Table 14)	36	40	44	Ω

Notes:

1. Tested according to relevant specifications.
2. Standards specified using the default I/O standard configuration. For details, see the *UltraScale Architecture SelectIO Resources User Guide* (UG571).

Table 14: **Table 13 Definitions for DC Output Levels for POD Standards**

Symbol	Description	All Speed Grades	Units
V_{OM_DC}	DC output Mid measurement level (for IV curve linearity).	0.8 x V_{CCO}	V

LVDS DC Specifications (LVDS)

Table 15: **LVDS DC Specifications**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{CCO}(1)	Supply voltage.		1.710	1.800	1.890	V
V_{ODIFF}(2)	Differential output voltage: ($\underline{Q}$ – $\overline{Q}$), $\underline{Q}$ = High ($\underline{Q}$ – $\overline{Q}$), $\overline{Q}$ = High	R_T = 100Ω across Q and $\overline{Q}$ signals	247	350	454	mV
V_{OCM}(2)	Output common-mode voltage.	R_T = 100 Ω across Q and $\overline{Q}$ signals	1.000	1.250	1.425	V
V_{IDIFF}	Differential input voltage: ($\underline{Q}$ – $\overline{Q}$), $\underline{Q}$ = High ($\underline{Q}$ – $\overline{Q}$), $\overline{Q}$ = High		100	350	600(3)	mV
V_{ICM_DC}(4)	Input common-mode voltage (DC coupling).		0.300	1.200	1.425	V
V_{ICM_AC}(5)	Input common-mode voltage (AC coupling).		0.600	–	1.100	V

Notes:

1. In I/O banks, when LVDS is used with input-only functionality, it can be placed in a bank where the V_{CCO} levels are different from the specified level only if internal differential termination is not used. In this scenario, V_{CCO} must be chosen to ensure the input pin voltage levels do not violate the *Recommended Operating Condition* (Table 2) specification for the V_{IN} I/O pin voltage.
2. V_{OCM} and V_{ODIFF} values are for LVDS_PRE_EMPHASIS = FALSE.
3. Maximum V_{IDIFF} value is specified for the maximum V_{ICM} specification. With a lower V_{ICM}, a higher V_{DIFF} is tolerated only when the recommended operating conditions and overshoot/undershoot V_{IN} specifications are maintained.
4. Input common mode voltage for DC coupled configurations. EQUALIZATION = EQ_NONE (Default).
5. External input common mode voltage specification for AC coupled configurations. EQUALIZATION = EQ_LEVEL0, EQ_LEVEL1, EQ_LEVEL2, EQ_LEVEL3, EQ_LEVEL4.

FPGA Logic Switching Characteristics

Table 24, high-performance IOB (HP), summarizes the values of standard-specific data input delay adjustments, output delays terminating at pads (based on standard) and 3-state delays.

- $T_{INBUF\_DELAY\_PAD\_I}$ is the delay from IOB pad through the input buffer to the I-pin of an IOB pad. The delay varies depending on the capability of the SelectIO input buffer.
- $T_{OUTBUF\_DELAY\_O\_PAD}$ is the delay from the O pin to the IOB pad through the output buffer of an IOB pad. The delay varies depending on the capability of the SelectIO output buffer.
- $T_{OUTBUF\_DELAY\_TD\_PAD}$ is the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is disabled. The delay varies depending on the SelectIO capability of the output buffer. In HP I/O banks, the internal DCI termination turn-on time is always faster than $T_{OUTBUF\_DELAY\_TD\_PAD}$ when the DCITERMDISABLE pin is used.

IOB High Performance (HP) Switching Characteristics

Table 24: **IOB High Performance (HP) Switching Characteristics**

I/O Standards	$T_{INBUF\_DELAY\_PAD\_I}$				$T_{OUTBUF\_DELAY\_O\_PAD}$				$T_{OUTBUF\_DELAY\_TD\_PAD}$				Units
	0.90V	0.85V		0.72V	0.90V	0.85V		0.72V	0.90V	0.85V		0.72V	
	-3	-2	-1	-2	-3	-2	-1	-2	-3	-2	-1	-2	
DIFF_HSTL_I_12_F	0.394	0.394	0.402	0.394	0.423	0.423	0.443	0.423	0.553	0.553	0.582	0.553	ns
DIFF_HSTL_I_12_M	0.394	0.394	0.402	0.394	0.552	0.552	0.583	0.552	0.641	0.641	0.679	0.641	ns
DIFF_HSTL_I_12_S	0.394	0.394	0.402	0.394	0.752	0.752	0.800	0.752	0.813	0.813	0.868	0.813	ns
DIFF_HSTL_I_18_F	0.319	0.319	0.339	0.319	0.456	0.456	0.474	0.456	0.576	0.576	0.606	0.576	ns
DIFF_HSTL_I_18_M	0.319	0.319	0.339	0.319	0.570	0.570	0.603	0.570	0.653	0.653	0.692	0.653	ns
DIFF_HSTL_I_18_S	0.319	0.319	0.339	0.319	0.782	0.782	0.834	0.782	0.816	0.816	0.871	0.816	ns
DIFF_HSTL_I_DCI_12_F	0.394	0.394	0.402	0.394	0.406	0.406	0.429	0.406	0.534	0.534	0.564	0.534	ns
DIFF_HSTL_I_DCI_12_M	0.394	0.394	0.402	0.394	0.557	0.557	0.587	0.557	0.653	0.653	0.694	0.653	ns
DIFF_HSTL_I_DCI_12_S	0.394	0.394	0.402	0.394	0.755	0.755	0.806	0.755	0.842	0.842	0.907	0.842	ns
DIFF_HSTL_I_DCI_18_F	0.323	0.323	0.339	0.323	0.445	0.445	0.461	0.445	0.566	0.566	0.595	0.566	ns
DIFF_HSTL_I_DCI_18_M	0.323	0.323	0.339	0.323	0.555	0.555	0.586	0.555	0.643	0.643	0.684	0.643	ns
DIFF_HSTL_I_DCI_18_S	0.323	0.323	0.339	0.323	0.762	0.762	0.818	0.762	0.836	0.836	0.900	0.836	ns
DIFF_HSTL_I_DCI_F	0.397	0.397	0.417	0.397	0.431	0.431	0.445	0.431	0.555	0.555	0.575	0.555	ns
DIFF_HSTL_I_DCI_M	0.397	0.397	0.417	0.397	0.553	0.553	0.583	0.553	0.644	0.644	0.684	0.644	ns
DIFF_HSTL_I_DCI_S	0.397	0.397	0.417	0.397	0.767	0.767	0.823	0.767	0.848	0.848	0.912	0.848	ns
DIFF_HSTL_I_F	0.404	0.404	0.417	0.404	0.423	0.423	0.443	0.423	0.549	0.549	0.581	0.549	ns
DIFF_HSTL_I_M	0.404	0.404	0.417	0.404	0.555	0.555	0.586	0.555	0.640	0.640	0.677	0.640	ns
DIFF_HSTL_I_S	0.404	0.404	0.417	0.404	0.767	0.767	0.818	0.767	0.811	0.811	0.866	0.811	ns
DIFF_HSUL_12_DCI_F	0.381	0.381	0.400	0.381	0.425	0.425	0.443	0.425	0.558	0.558	0.586	0.558	ns
DIFF_HSUL_12_DCI_M	0.381	0.381	0.400	0.381	0.557	0.557	0.587	0.557	0.653	0.653	0.694	0.653	ns
DIFF_HSUL_12_DCI_S	0.381	0.381	0.400	0.381	0.737	0.737	0.787	0.737	0.822	0.822	0.885	0.822	ns
DIFF_HSUL_12_F	0.394	0.394	0.402	0.394	0.412	0.412	0.430	0.412	0.538	0.538	0.566	0.538	ns
DIFF_HSUL_12_M	0.394	0.394	0.402	0.394	0.552	0.552	0.583	0.552	0.641	0.641	0.679	0.641	ns
DIFF_HSUL_12_S	0.394	0.394	0.402	0.394	0.752	0.752	0.800	0.752	0.813	0.813	0.868	0.813	ns

Table 24: **IOB High Performance (HP) Switching Characteristics *(Cont'd)***

I/O Standards	$T_{INBUF\_DELAY\_PAD\_I}$				$T_{OUTBUF\_DELAY\_O\_PAD}$				$T_{OUTBUF\_DELAY\_TD\_PAD}$				Units
	0.90V	0.85V		0.72V	0.90V	0.85V		0.72V	0.90V	0.85V		0.72V	
	-3	-2	-1	-2	-3	-2	-1	-2	-3	-2	-1	-2	
HSLVDCI_18_S	0.424	0.424	0.447	0.424	0.761	0.761	0.817	0.761	0.836	0.836	0.900	0.836	ns
HSTL_I_12_F	0.378	0.378	0.399	0.378	0.423	0.423	0.443	0.423	0.553	0.553	0.582	0.553	ns
HSTL_I_12_M	0.378	0.378	0.399	0.378	0.551	0.551	0.582	0.551	0.642	0.642	0.679	0.642	ns
HSTL_I_12_S	0.378	0.378	0.399	0.378	0.750	0.750	0.799	0.750	0.813	0.813	0.868	0.813	ns
HSTL_I_18_F	0.322	0.322	0.339	0.322	0.456	0.456	0.474	0.456	0.576	0.576	0.606	0.576	ns
HSTL_I_18_M	0.322	0.322	0.339	0.322	0.569	0.569	0.602	0.569	0.653	0.653	0.692	0.653	ns
HSTL_I_18_S	0.322	0.322	0.339	0.322	0.781	0.781	0.833	0.781	0.816	0.816	0.871	0.816	ns
HSTL_I_DCI_12_F	0.378	0.378	0.399	0.378	0.406	0.406	0.429	0.406	0.534	0.534	0.564	0.534	ns
HSTL_I_DCI_12_M	0.378	0.378	0.399	0.378	0.556	0.556	0.586	0.556	0.654	0.654	0.694	0.654	ns
HSTL_I_DCI_12_S	0.378	0.378	0.399	0.378	0.754	0.754	0.803	0.754	0.842	0.842	0.907	0.842	ns
HSTL_I_DCI_18_F	0.321	0.321	0.339	0.321	0.445	0.445	0.461	0.445	0.566	0.566	0.595	0.566	ns
HSTL_I_DCI_18_M	0.321	0.321	0.339	0.321	0.554	0.554	0.585	0.554	0.643	0.643	0.684	0.643	ns
HSTL_I_DCI_18_S	0.321	0.321	0.339	0.321	0.761	0.761	0.817	0.761	0.836	0.836	0.900	0.836	ns
HSTL_I_DCI_F	0.393	0.393	0.415	0.393	0.431	0.431	0.445	0.431	0.555	0.555	0.575	0.555	ns
HSTL_I_DCI_M	0.393	0.393	0.415	0.393	0.552	0.552	0.581	0.552	0.644	0.644	0.684	0.644	ns
HSTL_I_DCI_S	0.393	0.393	0.415	0.393	0.766	0.766	0.821	0.766	0.847	0.847	0.912	0.847	ns
HSTL_I_F	0.378	0.378	0.399	0.378	0.423	0.423	0.443	0.423	0.549	0.549	0.581	0.549	ns
HSTL_I_M	0.378	0.378	0.399	0.378	0.554	0.554	0.585	0.554	0.640	0.640	0.677	0.640	ns
HSTL_I_S	0.378	0.378	0.399	0.378	0.766	0.766	0.816	0.766	0.811	0.811	0.866	0.811	ns
HSUL_12_DCI_F	0.378	0.378	0.399	0.378	0.425	0.425	0.443	0.425	0.558	0.558	0.586	0.558	ns
HSUL_12_DCI_M	0.378	0.378	0.399	0.378	0.556	0.556	0.586	0.556	0.654	0.654	0.694	0.654	ns
HSUL_12_DCI_S	0.378	0.378	0.399	0.378	0.736	0.736	0.784	0.736	0.821	0.821	0.886	0.821	ns
HSUL_12_F	0.378	0.378	0.399	0.378	0.412	0.412	0.430	0.412	0.538	0.538	0.566	0.538	ns
HSUL_12_M	0.378	0.378	0.399	0.378	0.551	0.551	0.582	0.551	0.642	0.642	0.679	0.642	ns
HSUL_12_S	0.378	0.378	0.399	0.378	0.750	0.750	0.799	0.750	0.813	0.813	0.868	0.813	ns
LVCMOS12_F_2	0.512	0.512	0.555	0.512	0.672	0.672	0.692	0.672	0.898	0.898	0.922	0.898	ns
LVCMOS12_F_4	0.512	0.512	0.555	0.512	0.504	0.504	0.521	0.504	0.664	0.664	0.693	0.664	ns
LVCMOS12_F_6	0.512	0.512	0.555	0.512	0.485	0.485	0.507	0.485	0.634	0.634	0.669	0.634	ns
LVCMOS12_F_8	0.512	0.512	0.555	0.512	0.465	0.465	0.489	0.465	0.611	0.611	0.666	0.611	ns
LVCMOS12_M_2	0.512	0.512	0.555	0.512	0.708	0.708	0.727	0.708	0.916	0.916	0.945	0.916	ns
LVCMOS12_M_4	0.512	0.512	0.555	0.512	0.550	0.550	0.573	0.550	0.664	0.664	0.690	0.664	ns
LVCMOS12_M_6	0.512	0.512	0.555	0.512	0.527	0.527	0.554	0.527	0.622	0.622	0.652	0.622	ns
LVCMOS12_M_8	0.512	0.512	0.555	0.512	0.540	0.540	0.571	0.540	0.614	0.614	0.649	0.614	ns
LVCMOS12_S_2	0.512	0.512	0.555	0.512	0.767	0.767	0.803	0.767	0.990	0.990	1.024	0.990	ns
LVCMOS12_S_4	0.512	0.512	0.555	0.512	0.666	0.666	0.704	0.666	0.803	0.803	0.848	0.803	ns
LVCMOS12_S_6	0.512	0.512	0.555	0.512	0.657	0.657	0.695	0.657	0.732	0.732	0.774	0.732	ns
LVCMOS12_S_8	0.512	0.512	0.555	0.512	0.708	0.708	0.761	0.708	0.745	0.745	0.790	0.745	ns
LVCMOS15_F_12	0.414	0.414	0.445	0.414	0.500	0.500	0.522	0.500	0.647	0.647	0.682	0.647	ns
LVCMOS15_F_2	0.414	0.414	0.445	0.414	0.702	0.702	0.722	0.702	0.919	0.919	0.940	0.919	ns
LVCMOS15_F_4	0.414	0.414	0.445	0.414	0.579	0.579	0.601	0.579	0.755	0.755	0.781	0.755	ns
LVCMOS15_F_6	0.414	0.414	0.445	0.414	0.547	0.547	0.569	0.547	0.711	0.711	0.742	0.711	ns

Table 24: **IOB High Performance (HP) Switching Characteristics *(Cont'd)***

I/O Standards	$T_{INBUF\_DELAY\_PAD\_I}$				$T_{OUTBUF\_DELAY\_O\_PAD}$				$T_{OUTBUF\_DELAY\_TD\_PAD}$				Units
	0.90V	0.85V		0.72V	0.90V	0.85V		0.72V	0.90V	0.85V		0.72V	
	-3	-2	-1	-2	-3	-2	-1	-2	-3	-2	-1	-2	
POD12_DCI_F	0.409	0.409	0.431	0.409	0.425	0.425	0.443	0.425	0.558	0.558	0.586	0.558	ns
POD12_DCI_M	0.409	0.409	0.431	0.409	0.543	0.543	0.572	0.543	0.638	0.638	0.678	0.638	ns
POD12_DCI_S	0.409	0.409	0.431	0.409	0.772	0.772	0.822	0.772	0.862	0.862	0.929	0.862	ns
POD12_F	0.409	0.409	0.431	0.409	0.455	0.455	0.476	0.455	0.595	0.595	0.626	0.595	ns
POD12_M	0.409	0.409	0.431	0.409	0.551	0.551	0.582	0.551	0.641	0.641	0.679	0.641	ns
POD12_S	0.409	0.409	0.431	0.409	0.767	0.767	0.817	0.767	0.832	0.832	0.889	0.832	ns
SLVS_400_18	0.539	0.539	0.620	0.539	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	ns
SSTL12_DCI_F	0.381	0.381	0.399	0.381	0.425	0.425	0.443	0.425	0.558	0.558	0.586	0.558	ns
SSTL12_DCI_M	0.381	0.381	0.399	0.381	0.557	0.557	0.587	0.557	0.654	0.654	0.694	0.654	ns
SSTL12_DCI_S	0.381	0.381	0.399	0.381	0.754	0.754	0.803	0.754	0.842	0.842	0.908	0.842	ns
SSTL12_F	0.403	0.403	0.403	0.403	0.412	0.412	0.430	0.412	0.538	0.538	0.566	0.538	ns
SSTL12_M	0.403	0.403	0.403	0.403	0.553	0.553	0.584	0.553	0.641	0.641	0.676	0.641	ns
SSTL12_S	0.403	0.403	0.403	0.403	0.758	0.758	0.808	0.758	0.823	0.823	0.879	0.823	ns
SSTL135_DCI_F	0.366	0.366	0.399	0.366	0.411	0.411	0.428	0.411	0.537	0.537	0.565	0.537	ns
SSTL135_DCI_M	0.366	0.366	0.399	0.366	0.551	0.551	0.582	0.551	0.645	0.645	0.685	0.645	ns
SSTL135_DCI_S	0.366	0.366	0.399	0.366	0.746	0.746	0.799	0.746	0.829	0.829	0.893	0.829	ns
SSTL135_F	0.378	0.378	0.399	0.378	0.408	0.408	0.428	0.408	0.528	0.528	0.561	0.528	ns
SSTL135_M	0.378	0.378	0.399	0.378	0.555	0.555	0.585	0.555	0.641	0.641	0.679	0.641	ns
SSTL135_S	0.378	0.378	0.399	0.378	0.772	0.772	0.823	0.772	0.827	0.827	0.878	0.827	ns
SSTL15_DCI_F	0.402	0.402	0.417	0.402	0.412	0.412	0.429	0.412	0.531	0.531	0.563	0.531	ns
SSTL15_DCI_M	0.402	0.402	0.417	0.402	0.553	0.553	0.583	0.553	0.645	0.645	0.685	0.645	ns
SSTL15_DCI_S	0.402	0.402	0.417	0.402	0.768	0.768	0.822	0.768	0.847	0.847	0.912	0.847	ns
SSTL15_F	0.371	0.371	0.400	0.371	0.408	0.408	0.428	0.408	0.530	0.530	0.556	0.530	ns
SSTL15_M	0.371	0.371	0.400	0.371	0.554	0.554	0.585	0.554	0.639	0.639	0.677	0.639	ns
SSTL15_S	0.371	0.371	0.400	0.371	0.767	0.767	0.817	0.767	0.813	0.813	0.867	0.813	ns
SSTL18_I_DCI_F	0.329	0.329	0.336	0.329	0.445	0.445	0.461	0.445	0.566	0.566	0.595	0.566	ns
SSTL18_I_DCI_M	0.329	0.329	0.336	0.329	0.554	0.554	0.585	0.554	0.644	0.644	0.683	0.644	ns
SSTL18_I_DCI_S	0.329	0.329	0.336	0.329	0.762	0.762	0.818	0.762	0.837	0.837	0.899	0.837	ns
SSTL18_I_F	0.316	0.316	0.337	0.316	0.454	0.454	0.476	0.454	0.578	0.578	0.608	0.578	ns
SSTL18_I_M	0.316	0.316	0.337	0.316	0.571	0.571	0.603	0.571	0.652	0.652	0.692	0.652	ns
SSTL18_I_S	0.316	0.316	0.337	0.316	0.782	0.782	0.835	0.782	0.816	0.816	0.870	0.816	ns
SUB_LVDS	0.539	0.539	0.620	0.539	0.660	0.660	0.692	0.660	969.863	969.863	969.863	969.863	ns

IOB 3-state Output Switching Characteristics

Table 25 specifies the values of $T_{OUTBUF\_DELAY\_TE\_PAD}$ and $T_{INBUF\_DELAY\_IBUFDIS\_O}$. $T_{OUTBUF\_DELAY\_TE\_PAD}$ is the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is enabled (i.e., a high impedance state). $T_{INBUF\_DELAY\_IBUFDIS\_O}$ is the IOB delay from IBUFDISABLE to O output. In HP I/O banks, the internal DCI termination turn-off time is always faster than $T_{OUTBUF\_DELAY\_TE\_PAD}$ when the DCITERMDISABLE pin is used.

Table 25: **IOB 3-state Output Switching Characteristics**

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages				Units
		0.90V	0.85V		0.72V	
		-3	-2	-1	-2	
$T_{OUTBUF\_DELAY\_TE\_PAD}$	T input to pad high-impedance for the I/O banks	5.330	5.330	5.341	5.330	ns
$T_{INBUF\_DELAY\_IBUFDIS\_O}$	IBUF turn-on time from IBUFDISABLE to O output for the I/O banks	0.936	0.936	1.037	0.936	ns

Input Delay Measurement Methodology

Table 26 shows the test setup parameters used for measuring input delay.

Table 26: **Input Delay Measurement Methodology**

Description	I/O Standard Attribute	V_L (1)(2)	V_H (1)(2)	V_{MEAS} (1)(4)(6)	V_{REF} (1)(3)(5)
LVCMOS, 1.2V	LVCMOS12	0.1	1.1	0.6	–
LVCMOS, LVDCI, HSLVDCI, 1.5V	LVCMOS15, LVDCI_15, HSLVDCI_15	0.1	1.4	0.75	–
LVCMOS, LVDCI, HSLVDCI, 1.8V	LVCMOS18, LVDCI_18, HSLVDCI_18	0.1	1.7	0.9	–
HSTL (high-speed transceiver logic), class I, 1.2V	HSTL_I_12	V_{REF} – 0.25	V_{REF} + 0.25	V_{REF}	0.6
HSTL, class I, 1.5V	HSTL_I	V_{REF} – 0.325	V_{REF} + 0.325	V_{REF}	0.75
HSTL, class I, 1.8V	HSTL_I_18	V_{REF} – 0.4	V_{REF} + 0.4	V_{REF}	0.9
HSUL (high-speed unterminated logic), 1.2V	HSUL_12	V_{REF} – 0.25	V_{REF} + 0.25	V_{REF}	0.6
SSTL12 (stub series terminated logic), 1.2V	SSTL12	V_{REF} – 0.25	V_{REF} + 0.25	V_{REF}	0.6
SSTL135 and SSTL135 class II, 1.35V	SSTL135, SSTL135_II	V_{REF} – 0.2875	V_{REF} + 0.2875	V_{REF}	0.675
SSTL15 and SSTL15 class II, 1.5V	SSTL15, SSTL15_II	V_{REF} – 0.325	V_{REF} + 0.325	V_{REF}	0.75
SSTL18, class I and II, 1.8V	SSTL18_I, SSTL18_II	V_{REF} – 0.4	V_{REF} + 0.4	V_{REF}	0.9
POD10, 1.0V	POD10	V_{REF} – 0.2	V_{REF} + 0.2	V_{REF}	0.7
POD12, 1.2V	POD12	V_{REF} – 0.24	V_{REF} + 0.24	V_{REF}	0.84
DIFF_HSTL, class I, 1.2V	DIFF_HSTL_I_12	0.6 – 0.25	0.6 + 0.25	0 (6)	–
DIFF_HSTL, class I, 1.5V	DIFF_HSTL_I	0.75 – 0.325	0.75 + 0.325	0 (6)	–
DIFF_HSTL, class I, 1.8V	DIFF_HSTL_I_18	0.9 – 0.4	0.9 + 0.4	0 (6)	–

Clock Buffers and Networks

Table 32: **Clock Buffers Switching Characteristics**

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages				Units
		0.90V	0.85V		0.72V	
		-3	-2	-1	-2	
Global Clock Switching Characteristics (Including BUFGCTRL)						
F_{MAX}	Maximum frequency of a global clock tree (BUFG).	891	775	667	725	MHz
Global Clock Buffer with Input Divide Capability (BUFGCE_DIV)						
F_{MAX}	Maximum frequency of a global clock buffer with input divide capability (BUFGCE_DIV).	891	775	667	725	MHz
Global Clock Buffer with Clock Enable (BUFGCE)						
F_{MAX}	Maximum frequency of a global clock buffer with clock enable (BUFGCE).	891	775	667	725	MHz
Leaf Clock Buffer with Clock Enable (BUFCE_LEAF)						
F_{MAX}	Maximum frequency of a leaf clock buffer with clock enable (BUFCE_LEAF).	891	775	667	725	MHz
GTY Clock Buffer with Clock Enable and Clock Input Divide Capability (BUFG_GT)						
F_{MAX}	Maximum frequency of a serial transceiver clock buffer with clock enable and clock input divide capability.	512	512	512	512	MHz

MMCM Switching Characteristics

Table 33: **MMCM Specification**

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages				Units
		0.90V	0.85V		0.72V	
		-3	-2	-1	-2	
MMCM_F_{INMAX}	Maximum input clock frequency.	1066	933	800	933	MHz
MMCM_F_{INMIN}	Minimum input clock frequency.	10	10	10	10	MHz
MMCM_$F_{INJITTER}$	Maximum input clock period jitter.	< 20% of clock input period or 1 ns Max				
MMCM_F_{INDUTY}	Input duty cycle range: 10–49 MHz.	25–75				%
	Input duty cycle range: 50–199 MHz.	30–70				%
	Input duty cycle range: 200–399 MHz.	35–65				%
	Input duty cycle range: 400–499 MHz.	40–60				%
	Input duty cycle range: >500 MHz.	45–55				%
MMCM_F_{MIN_PSCLK}	Minimum dynamic phase shift clock frequency.	0.01	0.01	0.01	0.01	MHz
MMCM_F_{MAX_PSCLK}	Maximum dynamic phase shift clock frequency.	550	500	450	500	MHz
MMCM_F_{VCOMIN}	Minimum MMCM VCO frequency.	800	800	800	800	MHz
MMCM_F_{VCOMAX}	Maximum MMCM VCO frequency.	1600	1600	1600	1600	MHz
MMCM_$F_{BANDWIDTH}$	Low MMCM bandwidth at typical.(1)	1.00	1.00	1.00	1.00	MHz
	High MMCM bandwidth at typical.(1)	4.00	4.00	4.00	4.00	MHz
MMCM_$T_{STATPHAOFFSET}$	Static phase offset of the MMCM outputs.(2)	0.12	0.12	0.12	0.12	ns
MMCM_$T_{OUTJITTER}$	MMCM output jitter.	Note 3				
MMCM_$T_{OUTDUTY}$	MMCM output clock duty cycle precision.(4)	0.165	0.20	0.20	0.20	ns
MMCM_$T_{LOCKMAX}$	MMCM maximum lock time for MMCM_F_{PFDMIN}.	100	100	100	100	µs
MMCM_F_{OUTMAX}	MMCM maximum output frequency.	891	775	667	725	MHz
MMCM_F_{OUTMIN}	MMCM minimum output frequency.(4)(5)	6.25	6.25	6.25	6.25	MHz
MMCM_$T_{EXTFDVAR}$	External clock feedback variation.	< 20% of clock input period or 1 ns Max				
MMCM_$RST_{MINPULSE}$	Minimum reset pulse width.	5.00	5.00	5.00	5.00	ns
MMCM_F_{PFDMAX}	Maximum frequency at the phase frequency detector.	550	500	450	500	MHz
MMCM_F_{PFDMIN}	Minimum frequency at the phase frequency detector.	10	10	10	10	MHz
MMCM_$T_{FBDELAY}$	Maximum delay in the feedback path.	5 ns Max or one clock cycle				
MMCM_F_{DPRCLK_MAX}	Maximum DRP clock frequency	250	250	250	250	MHz

Notes:

1. The MMCM does not filter typical spread-spectrum input clocks because they are usually far below the bandwidth filter frequencies.
2. The static offset is measured between any MMCM outputs with identical phase.
3. Values for this parameter are available in the Clocking Wizard.
4. Includes global clock buffer.
5. Calculated as F_{VCO}/128 assuming output duty cycle is 50%.

Table 37: **Global Clock Input to Output Delay With MMCM**

Symbol	Description	Device	Speed Grade and V_{CCINT} Operating Voltages				Units
			0.90V	0.85V		0.72V	
			-3	-2	-1	-2	
SSTL15 Global Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, with MMCM.							
$T_{ICKOFMMCMCC}$	Global clock input and output flip-flop *with* MMCM.	XCVU3P	1.80	1.80	1.94	2.34	ns
		XCVU5P	1.80	1.80	1.94	2.34	ns
		XCVU7P	1.80	1.80	1.94	2.34	ns
		XCVU9P	1.80	1.80	1.94	2.34	ns
		XCVU11P	1.56	1.56	1.68	2.07	ns
		XCVU13P	1.56	1.56	1.68	2.07	ns

Notes:

1. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible I/O and CLB flip-flops are clocked by the global clock net in a single SLR.
2. MMCM output jitter is already included in the timing calculation.

Table 50: **GTY Transceiver Transmitter Switching Characteristics**

Symbol	Description	Condition	Min	Typ	Max	Units
F_{GTYTX}	Serial data rate range		0.500	–	F_{GTYMAX}	Gb/s
T_{RTX}	TX rise time	20%–80%	–	21	–	ps
T_{FTX}	TX fall time	80%–20%	–	21	–	ps
T_{LLSKEW}	TX lane-to-lane skew(1)		–	–	500.00	ps
$T_{J32.75}$	Total jitter(2)(4)	32.75 Gb/s	–	–	0.35	UI
$D_{J32.75}$	Deterministic jitter(2)(4)		–	–	0.19	UI
$T_{J28.21}$	Total jitter(2)(4)	28.21 Gb/s	–	–	0.28	UI
$D_{J28.21}$	Deterministic jitter(2)(4)		–	–	0.17	UI
$T_{J16.375}$	Total jitter(2)(4)	16.375 Gb/s	–	–	0.28	UI
$D_{J16.375}$	Deterministic jitter(2)(4)		–	–	0.17	UI
$T_{J15.0}$	Total jitter(2)(4)	15.0 Gb/s	–	–	0.28	UI
$D_{J15.0}$	Deterministic jitter(2)(4)		–	–	0.17	UI
$T_{J14.1}$	Total jitter(2)(4)	14.1 Gb/s	–	–	0.28	UI
$D_{J14.1}$	Deterministic jitter(2)(4)		–	–	0.17	UI
$T_{J14.1}$	Total jitter(2)(4)	14.025 Gb/s	–	–	0.28	UI
$D_{J14.1}$	Deterministic jitter(2)(4)		–	–	0.17	UI
$T_{J13.1}$	Total jitter(2)(4)	13.1 Gb/s	–	–	0.28	UI
$D_{J13.1}$	Deterministic jitter(2)(4)		–	–	0.17	UI
$T_{J12.5\_QPLL}$	Total jitter(2)(4)	12.5 Gb/s	–	–	0.28	UI
$D_{J12.5\_QPLL}$	Deterministic jitter(2)(4)		–	–	0.17	UI
$T_{J12.5\_CPLL}$	Total jitter(3)(4)	12.5 Gb/s	–	–	0.33	UI
$D_{J12.5\_CPLL}$	Deterministic jitter(3)(4)		–	–	0.17	UI
$T_{J11.3}$	Total jitter(2)(4)	11.3 Gb/s	–	–	0.28	UI
$D_{J11.3}$	Deterministic jitter(2)(4)		–	–	0.17	UI
$T_{J10.3125\_QPLL}$	Total jitter(2)(4)	10.3125 Gb/s	–	–	0.28	UI
$D_{J10.3125\_QPLL}$	Deterministic jitter(2)(4)		–	–	0.17	UI
$T_{J10.3125\_CPLL}$	Total jitter(3)(4)	10.3125 Gb/s	–	–	0.33	UI
$D_{J10.3125\_CPLL}$	Deterministic jitter(3)(4)		–	–	0.17	UI
$T_{J9.953\_QPLL}$	Total jitter(2)(4)	9.953 Gb/s	–	–	0.28	UI
$D_{J9.953\_QPLL}$	Deterministic jitter(2)(4)		–	–	0.17	UI
$T_{J9.953\_CPLL}$	Total jitter(3)(4)	9.953 Gb/s	–	–	0.33	UI
$D_{J9.953\_CPLL}$	Deterministic jitter(3)(4)		–	–	0.17	UI
$T_{J8.0}$	Total jitter(3)(4)	8.0 Gb/s	–	–	0.32	UI
$D_{J8.0}$	Deterministic jitter(3)(4)		–	–	0.17	UI
$T_{J6.6}$	Total jitter(3)(4)	6.6 Gb/s	–	–	0.30	UI
$D_{J6.6}$	Deterministic jitter(3)(4)		–	–	0.15	UI
$T_{J5.0}$	Total jitter(3)(4)	5.0 Gb/s	–	–	0.30	UI
$D_{J5.0}$	Deterministic jitter(3)(4)		–	–	0.15	UI
$T_{J4.25}$	Total jitter(3)(4)	4.25 Gb/s	–	–	0.30	UI
$D_{J4.25}$	Deterministic jitter(3)(4)		–	–	0.15	UI

Table 50: **GTY Transceiver Transmitter Switching Characteristics *(Cont'd)***

Symbol	Description	Condition	Min	Typ	Max	Units
$T_{J3.20}$	Total jitter(3)(4)	3.20 Gb/s(5)	–	–	0.20	UI
$D_{J3.20}$	Deterministic jitter(3)(4)		–	–	0.10	UI
$T_{J2.5}$	Total jitter(3)(4)	2.5 Gb/s(6)	–	–	0.20	UI
$D_{J2.5}$	Deterministic jitter(3)(4)		–	–	0.10	UI
$T_{J1.25}$	Total jitter(3)(4)	1.25 Gb/s(7)	–	–	0.15	UI
$D_{J1.25}$	Deterministic jitter(3)(4)		–	–	0.06	UI
T_{J500}	Total jitter(3)(4)	500 Mb/s(8)	–	–	0.10	UI
D_{J500}	Deterministic jitter(3)(4)		–	–	0.03	UI

Notes:

1. Using same REFCLK input with TX phase alignment enabled for up to four consecutive transmitters (one fully populated GTY Quad) at maximum line rate.
2. Using QPLL_FBDIV = 40, 20-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
3. Using CPLL_FBDIV = 2, 20-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
4. All jitter values are based on a bit-error ratio of 10^{-12}.
5. CPLL frequency at 3.2 GHz and TXOUT_DIV = 2.
6. CPLL frequency at 2.5 GHz and TXOUT_DIV = 2.
7. CPLL frequency at 2.5 GHz and TXOUT_DIV = 4.
8. CPLL frequency at 2.0 GHz and TXOUT_DIV = 8.

Table 52: **GTY Transceiver Protocol List *(Cont'd)***

Protocol	Specification	Serial Rate (Gb/s)	Electrical Compliance
Serial RapidIO	RapidIO specification 3.1	1.25–10.3125	Compliant
DisplayPort (source only)	DP 1.2B CTS	1.62–5.4	Compliant(3)
Fibre channel	FC-PI-4	1.0625–14.025	Compliant
SATA Gen1, 2, 3	Serial ATA revision 3.0 specification	1.5, 3.0, and 6.0	Compliant
SAS Gen1, 2, 3	T10/BSR INCITS 519	3.0, 6.0, and 12.0	Compliant
SFI-5	OIF-SFI5-01.0	0.625 - 12.5	Compliant
Aurora	CEI-6G, CEI-11G-LR	All rates	Compliant

Notes:

1. 25 dB loss at Nyquist without FEC.
2. The transition time of the transmitter is faster than the IEEE Std 802.3-2012 specification.
3. This protocol requires external circuitry to achieve compliance.

Integrated Interface Block for 100G Ethernet MAC and PCS

More information and documentation on solutions using the integrated 100 Gb/s Ethernet block can be found at UltraScale Integrated 100G Ethernet MAC/PCS. The *UltraScale Architecture and Product Overview* (DS890) lists how many blocks are in each Virtex UltraScale+ FPGA.

Table 56: **Maximum Performance for 100G Ethernet Designs**

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages				Units
		0.90V	0.85V		0.72V	
		-3	-2(1)	-1	-2	
F_{TX_CLK}	Transmit clock	390.625	390.625	322.223	322.223	MHz
F_{RX_CLK}	Receive clock	390.625	390.625	322.223	322.223	MHz
$F_{RX\_SERDES\_CLK}$	Receive serializer/deserializer clock	390.625	390.625	322.223	322.223	MHz
F_{DRP_CLK}	Dynamic reconfiguration port clock	250.00	250.00	250.00	250.00	MHz

Notes:

1. The maximum clock frequency of 390.625 MHz only applies to the CAUI-10 interface. The maximum clock frequency for the CAUI-4 interface is 322.223 MHz.

Integrated Interface Block for PCI Express Designs

More information and documentation on solutions for PCI Express designs can be found at PCI Express. The *UltraScale Architecture and Product Overview* (DS890) lists how many blocks are in each Virtex UltraScale+ FPGA.

Table 57: **Maximum Performance for PCI Express Designs(1)(2)**

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages				Units
		0.90V	0.85V		0.72V	
		-3	-2	-1	-2	
$F_{PIPECLK}$	Pipe clock maximum frequency.	250.00	250.00	250.00	250.00	MHz
$F_{CORECLK}$	Core clock maximum frequency.	500.00	500.00	500.00	250.00	MHz
F_{DRPCLK}	DRP clock maximum frequency.	250.00	250.00	250.00	250.00	MHz
$F_{MCAPCLK}$	MCAP clock maximum frequency.	125.00	125.00	125.00	125.00	MHz

Notes:

1. PCI Express Gen4 operation is supported for x1, x2, x4, and x8 widths.
2. PCI Express Gen4 operation is supported in -3E, -2E, and -2I speed grades.

System Monitor Specifications

Table 58: **System Monitor Specifications**

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
V_{CCADC} = 1.8V ±3%, V_{REFP} = 1.25V, V_{REFN} = 0V, ADCCLK = 5.2 MHz, T_j = –40°C to 100°C, typical values at T_j = 40°C						
ADC Accuracy(1)						
Resolution			10	–	–	Bits
Integral nonlinearity(2)	INL		–	–	±1.5	LSBs
Differential nonlinearity	DNL	No missing codes, guaranteed monotonic	–	–	±1	LSBs
Offset error		Offset calibration enabled	–	–	±2	LSBs
Gain error			–	–	±0.4	%
Sample rate			–	–	0.2	MS/s
RMS code noise		External 1.25V reference	–	–	1	LSBs
		On-chip reference	–	1	–	LSBs
ADC Accuracy at Extended Temperatures						
Resolution		T_j = –55°C to 125°C	10	–	–	Bits
Integral nonlinearity	INL	T_j = –55°C to 125°C	–	–	±1.5	LSBs
Differential nonlinearity	DNL	No missing codes, guaranteed monotonic T_j = –55°C to 125°C	–	–	±1	
Analog Inputs(2)						
ADC input ranges		Unipolar operation	0	–	1	V
		Bipolar operation	–0.5	–	+0.5	V
		Unipolar common mode range (FS input)	0	–	+0.5	V
		Bipolar common mode range (FS input)	+0.5	–	+0.6	V
Maximum external channel input ranges		Adjacent channels set within these ranges should not corrupt measurements on adjacent channels	–0.1	–	V_{CCADC}	V
On-Chip Sensor Accuracy						
Temperature sensor error(1)(3)		T_j = –55°C to 125°C (with external REF)	–	–	±3	°C
		T_j = –55°C to 110°C (with internal REF)	–	–	±3.5	°C
		T_j = 110°C to 125°C (with internal REF)	–	–	±5	°C

SYSMON I2C/PMBus Interfaces

Table 59: **SYSMON I2C Fast Mode Interface Switching Characteristics(1)**

Symbol	Description	Min	Max	Units
T_{SMFCKL}	SCL Low time	1.3	–	µs
T_{SMFCKH}	SCL High time	0.6	–	µs
T_{SMFCKO}	SDAO clock-to-out delay	–	900	ns
T_{SMFDCK}	SDAI setup time	100	–	ns
F_{SMFCLK}	SCL clock frequency	–	400	kHz

Notes:

1. The test conditions are configured to the LVCMOS 1.8V I/O standard.

Table 60: **SYSMON I2C Standard Mode Interface Switching Characteristics(1)**

Symbol	Description	Min	Max	Units
T_{SMSCKL}	SCL Low time	4.7	–	µs
T_{SMSCKH}	SCL High time	4.0	–	µs
T_{SMSCKO}	SDAO clock-to-out delay	–	3450	ns
T_{SMSDCK}	SDAI setup time	250	–	ns
F_{SMSCLK}	SCL clock frequency	–	100	kHz

Notes:

1. The test conditions are configured to the LVCMOS 1.8V I/O standard.

Table 61: **Configuration Switching Characteristics *(Cont'd)***

Symbol	Description		Speed Grade and V_{CCINT} Operating Voltages				Units
			0.90V	0.85V		0.72V	
			-3	-2	-1	-2	
SelectMAP Mode Programming Switching							
T_{SMDCCK}/T_{SMCCKD}	D[31:00] setup/hold.	XCVU3P, XCVU5P, XCVU7P, XCVU9P	4.0/0	4.0/0	4.0/0	5.0/0	ns, Min
		XCVU11P, XCVU13P	4.5/0	4.5/0	4.5/0	7.5/0	ns, Min
$T_{SMCSCCK}/T_{SMCCKCS}$	CSI_B setup/hold.	XCVU3P, XCVU5P, XCVU7P, XCVU9P	4.0/0	4.0/0	4.0/0	5.0/0	ns, Min
		XCVU11P, XCVU13P	4.5/0	4.5/0	4.5/0	7.5/0	ns, Min
T_{SMWCCK}/T_{SMCCKW}	RDWR_B setup/hold.	XCVU3P, XCVU5P, XCVU7P, XCVU9P	10.0/0	10.0/0	10.0/0	11.0/0	ns, Min
		XCVU11P, XCVU13P	11.0/0	11.0/0	11.0/0	17.0/0	ns, Min
$T_{SMCKCSO}$	CSO_B clock to out (330Ω pull-up resistor required).		7.0	7.0	7.0	7.0	ns, Max
T_{SMCO}	D[31:00] clock to out in readback.		8.0	8.0	8.0	8.0	ns, Max
F_{RBCCK}	Readback frequency.	XCVU3P, XCVU5P, XCVU7P, XCVU9P	125	125	125	100	MHz, Max
		XCVU11P, XCVU13P	125	125	125	66	MHz, Max
Boundary-Scan Port Timing Specifications							
T_{TAPTCK}/T_{TCKTAP}	TMS and TDI setup/hold.	XCVU3P	3.0/ 2.0	3.0/ 2.0	3.0/ 2.0	3.0/ 2.0	ns, Min
		XCVU5P, XCVU7P, XCVU9P, XCVU11P, XCVU13P	8.5/ 2.0	8.5/ 2.0	8.5/ 2.0	8.5/ 2.0	ns, Min
T_{TCKTDO}	TCK falling edge to TDO output.	XCVU3P	7.0	7.0	7.0	7.0	ns, Max
		XCVU5P, XCVU7P, XCVU9P, XCVU11P, XCVU13P	15.0	15.0	15.0	15.0	ns, Max
F_{TCK}	TCK frequency.	XCVU3P	66	66	66	66	MHz, Max
		XCVU5P, XCVU7P, XCVU9P, XCVU11P, XCVU13P	20	20	20	20	MHz, Max
BPI Master Flash Mode Programming Switching							
T_{BPICCO}	A[28:00], RS[1:0], FCS_B, FOE_B, FWE_B, ADV_B clock to out.		10	10	10	10	ns, Max
T_{BPIDCC}/T_{BPICCD}	D[15:00] setup/hold.	XCVU3P, XCVU5P, XCVU7P, XCVU9P	4.0/0	4.0/0	4.0/0	5.0/0	ns, Min
		XCVU11P, XCVU13P	4.5/0	4.5/0	4.5/0	7.5/0	ns, Min
SPI Master Flash Mode Programming Switching							
T_{SPIDCC}/T_{SPICCD}	D[03:00] setup/hold.		3.0/0	3.0/0	3.0/0	4.0/0	ns, Min
T_{SPIDCC}/T_{SPICCD}	D[07:04] setup/hold.	XCVU3P, XCVU5P, XCVU7P, XCVU9P	4.0/0	4.0/0	4.0/0	5.0/0	ns, Min
		XCVU11P, XCVU13P	4.5/0	4.5/0	4.5/0	7.5/0	ns, Min
T_{SPICCM}	MOSI clock to out.		8.0	8.0	8.0	8.0	ns, Max
$T_{SPICCFC}$	FCS_B clock to out.		8.0	8.0	8.0	8.0	ns, Max

Table 61: **Configuration Switching Characteristics *(Cont'd)***

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages				Units
		0.90V	0.85V		0.72V	
		-3	-2	-1	-2	
DNA Port Switching						
F_{DNACK}	DNA port frequency.	200	200	200	175	MHz, Max
STARTUPE3 Ports						
$T_{USRCCLKO}$	STARTUPE3 USRCCLKO input port to CCLK pin output delay.	0.25/ 6.00	0.25/ 6.50	0.25/ 7.50	0.25/ 9.00	ns, Min/Max
T_{DO}	DO[3:0] ports to D03-D00 pins output delay.	0.25/ 6.70	0.25/ 7.70	0.25/ 8.40	0.25/ 10.00	ns, Min/Max
T_{DTS}	DTS[3:0] ports to D03-D00 pins 3-state delays.	0.25/ 6.70	0.25/ 7.70	0.25/ 8.40	0.25/ 10.00	ns, Min/Max
T_{FCSBO}	FCSBO port to FCS_B pin output delay.	0.25/ 6.90	0.25/ 7.50	0.25/ 8.40	0.25/ 9.80	ns, Min/Max
T_{FCSBTS}	FCSBTS port to FCS_B pin 3-state delay.	0.25/ 6.90	0.25/ 7.50	0.25/ 8.40	0.25/ 9.80	ns, Min/Max
$T_{USRDONEO}$	USRDONEO port to DONE pin output delay.	0.25/ 8.60	0.25/ 9.40	0.25/ 10.50	0.25/ 12.10	ns, Min/Max
$T_{USRDONETS}$	USRDONETS port to DONE pin 3-state delay.	0.25/ 8.60	0.25/ 9.40	0.25/ 10.50	0.25/ 12.10	ns, Min/Max
T_{DI}	D03-D00 pins to DI[3:0] ports input delay.	0.5/ 2.6	0.5/ 3.1	0.5/ 3.5	0.5/ 4.0	ns, Min/Max
$F_{CFGMCLK}$	STARTUPE3 CFGMCLK output frequency.	50	50	50	50	MHz, Typ
$F_{CFGMCLKTOL}$	STARTUPE3 CFGMCLK output frequency tolerance.	±15	±15	±15	±15	%, Max
T_{DCI_MATCH}	Specifies a stall in the startup cycle until the digitally controlled impedance (DCI) match signals are asserted.	4	4	4	4	ms, Max

Notes:

1. When the CCLK is sourced from the EMCCLK pin with a divide-by-one setting, the external EMCCLK must meet this duty-cycle requirement.