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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	147780
Number of Logic Elements/Cells	2586150
Total RAM Bits	391168000
Number of I/O	702
Number of Gates	-
Voltage - Supply	0.873V ~ 0.927V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 100°C (TJ)
Package / Case	2104-BBGA, FCBGA
Supplier Device Package	2104-FCBGA (47.5x47.5)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xcvu9p-3flgb2104e

Table 1: **Absolute Maximum Ratings(1) *(Cont'd)***

Symbol	Description	Min	Max	Units
I_{RMS}	Available RMS output current at the pad.	–20	20	mA
GTY Transceivers				
$V_{MGTAVCC}$	Analog supply voltage for transceiver circuits.	–0.500	1.000	V
$V_{MGTAVTT}$	Analog supply voltage for transceiver termination circuits.	–0.500	1.300	V
$V_{MGTVCCAUX}$	Auxiliary analog Quad PLL (QPLL) voltage supply for transceivers.	–0.500	1.900	V
$V_{MGTREFCLK}$	Transceiver reference clock absolute input voltage.	–0.500	1.300	V
$V_{MGTAVTTRCAL}$	Analog supply voltage for the resistor calibration circuit of the transceiver column.	–0.500	1.300	V
V_{IN}	Receiver (RXP/RXN) and transmitter (TXP/TXN) absolute input voltage.	–0.500	1.200	V
$I_{DCIN-FLOAT}$	DC input current for receiver input pins DC coupled RX termination = floating.(7)	–	10	mA
$I_{DCIN-MGTAVTT}$	DC input current for receiver input pins DC coupled RX termination = $V_{MGTAVTT}$.	–	10	mA
$I_{DCIN-GND}$	DC input current for receiver input pins DC coupled RX termination = GND.(8)	–	0	mA
$I_{DCIN-PROG}$	DC input current for receiver input pins DC coupled RX termination = programmable.(9)	–	0	mA
$I_{DCOUT-FLOAT}$	DC output current for transmitter pins DC coupled RX termination = floating.	–	6	mA
$I_{DCOUT-MGTAVTT}$	DC output current for transmitter pins DC coupled RX termination = $V_{MGTAVTT}$.	–	6	mA
System Monitor				
V_{CCADC}	System Monitor supply relative to GNDADC.	0.500	2.000	V
V_{REFP}	System Monitor reference input relative to GNDADC.	0.500	2.000	V
Temperature				
T_{STG}	Storage temperature (ambient).	–65	150	°C
T_{SOL}	Maximum soldering temperature.(11)	–	260	°C
T_j	Maximum junction temperature.(11)	–	125	°C

Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.
2. V_{CCINT_IO} must be connected to V_{CCBRAM}.
3. V_{CCAUX_IO} must be connected to V_{CCAUX}.
4. The lower absolute voltage specification always applies.
5. For I/O operation, see the *UltraScale Architecture SelectIO Resources User Guide* (UG571).
6. When operating outside of the recommended operating conditions, refer to Table 4 for maximum overshoot and undershoot specifications.
7. AC coupled operation is not supported for RX termination = floating.
8. For GTY transceivers, DC coupled operation is not supported for RX termination = GND.
9. DC coupled operation is not supported for RX termination = programmable.
10. For more information on supported GTY transceiver terminations see the or *UltraScale Architecture GTY Transceiver User Guide* (UG578)
11. For soldering guidelines and thermal considerations, see the *UltraScale and UltraScale+ FPGA Packaging and Pinout Specifications* (UG575).

Table 3: **DC Characteristics Over Recommended Operating Conditions *(Cont'd)***

Symbol	Description	Min	Typ(1)	Max	Units
Uncalibrated programmable on-die termination in I/O banks (measured per JEDEC specification)					
$R^{(9)}$	Thevenin equivalent resistance of programmable input termination to $V_{CCO}/2$ where ODT = RTT_40.	–50%	40	+50%	Ω
	Thevenin equivalent resistance of programmable input termination to $V_{CCO}/2$ where ODT = RTT_48.	–50%	48	+50%	Ω
	Thevenin equivalent resistance of programmable input termination to $V_{CCO}/2$ where ODT = RTT_60.	–50%	60	+50%	Ω
	Programmable input termination to V_{CCO} where ODT = RTT_40.	–50%	40	+50%	Ω
	Programmable input termination to V_{CCO} where ODT = RTT_48.	–50%	48	+50%	Ω
	Programmable input termination to V_{CCO} where ODT = RTT_60.	–50%	60	+50%	Ω
	Programmable input termination to V_{CCO} where ODT = RTT_120.	–50%	120	+50%	Ω
	Programmable input termination to V_{CCO} where ODT = RTT_240.	–50%	240	+50%	Ω
Internal V_{REF}	50% V_{CCO}	V_{CCO} x 0.49	V_{CCO} x 0.50	V_{CCO} x 0.51	V
	70% V_{CCO}	V_{CCO} x 0.69	V_{CCO} x 0.70	V_{CCO} x 0.71	V
Differential termination	Programmable differential termination (TERM_100) for the I/O banks.	–35%	100	+35%	Ω
n	Temperature diode ideality factor.	–	1.026	–	–
r	Temperature diode series resistance.	–	2	–	Ω

Notes:

1. Typical values are specified at nominal voltage, 25°C.
2. For the I/O banks with a V_{CCO} of 1.8V and separated V_{CCO} and V_{CCAUX_IO} power supplies, the I_L maximum current is 70 µA.
3. This measurement represents the die capacitance at the pad, not including the package.
4. Maximum value specified for worst case process at 25°C.
5. I_{BATT} is measured when the battery-backed RAM (BBRAM) is enabled.
6. Do not program eFUSE during device configuration (e.g., during configuration, during configuration readback, or when readback CRC is active).
7. If VRP resides at a different bank (DCI cascade), the range increases to ±15%.
8. VRP resistor tolerance is (240Ω ±1%)
9. On-die input termination resistance, for more information see the *UltraScale Architecture SelectIO Resources User Guide* (UG571).

Table 5: **Typical Quiescent Supply Current(1)(2)(3) *(Cont'd)***

Symbol	Description	Device	Speed Grade and V_{CCINT} Operating Voltages				Units
			0.90V	0.85V		0.72V	
			-3	-2	-1	-2	
I_{CCAUX_IOQ}	Quiescent V_{CCAUX_IO} supply current.	XCVU3P	62	62	62	62	mA
		XCVU5P	124	124	124	124	mA
		XCVU7P	124	124	124	124	mA
		XCVU9P	187	187	187	187	mA
		XCVU11P	79	79	79	79	mA
		XCVU13P	105	105	105	105	mA
$I_{CCBRAMQ}$	Quiescent V_{CCBRAM} supply current.	XCVU3P	45	43	43	43	mA
		XCVU5P	90	85	85	85	mA
		XCVU7P	90	85	85	85	mA
		XCVU9P	134	128	128	128	mA
		XCVU11P	130	124	124	124	mA
		XCVU13P	174	165	165	165	mA

Notes:

1. Typical values are specified at nominal voltage, 85°C junction temperatures (T_j) with single-ended SelectIO™ resources.
2. Typical values are for blank configured devices with no output current loads, no active input pull-up resistors, all I/O pins are 3-state and floating.
3. Use the Xilinx Power Estimator (XPE) spreadsheet tool (download at www.xilinx.com/power) to estimate static power consumption for conditions other than those specified.

Power-On/Off Power Supply Sequencing

The recommended power-on sequence is V_{CCINT}, V_{CCINT_IO}/V_{CCBRAM}, V_{CCAUX}/V_{CCAUX_IO}, and V_{CCO} to achieve minimum current draw and ensure that the I/Os are 3-stated at power-on. The recommended power-off sequence is the reverse of the power-on sequence. If V_{CCINT} and V_{CCINT_IO}/V_{CCBRAM} have the same recommended voltage levels, they can be powered by the same supply and ramped simultaneously. V_{CCINT_IO} must be connected to V_{CCBRAM}. If V_{CCAUX}/V_{CCAUX_IO} and V_{CCO} have the same recommended voltage levels, they can be powered by the same supply and ramped simultaneously. V_{CCAUX} and V_{CCAUX_IO} must be connected together. V_{CCADC} and V_{REF} can be powered at any time and have no power-up sequencing requirements.

The recommended power-on sequence to achieve minimum current draw for the GTY transceivers are V_{CCINT}, $V_{MGTAVCC}$, $V_{MGTAVTT}$ OR $V_{MGTAVCC}$, V_{CCINT}, $V_{MGTAVTT}$. There is no recommended sequencing for $V_{MGTVCCAUX}$. Both $V_{MGTAVCC}$ and V_{CCINT} can be ramped simultaneously. The recommended power-off sequence is the reverse of the power-on sequence to achieve minimum current draw.

If these recommended sequences are not met, current drawn from $V_{MGTAVTT}$ can be higher than specifications during power-up and power-down.

DC Input and Output Levels

Values for V_{IL} and V_{IH} are recommended input voltages. Values for I_{OL} and I_{OH} are guaranteed over the recommended operating conditions at the V_{OL} and V_{OH} test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at a minimum V_{CCO} with the respective V_{OL} and V_{OH} voltage levels shown. Other standards are sample tested.

Table 8: **SelectIO DC Input and Output Levels for the I/O Banks(1)(2)(3)**

I/O Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
HSTL_I	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	5.8	–5.8
HSTL_I_12	–0.300	V_{REF} – 0.080	V_{REF} + 0.080	V_{CCO} + 0.300	25% V_{CCO}	75% V_{CCO}	4.1	–4.1
HSTL_I_18	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	6.2	–6.2
HSUL_12	–0.300	V_{REF} – 0.130	V_{REF} + 0.130	V_{CCO} + 0.300	20% V_{CCO}	80% V_{CCO}	0.1	–0.1
LVCMOS12	–0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	Note 4	Note 4
LVCMOS15	–0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	0.450	V_{CCO} – 0.450	Note 5	Note 5
LVCMOS18	–0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	0.450	V_{CCO} – 0.450	Note 5	Note 5
LVDCI_15	–0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	0.450	V_{CCO} – 0.450	7.0	–7.0
LVDCI_18	–0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	0.450	V_{CCO} – 0.450	7.0	–7.0
SSTL12	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	V_{CCO}/2 – 0.150	V_{CCO}/2 + 0.150	8.0	–8.0
SSTL135	–0.300	V_{REF} – 0.090	V_{REF} + 0.090	V_{CCO} + 0.300	V_{CCO}/2 – 0.150	V_{CCO}/2 + 0.150	9.0	–9.0
SSTL15	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	V_{CCO}/2 – 0.175	V_{CCO}/2 + 0.175	10.0	–10.0
SSTL18_I	–0.300	V_{REF} – 0.125	V_{REF} + 0.125	V_{CCO} + 0.300	V_{CCO}/2 – 0.470	V_{CCO}/2 + 0.470	7.0	–7.0
MIPI_DPHY_DCI_LP(6)	–0.300	0.550	0.880	V_{CCO} + 0.300	0.050	1.100	0.01	–0.01

Notes:

1. Tested according to relevant specifications.
2. Standards specified using the default I/O standard configuration. For details, see the *UltraScale Architecture SelectIO Resources User Guide* (UG571).
3. POD10 and POD12 DC input and output levels are shown in Table 9, Table 13, and Table 14.
4. Supported drive strengths of 2, 4, 6, or 8 mA in the I/O banks.
5. Supported drive strengths of 2, 4, 6, 8, or 12 mA in the I/O banks.
6. Low-power option for MIPI_DPHY_DCI.

Table 9: **DC Input Levels for Single-ended POD10 and POD12 I/O Standards(1)(2)**

I/O Standard	V_{IL}		V_{IH}	
	V, Min	V, Max	V, Min	V, Max
POD10	–0.300	V_{REF} – 0.068	V_{REF} + 0.068	V_{CCO} + 0.300
POD12	–0.300	V_{REF} – 0.068	V_{REF} + 0.068	V_{CCO} + 0.300

Notes:

1. Tested according to relevant specifications.
2. Standards specified using the default I/O standard configuration. For details, see the *UltraScale Architecture SelectIO Resources User Guide* (UG571).

Speed Grade Designations

Since individual family members are produced at different times, the migration from one category to another depends completely on the status of the fabrication process for each device. Table 16 correlates the current status of the Virtex UltraScale+ FPGA on a per speed grade basis.

Table 17: **Speed Grade Designations by Device**

Device	Speed Grade, Temperature Ranges, and V_{CCINT} Operating Voltages		
	Advance	**Preliminary**	**Production**
XCVU3P	-3E (V_{CCINT} = 0.90V) -2LE (V_{CCINT} = 0.85V) -2LE (V_{CCINT} = 0.72V)(1)		-2I (V_{CCINT} = 0.85V) -1E (V_{CCINT} = 0.85V) -1I (V_{CCINT} = 0.85V)
XCVU5P	-3E (V_{CCINT} = 0.90V) -2I (V_{CCINT} = 0.85V), -2LE (V_{CCINT} = 0.85V) -1E (V_{CCINT} = 0.85V), -1I (V_{CCINT} = 0.85V) -2LE (V_{CCINT} = 0.72V)(1)		
XCVU7P	-3E (V_{CCINT} = 0.90V) -2I (V_{CCINT} = 0.85V), -2LE (V_{CCINT} = 0.85V) -1E (V_{CCINT} = 0.85V), -1I (V_{CCINT} = 0.85V) -2LE (V_{CCINT} = 0.72V)(1)		
XCVU9P	-3E (V_{CCINT} = 0.90V) -2I (V_{CCINT} = 0.85V), -2LE (V_{CCINT} = 0.85V) -1E (V_{CCINT} = 0.85V), -1I (V_{CCINT} = 0.85V) -2LE (V_{CCINT} = 0.72V)(1)		
XCVU11P	-3E (V_{CCINT} = 0.90V) -2I (V_{CCINT} = 0.85V), -2LE (V_{CCINT} = 0.85V) -1E (V_{CCINT} = 0.85V), -1I (V_{CCINT} = 0.85V), -2LE (V_{CCINT} = 0.72V)(1)		
XCVU13P	-3E (V_{CCINT} = 0.90V) -2I (V_{CCINT} = 0.85V), -2LE (V_{CCINT} = 0.85V) -1E (V_{CCINT} = 0.85V), -1I (V_{CCINT} = 0.85V) -2LE (V_{CCINT} = 0.72V)(1)		

Notes:

1. The lowest power -2L devices, where V_{CCINT} = 0.72V, are listed in the Vivado Design Suite as -2LV.

Production Silicon and Software Status

In some cases, a particular family member (and speed grade) is released to production before a speed specification is released with the correct label (Advance, Preliminary, Production). Any labeling discrepancies are corrected in subsequent speed specification releases.

Table 18 lists the production released Virtex UltraScale+ FPGA, speed grade, and the minimum corresponding supported speed specification version and Vivado software revisions. The Vivado software and speed specifications listed are the minimum releases required for production. All subsequent releases of software and speed specifications are valid.

Table 18: **Virtex UltraScale+ FPGA Device Production Software and Speed Specification Release**

Device	Speed Grade and V_{CCINT} Operating Voltages				
	0.90V	0.85V			0.72V
	-3	-2	-1	-2L	-2L
XCVU3P		Vivado tools 2017.1 v1.10			
XCVU5P					
XCVU7P					
XCVU9P					
XCVU11P					
XCVU13P					

Notes:

1. Blank entries indicate a device and/or speed grade in Advance or Preliminary status.

FPGA Logic Performance Characteristics

This section provides the performance characteristics of some common functions and designs implemented in Virtex UltraScale+ FPGAs. These values are subject to the same guidelines as the AC Switching Characteristics, page 13.

Table 19: **LVDS Component Mode Performance**

Description	Speed Grade and V_{CCINT} Operating Voltages								Units
	0.90V		0.85V				0.72V		
	-3		-2		-1		-2		
	Min	Max	Min	Max	Min	Max	Min	Max	
LVDS TX DDR (OSERDES 4:1, 8:1)	0	1250	0	1250	0	1250	0	1250	Mb/s
LVDS TX SDR (OSERDES 2:1, 4:1)	0	625	0	625	0	625	0	625	Mb/s
LVDS RX DDR (ISERDES 1:4, 1:8)(1)	0	1250	0	1250	0	1250	0	1250	Mb/s
LVDS RX SDR (ISERDES 1:2, 1:4)(1)	0	625	0	625	0	625	0	625	Mb/s

Notes:

1. LVDS receivers are typically bounded with certain applications to achieve maximum performance. Package skews are not included and should be removed through PCB routing.

Table 20: **LVDS Native Mode Performance(1)(2)**

Description	DATA_WIDTH	Speed Grade and V_{CCINT} Operating Voltages								Units
		0.90V		0.85V				0.72V		
		-3		-2		-1		-2		
		Min	Max	Min	Max	Min	Max	Min	Max	
LVDS TX DDR (TX_BITSLICE)	4	375	1600	375	1600	375	1260	375	1400	Mb/s
	8	375	1600	375	1600	375	1260	375	1600	Mb/s
LVDS TX SDR (TX_BITSLICE)	4	187.5	800	187.5	800	187.5	630	187.5	700	Mb/s
	8	187.5	800	187.5	800	187.5	630	187.5	800	Mb/s
LVDS RX DDR (RX_BITSLICE)(3)	4	375	1600	375	1600	375	1260	375	1400	Mb/s
	8	375	1600	375	1600	375	1260	375	1600	Mb/s
LVDS RX SDR (RX_BITSLICE)(3)	4	187.5	800	187.5	800	187.5	630	187.5	700	Mb/s
	8	187.5	800	187.5	800	187.5	630	187.5	800	Mb/s

Notes:

1. Native mode is supported through the High-Speed SelectIO Interface Wizard available with the Vivado Design Suite.
2. PLL settings can restrict the minimum allowable data rate. For example, when using the PLL with CLKOUTPHY_MODE = VCO_HALF the minimum frequency is PLL_FVCOMIN/2.
3. LVDS receivers are typically bounded with certain applications to achieve maximum performance. Package skews are not included and should be removed through PCB routing.

Table 21: **MIPI D-PHY Performance**

Description	Speed Grade and V_{CCINT} Operating Voltages				Units
	0.90V	0.85V		0.72V	
	-3	-2	-1	-2	
MIPI D-PHY transmitter or receiver.	1500	1500	1260	1260	Mb/s

Table 24: **IOB High Performance (HP) Switching Characteristics *(Cont'd)***

I/O Standards	$T_{INBUF\_DELAY\_PAD\_I}$				$T_{OUTBUF\_DELAY\_O\_PAD}$				$T_{OUTBUF\_DELAY\_TD\_PAD}$				Units
	0.90V	0.85V		0.72V	0.90V	0.85V		0.72V	0.90V	0.85V		0.72V	
	-3	-2	-1	-2	-3	-2	-1	-2	-3	-2	-1	-2	
POD12_DCI_F	0.409	0.409	0.431	0.409	0.425	0.425	0.443	0.425	0.558	0.558	0.586	0.558	ns
POD12_DCI_M	0.409	0.409	0.431	0.409	0.543	0.543	0.572	0.543	0.638	0.638	0.678	0.638	ns
POD12_DCI_S	0.409	0.409	0.431	0.409	0.772	0.772	0.822	0.772	0.862	0.862	0.929	0.862	ns
POD12_F	0.409	0.409	0.431	0.409	0.455	0.455	0.476	0.455	0.595	0.595	0.626	0.595	ns
POD12_M	0.409	0.409	0.431	0.409	0.551	0.551	0.582	0.551	0.641	0.641	0.679	0.641	ns
POD12_S	0.409	0.409	0.431	0.409	0.767	0.767	0.817	0.767	0.832	0.832	0.889	0.832	ns
SLVS_400_18	0.539	0.539	0.620	0.539	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	ns
SSTL12_DCI_F	0.381	0.381	0.399	0.381	0.425	0.425	0.443	0.425	0.558	0.558	0.586	0.558	ns
SSTL12_DCI_M	0.381	0.381	0.399	0.381	0.557	0.557	0.587	0.557	0.654	0.654	0.694	0.654	ns
SSTL12_DCI_S	0.381	0.381	0.399	0.381	0.754	0.754	0.803	0.754	0.842	0.842	0.908	0.842	ns
SSTL12_F	0.403	0.403	0.403	0.403	0.412	0.412	0.430	0.412	0.538	0.538	0.566	0.538	ns
SSTL12_M	0.403	0.403	0.403	0.403	0.553	0.553	0.584	0.553	0.641	0.641	0.676	0.641	ns
SSTL12_S	0.403	0.403	0.403	0.403	0.758	0.758	0.808	0.758	0.823	0.823	0.879	0.823	ns
SSTL135_DCI_F	0.366	0.366	0.399	0.366	0.411	0.411	0.428	0.411	0.537	0.537	0.565	0.537	ns
SSTL135_DCI_M	0.366	0.366	0.399	0.366	0.551	0.551	0.582	0.551	0.645	0.645	0.685	0.645	ns
SSTL135_DCI_S	0.366	0.366	0.399	0.366	0.746	0.746	0.799	0.746	0.829	0.829	0.893	0.829	ns
SSTL135_F	0.378	0.378	0.399	0.378	0.408	0.408	0.428	0.408	0.528	0.528	0.561	0.528	ns
SSTL135_M	0.378	0.378	0.399	0.378	0.555	0.555	0.585	0.555	0.641	0.641	0.679	0.641	ns
SSTL135_S	0.378	0.378	0.399	0.378	0.772	0.772	0.823	0.772	0.827	0.827	0.878	0.827	ns
SSTL15_DCI_F	0.402	0.402	0.417	0.402	0.412	0.412	0.429	0.412	0.531	0.531	0.563	0.531	ns
SSTL15_DCI_M	0.402	0.402	0.417	0.402	0.553	0.553	0.583	0.553	0.645	0.645	0.685	0.645	ns
SSTL15_DCI_S	0.402	0.402	0.417	0.402	0.768	0.768	0.822	0.768	0.847	0.847	0.912	0.847	ns
SSTL15_F	0.371	0.371	0.400	0.371	0.408	0.408	0.428	0.408	0.530	0.530	0.556	0.530	ns
SSTL15_M	0.371	0.371	0.400	0.371	0.554	0.554	0.585	0.554	0.639	0.639	0.677	0.639	ns
SSTL15_S	0.371	0.371	0.400	0.371	0.767	0.767	0.817	0.767	0.813	0.813	0.867	0.813	ns
SSTL18_I_DCI_F	0.329	0.329	0.336	0.329	0.445	0.445	0.461	0.445	0.566	0.566	0.595	0.566	ns
SSTL18_I_DCI_M	0.329	0.329	0.336	0.329	0.554	0.554	0.585	0.554	0.644	0.644	0.683	0.644	ns
SSTL18_I_DCI_S	0.329	0.329	0.336	0.329	0.762	0.762	0.818	0.762	0.837	0.837	0.899	0.837	ns
SSTL18_I_F	0.316	0.316	0.337	0.316	0.454	0.454	0.476	0.454	0.578	0.578	0.608	0.578	ns
SSTL18_I_M	0.316	0.316	0.337	0.316	0.571	0.571	0.603	0.571	0.652	0.652	0.692	0.652	ns
SSTL18_I_S	0.316	0.316	0.337	0.316	0.782	0.782	0.835	0.782	0.816	0.816	0.870	0.816	ns
SUB_LVDS	0.539	0.539	0.620	0.539	0.660	0.660	0.692	0.660	969.863	969.863	969.863	969.863	ns

Output Delay Measurement Methodology

Output delays are measured with short output traces. Standard termination was used for all testing. The propagation delay of the trace is characterized separately and subtracted from the final measurement, and is therefore not included in the generalized test setups shown in Figure 1 and Figure 2.

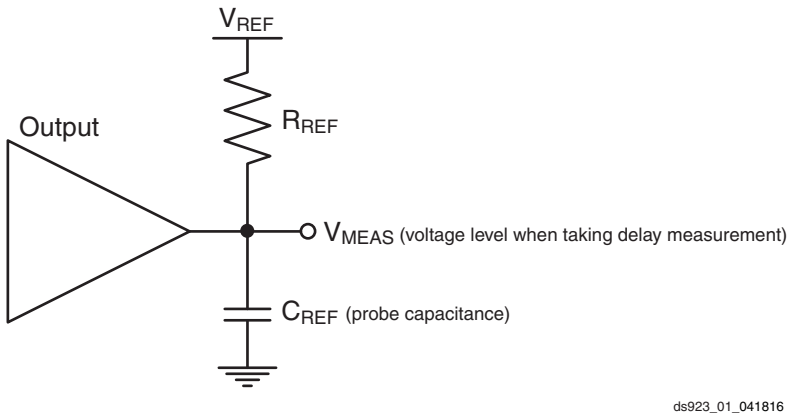

Figure 1: **Single-Ended Test Setup**

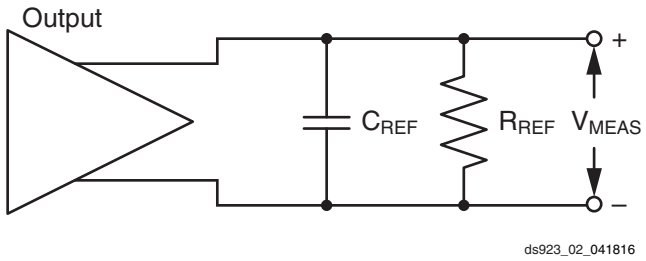

Figure 2: **Differential Test Setup**

Parameters V_{REF}, R_{REF}, C_{REF}, and V_{MEAS} fully describe the test conditions for each I/O standard. The most accurate prediction of propagation delay in any given application can be obtained through IBIS simulation, using this method:

1. Simulate the output driver of choice into the generalized test setup using values from Table 27.
2. Record the time to V_{MEAS}.
3. Simulate the output driver of choice into the actual PCB trace and load using the appropriate IBIS model or capacitance value to represent the load.
4. Record the time to V_{MEAS}.
5. Compare the results of step 2 and step 4. The increase or decrease in delay yields the actual propagation delay of the PCB trace.

Input/Output Delay Switching Characteristics

Table 30: **Input/Output Delay Switching Characteristics**

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages				Units
		0.90V	0.85V		0.72V	
		-3	-2	-1	-2	
F_{REFCLK}	REFCLK frequency for IDELAYCTRL (component mode).	300 to 800				MHz
	REFCLK frequency for BITSLICE_CONTROL (native mode).(1)	300 to 2666.67	300 to 2666.67	300 to 2400	300 to 2400	MHz
T_{MINPER_CLK}	Minimum period for IODELAY clock.	3.195	3.195	3.195	3.195	ns
T_{MINPER_RST}	Minimum reset pulse width.	52.00				ns
$T_{IDELAY\_RESOLUTION}$/ $T_{ODELAY\_RESOLUTION}$	IDELAY/ODELAY chain resolution.	2.1 to 12				ps

Notes:

1. PLL settings could restrict the minimum allowable data rate. For example, when using a PLL with CLKOUTPHY_MODE = VCO_HALF, the minimum frequency is PLL_FVCOMIN/2.

DSP48 Slice Switching Characteristics

Table 31: **DSP48 Slice Switching Characteristics**

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages				Units
		0.90V	0.85V		0.72V	
		-3	-2	-1	-2	
Maximum Frequency						
F_{MAX}	With all registers used.	891	775	645	644	MHz
F_{MAX_PATDET}	With pattern detector.	794	687	571	562	MHz
$F_{MAX\_MULT\_NOMREG}$	Two register multiply without MREG.	635	544	456	440	MHz
$F_{MAX\_MULT\_NOMREG\_PATDET}$	Two register multiply without MREG with pattern detect.	577	492	410	395	MHz
$F_{MAX\_PREADD\_NOADREG}$	Without ADREG.	655	565	468	453	MHz
$F_{MAX\_NOPIPELINEREG}$	Without pipeline registers (MREG, ADREG).	483	410	338	323	MHz
$F_{MAX\_NOPIPELINEREG\_PATDET}$	Without pipeline registers (MREG, ADREG) with pattern detect.	448	379	314	299	MHz

Table 37: **Global Clock Input to Output Delay With MMCM**

Symbol	Description	Device	Speed Grade and V_{CCINT} Operating Voltages				Units
			0.90V	0.85V		0.72V	
			-3	-2	-1	-2	
SSTL15 Global Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, with MMCM.							
$T_{ICKOFMMCMCC}$	Global clock input and output flip-flop *with* MMCM.	XCVU3P	1.80	1.80	1.94	2.34	ns
		XCVU5P	1.80	1.80	1.94	2.34	ns
		XCVU7P	1.80	1.80	1.94	2.34	ns
		XCVU9P	1.80	1.80	1.94	2.34	ns
		XCVU11P	1.56	1.56	1.68	2.07	ns
		XCVU13P	1.56	1.56	1.68	2.07	ns

Notes:

1. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible I/O and CLB flip-flops are clocked by the global clock net in a single SLR.
2. MMCM output jitter is already included in the timing calculation.

GTY Transceiver Specifications

The *UltraScale Architecture and Product Overview* (DS890) lists the Virtex UltraScale+ FPGAs that include the GTY transceivers.

GTY Transceiver DC Input and Output Levels

Table 41 summarizes the DC specifications of the GTY transceivers in Virtex UltraScale+ FPGAs. Consult the *UltraScale Architecture GTY Transceiver User Guide* (UG578) for further information.

Table 41: **GTY Transceiver DC Specifications**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
DV_{PPIN}	Differential peak-to-peak input voltage (external AC coupled)	>10.3125 Gb/s	150	–	1250	mV
		6.6 Gb/s to 10.3125 Gb/s	150	–	1250	mV
		≤ 6.6 Gb/s	150	–	2000	mV
V_{IN}	Single-ended input voltage. Voltage measured at the pin referenced to GND.	DC coupled $V_{MGTAVTT}$ = 1.2V	–400	–	$V_{MGTAVTT}$	mV
V_{CMIN}	Common mode input voltage	DC coupled $V_{MGTAVTT}$ = 1.2V	–	2/3 $V_{MGTAVTT}$	–	mV
D_{VPPOUT}	Differential peak-to-peak output voltage(1)	Transmitter output swing is set to 1010	800	–	–	mV
$V_{CMOUTDC}$	Common mode output voltage: DC coupled (equation based)	When remote RX is terminated to GND	$V_{MGTAVTT}/2 - D_{VPPOUT}/4$			mV
		When remote RX termination is floating	$V_{MGTAVTT} - D_{VPPOUT}/2$			mV
		When remote RX is terminated to V_{RX_TERM}(2)	$V_{MGTAVTT} - \frac{D_{VPPOUT}}{4} - \left(\frac{V_{MGTAVTT} - V_{RX\_TERM}}{2}\right)$			mV
$V_{CMOUTAC}$	Common mode output voltage: AC coupled	Equation based	$V_{MGTAVTT} - D_{VPPOUT}/2$			mV
R_{IN}	Differential input resistance		–	100	–	Ω
R_{OUT}	Differential output resistance		–	100	–	Ω
T_{OSKEW}	Transmitter output pair (TXP and TXN) intra-pair skew		–	–	10	ps
C_{EXT}	Recommended external AC coupling capacitor(3)		–	100	–	nF

Notes:

1. The output swing and pre-emphasis levels are programmable using the GTY transceiver attributes discussed in the *UltraScale Architecture GTY Transceiver User Guide* (UG578) and can result in values lower than reported in this table.
2. V_{RX_TERM} is the remote RX termination voltage.
3. Other values can be used as appropriate to conform to specific protocols and standards.

Table 45: **GTY Transceiver Dynamic Reconfiguration Port (DRP) Switching Characteristics**

Symbol	Description	All Speed Grades	Units
$F_{GTYDRPCLK}$	GTYDRPCLK maximum frequency.	250	MHz

Table 46: **GTY Transceiver Reference Clock Switching Characteristics**

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
F_{GCLK}	Reference clock frequency range.		60	–	820	MHz
T_{RCLK}	Reference clock rise time.	20% – 80%	–	200	–	ps
T_{FCLK}	Reference clock fall time.	80% – 20%	–	200	–	ps
T_{DCREF}	Reference clock duty cycle.	Transceiver PLL only	40	50	60	%

Table 47: **GTY Transceiver Reference Clock Oscillator Selection Phase Noise Mask(1)**

Symbol	Description	Offset Frequency	Min	Typ	Max	Units
$QPLL_{REFCLKMASK}$	QPLL0/QPLL1 reference clock select phase noise mask at REFCLK frequency = 156.25 MHz.	10 kHz	–	–	–112	dBc/Hz
		100 kHz	–	–	–128	
		1 MHz	–	–	–145	
	QPLL0/QPLL1 reference clock select phase noise mask at REFCLK frequency = 312.5 MHz.	10 kHz	–	–	–103	dBc/Hz
		100 kHz	–	–	–123	
		1 MHz	–	–	–143	
	QPLL0/QPLL1 reference clock select phase noise mask at REFCLK frequency =625 MHz.	10 kHz	–	–	–98	dBc/Hz
		100 kHz	–	–	–117	
		1 MHz	–	–	–140	
$CPLL_{REFCLKMASK}$	CPLL reference clock select phase noise mask at REFCLK frequency = 156.25 MHz.	10 kHz	–	–	–112	dBc/Hz
		100 kHz	–	–	–128	
		1 MHz	–	–	–145	
		50 MHz	–	–	–145	
	CPLL reference clock select phase noise mask at REFCLK frequency = 312.5 MHz.	10 kHz	–	–	–103	dBc/Hz
		100 kHz	–	–	–123	
		1 MHz	–	–	–143	
		50 MHz	–	–	–145	
	CPLL reference clock select phase noise mask at REFCLK frequency = 625 MHz.	10 kHz	–	–	–98	dBc/Hz
		100 kHz	–	–	–117	
		1 MHz	–	–	–140	
		50 MHz	–	–	–144	

Notes:

1. For reference clock frequencies not in this table, use the phase-noise mask for the nearest reference clock frequency.

Table 50: **GTY Transceiver Transmitter Switching Characteristics *(Cont'd)***

Symbol	Description	Condition	Min	Typ	Max	Units
$T_{J3.20}$	Total jitter(3)(4)	3.20 Gb/s(5)	–	–	0.20	UI
$D_{J3.20}$	Deterministic jitter(3)(4)		–	–	0.10	UI
$T_{J2.5}$	Total jitter(3)(4)	2.5 Gb/s(6)	–	–	0.20	UI
$D_{J2.5}$	Deterministic jitter(3)(4)		–	–	0.10	UI
$T_{J1.25}$	Total jitter(3)(4)	1.25 Gb/s(7)	–	–	0.15	UI
$D_{J1.25}$	Deterministic jitter(3)(4)		–	–	0.06	UI
T_{J500}	Total jitter(3)(4)	500 Mb/s(8)	–	–	0.10	UI
D_{J500}	Deterministic jitter(3)(4)		–	–	0.03	UI

Notes:

1. Using same REFCLK input with TX phase alignment enabled for up to four consecutive transmitters (one fully populated GTY Quad) at maximum line rate.
2. Using QPLL_FBDIV = 40, 20-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
3. Using CPLL_FBDIV = 2, 20-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
4. All jitter values are based on a bit-error ratio of 10^{-12}.
5. CPLL frequency at 3.2 GHz and TXOUT_DIV = 2.
6. CPLL frequency at 2.5 GHz and TXOUT_DIV = 2.
7. CPLL frequency at 2.5 GHz and TXOUT_DIV = 4.
8. CPLL frequency at 2.0 GHz and TXOUT_DIV = 8.

GTY Transceiver Electrical Compliance

The *UltraScale Architecture GTY Transceiver User Guide* (UG578) contains recommended use modes that ensure compliance for the protocols listed in Table 52. The transceiver wizard provides the recommended settings for those use cases and for protocol specific characteristics.

Table 52: **GTY Transceiver Protocol List**

Protocol	Specification	Serial Rate (Gb/s)	Electrical Compliance
CAUI-4	IEEE 802.3-2012	25.78125	Compliant
28 Gb/s backplane	CEI-25G-LR	25–28.05	Compliant
Interlaken	OIF-CEI-6G, OIF-CEI-11GSR, OIF-CEI-28G-MR	4.25–25.78125	Compliant
100GBASE-KR4	IEEE 802.3bj-2014, CEI-25G-LR	25.78125	Compliant(1)
100GBASE-CR4	IEEE 802.3bj-2014, CEI-25G-LR	25.78125	Compliant(1)
50GBASE-KR4	IEEE 802.3by-2014, CEI-25G-LR	25.78125	Compliant(1)
50GBASE-CR4	IEEE 802.3by-2014, CEI-25G-LR	25.78125	Compliant(1)
25GBASE-KR4	IEEE 802.3by-2014, CEI-25G-LR	25.78125	Compliant(1)
25GBASE-CR4	IEEE 802.3by-2014, CEI-25G-LR	25.78125	Compliant(1)
OTU4 (OTL4.4) CFP2	OIF-CEI-28G-VSR	27.952493-32.75	Compliant
OTU4 (OTL4.4) CFP	OIF-CEI-11G-MR	11.18–13.1	Compliant
CAUI-10	IEEE 802.3-2012	10.3125	Compliant
nPPI	IEEE 802.3-2012	10.3125	Compliant
10GBASE-KR(2)	IEEE 802.3-2012	10.3125	Compliant
SFP+	SFF-8431 (SR and LR)	9.95328–11.10	Compliant
XFP	INF-8077i, revision 4.5	10.3125	Compliant
RXAUI	CEI-6G-SR	6.25	Compliant
XAUI	IEEE 802.3-2012	3.125	Compliant
1000BASE-X	IEEE 802.3-2012	1.25	Compliant
5.0G Ethernet	IEEE 802.3bx (PAR)	5	Compliant
2.5G Ethernet	IEEE 802.3bx (PAR)	2.5	Compliant
HiGig, HiGig+, HiGig2	IEEE 802.3-2012	3.74, 6.6	Compliant
QSGMII	QSGMII v1.2 (Cisco System, ENG-46158)	5	Compliant
OTU2	ITU G.8251	10.709225	Compliant
OTU4 (OTL4.10)	OIF-CEI-11G-SR	11.180997	Compliant
OC-3/12/48/192	GR-253-CORE	0.1555–9.956	Compliant
PCIe Gen1, 2, 3	PCI Express base 3.0	2.5, 5.0, and 8.0	Compliant
SDI(3)	SMPTE 424M-2006	0.27–2.97	Compliant
UHD-SDI(3)	SMPTE ST-2081 6G, SMPTE ST-2082 12G	6 and 12	Compliant
Hybrid memory cube (HMC)	HMC-15G-SR	10, 12.5, and 15.0	Compliant
MoSys bandwidth engine	CEI-11-SR and CEI-11-SR (overclocked)	10.3125, 15.5	Compliant
CPRI	CPRI_v_6_1_2014-07-01	0.6144–12.165	Compliant
Passive optical network (PON)	10G-EPON, 1G-EPON, NG-PON2, XG-PON, and 2.5G-PON	0.155–10.3125	Compliant
JESD204a/b	OIF-CEI-6G, OIF-CEI-11G	3.125–12.5	Compliant

Integrated Interface Block for Interlaken

More information and documentation on solutions using the integrated interface block for Interlaken can be found at UltraScale Interlaken. The *UltraScale Architecture and Product Overview* (DS890) lists how many blocks are in each Virtex UltraScale+ FPGA. This section describes the following Interlaken configurations.

- 12 x 12.5 Gb/s protocol and lane logic mode (Table 53).
- 6 x 25.78125 Gb/s and 6 x 28.21 Gb/s protocol and lane logic mode (Table 54).
- 12 x 25.78125 Gb/s lane logic only mode (Table 55).

XCVU11P devices in the FLVF1924 package are only supported using the 12 x 12.5 Gb/s Interlaken configuration. See Table 44 for the F_{GTYMAX} description.

Table 53: **Maximum Performance for Interlaken 12 x 12.5 Gb/s Protocol and Lane Logic Mode Designs**

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages										Units
		0.90V		0.85V				0.72V				
		-3		-2		-1		-2		-1		
$F_{RX\_SERDES\_CLK}$	Receive serializer/ deserializer clock	195.32		195.32		195.32		195.32		195.32		MHz
$F_{TX\_SERDES\_CLK}$	Transmit serializer/ deserializer clock	195.32		195.32		195.32		195.32		195.32		MHz
F_{DRP_CLK}	Dynamic reconfiguration port clock	250.00		250.00		250.00		250.00		250.00		MHz
		Min(1)	Max	Min(1)	Max	Min(1)	Max	Min(1)	Max	Min(1)	Max	
F_{CORE_CLK}	Interlaken core clock	300.00	322.27	300.00	322.27	300.00	322.27	300.00	322.27	300.00	322.27	MHz
F_{LBUS_CLK}	Interlaken local bus clock	300.00	322.27	300.00	322.27	300.00	322.27	300.00	322.27	300.00	322.27	MHz

Notes:

1. These are the minimum clock frequencies at the maximum lane performance.

Table 54: **Maximum Performance for Interlaken 6 x 25.78125 Gb/s and 6 x 28.21 Gb/s Protocol and Lane Logic Mode Designs**

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages										Units
		0.90V		0.85V				0.72V				
		-3(1)		-2(1)		-1		-2		-1		
$F_{RX\_SERDES\_CLK}$	Receive serializer/ deserializer clock	440.79		440.79		N/A		402.84		N/A		MHz
$F_{TX\_SERDES\_CLK}$	Transmit serializer/ deserializer clock	440.79		440.79		N/A		402.84		N/A		MHz
F_{DRP_CLK}	Dynamic reconfiguration port clock	250.00		250.00		N/A		250.00		N/A		MHz
		Min(2)	Max	Min(2)	Max	Min	Max	Min(2)	Max	Min	Max	
F_{CORE_CLK}	Interlaken core clock	412.50(3)	479.20	412.50(3)	479.20	N/A		412.50	429.69	N/A		MHz
F_{LBUS_CLK}	Interlaken local bus clock	300.00(4)	349.52	300.00(4)	349.52	N/A		300.00	349.52	N/A		MHz

Notes:

1. 6 x 28.21 mode is only supported in the -2 (V_{CCINT}=0.85V) and -3 (V_{CCINT}=0.90V) speed grades.
2. These are the minimum clock frequencies at the maximum lane performance.
3. The minimum value for CORE_CLK is 451.36 MHz for the 6 x 28.21 Gb/s protocol.
4. The minimum value for LBUS_CLK is 330.00 MHz for the 6 x 28.21 Gb/s protocol.

Table 55: **Maximum Performance for Interlaken 12 x 25.78125 Gb/s Lane Logic Only Mode Designs**

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages					Units
		0.90V	0.85V		0.72V		
		-3	-2	-1	-2	-1	
$F_{RX\_SERDES\_CLK}$	Receive serializer/ deserializer clock	402.84	402.84	N/A	N/A	N/A	MHz
$F_{TX\_SERDES\_CLK}$	Transmit serializer/ deserializer clock	402.84	402.84	N/A	N/A	N/A	MHz
F_{DRP_CLK}	Dynamic reconfiguration port clock	250.00	250.00	N/A	N/A	N/A	MHz
F_{CORE_CLK}	Interlaken core clock	412.50	412.50	N/A	N/A	N/A	MHz
F_{LBUS_CLK}	Interlaken local bus clock	349.52	349.52	N/A	N/A	N/A	MHz

Integrated Interface Block for 100G Ethernet MAC and PCS

More information and documentation on solutions using the integrated 100 Gb/s Ethernet block can be found at UltraScale Integrated 100G Ethernet MAC/PCS. The *UltraScale Architecture and Product Overview* (DS890) lists how many blocks are in each Virtex UltraScale+ FPGA.

Table 56: **Maximum Performance for 100G Ethernet Designs**

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages				Units
		0.90V	0.85V		0.72V	
		-3	-2(1)	-1	-2	
F_{TX_CLK}	Transmit clock	390.625	390.625	322.223	322.223	MHz
F_{RX_CLK}	Receive clock	390.625	390.625	322.223	322.223	MHz
$F_{RX\_SERDES\_CLK}$	Receive serializer/deserializer clock	390.625	390.625	322.223	322.223	MHz
F_{DRP_CLK}	Dynamic reconfiguration port clock	250.00	250.00	250.00	250.00	MHz

Notes:

1. The maximum clock frequency of 390.625 MHz only applies to the CAUI-10 interface. The maximum clock frequency for the CAUI-4 interface is 322.223 MHz.

Integrated Interface Block for PCI Express Designs

More information and documentation on solutions for PCI Express designs can be found at PCI Express. The *UltraScale Architecture and Product Overview* (DS890) lists how many blocks are in each Virtex UltraScale+ FPGA.

Table 57: **Maximum Performance for PCI Express Designs(1)(2)**

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages				Units
		0.90V	0.85V		0.72V	
		-3	-2	-1	-2	
$F_{PIPECLK}$	Pipe clock maximum frequency.	250.00	250.00	250.00	250.00	MHz
$F_{CORECLK}$	Core clock maximum frequency.	500.00	500.00	500.00	250.00	MHz
F_{DRPCLK}	DRP clock maximum frequency.	250.00	250.00	250.00	250.00	MHz
$F_{MCAPCLK}$	MCAP clock maximum frequency.	125.00	125.00	125.00	125.00	MHz

Notes:

1. PCI Express Gen4 operation is supported for x1, x2, x4, and x8 widths.
2. PCI Express Gen4 operation is supported in -3E, -2E, and -2I speed grades.

Table 61: **Configuration Switching Characteristics *(Cont'd)***

Symbol	Description	Speed Grade and V_{CCINT} Operating Voltages				Units
		0.90V	0.85V		0.72V	
		-3	-2	-1	-2	
DNA Port Switching						
F_{DNACK}	DNA port frequency.	200	200	200	175	MHz, Max
STARTUPE3 Ports						
$T_{USRCCLKO}$	STARTUPE3 USRCCLKO input port to CCLK pin output delay.	0.25/ 6.00	0.25/ 6.50	0.25/ 7.50	0.25/ 9.00	ns, Min/Max
T_{DO}	DO[3:0] ports to D03-D00 pins output delay.	0.25/ 6.70	0.25/ 7.70	0.25/ 8.40	0.25/ 10.00	ns, Min/Max
T_{DTS}	DTS[3:0] ports to D03-D00 pins 3-state delays.	0.25/ 6.70	0.25/ 7.70	0.25/ 8.40	0.25/ 10.00	ns, Min/Max
T_{FCSBO}	FCSBO port to FCS_B pin output delay.	0.25/ 6.90	0.25/ 7.50	0.25/ 8.40	0.25/ 9.80	ns, Min/Max
T_{FCSBTS}	FCSBTS port to FCS_B pin 3-state delay.	0.25/ 6.90	0.25/ 7.50	0.25/ 8.40	0.25/ 9.80	ns, Min/Max
$T_{USRDONEO}$	USRDONEO port to DONE pin output delay.	0.25/ 8.60	0.25/ 9.40	0.25/ 10.50	0.25/ 12.10	ns, Min/Max
$T_{USRDONETS}$	USRDONETS port to DONE pin 3-state delay.	0.25/ 8.60	0.25/ 9.40	0.25/ 10.50	0.25/ 12.10	ns, Min/Max
T_{DI}	D03-D00 pins to DI[3:0] ports input delay.	0.5/ 2.6	0.5/ 3.1	0.5/ 3.5	0.5/ 4.0	ns, Min/Max
$F_{CFGMCLK}$	STARTUPE3 CFGMCLK output frequency.	50	50	50	50	MHz, Typ
$F_{CFGMCLKTOL}$	STARTUPE3 CFGMCLK output frequency tolerance.	±15	±15	±15	±15	%, Max
T_{DCI_MATCH}	Specifies a stall in the startup cycle until the digitally controlled impedance (DCI) match signals are asserted.	4	4	4	4	ms, Max

Notes:

1. When the CCLK is sourced from the EMCCLK pin with a divide-by-one setting, the external EMCCLK must meet this duty-cycle requirement.

Revision History

The following table shows the revision history for this document.

Date	Version	Description of Revisions
04/19/2017	1.1	Updated the Summary description. In Table 1, updated Note 6, added data, and added Note 7, Note 8, and Note 9. Updated and added data to Table 2 though Table 6. Removed the -1LI speed grade. Updated Table 16, Table 17, and Table 18 to production release in Vivado Design Suite 2017.1 for the XCVU3P: -2E, -2I, -1E, -1I. Updated Table 15. Added Note 1 to Table 17. Updated Table 19, Table 20, Table 24, Table 25, Table 26, Table 28, Table 29, and Table 30. Added Table 21. Added MMCM_F_{DPRCLK_MAX} to Table 33 and PLL_F_{DPRCLK_MAX} to Table 34. Updated to Vivado Design Suite 2017.1 Table 35, Table 36, Table 37, and Table 38. Added data to Table 39 and Table 40. Updated the GTY Transceiver Specifications section. Revised the Integrated Interface Block for Interlaken section. Updated the System Monitor Specifications section adding notes to the tables. Updated the Configuration Switching Characteristics section. Removed the *eFUSE Programming Conditions* table and added the specifications to Table 2 and Table 3. Updated the Automotive Applications Disclaimer.
04/20/2016	1.0	Initial Xilinx release.

Notice of Disclaimer

Automotive Applications Disclaimer