Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	56800E
Core Size	16-Bit
Speed	120MHz
Connectivity	EBI/EMI, SCI, SPI, SSI
Peripherals	DMA, POR, WDT
Number of I/O	47
Program Memory Size	80KB (40K x 16)
Program Memory Type	SRAM
EEPROM Size	-
RAM Size	24K x 16
Voltage - Supply (Vcc/Vdd)	1.62V ~ 1.98V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/dsp56858fve

Part 1 Overview

1.1 56858 Features

1.1.1 Digital Signal Processing Core

- Efficient 16-bit engine with dual Harvard architecture
- 120 Million Instructions Per Second (MIPS) at 120MHz core frequency
- Single-cycle 16 × 16-bit parallel Multiplier-Accumulator (MAC)
- Four (4) 36-bit accumulators including extension bits
- 16-bit bidirectional shifter
- Parallel instruction set with unique DSP addressing modes
- Hardware DO and REP loops
- Three (3) internal address buses and one (1) external address bus
- Four (4) internal data buses and one (1) external data bus
- Instruction set supports both DSP and controller functions
- Four (4) hardware interrupt levels
- Five (5) software interrupt levels
- Controller-style addressing modes and instructions for compact code
- Efficient C-Compiler and local variable support
- Software subroutine and interrupt stack with depth limited only by memory
- JTAG/Enhanced OnCE debug programming interface

1.1.2 Memory

- Harvard architecture permits up to three (3) simultaneous accesses to program and data memory
- On-Chip Memory
  - 40K × 16-bit Program RAM
  - 24K × 16-bit Data RAM
  - 1K × 16-bit Boot ROM
- Off-Chip Memory Expansion (EMI)
  - Access up to 2M words of program or 8M data memory (using chip selects)
  - Chip Select Logic for glue-less interface to ROM and SRAM

1.1.3 56858 Peripheral Circuit Features

- General Purpose 16-bit Quad Timer*
- Two Serial Communication Interfaces (SCI)*
- Serial Peripheral Interface (SPI) Port*
- Two (2) Enhanced Synchronous Serial Interface (ESSI) modules*
- Computer Operating Properly (COP)/Watchdog Timer
- JTAG/Enhanced On-Chip Emulation (EOnCE) for unobtrusive, real-time debugging

Table 3-1 56858 Signal and Package Information for the 144-pin LQFP and MAPBGA

Signal Name	BGA Pin No.	LQFP Pin No.	Type	Description
D0	H7	81	**Input**/ Output(Z)	**Data Bus (D0-D15)**—These pins provide the bidirectional data for external program or data memory accesses.
D1	G7	94		
D2	F9	95		
D3	F10	96		
D4	F11	97		
D5	E10	98		
D6	D7	120		
D7	B7	121		
D8	E7	122		
D9	F8	123		
D10	F7	124		
D11	D5	137		
D12	B4	138		
D13	C4	142		
D14	F6	143		
D15	B3	144		
$\overline{RD}$	D3	8	Output	**Read Enable ($\overline{RD}$)** — is asserted during external memory read cycles. This signal is pulled high during reset.
$\overline{WR}$	D4	9	Output	**Write Enable ($\overline{WR}$)** —is asserted during external memory write cycles. This signal is pulled high during reset.
$\overline{CS0}$ GPIOA0	H8	83	**Output** **Input**/Output	**External Chip Select ($\overline{CS0}$)**—This pin is used as a dedicated GPIO. **Port A GPIO (0)** —This pin is a General Purpose I/O (GPIO) pin when not configured for host port usage.
$\overline{CS1}$ GPIOA1	H9	84	**Output** **Input**/Output	**External Chip Select ($\overline{CS1}$)**—This pin is used as a dedicated GPIO. **Port A GPIO (1)** —This pin is a General Purpose I/O (GPIO) pin when not configured for host port usage.
$\overline{CS2}$ GPIOA2	H11	85	**Output** **Input**/Output	**External Chip Select ($\overline{CS2}$)**—This pin is used as a dedicated GPIO. **Port A GPIO (2)** —This pin is a General Purpose I/O (GPIO) pin when not configured for host port usage.
$\overline{CS3}$ GPIOA3	H10	86	**Output** **Input**/Output	**External Chip Select ($\overline{CS3}$)**—This pin is used as a dedicated GPIO. **Port A GPIO (3)**—This pin is a General Purpose I/O (GPIO) pin when not configured for host port usage.

Table 3-1 56858 Signal and Package Information for the 144-pin LQFP and MAPBGA

Signal Name	BGA Pin No.	LQFP Pin No.	Type	Description
$\overline{\text{HACK}}$	C7	119	**Input**	**Host Acknowledge ($\overline{\text{HACK}}$)**—When the HI08 is programmed for HRMS=0 functionality (typically used on a single-data-strobe bus), this input has two functions: (1) provide a Host Acknowledge signal for DMA transfers or (2) to control handshaking and provide a Host Interrupt Acknowledge compatible with the MC68000 family processors. These pins are disconnected internally during reset.
HRRQ			Open Drain Output	**Receive Host Request (HRRQ)**—This signal is the Receive Host Request output when the HI08 is programmed for HRMS=1 functionality and is typically used on a double-data-strobe bus.
GPIOB15			Input/Output	**Port B GPIO (15)**—This pin is a General Purpose I/O (GPIO) pin when not configured for host port usage.
TIO0	B9	114	**Input**/Output	**Timer Input/Outputs (TIO0)**—This pin can be independently configured to be either a timer input source or an output flag.
GPIOG0			Input/Output	**Port G GPIOG0**—This pin is a General Purpose I/O (GPIO) pin that can individually be programmed as an input or output pin.
TIO1	C9	112	**Input**/Output	**Timer Input/Outputs (TIO1)**—This pin can be independently configured to be either a timer input source or an output flag.
GPIOG1			Input/Output	**Port G GPIO (1)**—This pin is a General Purpose I/O (GPIO) pin that can individually be programmed as an input or output pin.
TIO2	D9	111	**Input**/Output	**Timer Input/Outputs (TIO2)**—This pin can be independently configured to be either a timer input source or an output flag.
GPIOG2			Input/Output	**Port G GPIO (2)**—This pin is a General Purpose I/O (GPIO) pin that can individually be programmed as an input or output pin.
TIO3	B10	110	**Input**/Output	**Timer Input/Outputs (TIO3)**—This pin can be independently configured to be either a timer input source or an output flag.
GPIOG3			Input/Output	**Port G GPIO (3)**—This pin is a General Purpose I/O (GPIO) pin that can individually be programmed as an input or output pin.
$\overline{\text{IRQA}}$	G2	22	Input	**External Interrupt Request A and B**—The $\overline{\text{IRQA}}$ and $\overline{\text{IRQB}}$ inputs are asynchronous external interrupt requests that indicate that an external device is requesting service. A Schmitt trigger input is used for noise immunity. They can be programmed to be level-sensitive or negative-edge-triggered. If level-sensitive triggering is selected, an external pull-up resistor is required for Wired-OR operation.
$\overline{\text{IRQB}}$	F5	23		
MODE A	F4	17	**Input**	**Mode Select (MODE A)**—During the bootstrap process MODE A selects one of the eight bootstrap modes.
GPIOH0			Input/Output	**Port H GPIO (0)**—This pin is a General Purpose I/O (GPIO) pin after the bootstrap process has completed.

Table 3-1 56858 Signal and Package Information for the 144-pin LQFP and MAPBGA

Signal Name	BGA Pin No.	LQFP Pin No.	Type	Description
MISO	B2	1	**Input**/Output	**SPI Master In/Slave Out (MISO)**—This serial data pin is an input to a master device and an output from a slave device. The MISO line of a slave device is placed in the high-impedance state if the slave device is not selected. The driver on this pin can be configured as an open-drain driver by the SPI's Wired-OR mode (WOM) bit when this pin is configured for SPI operation.
GPIOF0			Input/Output	**Port F GPIO (0)**—This pin is a General Purpose I/O (GPIO) pin that can individually be programmed as input or output pin.
MOSI	C3	2	Input/ **Output (Z)**	**SPI Master Out/Slave In (MOSI)**—This serial data pin is an output from a master device and an input to a slave device. The master device places data on the MOSI line a half-cycle before the clock edge that the slave device uses to latch the data. The driver on this pin can be configured as an open-drain driver by the SPI's WOM bit when this pin is configured for SPI operation.
GPIOF1			Input/Output	**Port F GPIO (1)**—This pin is a General Purpose I/O (GPIO) pin that can be individually programmed as input or output pin.
SCK	C2	3	**Input**/Output	**SPI Serial Clock (SCK)**—This bidirectional pin provides a serial bit rate clock for the SPI. This gated clock signal is an input to a slave device and is generated as an output by a master device. Slave devices ignore the SCK signal unless the $\overline{SS}$ pin is active low. In both master and slave SPI devices, data is shifted on one edge of the SCK signal and is sampled on the opposite edge where data is stable. The driver on this pin can be configured as an open-drain driver by the SPI's WOM bit when this pin is configured for SPI operation. When using Wired-OR mode, the user must provide an external pull-up device.
GPIOF2			Input/Output	**Port F GPIO (2)**—This pin is a General Purpose I/O (GPIO) pin that can individually be programmed as input or output pin.
$\overline{SS}$	D2	4	**Input**	**SPI Slave Select ($\overline{SS}$)**—This input pin selects a slave device before a master device can exchange data with the slave device. $\overline{SS}$ must be low before data transactions and must stay low for the duration of the transaction. The $\overline{SS}$ line of the master must be held high.
GPIOF3			Input/Output	**Port F GPIO (3)**—This pin is a General Purpose I/O (GPIO) pin that can individually be programmed as input or output pin.
XTAL	H2	27	Input/Output	**Crystal Oscillator Output (XTAL)**—This output connects the internal crystal oscillator output to an external crystal. If an external clock source other than a crystal oscillator is used, XTAL must be used as the input.
EXTAL	G3	28	Input	**External Crystal Oscillator Input (EXTAL)**—This input should be connected to an external crystal. If an external clock source other than a crystal oscillator is used, EXTAL must be tied off. See Section 4.5.2
CLKO	L3	37	Output	**Clock Output (CLKO)**—This pin outputs a buffered clock signal. When enabled, this signal is the system clock divided by four.

Table 3-1 56858 Signal and Package Information for the 144-pin LQFP and MAPBGA

Signal Name	BGA Pin No.	LQFP Pin No.	Type	Description
TCK	L8	60	Input	**Test Clock Input (TCK)**—This input pin provides a gated clock to synchronize the test logic and to shift serial data to the JTAG/OnCE port. The pin is connected internally to a pull-down resistor.
TDI	K7	58	Input	**Test Data Input (TDI)**—This input pin provides a serial input data stream to the JTAG/OnCE port. It is sampled on the rising edge of TCK and has an on-chip pull-up resistor.
TDO	G6	57	Output(Z)	**Test Data Output (TDO)**—This tri-statable output pin provides a serial output data stream from the JTAG/Enhanced OnCE port. It is driven in the Shift-IR and Shift-DR controller states, and changes on the falling edge of TCK.
TMS	J7	59	Input	**Test Mode Select Input (TMS)**—This input pin is used to sequence the JTAG TAP controller's state machine. It is sampled on the rising edge of TCK and has an on-chip pull-up resistor. **Note:** Always tie the TMS pin to V_{DD} through a 2.2K resistor.
$\overline{\text{TRST}}$	L7	56	Input	**Test Reset ($\overline{\text{TRST}}$)**—As an input, a low signal on this pin provides a reset signal to the JTAG TAP controller. To ensure complete hardware reset, $\overline{\text{TRST}}$ should be asserted whenever $\overline{\text{RESET}}$ is asserted. The only exception occurs in a debugging environment, since the Enhanced OnCE/JTAG module is under the control of the debugger. In this case it is not necessary to assert $\overline{\text{TRST}}$ when asserting $\overline{\text{RESET}}$. Outside of a debugging environment $\overline{\text{RESET}}$ should be permanently asserted by grounding the signal, thus disabling the Enhanced OnCE/JTAG module on the device. **Note:** For normal operation, connect $\overline{\text{TRST}}$ directly to V_{SS}. If the design is to be used in a debugging environment, $\overline{\text{TRST}}$ may be tied to V_{SS} through a 1K resistor.

Table 4-4 DC Electrical Characteristics (Continued)

Operating Conditions: $V_{SS} = V_{SSIO} = V_{SSA} = 0$ V, $V_{DD} = 1.62\text{-}1.98$V, $V_{DDIO} = V_{DDA} = 3.0\text{–}3.6$V, $T_A = -40°$ to $+120°$C, $C_L \leq 50$pF, $f_{op} = 120$MHz

Characteristic	Symbol	Min	Typ	Max	Unit
Input current low (pullups disabled)	I_{IL}	-1	—	1	μA
Input current high (pullups disabled)	I_{IH}	-1	—	1	μA
Output tri-state current low	I_{OZL}	-10	—	10	μA
Output tri-state current high	I_{OZH}	-10	—	10	μA
Output High Voltage	V_{OH}	$V_{DDIO} - 0.7$	—	—	V
Output Low Voltage	V_{OL}	—	—	0.4	V
Output High Current	I_{OH}	8	—	16	mA
Output Low Current	I_{OL}	8	—	16	mA
Input capacitance	C_{IN}	—	8	—	pF
Output capacitance	C_{OUT}	—	12	—	pF
V_{DD} supply current (Core logic, memories, peripherals) Run [1] Deep Stop[2] Light Stop[3]	I_{DD}[4]	 — — —	 70 0.05 5	 110 10 14	 mA mA mA
V_{DDIO} supply current (I/O circuity) Run[5] Deep Stop[2]	I_{DDIO}	—	 40 0	 50 1.5	 mA mA
V_{DDA} supply current (analog circuity) Deep Stop[2]	I_{DDA}	—	 60	 120	 μA
Low Voltage Interrupt[6]	V_{EI}	—	2.5	2.85	V
Low Voltage Interrupt Recovery Hysteresis	V_{EIH}	—	50	—	mV
Power on Reset[7]	POR	—	1.5	2.0	V

Note: Run (operating) I_{DD} measured using external square wave clock source (f_{osc} = 4MHz) into XTAL. All inputs 0.2V from rail; no DC loads; outputs unloaded. All ports configured as inputs; measured with all modules enabled. PLL set to 240MHz out.

1. Running Core, performing 50% NOP and 50% FIR. Clock at 120 MHz.
2. Deep Stop Mode - Operation frequency = 4 MHz, PLL set to 4 MHz, crystal oscillator and time of day module operating.
3. Light Stop Mode - Operation frequency = 120 MHz, PLL set to 240 MHz, crystal oscillator and time of day module operating.
4. I_{DD} includes current for core logic, internal memories, and all internal peripheral logic circuitry.
5. Running core and performing external memory access. Clock at 120 MHz.
6. When V_{DD} drops below V_{EI} max value, an interrupt is generated.
7. Power-on reset occurs whenever the digital supply drops below 1.8V. While power is ramping up, this signal remains active for as long as the internal 2.5V is below 1.8V no matter how long the ramp up rate is. The internally regulated voltage is typically 100 mV less than V_{DD} during ramp up until 2.5V is reached, at which time it self-regulates.

Figure 4-5 shows the definitions of the following signal states:

- Active state, when a bus or signal is driven, and enters a low impedance state
- Tri-stated, when a bus or signal is placed in a high impedance state
- Data Valid state, when a signal level has reached V_{OL} or V_{OH}
- Data Invalid state, when a signal level is in transition between V_{OL} and V_{OH}

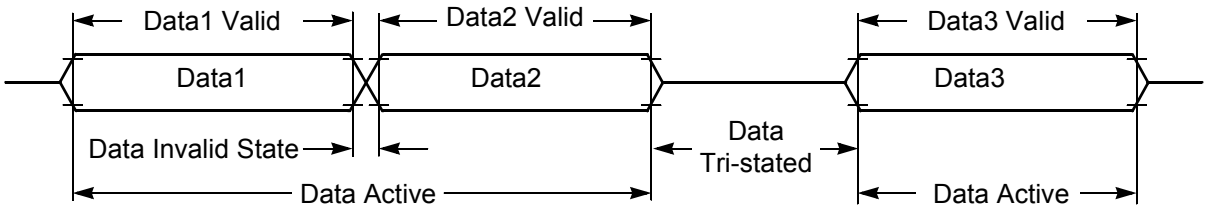


Figure 4-5 Signal States

4.5 External Clock Operation

The 56858 system clock can be derived from a crystal or an external system clock signal. To generate a reference frequency using the internal oscillator, a reference crystal must be connected between the EXTAL and XTAL pins.

4.5.1 Crystal Oscillator

The internal oscillator is designed to interface with a parallel-resonant crystal resonator in the frequency range specified for the external crystal in Table 4-6. In Figure 4-6 a typical crystal oscillator circuit is shown. Follow the crystal supplier's recommendations when selecting a crystal, because crystal parameters determine the component values required to provide maximum stability and reliable start-up. The crystal and associated components should be mounted as close as possible to the EXTAL and XTAL pins to minimize output distortion and start-up stabilization time.

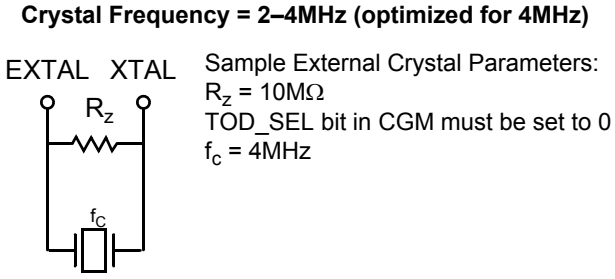


Figure 4-6 Crystal Oscillator

4.5.2 High Speed External Clock Source (> 4MHz)

The recommended method of connecting an external clock is given in **Figure 4-7.** The external clock source is connected to XTAL and the EXTAL pin is held at ground, V_{DDA}, or $V_{DDA}/2$. The TOD_SEL bit in CGM must be set to 0.

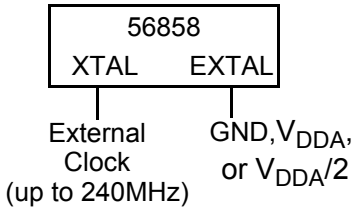


Figure 4-7 Connecting a High Speed External Clock Signal using XTAL

4.5.3 Low Speed External Clock Source (2-4MHz)

The recommended method of connecting an external clock is given in **Figure 4-8.** The external clock source is connected to XTAL and the EXTAL pin is held at $V_{DDA}/2$. The TOD_SEL bit in CGM must be set to 0.

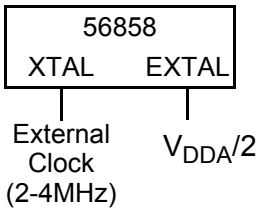


Figure 4-8 Connecting a Low Speed External Clock Signal using XTAL

Table 4-5 External Clock Operation Timing Requirements[4]

Operating Conditions: $V_{SS} = V_{SSIO} = V_{SSA} = 0$ V, $V_{DD} = 1.62\text{-}1.98$V, $V_{DDIO} = V_{DDA} = 3.0\text{–}3.6$V, $T_A = -40°$ to $+120°$C, $C_L \leq 50$pF, $f_{op} = 120$MHz

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency of operation (external clock driver)[1]	f_{osc}	0	—	240	MHz
Clock Pulse Width[4]	t_{PW}	6.25	—	—	ns
External clock input rise time[2, 4]	t_{rise}	—	—	TBD	ns
External clock input fall time[3, 4]	t_{fall}	—	—	TBD	ns

1. See **Figure 4-7** for details on using the recommended connection of an external clock driver.
2. External clock input rise time is measured from 10% to 90%.
3. External clock input fall time is measured from 90% to 10%.
4. Parameters listed are guaranteed by design.

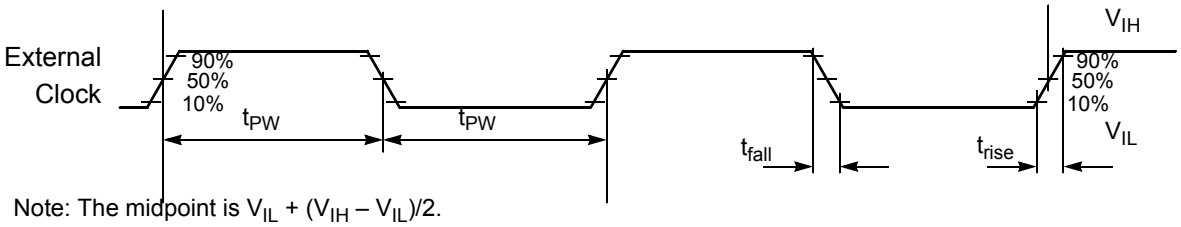


Figure 4-9 External Clock Timing

Table 4-6 PLL Timing

Operating Conditions: $V_{SS} = V_{SSIO} = V_{SSA} = 0$ V, $V_{DD} = 1.62\text{-}1.98$V, $V_{DDIO} = V_{DDA} = 3.0\text{–}3.6$V, $T_A = -40°$ to $+120°$C, $C_L \leq 50$pF, $f_{op} = 120$MHz

Characteristic	Symbol	Min	Typ	Max	Unit
External reference crystal frequency for the PLL[1]	f_{osc}	2	4	4	MHz
PLL output frequency	f_{clk}	40	—	240	MHz
PLL stabilization time [2]	t_{plls}	—	1	10	ms

1. An externally supplied reference clock should be as free as possible from any phase jitter for the PLL to work correctly. The PLL is optimized for 4MHz input crystal.
2. This is the minimum time required after the PLL setup is changed to ensure reliable operation.

4.6 External Memory Interface Timing

The External Memory Interface is designed to access static memory and peripheral devices. **Figure 4-10** shows sample timing and parameters that are detailed in **Table 4-7**.

The timing of each parameter consists of both a fixed delay portion and a clock related portion; as well as user controlled wait states. The equation:

$$t = D + P * (M + W)$$

should be used to determine the actual time of each parameter. The terms in the above equation are defined as:

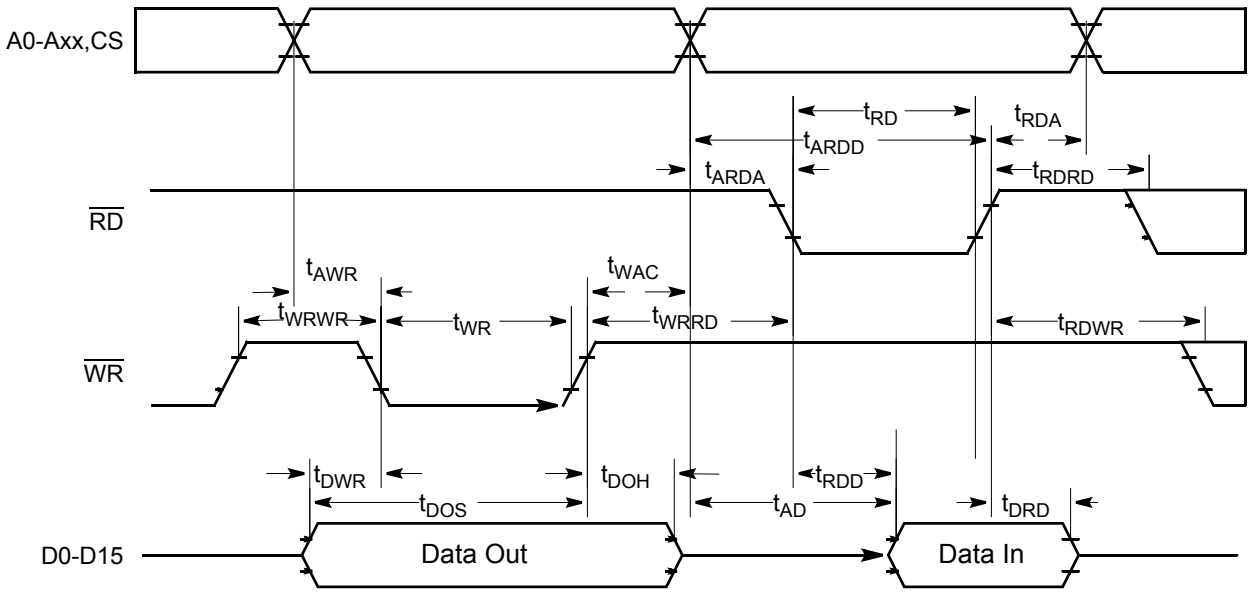
- t parameter delay time
- D fixed portion of the delay, due to on-chip path delays.
- P the period of the system clock, which determines the execution rate of the part (i.e. when the device is operating at 120 MHz, P = 8.33 ns).

M Fixed portion of a clock period inherent in the design. This number is adjusted to account for possible clock duty cycle derating.

W the sum of the applicable wait state controls. See the “Wait State Controls” column of **Table 4-7** for the applicable controls for each parameter. See the EMI chapter of the 83x Peripheral Manual for details of what each wait state field controls.

Some of the parameters contain two sets of numbers. These parameters have two different paths and clock edges that must be considered. Check both sets of numbers and use the smaller result. The appropriate entry may change if the operating frequency of the part changes.

The timing of write cycles is different when WWS = 0 than when WWS > 0. Therefore, some parameters contain two sets of numbers to account for this difference. The “Wait States Configuration” column of **Table 4-7** should be used to make the appropriate selection.



Note: During read-modify-write instructions and internal instructions, the address lines do not change state.

Figure 4-10 External Memory Interface Timing

4.7 Reset, Stop, Wait, Mode Select, and Interrupt Timing

Table 4-8 Reset, Stop, Wait, Mode Select, and Interrupt Timing[1, 2]

Operating Conditions: $V_{SS} = V_{SSIO} = V_{SSA} = 0$ V, $V_{DD} = 1.62$-1.98V, $V_{DDIO} = V_{DDA} = 3.0$–3.6V, $T_A = -40°$ to $+120°$C, $C_L \leq 50$pF, $f_{op} = 120$MHz

Characteristic	Symbol	Min	Max	Unit	See Figure
$\overline{\text{RESET}}$ Assertion to Address, Data and Control Signals High Impedance	t_{RAZ}	—	11	ns	Figure 4-11
Minimum $\overline{\text{RESET}}$ Assertion Duration[3]	t_{RA}	30	—	ns	Figure 4-11
$\overline{\text{RESET}}$ Deassertion to First External Address Output	t_{RDA}	—	120T	ns	Figure 4-11
Edge-sensitive Interrupt Request Width	t_{IRW}	1T + 3	—	ns	Figure 4-12
$\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$ Assertion to External Data Memory Access Out Valid, caused by first instruction execution in the interrupt service routine	t_{IDM}	18T	—	ns	Figure 4-13
	$t_{IDM\ -FAST}$	14T	—		
$\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$ Assertion to General Purpose Output Valid, caused by first instruction execution in the interrupt service routine	t_{IG}	18T	—	ns	Figure 4-13
	$t_{IG\ -FAST}$	14T	—		
$\overline{\text{IRQA}}$ Low to First Valid Interrupt Vector Address Out recovery from Wait State[4]	t_{IRI}	22T	—	ns	Figure 4-14
	$t_{IRI\ -FAST}$	18T	—		
Delay from $\overline{\text{IRQA}}$ Assertion (exiting Stop) to External Data Memory[5]	t_{IW}	1.5T	—	ns	Figure 4-15
Delay from $\overline{\text{IRQA}}$ Assertion (exiting Wait) to External Data Memory Fast[6] Normal[7]	t_{IF}	 18T 22ET	 — —	 ns ns	Figure 4-15
$\overline{\text{RSTO}}$ pulse width[8] normal operation internal reset mode	t_{RSTO}	 128ET 8ET	 — —	 — —	Figure 4-16

1. In the formulas, T = clock cycle. For $f_{op} = 120$MHz operation and $f_{ipb} = 60$MHz, T = 8.33ns.
2. Parameters listed are guaranteed by design.
3. At reset, the PLL is disabled and bypassed. The part is then put into Run mode and t_{clk} assumes the period of the source clock, t_{xtal}, t_{extal} or t_{osc}.
4. The minimum is specified for the duration of an edge-sensitive IRQA interrupt required to recover from the Stop state. This is not the minimum required so that the IRQA interrupt is accepted.
5. The interrupt instruction fetch is visible on the pins only in Mode 3.
6. Fast stop mode:
   Fast stop recovery applies when external clocking is in use (direct clocking to XTAL) or when fast stop mode recovery is requested (OMR bit 6 is set to 1). In both cases the PLL and the master clock are unaffected by stop mode entry. Recovery takes one less cycle and t_{clk} will continue same value it had before stop mode was entered.

7. Normal stop mode:
   As a power saving feature, normal stop mode disables and bypasses the PLL. Stop mode will then shut down the master clock, recovery will take an extra cycle (to restart the clock), and t_{clk} will resume at the input clock source rate.
8. ET = External Clock period, For an external crystal frequency of 8MHz, ET=125 ns.

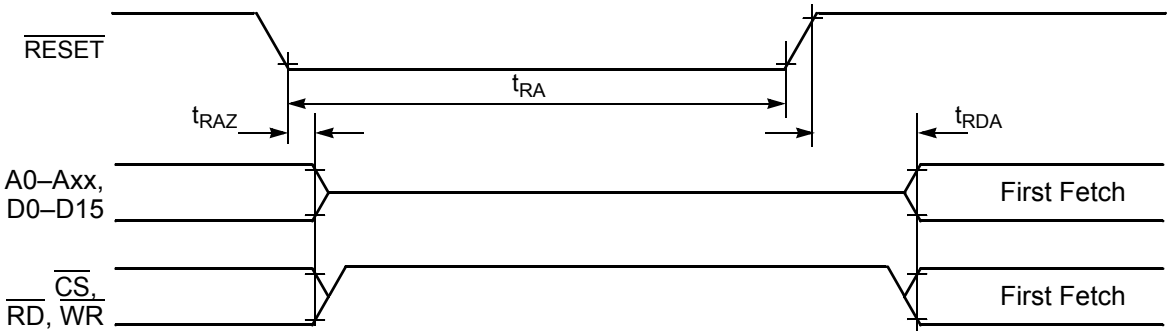


Figure 4-11 Asynchronous Reset Timing

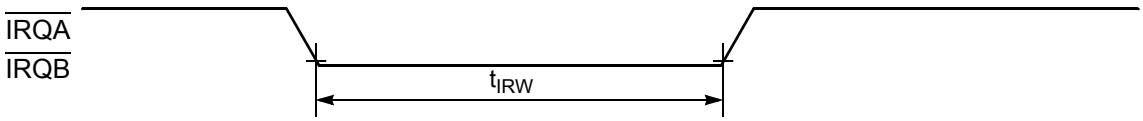


Figure 4-12 External Interrupt Timing (Negative-Edge-Sensitive)

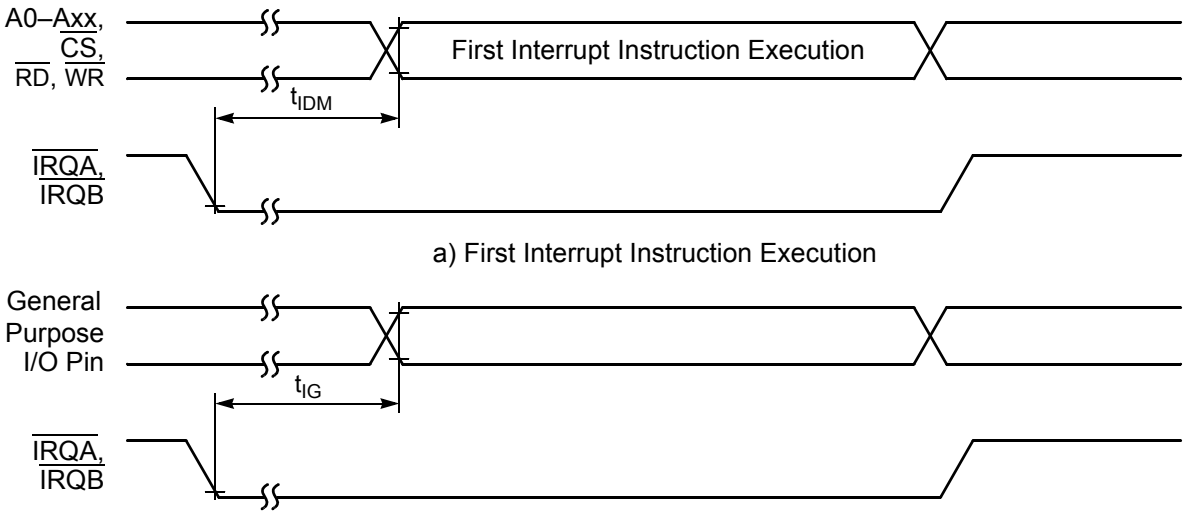


Figure 4-13 External Level-Sensitive Interrupt Timing

4.8 Host Interface Port

Table 4-9 Host Interface Port Timing[1]

Operating Conditions: $V_{SS} = V_{SSIO} = V_{SSA} = 0$ V, $V_{DD} = 1.62\text{-}1.98$V, $V_{DDIO} = V_{DDA} = 3.0\text{–}3.6$V, $T_A = -40°$ to $+120°$C, $C_L \leq 50$pF, $f_{op} = 120$MHz

Characteristic	Symbol	Min	Max	Unit	See Figure
Access time	TACKDV	—	13	ns	4-17
Disable time	TACKDZ	3	—	ns	4-17
Time to disassert	TACKREQH	3.5	9	ns	4-17 4-20
Lead time	TREQACKL	0	—	ns	4-17 4-20
Access time	TRADV	—	13	ns	4-18 4-19
Disable time	TRADX	5	—	ns	4-18 4-19
Disable time	TRADZ	3	—	ns	4-18 4-19
Setup time	TDACKS	3	—	ns	4-20
Hold time	TACKDH	1	—	ns	4-20
Setup time	TADSS	3	—	ns	4-21 4-22
Hold time	TDSAH	1	—	ns	4-21 4-22
Pulse width	TWDS	5	—	ns	4-21 4-22
Time to re-assert 1. After second write in 16-bit mode 2. After first write in 16-bit mode or after write in 8-bit mode	TACKREQL	4T + 5 5	5T + 9 13	ns ns	4-19 4-20

1. The formulas: T = clock cycle. f ipb = 60MHz, T = 16.7ns.

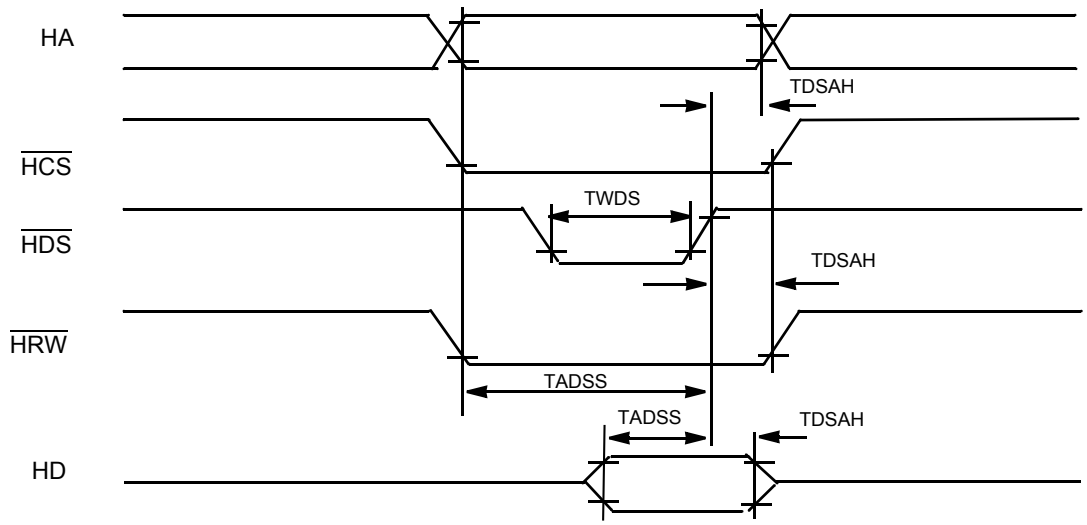


Figure 4-21 Single Strobe Write Mode

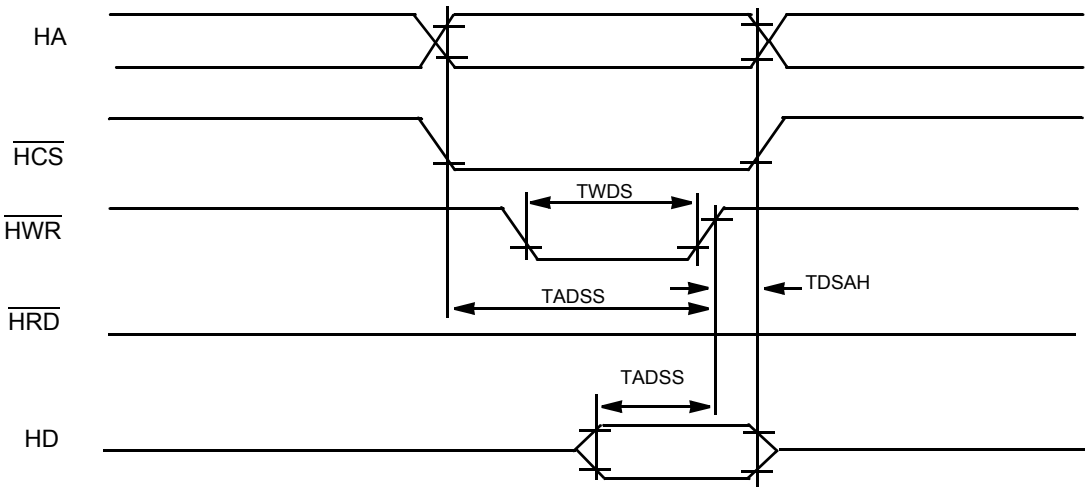


Figure 4-22 Dual Strobe Write Mode

4.9 Serial Peripheral Interface (SPI) Timing

Figure 4-23 SPI Timing [1]

Operating Conditions: $V_{SS} = V_{SSIO} = V_{SSA} = 0$ V, $V_{DD} = 1.62\text{-}1.98$V, $V_{DDIO} = V_{DDA} = 3.0\text{–}3.6$V, $T_A = -40°$ to $+120°$C, $C_L \leq 50$pF, $f_{op} = 120$MHz

Characteristic	Symbol	Min	Max	Unit	See Figure
Cycle time Master Slave	t_C	 25 25	 — —	 ns ns	4-24, 4-25, 4-26, 4-27
Enable lead time Master Slave	t_{ELD}	 — 12.5	 — —	 ns ns	4-27
Enable lag time Master Slave	t_{ELG}	 — 12.5	 — —	 ns ns	4-27
Clock (SCLK) high time Master Slave	t_{CH}	 9 12.5	 — —	ns ns	4-24, 4-25, 4-26, 4-27
Clock (SCLK) low time Master Slave	t_{CL}	 12 12.5	 — —	 ns ns	4-27
Data set-up time required for inputs Master Slave	t_{DS}	 10 2	 — —	 ns ns	4-24, 4-25, 4-26, 4-27
Data hold time required for inputs Master Slave	t_{DH}	 0 2	 — —	 ns ns	4-24, 4-25, 4-26, 4-27
Access time (time to data active from high-impedance state) Slave	t_A	 5	 15	ns ns	4-27
Disable time (hold time to high-impedance state) Slave	t_D	 2	 9	ns ns	4-27
Data valid for outputs Master Slave (after enable edge)	t_{DV}	 — —	 2 14	 ns ns	4-24, 4-25, 4-26, 4-27
Data invalid Master Slave	t_{DI}	 0 0	 — —	 ns ns	4-24, 4-25, 4-26, 4-27
Rise time Master Slave	t_R	 — —	 11.5 10.0	 ns ns	4-24, 4-25, 4-26, 4-27
Fall time Master Slave	t_F	 — —	 9.7 9.0	 ns ns	4-24, 4-25, 4-26, 4-27

1. Parameters listed are guaranteed by design.

4.10 Quad Timer Timing

Table 4-10 Quad Timer Timing[1, 2]

Operating Conditions: $V_{SS} = V_{SSIO} = V_{SSA} = 0$ V, $V_{DD} = 1.62\text{-}1.98$V, $V_{DDIO} = V_{DDA} = 3.0\text{–}3.6$V, $T_A = -40°$ to $+120°$C, $C_L \leq 50$pF, $f_{op} = 120$MHz

Characteristic	Symbol	Min	Max	Unit
Timer input period	P_{IN}	2T + 3	—	ns
Timer input high/low period	P_{INHL}	1T + 3	—	ns
Timer output period	P_{OUT}	2T - 3	—	ns
Timer output high/low period	P_{OUTHL}	1T - 3	—	ns

1. In the formulas listed, T = clock cycle. For $f_{op} = 120$MHz operation and fipb = 60MHz, T = 8.33ns.
2. Parameters listed are guaranteed by design.

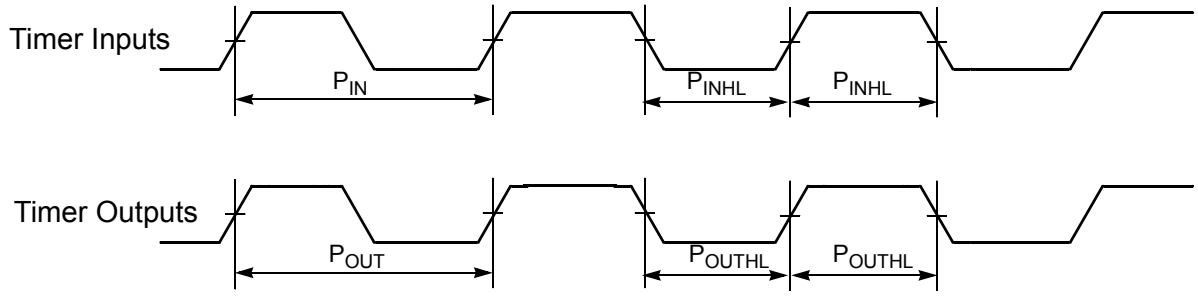


Figure 4-28 Timer Timing

4.11 Enhanced Synchronous Serial Interface (ESSI) Timing

Table 4-11 ESSI Master Mode[1] Switching Characteristics

Operating Conditions: $V_{SS} = V_{SSIO} = V_{SSA} = 0$ V, $V_{DD} = 1.62\text{-}1.98$V, $V_{DDIO} = V_{DDA} = 3.0\text{–}3.6$V, $T_A = -40°$ to $+120°$C, $C_L \leq 50$pF, $f_{op} = 120$MHz

Parameter	Symbol	Min	Typ	Max	Units
SCK frequency	fs	—	—	15[2]	MHz
SCK period[3]	t_{SCKW}	66.7	—	—	ns
SCK high time	t_{SCKH}	33.4[4]	—	—	ns
SCK low time	t_{SCKL}	33.4[4]	—	—	ns
Output clock rise/fall time	—	—	4	—	ns
Delay from SCK high to SC2 (bl) high - Master[5]	t_{TFSBHM}	-1.0	—	1.0	ns

This section contains package and pin-out information for the 144-pin MAPBGA configuration of the 56858.

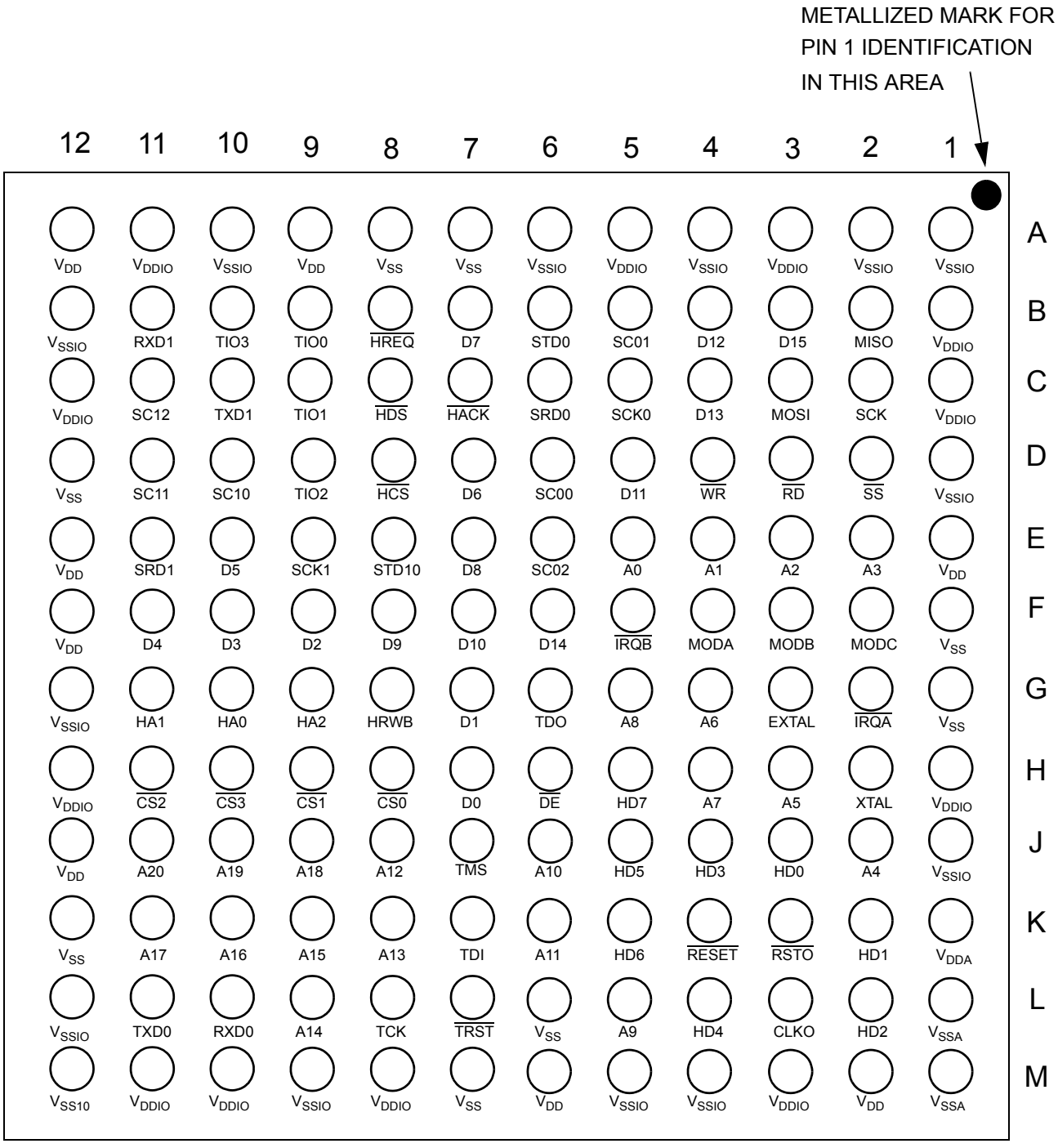


Figure 5-3 Bottom-View, 56858 144-pin MAPBGA Package

Table 5-2 56858 Pin Identification by Pin Number

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
E5	A0	F7	D10	D8	$\overline{HCS}$	A5	V_{DDIO}
E4	A1	D5	D11	J3	HD0	A3	V_{DDIO}
E3	A2	B4	D12	K2	HD1	C1	V_{DDIO}
E2	A3	C4	D13	L2	HD2	M10	V_{DDIO}
J2	A4	F6	D14	J4	HD3	D3	$\overline{RD}$
H3	A5	B3	D15	L4	HD4	K4	$\overline{RESET}$
G4	A6	H6	$\overline{DE}$	J5	HD5	K3	$\overline{RSTO}$
H4	A7	G3	EXTAL	K5	HD6	L10	RXD0
G5	A8	M1	V_{SSA}	H5	HD7	B11	RXD1
L5	A9	L1	V_{SSA}	C8	$\overline{HDS}$	D6	SC00
J6	A10	G1	V_{SS}	B8	$\overline{HREQ}$	B5	SC01
K6	A11	L6	V_{SS}	G8	HRWB	E6	SC02
J8	A12	D12	V_{SS}	G2	$\overline{IRQA}$	D10	SC10
K8	A13	A7	V_{SS}	F5	$\overline{IRQB}$	D11	SC11
L9	A14	F1	V_{SS}	B2	MISO	C11	SC12
K9	A15	M7	V_{SS}	F4	MODA	C5	SCK0
K10	A16	K12	V_{SS}	F3	MODB	E9	SCK1
K11	A17	A8	V_{SS}	F2	MODC	C2	SCK
J9	A18	D1	V_{SSIO}	C3	MOSI	C6	SRD0
J10	A19	J1	V_{SSIO}	K1	V_{DDA}	E11	SRD1
J11	A20	M5	V_{SSIO}	E1	V_{DD}	D2	$\overline{SS}$
L3	CLKO	M9	V_{SSIO}	M6	V_{DD}	B6	STD0
H8	$\overline{CS0}$	L12	V_{SSIO}	F12	V_{DD}	E8	STD1
H9	$\overline{CS1}$	G12	V_{SSIO}	A9	V_{DD}	L8	TCK

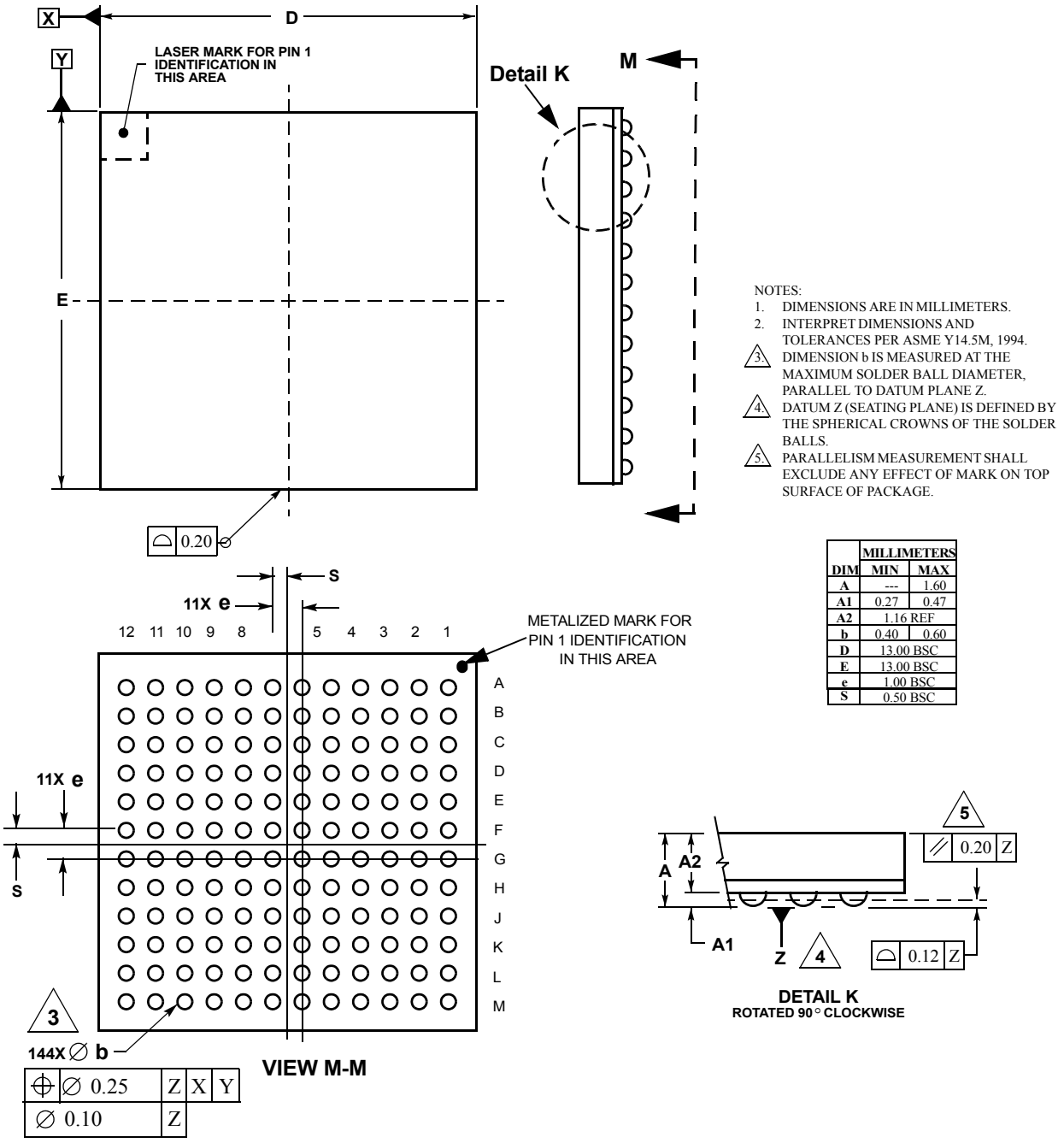


Figure 5-4 144-pin MAPBGA Mechanical Information

Please see **www.freescale.com** for the most current case outline.

How to Reach Us:

Home Page:
www.freescale.com

E-mail:
support@freescale.com

USA/Europe or Locations Not Listed:
Freescale Semiconductor
Technical Information Center, CH370
1300 N. Alma School Road
Chandler, Arizona 85224
+1-800-521-6274 or +1-480-768-2130
support@freescale.com

Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
support@freescale.com

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064, Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor Hong Kong Ltd.
Technical Information Center
2 Dai King Street
Tai Po Industrial Estate
Tai Po, N.T., Hong Kong
+800 2666 8080
support.asia@freescale.com

For Literature Requests Only:
Freescale Semiconductor Literature Distribution Center
P.O. Box 5405
Denver, Colorado 80217
1-800-441-2447 or 303-675-2140
Fax: 303-675-2150
LDCForFreescaleSemiconductor@hibbertgroup.com

DSP56858
Rev. 6
01/2007