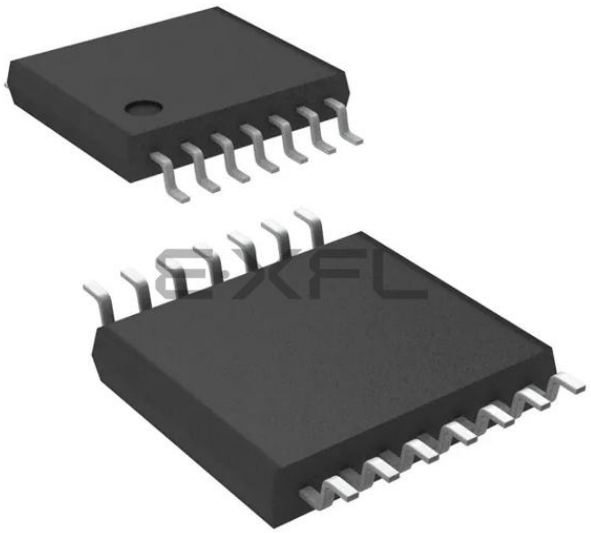

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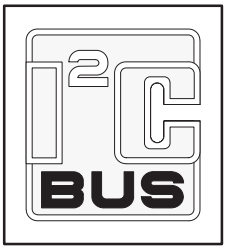
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	20MHz
Connectivity	I²C, UART/USART
Peripherals	Brown-out Detect/Reset, LED, POR, WDT
Number of I/O	12
Program Memory Size	1KB (1K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	14-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	14-TSSOP
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/p87lpc760bdh-112

Low power, low price, low pin count (14 pin) microcontroller with 1 kbyte OTP

P87LPC760



GENERAL DESCRIPTION

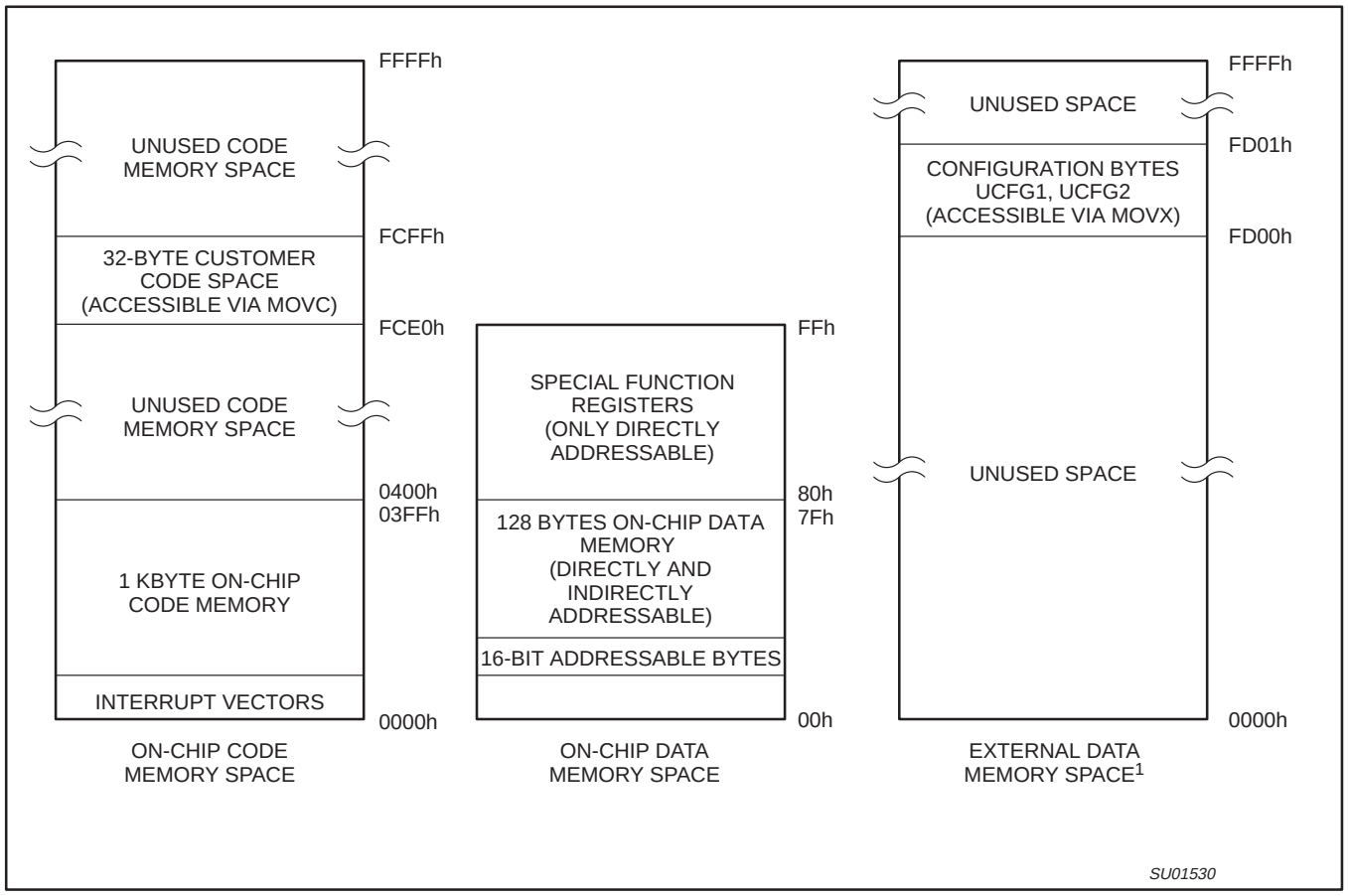
The P87LPC760 is a 14-pin single-chip microcontroller designed for low pin count applications demanding high-integration, low cost solutions over a wide range of performance requirements. A member of the Philips low pin count family, the P87LPC760 offers programmable oscillator configurations for high and low speed crystals or RC operation, wide operating voltage range, programmable port output configurations, selectable Schmitt trigger inputs, LED drive outputs, and a built-in watchdog timer. The P87LPC760 is based on an accelerated 80C51 processor architecture that executes instructions at twice the rate of standard 80C51 devices.

FEATURES

- An accelerated 80C51 CPU provides instruction cycle times of 300–600 ns for all instructions except multiply and divide when executing at 20 MHz. Execution at up to 20 MHz when V_{DD} = 4.5 V to 6.0 V, 10 MHz when V_{DD} = 2.7 V to 6.0 V
- 2.7 V to 6.0 V operating range for digital functions
- 1 kbyte EPROM code memory
- 128 byte RAM data memory
- 32 byte customer code EPROM allows serialization of devices, storage of setup parameters, etc
- Two 16-bit counter/timers. One timer may be configured to toggle a port output upon timer overflow
- One analog comparator
- Full duplex UART
- I^2C communication port
- Four keypad interrupt inputs, plus one additional external interrupt input
- Four interrupt priority levels
- Watchdog timer with separate on-chip oscillator, requiring no external components. The watchdog timeout time is selectable from 8 values
- Active low reset. On-chip power-on reset allows operation with no external reset components
- Low voltage reset. One of two preset low voltage levels may be selected to allow a graceful system shutdown when power fails. May optionally be configured as an interrupt
- Oscillator Fail Detect. The watchdog timer has a separate fully on-chip oscillator, allowing it to perform an oscillator fail detect function
- Configurable on-chip oscillator with frequency range and RC oscillator options (selected by user programmed EPROM bits). The RC oscillator option allows operation with no external oscillator components
- Programmable port output configuration options: quasi-bidirectional, open drain, push-pull, input-only
- Selectable Schmitt trigger port inputs
- LED drive capability (20 mA) on all port pins
- Controlled slew rate port outputs to reduce EMI. Outputs have approximately 10 ns minimum ramp times
- Nine I/O pins minimum. Up to 12 I/O pins using on-chip oscillator and reset options
- Only power and ground connections are required to operate the P87LPC760 when fully on-chip oscillator and reset options are selected
- Serial EPROM programming allows simple in-circuit production coding. Two EPROM security bits prevent reading of sensitive application programs
- Idle and Power Down reduced power modes. Improved wakeup from Power Down mode (a low interrupt input starts execution). Typical Power Down current is 1 μA
- 14-pin TSSOP and 14-pin DIP packages

ORDERING INFORMATION

Part Number	Temperature Range °C and Package	Frequency	Drawing Number
P87LPC760BDH	0 to +70, plastic thin shrink small outline package; 14 leads; body width 4.4 mm	20 MHz (5 V), 10 MHz (3 V)	SOT402-1
P87LPC760BN	0 to +70, plastic dual in-line package; 14 leads (300 mil)	20 MHz (5 V), 10 MHz (3 V)	SOT27-1



1. The P87LPC760 does not support access to external data memory. However, the User Configuration Bytes are accessed via the MOVX instruction as if they were in external data memory.

Figure 1. P87LPC760 Program and Data Memory Map

Name	Description	SFR Address	Bit Functions and Addresses MSB							LSB	Reset Value
P2M2#	Port 2 output mode 2	A5h	–	–	–	–	–	–	(P2M2.1)	(P2M2.0)	00h[1]
PCON	Power control register	87h	SMOD1	SMOD0	BOF	POF	GF1	GF0	PD	IDL	Note 3
			D7	D6	D5	D4	D3	D2	D1	D0	
PSW*	Program status word	D0h	CY	AC	F0	RS1	RS0	OV	F1	P	00h
PT0AD#	Port 0 digital input disable	F6h									00h
			9F	9E	9D	9C	9B	9A	99	98	
SCON*	Serial port control	98h	SM0	SM1	SM2	REN	TB8	RB8	TI	RI	00h
SBUF	Serial port data buffer register	99h									XXh
SADDR#	Serial port address register	A9h									00h
SADEN#	Serial port address enable	B9h									00h
SP	Stack pointer	81h									07h
			8F	8E	8D	8C	8B	8A	89	88	
TCON*	Timer 0 and 1 control	88h	TF1	TR1	TF0	TR0	–	–	IE0	IT0	00h
TH0	Timer 0 high byte	8Ch									00h
TH1	Timer 1 high byte	8Dh									00h
TL0	Timer 0 low byte	8Ah									00h
TL1	Timer 1 low byte	8Bh									00h
TMOD	Timer 0 and 1 mode	89h	–	–	M1	M0	GATE	C/$\overline{T}$	M1	M0	00h
WDCON#	Watchdog control register	A7h	–	–	WDOVF	WDRUN	WDCLK	WDS2	WDS1	WDS0	Note 4
WDRST#	Watchdog reset register	A6h									XXh

NOTES:
* SFRs are bit addressable.
# SFRs are modified from or added to the 80C51 SFRs.
1. Unimplemented bits in SFRs are X (unknown) at all times. Ones should not be written to these bits since they may be used for other purposes in future derivatives. The reset value shown in the table for these bits is 0.
2. I/O port values at reset are determined by the PRHI bit in the UCFG1 configuration byte.
3. The PCON reset value is x x BOF POF–0 0 0 0b. The BOF and POF flags are not affected by reset. The POF flag is set by hardware upon power up. The BOF flag is set by the occurrence of a brownout reset/interrupt and upon power up.
4. The WDCON reset value is xx11 0000b for a Watchdog reset, xx01 0000b for all other reset causes if the watchdog is enabled, and xx00 0000b for all other reset causes if the watchdog is disabled.

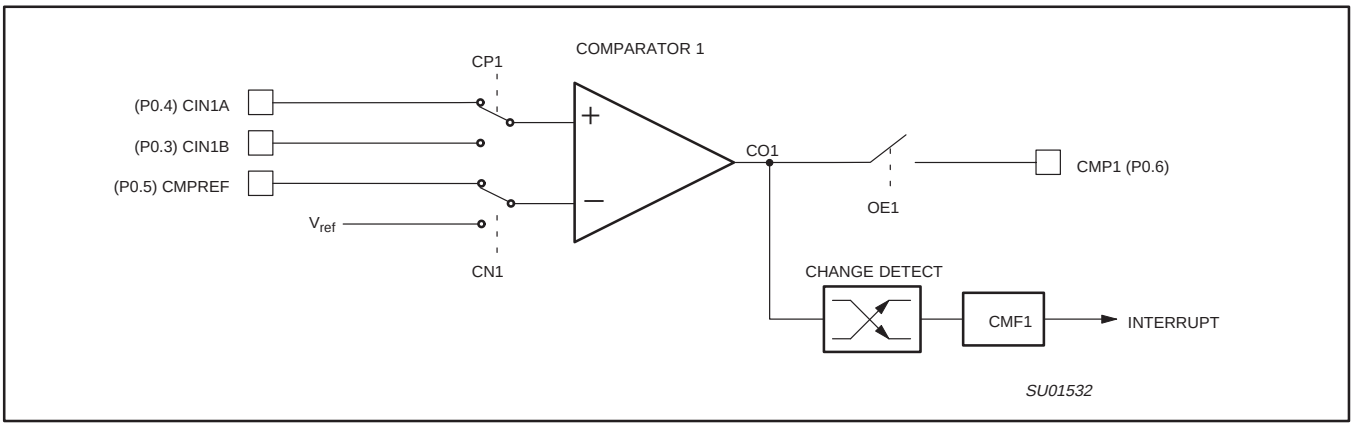


Figure 3. Comparator Input and Output Connections

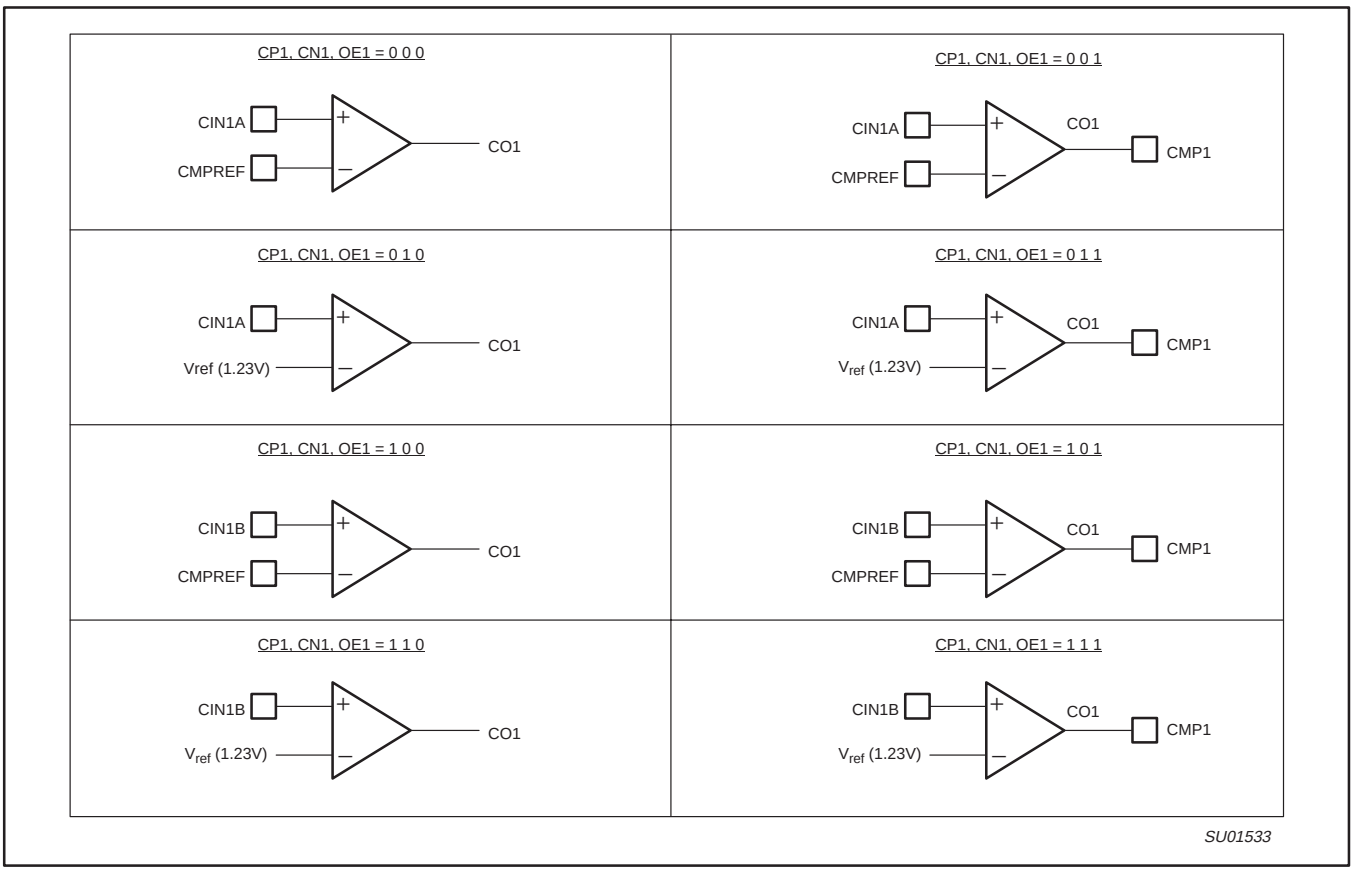


Figure 4. Comparator Configurations

I2CFG Address: C8h Reset Value: 00h

Bit Addressable

7	6	5	4	3	2	1	0
SLAVEN	MASTRQ	CLRTI	TIRUN	—	—	CT1	CT0

BIT	SYMBOL	FUNCTION
I2CFG.7	SLAVEN	Slave Enable. Writing a 1 this bit enables the slave functions of the I^2C subsystem. If SLAVEN and MASTRQ are 0, the I^2C hardware is disabled. This bit is cleared to 0 by reset and by an I^2C time-out.
I2CFG.6	MASTRQ	Master Request. Writing a 1 to this bit requests mastership of the I^2C bus. If a transmission is in progress when this bit is changed from 0 to 1, action is delayed until a stop condition is detected. A start condition is sent and DRDY is set (thus making ATN = 1 and generating an I^2C interrupt). When a master wishes to release mastership status of the I^2C, it writes a 1 to XSTP in I2CON. MASTRQ is cleared by an I^2C time-out.
I2CFG.5	CLRTI	Writing a 1 to this bit clears the Timer I overflow flag. This bit position always reads as a 0.
I2CFG.4	TIRUN	Writing a 1 to this bit lets Timer I run; a zero stops and clears it. Together with SLAVEN, MASTRQ, and MASTER, this bit determines operational modes as shown in Table 1.
I2CFG.2, 3	—	Reserved for future use. Should not be set to 1 by user programs.
I2CFG.1, 0	CT1, CT0	These two bits are programmed as a function of the CPU clock rate, to optimize the MIN HI and LO time of SCL when this device is a master on the I^2C. The time value determined by these bits controls both of these parameters, and also the timing for stop and start conditions.

SU01552

Figure 8. I^2C Configuration Register (I2CFG)

Regarding Software Response Time

Because the P87LPC760 can run at 20 MHz, and because the I^2C interface is optimized for high-speed operation, it is quite likely that an I^2C service routine will sometimes respond to DRDY (which is set at a rising edge of SCL) and write I2DAT before SCL has gone low again. If XDAT were applied directly to SDA, this situation would produce an I^2C protocol violation. The programmer need not worry about this possibility because XDAT is applied to SDA only when SCL is low.

Conversely, a program that includes an I^2C service routine may take a long time to respond to DRDY. Typically, an I^2C routine operates on a flag-polling basis during a message, with interrupts from other peripheral functions enabled. If an interrupt occurs, it will delay the response of the I^2C service routine. The programmer need not worry about this very much either, because the I^2C hardware stretches the SCL low time until the service routine responds. The only constraint on the response is that it must not exceed the Timer I time-out.

Values to be used in the CT1 and CT0 bits are shown in Table 2. To allow the I^2C bus to run at the maximum rate for a particular oscillator frequency, compare the actual oscillator rate to the f OSC max column in the table. The value for CT1 and CT0 is found in the first line of the table where CPU clock max is greater than or equal to the actual frequency.

Table 2 also shows the machine cycle count for various settings of CT1/CT0. This allows calculation of the actual minimum high and low times for SCL as follows:

$$\text{SCL min high/low time in microseconds} = \frac{6 * \text{Min Time Count}}{\text{CPU clock in MHz}}$$

For instance, at an 8 MHz frequency, with CT1/CT0 set to 1 0, the minimum SCL high and low times will be 5.25 μs.

Table 2 also shows the Timer I timeout period (given in machine cycles) for each CT1/CT0 combination. The timeout period varies because of the way in which minimum SCL high and low times are measured. When the I^2C interface is operating, Timer I is pre-loaded at every SCL transition with a value dependent upon CT1/CT0. The pre-load value is chosen such that a minimum SCL high or low time has elapsed when Timer I reaches a count of 008 (the actual value pre-loaded into Timer I is 8 minus the machine cycle count).

Table 1. Interaction of TIRUN with SLAVEN, MASTRQ, and MASTER

SLAVEN, MASTRQ, MASTER	TIRUN	OPERATING MODE
All 0	0	The I^2C interface is disabled. Timer I is cleared and does not run. This is the state assumed after a reset. If an I^2C application wants to ignore the I^2C at certain times, it should write SLAVEN, MASTRQ, and TIRUN all to zero.
All 0	1	The I^2C interface is disabled.
Any or all 1	0	The I^2C interface is enabled. The 3 low-order bits of Timer I run for min-time generation, but the hi-order bits do not, so that there is no checking for I^2C being “hung.” This configuration can be used for very slow I^2C operation.
Any or all 1	1	The I^2C interface is enabled. Timer I runs during frames on the I^2C, and is cleared by transitions on SCL, and by Start and Stop conditions. This is the normal state for I^2C operation.

Table 2. CT1, CT0 Values

CT1, CT0	Min Time Count (Machine Cycles)	CPU Clock Max (for 100 kHz I^2C)	Timeout Period (Machine Cycles)
1 0	7	8.4 MHz	1023
0 1	6	7.2 MHz	1022
0 0	5	6.0 MHz	1021
1 1	4	4.8 MHz	1020

Interrupts

The P87LPC760 uses a four priority level interrupt structure. This allows great flexibility in controlling the handling of the P87LPC760’s many interrupt sources. The P87LPC760 supports up to 10 interrupt sources.

Each interrupt source can be individually enabled or disabled by setting or clearing a bit in registers IEN0 or IEN1. The IEN0 register also contains a global disable bit, EA, which disables all interrupts at once.

Each interrupt source can be individually programmed to one of four priority levels by setting or clearing bits in the IP0, IP0H, IP1, and IP1H registers. An interrupt service routine in progress can be interrupted by a higher priority interrupt, but not by another interrupt of the same or lower priority. The highest priority interrupt service cannot be interrupted by any other interrupt source. So, if two requests of different priority levels are received simultaneously, the request of higher priority level is serviced.

If requests of the same priority level are received simultaneously, an internal polling sequence determines which request is serviced. This is called the arbitration ranking. Note that the arbitration ranking is only used to resolve simultaneous requests of the same priority level.

Table 3 summarizes the interrupt sources, flag bits, vector addresses, enable bits, priority bits, arbitration ranking, and whether each interrupt may wake up the CPU from Power Down mode.

Table 3. Summary of Interrupts

Description	Interrupt Flag Bit(s)	Vector Address	Interrupt Enable Bit(s)	Interrupt Priority	Arbitration Ranking	Power Down Wakeup
External Interrupt 0	IE0	0003h	EX0 (IEN0.0)	IP0H.0, IP0.0	1 (highest)	Yes
Timer 0 Interrupt	TF0	000Bh	ET0 (IEN0.1)	IP0H.1, IP0.1	4	No
Timer 1 Interrupt	TF1	001Bh	ET1 (IEN0.3)	IP0H.3, IP0.3	8	No
Serial Port Tx and Rx	TI & RI	0023h	ES (IEN0.4)	IP0H.4, IP0.4	9	No
Brownout Detect	BOF	002Bh	EBO (IEN0.5)	IP0H.5, IP0.5	2	Yes
I^2C Interrupt	ATN	0033h	EI2 (IEN1.0)	IP1H.0, IP1.0	5	No
KBI Interrupt	KBF	003Bh	EKB (IEN1.1)	IP1H.1, IP1.1	6	Yes
Watchdog Timer	WDOVF	0053h	EWD (IEN0.6)	IP0H.6, IP0.6	3	Yes
Comparator 1 interrupt	CMF1	0063h	EC1 (IEN1.5)	IP1H.5, IP1.5	7	Yes
Timer I interrupt	–	0073h	ETI (IEN1.7)	IP1H.7, IP1.7	10 (lowest)	No

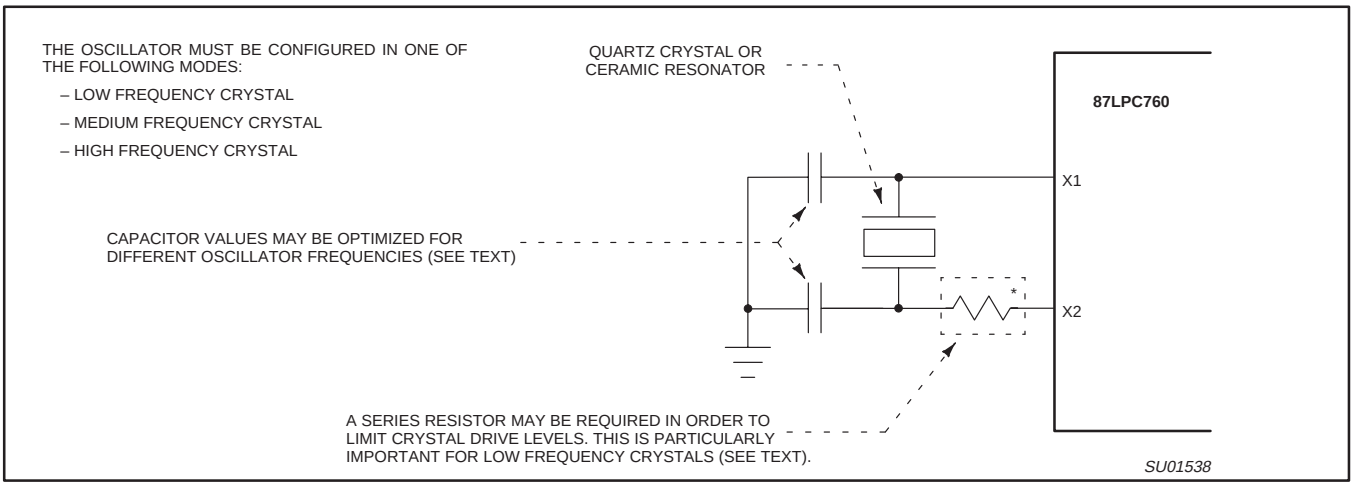


Figure 16. Using the Crystal Oscillator

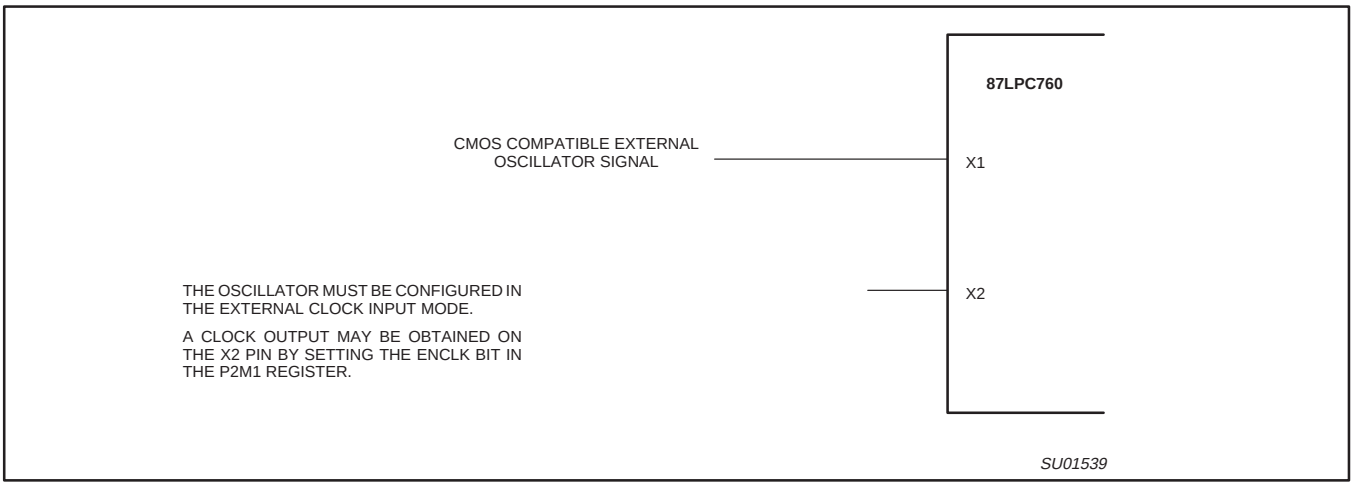


Figure 17. Using an External Clock Input

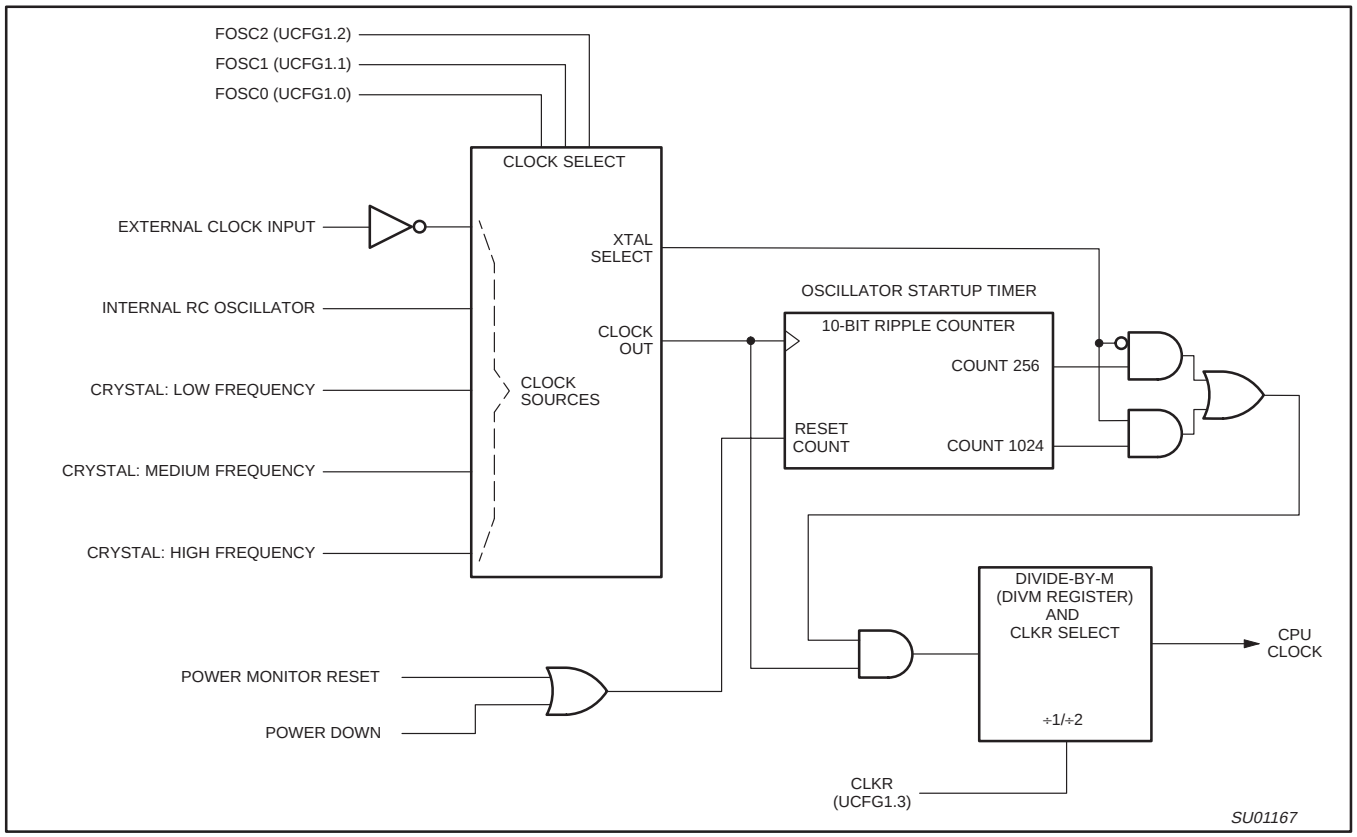


Figure 18. Block Diagram of Oscillator Control

CPU Clock Modification: CLKR and DIVM

For backward compatibility, the CLKR configuration bit allows setting the P87LPC760 instruction and peripheral timing to match standard 80C51 timing by dividing the CPU clock by two. Default timing for the P87LPC760 is 6 CPU clocks per machine cycle while standard 80C51 timing is 12 clocks per machine cycle. This division also applies to peripheral timing, allowing 80C51 code that is oscillator frequency and/or timer rate dependent. The CLKR bit is located in the EPROM configuration register UCFG1, described under EPROM Characteristics

In addition to this, the CPU clock may be divided down from the oscillator rate by a programmable divider, under program control. This function is controlled by the DIVM register. If the DIVM register is set to zero (the default value), the CPU will be clocked by either the unmodified oscillator rate, or that rate divided by two, as determined by the previously described CLKR function.

When the DIVM register is set to some value N (between 1 and 255), the CPU clock is divided by 2 * (N + 1). Clock division values from 4 through 512 are thus possible. This feature makes it possible to temporarily run the CPU at a lower rate, reducing power consumption, in a manner similar to Idle mode. By dividing the clock, the CPU can retain the ability to respond to events other than those that can cause interrupts (i.e. events that allow exiting the Idle mode) by executing its normal program at a lower rate. This can allow bypassing the oscillator startup time in cases where Power Down mode would otherwise be used. The value of DIVM may be changed by the program at any time without interrupting code execution.

Power Monitoring Functions

The P87LPC760 incorporates power monitoring functions designed to prevent incorrect operation during initial power up and power loss or reduction during operation. This is accomplished with two hardware functions: Power-On Detect and Brownout Detect.

Brownout Detection

The Brownout Detect function allows preventing the processor from failing in an unpredictable manner if the power supply voltage drops below a certain level. The default operation is for a brownout detection to cause a processor reset, however it may alternatively be configured to generate an interrupt by setting the BOI bit in the AUXR1 register (AUXR1.5).

The P87LPC760 allows selection of two Brownout levels: 2.5 V or 3.8 V. When V_{DD} drops below the selected voltage, the brownout detector triggers and remains active until V_{DD} is returns to a level above the Brownout Detect voltage. When Brownout Detect causes a processor reset, that reset remains active as long as V_{DD} remains below the Brownout Detect voltage. When Brownout Detect generates an interrupt, that interrupt occurs once as V_{DD} crosses from above to below the Brownout Detect voltage. For the interrupt to be processed, the interrupt system and the BOI interrupt must both be enabled (via the EA and EBO bits in IEN0).

When Brownout Detect is activated, the BOF flag in the PCON register is set so that the cause of processor reset may be determined by software. This flag will remain set until cleared by software.

Table 8. Sources of Wakeup from Power Down Mode

Wakeup Source	Conditions
External Interrupt 0	The interrupt must be enabled.
Keyboard Interrupt	The keyboard interrupt feature must be enabled and properly set up. The corresponding interrupt must be enabled.
Comparator 1	The comparator must be enabled and properly set up. The corresponding interrupt must be enabled.
Watchdog Timer Reset	The watchdog timer must be enabled via the WDTE bit in the UCFG1 EPROM configuration byte.
Watchdog Timer Interrupt	The WDTE bit in the UCFG1 EPROM configuration byte must not be set. The corresponding interrupt must be enabled.
Brownout Detect Reset	The BOD bit in AUXR1 must not be set (brownout detect not disabled). The BOI bit in AUXR1 must not be set (brownout interrupt disabled).
Brownout Detect Interrupt	The BOD bit in AUXR1 must not be set (brownout detect not disabled). The BOI bit in AUXR1 must be set (brownout interrupt enabled). The corresponding interrupt must be enabled.
Reset Input	The external reset input must be enabled.

Low Voltage EPROM Operation

The EPROM array contains some analog circuits that are not required when V_{DD} is less than 4 V, but are required for a V_{DD} greater than 4 V. The LPEP bit (AUXR.4), when set by software, will power down these analog circuits resulting in a reduced supply current. LPEP is cleared only by power-on reset, so it may be set ONLY for applications that always operate with V_{DD} less than 4 V.

Reset

The P87LPC760 has an integrated power-on reset circuit which always provides a reset when power is initially applied to the device. It is recommended to use the internal reset whenever possible to save external components and to be able to use pin P1.5 as a general-purpose input pin.

The P87LPC760 can additionally be configured to use P1.5 as an external active-low reset pin $\overline{RST}$ by programming the RPD bit in the User Configuration Register UCFG1 to 0. The internal reset is still active on power-up of the device. While the signal on the $\overline{RST}$ pin is low, the P87LPC760 is held in reset until the signal goes high.

The watchdog timer on the P87LPC760 can act as an oscillator fail detect because it uses an independent, fully on-chip oscillator.

UCFG1 is described in the System Configuration Bytes section of this datasheet.

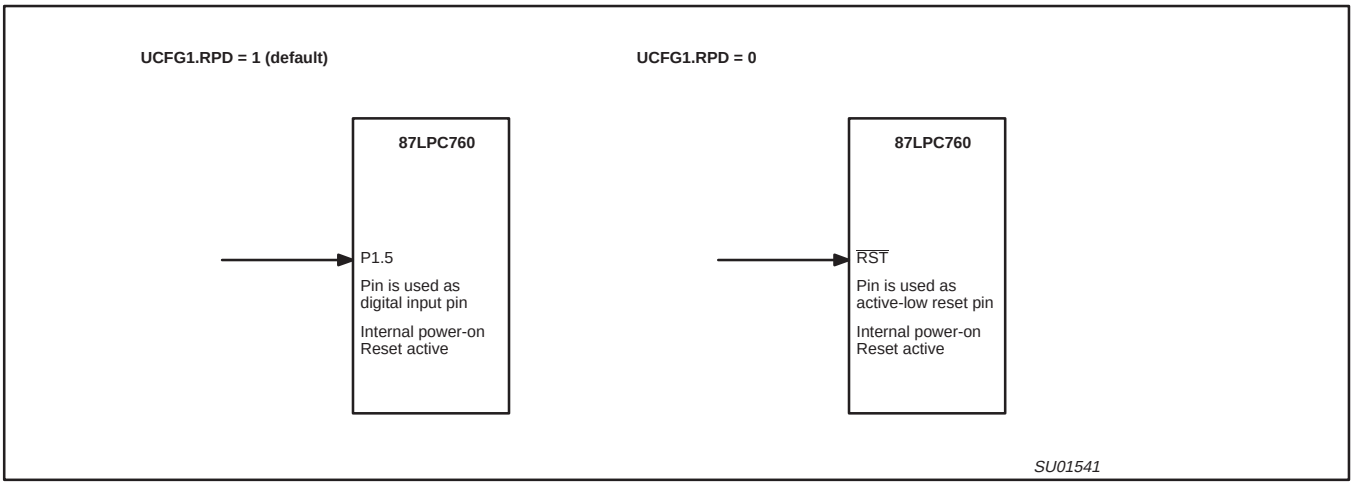


Figure 20. Using pin P1.5 as general purpose input pin or as low-active reset pin

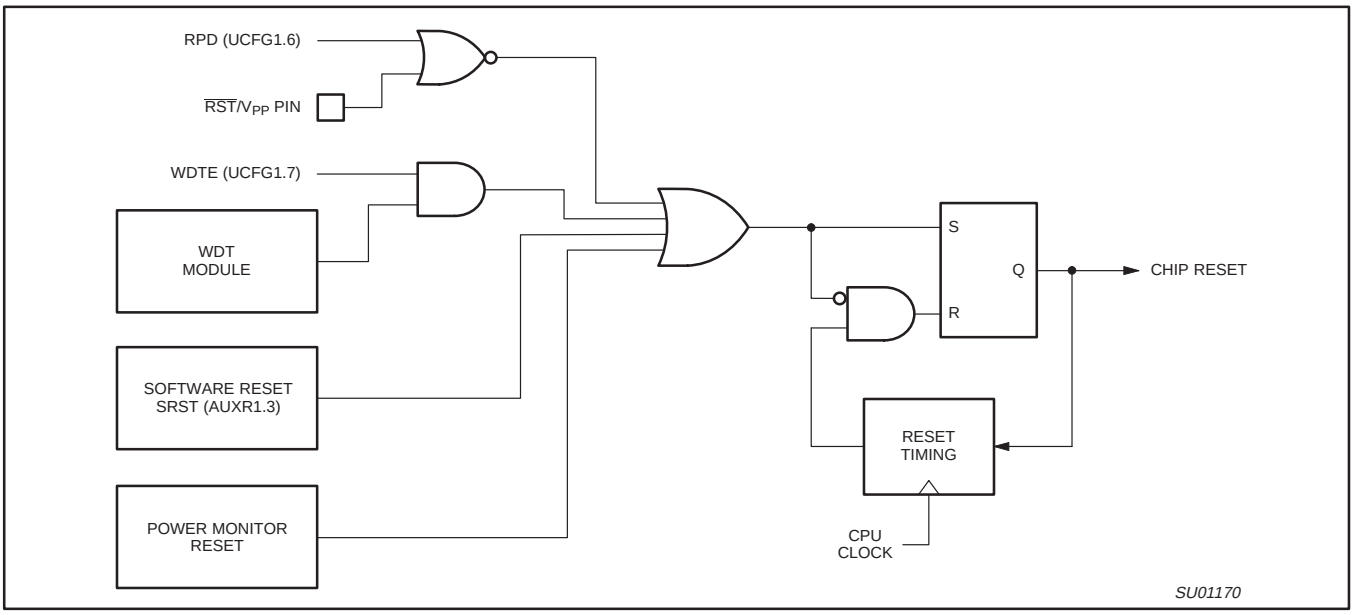


Figure 21. Block Diagram Showing Reset Sources

Timer/Counters

The P87LPC760 has two general purpose counter/timers which are upward compatible with the standard 80C51 Timer 0 and Timer 1. Both can be configured to operate as timers or can be configured to be an event counter (see Figure 22). An option to automatically toggle the T0 pin upon timer overflow has been added.

In the “Timer” function, the register is incremented every machine cycle. Thus, one can think of it as counting machine cycles. Since a machine cycle consists of 6 CPU clock periods, the count rate is 1/6 of the CPU clock frequency. Refer to the section Enhanced CPU for a description of the CPU clock.

In the “Counter” function of Timer 0, the register is incremented in response to a 1-to-0 transition at its corresponding external input pin, T0. In this function, the external input is sampled once during every machine cycle. When the samples of the pin state show a high in one cycle and a low in the next cycle, the count is incremented. The new count value appears in the register during the cycle following the one in which the transition was detected. Since it takes 2 machine cycles (12 CPU clocks) to recognize a 1-to-0 transition, the maximum count rate is 1/6 of the CPU clock frequency. There are no restrictions on the duty cycle of the external input signal, but to ensure that a given level is sampled at least once before it changes, it should be held for at least one full machine cycle.

The “Timer” or “Counter” function of Timer 0 is selected by control bit C/$\overline{T}$ in the Special Function Register TMOD. In addition to the “Timer” or “Counter” selection, Timer 0 and Timer 1 have four operating modes, which are selected by bit-pairs (M1, M0) in TMOD. Modes 0, 1, and 2 are the same for both Timers/Counters. Mode 3 is different. The four operating modes are described in the following text.

TMOD Address: 89h Reset Value: 00h

Not Bit Addressable

7	6	5	4	3	2	1	0
–	–	M1	M0	GATE	C/$\overline{T}$	M1	M0
		T1		T0			

BIT	SYMBOL	FUNCTION
TMOD.7, 6	–	Reserved. Must be written with zeros only.
TMOD.5, 4	M1, M0	Mode Select for Timer 1 (see table below).
TMOD.3	GATE	Gating control for Timer 0. When set, Timer/Counter is enabled only while the $\overline{INT0}$ pin is high and the TR0 control pin is set. When cleared, Timer 0 is enabled when the TR0 control bit is set.
TMOD.2	C/$\overline{T}$	Timer or Counter Selector for Timer 0. Cleared for Timer operation (input from internal system clock.) Set for Counter operation (input from T0 input pin).
TMOD.1, 0	M1, M0	Mode Select for Timer 0 (see table below).
	M1, M0	Timer Mode
	0 0	8048 Timer “TLn” serves as 5-bit prescaler.
	0 1	16-bit Timer/Counter “THn” and “TLn” are cascaded; there is no prescaler.
	1 0	8-bit auto-reload Timer/Counter. THn holds a value which is loaded into TLn when it overflows.
	1 1	Timer 0 is a dual 8-bit Timer/Counter in this mode. TL0 is an 8-bit Timer/Counter controlled by the standard Timer 0 control bits. TH0 is an 8-bit timer only, controlled by the Timer 1 control bits (see text). Timer 1 in this mode is stopped.

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Figure 22. Timer/Counter Mode Control Register (TMOD)

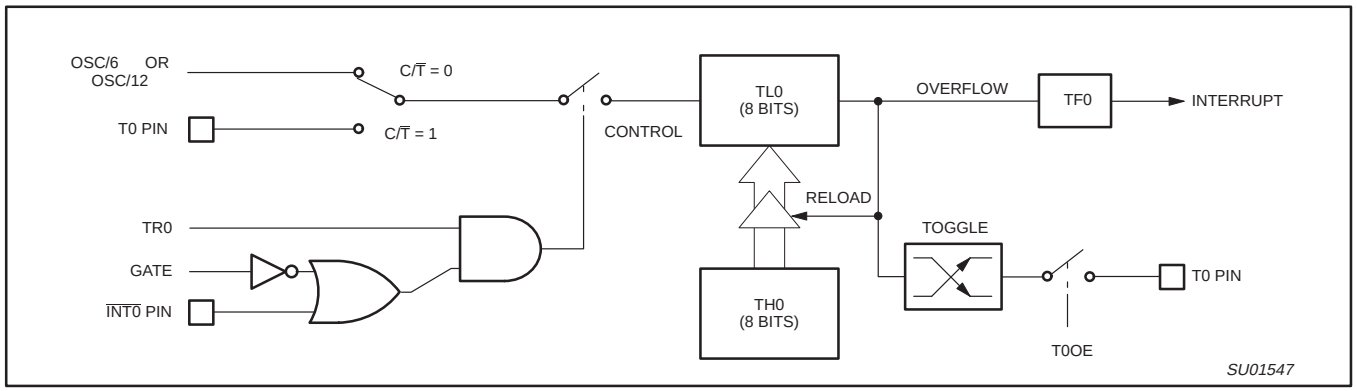

Figure 28. Timer/Counter 0 in Mode 2 (8-Bit Auto-Reload)

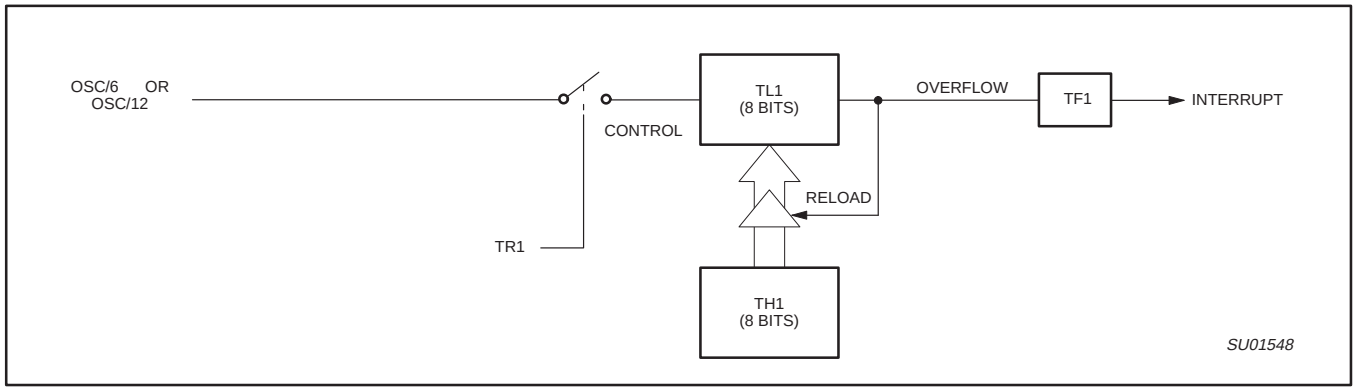

Figure 29. Timer 1 in Mode 2 (8-Bit Auto-Reload)

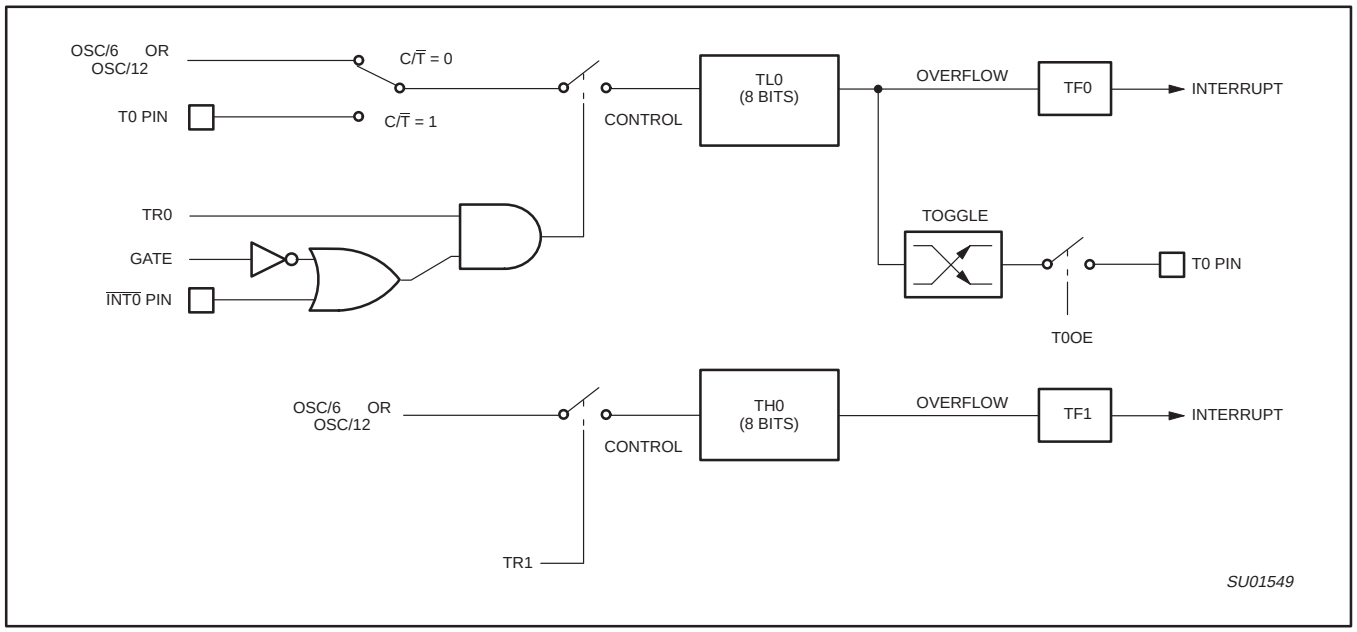

Figure 30. Timer/Counter 0 Mode 3 (Two 8-Bit Timer/Counters)

Table 9. Baud Rates, Timer Values, and CPU Clock Frequencies for SMOD1 = 0

Timer Count	Baud Rate					
	2400	4800	9600	19.2k	38.4k	57.6k
–1	0.4608	0.9216	* 1.8432	* 3.6864	* 7.3728	* 11.0592
–2	0.9216	1.8432	* 3.6864	* 7.3728	* 14.7456	
–3	1.3824	2.7648	5.5296	* 11.0592	–	–
–4	* 1.8432	* 3.6864	* 7.3728	* 14.7456	–	–
–5	2.3040	4.6080	9.2160	* 18.4320	–	–
–6	2.7648	5.5296	* 11.0592	–	–	–
–7	3.2256	6.4512	12.9024	–	–	–
–8	* 3.6864	* 7.3728	* 14.7456	–	–	–
–9	4.1472	8.2944	16.5888	–	–	–
–10	4.6080	9.2160	* 18.4320	–	–	–

Table 10. Baud Rates, Timer Values, and CPU Clock Frequencies for SMOD1 = 1

Timer Count	Baud Rate						
	2400	4800	9600	19.2 k	38.4 k	57.6 k	115.2 k
–1	0.2304	0.4608	0.9216	* 1.8432	* 3.6864	5.5296	* 11.0592
–2	0.4608	0.9216	* 1.8432	* 3.6864	* 7.3728	* 11.0592	–
–3	0.6912	1.3824	2.7648	5.5296	* 11.0592	16.5888	–
–4	0.9216	* 1.8432	* 3.6864	* 7.3728	* 14.7456	–	–
–5	1.1520	2.3040	4.6080	9.2160	* 18.4320	–	–
–6	1.3824	2.7648	5.5296	* 11.0592	–	–	–
–7	1.6128	3.2256	6.4512	12.9024	–	–	–
–8	* 1.8432	* 3.6864	* 7.3728	* 14.7456	–	–	–
–9	2.0736	4.1472	8.2944	16.5888	–	–	–
–10	2.3040	4.6080	9.2160	* 18.4320	–	–	–
–11	2.5344	5.0688	10.1376	–	–	–	–
–12	2.7648	5.5296	* 11.0592	–	–	–	–
–13	2.9952	5.9904	11.9808	–	–	–	–
–14	3.2256	6.4512	12.9024	–	–	–	–
–15	3.4560	6.9120	13.8240	–	–	–	–
–16	* 3.6864	* 7.3728	* 14.7456	–	–	–	–
–17	3.9168	7.8336	15.6672	–	–	–	–
–18	4.1472	8.2944	16.5888	–	–	–	–
–19	4.3776	8.7552	17.5104	–	–	–	–
–20	4.6080	9.2160	* 18.4320	–	–	–	–
–21	4.8384	9.6768	19.3536	–	–	–	–

NOTES TO TABLES 9 AND 10:

1. Tables 6 and 7 apply to UART modes 1 and 3 (variable rate modes), and show CPU clock rates in MHz for standard baud rates from 2400 to 115.2k baud.
2. Table 6 shows timer settings and CPU clock rates with the SMOD1 bit in the PCON register = 0 (the default after reset), while Table 7 reflects the SMOD1 bit = 1.
3. The tables show all potential CPU clock frequencies up to 20 MHz that may be used for baud rates from 9600 baud to 115.2 k baud. Other CPU clock frequencies that would give only lower baud rates are not shown.
4. Table entries marked with an asterisk (*) indicate standard crystal and ceramic resonator frequencies that may be obtained from many sources without special ordering.

More About UART Mode 0

Serial data enters and exits through RxD. TxD outputs the shift clock. 8 bits are transmitted/received: 8 data bits (LSB first). The baud rate is fixed at 1/6 the CPU clock frequency. Figure 32 shows a simplified functional diagram of the serial port in Mode 0, and associated timing.

Transmission is initiated by any instruction that uses SBUF as a destination register. The “write to SBUF” signal at S6P2 also loads a 1 into the 9th position of the transmit shift register and tells the TX Control block to commence a transmission. The internal timing is such that one full machine cycle will elapse between “write to SBUF” and activation of SEND.

SEND enables the output of the shift register to the alternate output function line of P1.1 and also enable SHIFT CLOCK to the alternate output function line of P1.0. SHIFT CLOCK is low during S3, S4, and S5 of every machine cycle, and high during S6, S1, and S2. At S6P2 of every machine cycle in which SEND is active, the contents of the transmit shift are shifted to the right one position.

As data bits shift out to the right, zeros come in from the left. When the MSB of the data byte is at the output position of the shift register, then the 1 that was initially loaded into the 9th position, is just to the left of the MSB, and all positions to the left of that contain zeros. This condition flags the TX Control block to do one last shift and then deactivate SEND and set T1. Both of these actions occur at S1P1 of the 10th machine cycle after “write to SBUF.” Reception is initiated by the condition REN = 1 and R1 = 0. At S6P2 of the next machine cycle, the RX Control unit writes the bits 11111110 t o the receive shift register, and in the next clock phase activates RECEIVE.

RECEIVE enable SHIFT CLOCK to the alternate output function line of P1.0. SHIFT CLOCK makes transitions at S3P1 and S6P1 of every machine cycle. At S6P2 of every machine cycle in which RECEIVE is active, the contents of the receive shift register are shifted to the left one position. The value that comes in from the right is the value that was sampled at the P1.1 pin at S5P2 of the same machine cycle.

As data bits come in from the right, 1s shift out to the left. When the 0 that was initially loaded into the rightmost position arrives at the leftmost position in the shift register, it flags the RX Control block to do one last shift and load SBUF. At S1P1 of the 10th machine cycle after the write to SCON that cleared RI, RECEIVE is cleared as RI is set.

More About UART Mode 1

Ten bits are transmitted (through TxD), or received (through RxD): a start bit (0), 8 data bits (LSB first), and a stop bit (1). On receive, the stop bit goes into RB8 in SCON. In the P87LPC760 the baud rate is determined by the Timer 1 overflow rate. Figure 33 shows a simplified functional diagram of the serial port in Mode 1, and associated timings for transmit receive.

Transmission is initiated by any instruction that uses SBUF as a destination register. The “write to SBUF” signal also loads a 1 into the 9th bit position of the transmit shift register and flags the TX Control unit that a transmission is requested. Transmission actually commences at S1P1 of the machine cycle following the next rollover in the divide-by-16 counter. (Thus, the bit times are synchronized to the divide-by-16 counter, not to the “write to SBUF” signal.)

The transmission begins with activation of SEND, which puts the start bit at TxD. One bit time later, DATA is activated, which enables the output bit of the transmit shift register to TxD. The first shift pulse occurs one bit time after that.

As data bits shift out to the right, zeros are clocked in from the left. When the MSB of the data byte is at the output position of the shift register, then the 1 that was initially loaded into the 9th position is just to the left of the MSB, and all positions to the left of that contain zeros. This condition flags the TX Control unit to do one last shift and then deactivate SEND and set TI. This occurs at the 10th divide-by-16 rollover after “write to SBUF.”

Reception is initiated by a detected 1-to-0 transition at RxD. For this purpose RxD is sampled at a rate of 16 times whatever baud rate has been established. When a transition is detected, the divide-by-16 counter is immediately reset, and 1FFH is written into the input shift register. Resetting the divide-by-16 counter aligns its rollovers with the boundaries of the incoming bit times.

The 16 states of the counter divide each bit time into 16ths. At the 7th, 8th, and 9th counter states of each bit time, the bit detector samples the value of RxD. The value accepted is the value that was seen in at least 2 of the 3 samples. This is done for noise rejection. If the value accepted during the first bit time is not 0, the receive circuits are reset and the unit goes back to looking for another 1-to-0 transition. This is to provide rejection of false start bits. If the start bit proves valid, it is shifted into the input shift register, and reception of the rest of the frame will proceed.

As data bits come in from the right, 1s shift out to the left. When the start bit arrives at the leftmost position in the shift register (which in mode 1 is a 9-bit register), it flags the RX Control block to do one last shift, load SBUF and RB8, and set RI. The signal to load SBUF and RB8, and to set RI, will be generated if, and only if, the following conditions are met at the time the final shift pulse is generated: 1. R1 = 0, and 2. Either SM2 = 0, or the received stop bit = 1.

If either of these two conditions is not met, the received frame is irretrievably lost. If both conditions are met, the stop bit goes into RB8, the 8 data bits go into SBUF, and RI is activated. At this time, whether the above conditions are met or not, the unit goes back to looking for a 1-to-0 transition in RxD.

More About UART Modes 2 and 3

Eleven bits are transmitted (through TxD), or received (through RxD): a start bit (0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (1). On transmit, the 9th data bit (TB8) can be assigned the value of 0 or 1. On receive, the 9the data bit goes into RB8 in SCON. The baud rate is programmable to either 1/16 or 1/32 of the CPU clock frequency in Mode 2. Mode 3 may have a variable baud rate generated from Timer 1.

Figures 34 and 35 show a functional diagram of the serial port in Modes 2 and 3. The receive portion is exactly the same as in Mode 1. The transmit portion differs from Mode 1 only in the 9th bit of the transmit shift register.

Transmission is initiated by any instruction that uses SBUF as a destination register. The “write to SBUF” signal also loads TB8 into the 9th bit position of the transmit shift register and flags the TX Control unit that a transmission is requested. Transmission commences at S1P1 of the machine cycle following the next rollover in the divide-by-16 counter. (Thus, the bit times are synchronized to the divide-by-16 counter, not to the “write to SBUF” signal.)

The transmission begins with activation of SEND, which puts the start bit at TxD. One bit time later, DATA is activated, which enables the output bit of the transmit shift register to TxD. The first shift pulse occurs one bit time after that. The first shift clocks a 1 (the stop bit) into the 9th bit position of the shift register. Thereafter, only zeros are clocked in. Thus, as data bits shift out to the right, zeros are clocked in from the left. When TB8 is at the output position of the shift register, then the stop bit is just to the left of TB8, and all positions to the left of that contain zeros. This condition flags the TX Control unit to do one last shift and then deactivate SEND and set TI. This occurs at the 11th divide-by-16 rollover after “write to SBUF.”

Reception is initiated by a detected 1-to-0 transition at RxD. For this purpose RxD is sampled at a rate of 16 times whatever baud rate has been established. When a transition is detected, the divide-by-16 counter is immediately reset, and 1FFH is written to the input shift register.

At the 7th, 8th, and 9th counter states of each bit time, the bit detector samples the value of R–D. The value accepted is the value that was seen in at least 2 of the 3 samples. If the value accepted during the first bit time is not 0, the receive circuits are reset and the unit goes back to looking for another 1-to-0 transition. If the start bit proves valid, it is shifted into the input shift register, and reception of the rest of the frame will proceed.

As data bits come in from the right, 1s shift out to the left. When the start bit arrives at the leftmost position in the shift register (which in Modes 2 and 3 is a 9-bit register), it flags the RX Control block to do one last shift, load SBUF and RB8, and set RI.

The signal to load SBUF and RB8, and to set RI, will be generated if, and only if, the following conditions are met at the time the final shift pulse is generated. 1. RI = 0, and 2. Either SM2 = 0, or the received 9th data bit = 1.

If either of these conditions is not met, the received frame is irretrievably lost, and RI is not set. If both conditions are met, the received 9th data bit goes into RB8, and the first 8 data bits go into SBUF. One bit time later, whether the above conditions were met or not, the unit goes back to looking for a 1-to-0 transition at the RxD input.

Multiprocessor Communications

UART modes 2 and 3 have a special provision for multiprocessor communications. In these modes, 9 data bits are received or transmitted. When data is received, the 9th bit is stored in RB8. The UART can be programmed such that when the stop bit is received, the serial port interrupt will be activated only if RB8 = 1. This feature is enabled by setting bit SM2 in SCON. One way to use this feature in multiprocessor systems is as follows:

When the master processor wants to transmit a block of data to one of several slaves, it first sends out an address byte which identifies the target slave. An address byte differs from a data byte in that the 9th bit is 1 in an address byte and 0 in a data byte. With SM2 = 1, no slave will be interrupted by a data byte. An address byte, however, will interrupt all slaves, so that each slave can examine the received byte and see if it is being addressed. The addressed slave will clear its SM2 bit and prepare to receive the data bytes that follow. The slaves that weren’t being addressed leave their SM2 bits set and go on about their business, ignoring the subsequent data bytes.

SM2 has no effect in Mode 0, and in Mode 1 can be used to check the validity of the stop bit, although this is better done with the Framing Error flag. In a Mode 1 reception, if SM2 = 1, the receive interrupt will not be activated unless a valid stop bit is received.

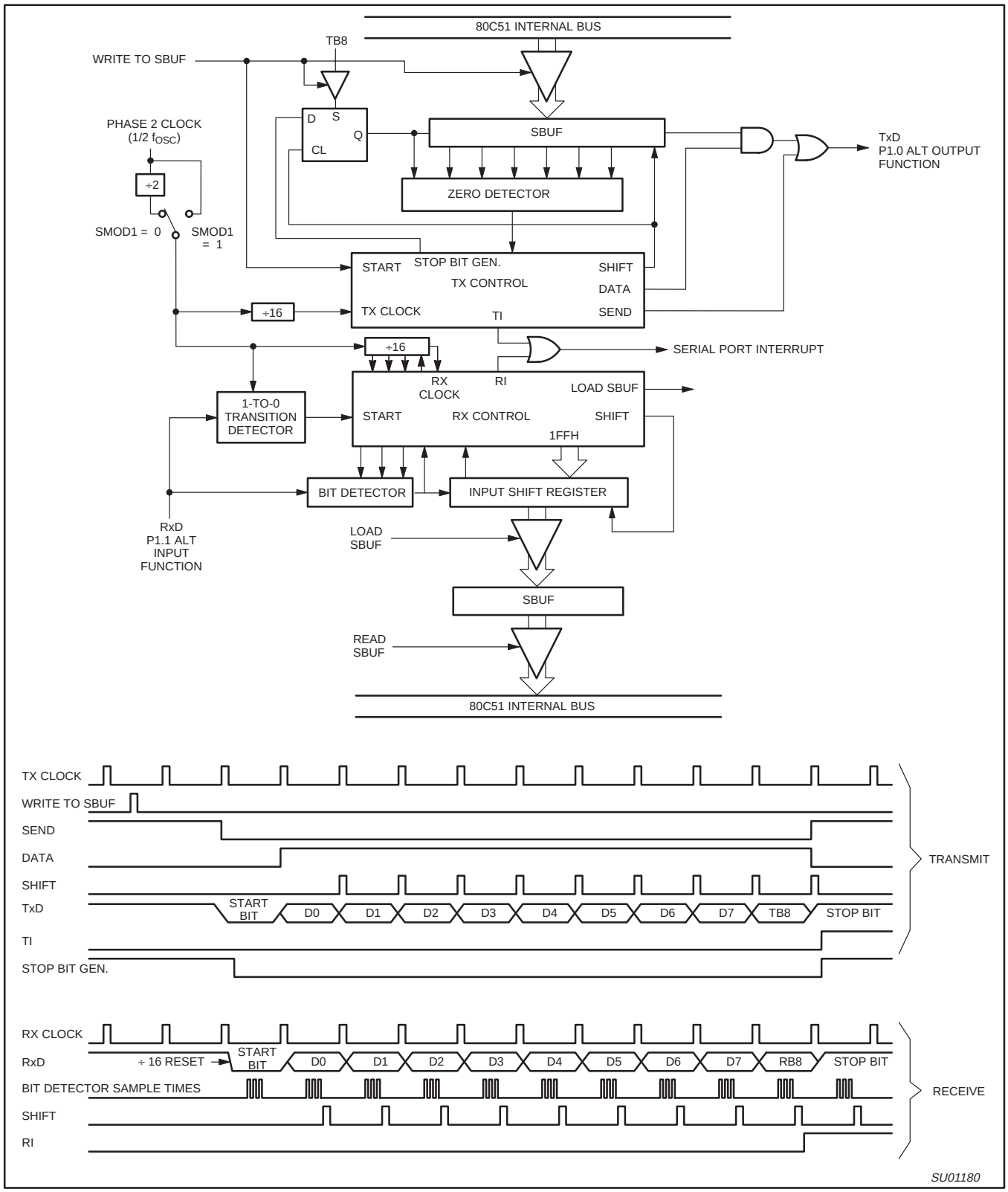

Figure 34. Serial Port Mode 2

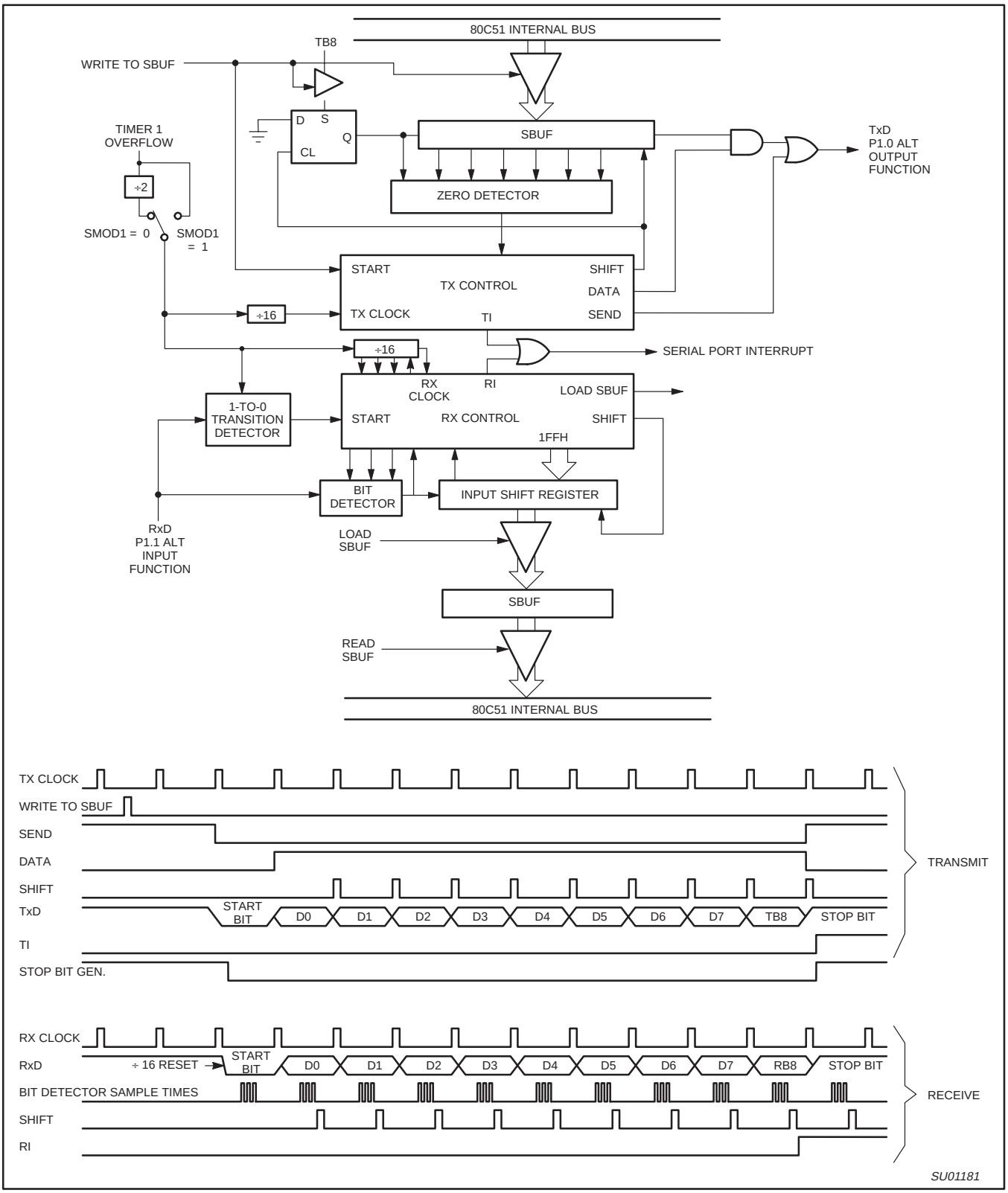

Figure 35. Serial Port Mode 3

Additional Features

The AUXR1 register contains several special purpose control bits that relate to several chip features. AUXR1 is described in Figure 38.

Software Reset

The SRST bit in AUXR1 allows software the opportunity to reset the processor completely, as if an external reset or watchdog reset had occurred. If a value is written to AUXR1 that contains a 1 at bit position 3, all SFRs will be initialized and execution will resume at program address 0000. Care should be taken when writing to AUXR1 to avoid accidental software resets.

Dual Data Pointers

The dual Data Pointer (DPTR) adds to the ways in which the processor can specify the address used with certain instructions. The DPS bit in the AUXR1 register selects one of the two Data Pointers. The DPTR that is not currently selected is not accessible to software unless the DPS bit is toggled.

Specific instructions affected by the Data Pointer selection are:

- INC DPTR — Increments the Data Pointer by 1.
- JMP @A+DPTR — Jump indirect relative to DPTR value.
- MOV DPTR, #data16 — Load the Data Pointer with a 16-bit constant.
- MOVC A, @A+DPTR — Move code byte relative to DPTR to the accumulator.
- MOVX A, @DPTR — Move data byte the accumulator to data memory relative to DPTR.
- MOVX @DPTR, A — Move data byte from data memory relative to DPTR to the accumulator.

Also, any instruction that reads or manipulates the DPH and DPL registers (the upper and lower bytes of the current DPTR) will be affected by the setting of DPS. The MOVX instructions have limited application for the P87LPC760 since the part does not have an external data bus. However, they may be used to access EPROM configuration information (see EPROM Characteristics section).

Bit 2 of AUXR1 is permanently wired as a logic 0. This is so that the DPS bit may be toggled (thereby switching Data Pointers) simply by incrementing the AUXR1 register, without the possibility of inadvertently altering other bits in the register.

AUXR1 Address: A2h Reset Value: 00h

Not Bit Addressable

7	6	5	4	3	2	1	0
KBF	BOD	BOI	LPEP	SRST	0	—	DPS

BIT	SYMBOL	FUNCTION
AUXR1.7	KBF	Keyboard Interrupt Flag. Set when any pin of port 0 that is enabled for the Keyboard Interrupt function goes low. Must be cleared by software.
AUXR1.6	BOD	Brown Out Disable. When set, turns off brownout detection and saves power. See Power Monitoring Functions section for details.
AUXR1.5	BOI	Brown Out Interrupt. When set, prevents brownout detection from causing a chip reset and allows the brownout detect function to be used as an interrupt. See the Power Monitoring Functions section for details.
AUXR1.4	LPEP	Low Power EPROM control bit. Allows power savings in low voltage systems. Set by software. Can only be cleared by power-on or brownout reset. See the Power Reduction Modes section for details.
AUXR1.3	SRST	Software Reset. When set by software, resets the 87LPC760 as if a hardware reset occurred.
AUXR1.2	—	This bit contains a hard-wired 0. Allows toggling of the DPS bit by incrementing AUXR1, without interfering with other bits in the register.
AUXR1.1	—	Reserved for future use. Should not be set to 1 by user programs.
AUXR1.0	DPS	Data Pointer Select. Chooses one of two Data Pointers for use by the program. See text for details.

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Figure 38. AUXR1 Register

EPROM Characteristics

Programming of the EPROM on the P87LPC760 is accomplished with a serial programming method. Commands, addresses, and data are transmitted to and from the device on two pins after programming mode is entered. Serial programming allows easy implementation of In-System Programming of the P87LPC760 in an application board. Details of In-System Programming can be found in application note AN466.

The P87LPC760 contains three signature bytes that can be read and used by an EPROM programming system to identify the device. The signature bytes designate the device as an P87LPC760 manufactured by Philips. The signature bytes may be read by the user program at addresses FC30h, FC31h and FC60h with the MOVC instruction, using the DPTR register for addressing.

A special user data area is also available for access via the MOVC instruction at addresses FCE0h through FCFFh. This “customer code” space is programmed in the same manner as the main code EPROM and may be used to store a serial number, manufacturing date, or other application information.

32-Byte Customer Code Space

A small supplemental EPROM space is reserved for use by the customer in order to identify code revisions, store checksums, add a serial number to each device, or any other desired use. This area exists in the code memory space from addresses FCE0h through FCFFh. Code execution from this space is not supported, but it may be read as data through the use of the MOVC instruction with the appropriate addresses. The memory may be programmed at the same time as the rest of the code memory and UCFG bytes are programmed.

System Configuration Bytes

A number of user configurable features of the P87LPC760 must be defined at power up and therefore cannot be set by the program after start of execution. Those features are configured through the use of two EPROM bytes that are programmed in the same manner as the EPROM program space. The contents of the two configuration bytes, UCFG1 and UCFG2, are shown in Figures 39 and 40. The values of these bytes may be read by the program through the use of the MOVX instruction at the addresses shown in the figure.

UCFG1 Address: FD00h Unprogrammed Value: FFh

7	6	5	4	3	2	1	0
WDTE	RPD	PRHI	BOV	CLKR	FOSC2	FOSC1	FOSC0

BIT	SYMBOL	FUNCTION
UCFG1.7	WDTE	Watchdog timer enable. When programmed (0), disables the watchdog timer. The timer may still be used to generate an interrupt.
UCFG1.6	RPD	Reset pin disable. When 1 disables the reset function of pin P1.5, allowing it to be used as an input only port pin.
UCFG1.5	PRHI	Port reset high. When 1, ports reset to a high state. When 0, ports reset to a low state.
UCFG1.4	BOV	Brownout voltage select. When 1, the brownout detect voltage is 2.5V. When 0, the brownout detect voltage is 3.8V. This is described in the Power Monitoring Functions section.
UCFG1.3	CLKR	Clock rate select. When 0, the CPU clock rate is divided by 2. This results in machine cycles taking 12 CPU clocks to complete as in the standard 80C51. For full backward compatibility, this division applies to peripheral timing as well.
UCFG1.2–0	FOSC2–FSOC0	CPU oscillator type select. See Oscillator section for additional information. Combinations other than those shown below should not be used. They are reserved for future use.
	FOSC2–FOSC0	Oscillator Configuration
	1 1 1	External clock input on X1 (default setting for an unprogrammed part).
	0 1 1	Internal RC oscillator, 6 MHz. For tolerance, see AC Electrical Characteristics table.
	0 1 0	Low frequency crystal, 20 kHz to 100 kHz.
	0 0 1	Medium frequency crystal or resonator, 100 kHz to 4 MHz.
	0 0 0	High frequency crystal or resonator, 4 MHz to 20 MHz.

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Figure 39. EPROM System Configuration Byte 1 (UCFG1)

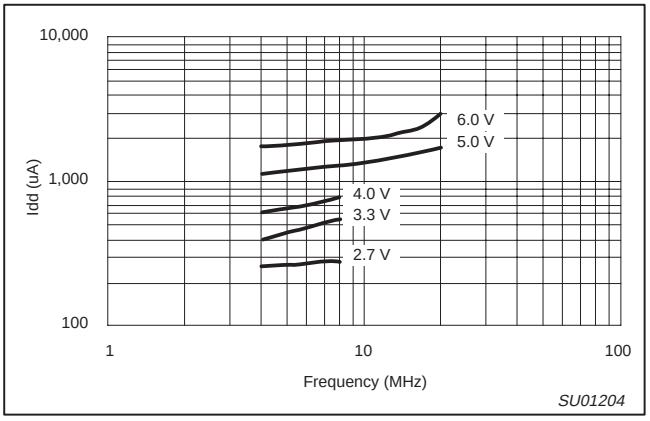

Figure 45. Typical Idd versus frequency (high frequency oscillator, 25 °C)

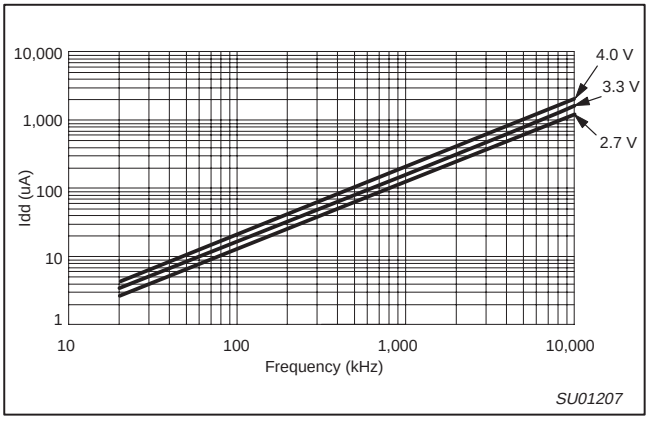

Figure 48. Typical Idle Idd versus frequency (external clock, 25 °C, LPEP=1)

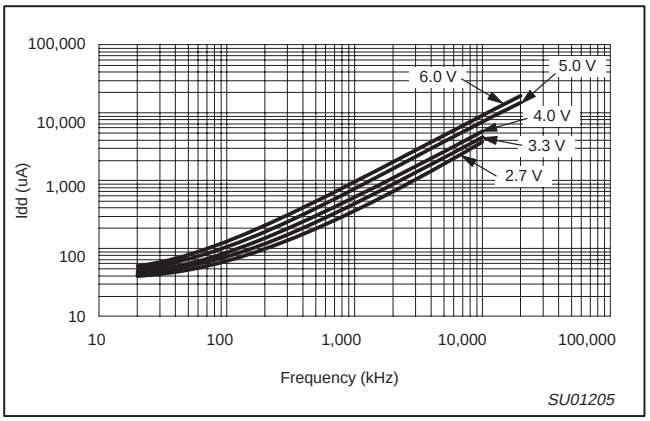

Figure 46. Typical Active Idd versus frequency (external clock, 25 °C, LPEP=0)

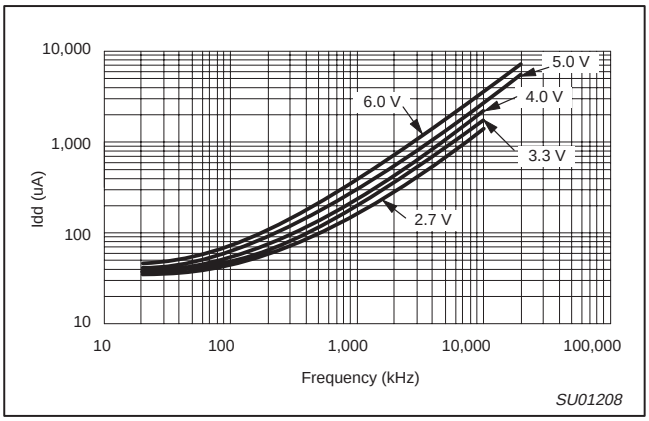

Figure 49. Typical Idle Idd versus frequency (external clock, 25 °C, LPEP=0)

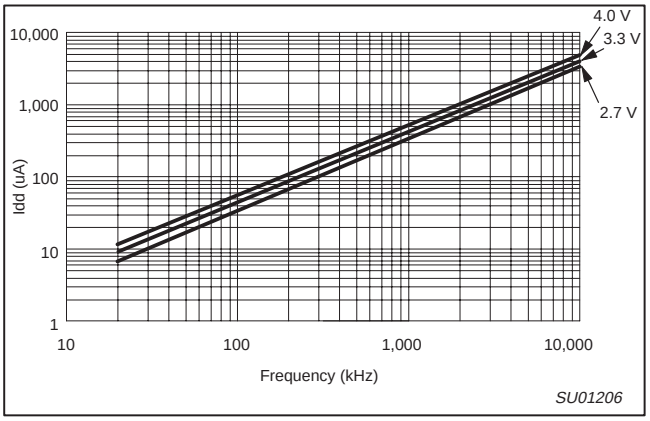

Figure 47. Typical Active Idd versus frequency (external clock, 25 °C, LPEP=1)