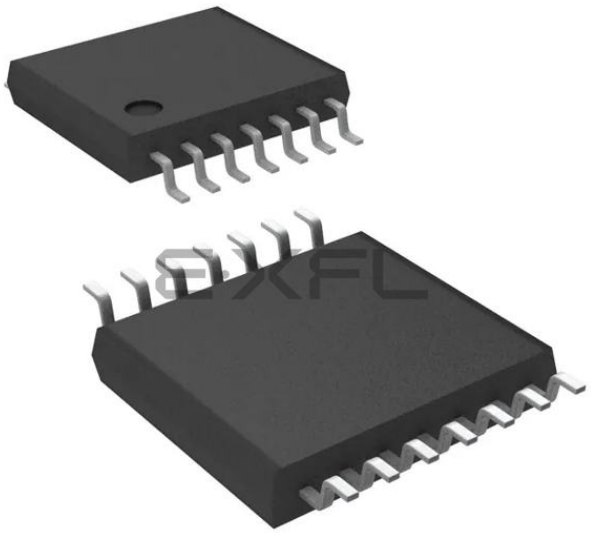

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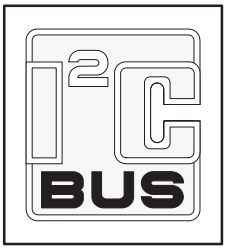
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	20MHz
Connectivity	I²C, UART/USART
Peripherals	Brown-out Detect/Reset, LED, POR, WDT
Number of I/O	12
Program Memory Size	1KB (1K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	14-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	14-TSSOP
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/p87lpc760bdh-118

Low power, low price, low pin count (14 pin) microcontroller with 1 kbyte OTP

P87LPC760



GENERAL DESCRIPTION

The P87LPC760 is a 14-pin single-chip microcontroller designed for low pin count applications demanding high-integration, low cost solutions over a wide range of performance requirements. A member of the Philips low pin count family, the P87LPC760 offers programmable oscillator configurations for high and low speed crystals or RC operation, wide operating voltage range, programmable port output configurations, selectable Schmitt trigger inputs, LED drive outputs, and a built-in watchdog timer. The P87LPC760 is based on an accelerated 80C51 processor architecture that executes instructions at twice the rate of standard 80C51 devices.

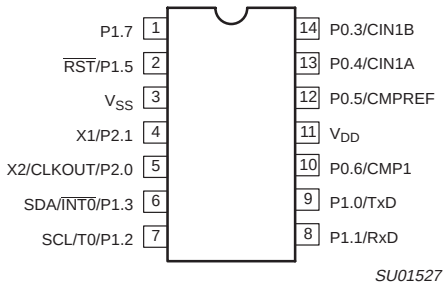
FEATURES

- An accelerated 80C51 CPU provides instruction cycle times of 300–600 ns for all instructions except multiply and divide when executing at 20 MHz. Execution at up to 20 MHz when V_{DD} = 4.5 V to 6.0 V, 10 MHz when V_{DD} = 2.7 V to 6.0 V
- 2.7 V to 6.0 V operating range for digital functions
- 1 kbyte EPROM code memory
- 128 byte RAM data memory
- 32 byte customer code EPROM allows serialization of devices, storage of setup parameters, etc
- Two 16-bit counter/timers. One timer may be configured to toggle a port output upon timer overflow
- One analog comparator
- Full duplex UART
- I^2C communication port
- Four keypad interrupt inputs, plus one additional external interrupt input
- Four interrupt priority levels
- Watchdog timer with separate on-chip oscillator, requiring no external components. The watchdog timeout time is selectable from 8 values
- Active low reset. On-chip power-on reset allows operation with no external reset components
- Low voltage reset. One of two preset low voltage levels may be selected to allow a graceful system shutdown when power fails. May optionally be configured as an interrupt
- Oscillator Fail Detect. The watchdog timer has a separate fully on-chip oscillator, allowing it to perform an oscillator fail detect function
- Configurable on-chip oscillator with frequency range and RC oscillator options (selected by user programmed EPROM bits). The RC oscillator option allows operation with no external oscillator components
- Programmable port output configuration options: quasi-bidirectional, open drain, push-pull, input-only
- Selectable Schmitt trigger port inputs
- LED drive capability (20 mA) on all port pins
- Controlled slew rate port outputs to reduce EMI. Outputs have approximately 10 ns minimum ramp times
- Nine I/O pins minimum. Up to 12 I/O pins using on-chip oscillator and reset options
- Only power and ground connections are required to operate the P87LPC760 when fully on-chip oscillator and reset options are selected
- Serial EPROM programming allows simple in-circuit production coding. Two EPROM security bits prevent reading of sensitive application programs
- Idle and Power Down reduced power modes. Improved wakeup from Power Down mode (a low interrupt input starts execution). Typical Power Down current is 1 μA
- 14-pin TSSOP and 14-pin DIP packages

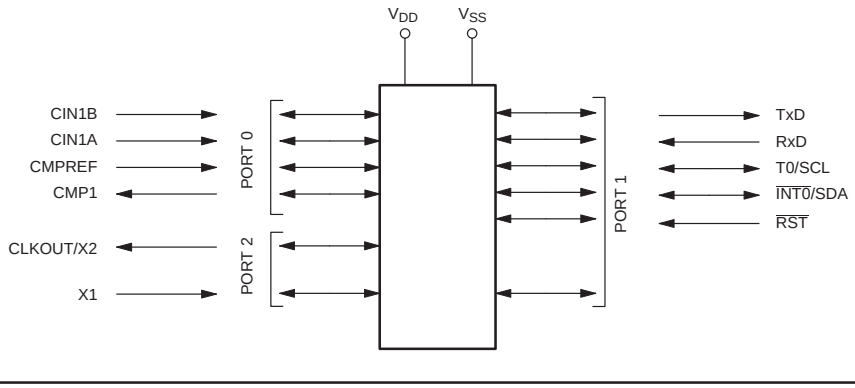
ORDERING INFORMATION

Part Number	Temperature Range °C and Package	Frequency	Drawing Number
P87LPC760BDH	0 to +70, plastic thin shrink small outline package; 14 leads; body width 4.4 mm	20 MHz (5 V), 10 MHz (3 V)	SOT402-1
P87LPC760BN	0 to +70, plastic dual in-line package; 14 leads (300 mil)	20 MHz (5 V), 10 MHz (3 V)	SOT27-1

PIN CONFIGURATION, 14-PIN TSSOP AND 14-PIN DIP PACKAGES



LOGIC SYMBOL



SPECIAL FUNCTION REGISTERS

Name	Description	SFR Address	Bit Functions and Addresses MSB							LSB	Reset Value
			E7	E6	E5	E4	E3	E2	E1	E0	
ACC*	Accumulator	E0h									00h
AUXR1#	Auxiliary Function Register	A2h	KBF	BOD	BOI	LPEP	SRST	0	–	DPS	02h[1]
			F7	F6	F5	F4	F3	F2	F1	F0	
B*	B register	F0h									00h
CMP1#	Comparator 1 control register	ACh	–	–	CE1	CP1	CN1	OE1	CO1	CMF1	00h[1]
DIVM#	CPU clock divide-by-M control	95h									00h
DPTR:	Data pointer (2 bytes)										
DPH	Data pointer high byte	83h									00h
DPL	Data pointer low byte	82h									00h
			CF	CE	CD	CC	CB	CA	C9	C8	
I2CFG#*	I^2C configuration register	C8h/RD	SLAVEN	MASTRQ	0	TIRUN	–	–	CT1	CT0	00h[1]
		C8h/WR	SLAVEN	MASTRQ	CLRTI	TIRUN	–	–	CT1	CT0	
			DF	DE	DD	DC	DB	DA	D9	D8	
I2CON#*	I^2C control register	D8h/RD	RDAT	ATN	DRDY	ARL	STR	STP	MASTER	–	80h[1]
		D8h/WR	CXA	IDLE	CDR	CARL	CSTR	CSTP	XSTR	XSTP	
I2DAT#	I^2C data register	D9h/RD	RDAT	0	0	0	0	0	0	0	80h
		D9h/WR	XDAT	x	x	X	x	x	x	x	
			AF	AE	AD	AC	AB	AA	A9	A8	
IEN0*	Interrupt enable 0	A8h	EA	EWD	EBO	ES	ET1	–	ET0	EX0	00h
			EF	EE	ED	EC	EB	EA	E9	E8	
IEN1#*	Interrupt enable 1	E8h	ETI	–	EC1	–	–	–	EKB	EI2	00h[1]
			BF	BE	BD	BC	BB	BA	B9	B8	
IP0*	Interrupt priority 0	B8h	–	PWD	PBO	PS	PT1	–	PT0	PX0	00h[1]
IP0H#	Interrupt priority 0 high byte	B7h	–	PWDH	PBOH	PSH	PT1H	–	PT0H	PX0H	00h[1]
			FF	FE	FD	FC	FB	FA	F9	F8	
IP1*	Interrupt priority 1	F8h	PTI	–	PC1	–	–	–	PKB	PI2	00h[1]
IP1H#	Interrupt priority 1 high byte	F7h	PTIH	–	PC1H	–	–	–	PKBH	PI2H	00h[1]
KBI#	Keyboard Interrupt	86h									00h
			87	86	85	84	83	82	81	80	
P0*	Port 0	80h	–	CMP1	CMPREF	CIN1A	CIN1B	–	–	–	Note 2
			97	96	95	94	93	92	91	90	
P1*	Port 1	90h	(P1.7)	–	$\overline{RST}$	–	INT0	T0	RxD	TxD	Note 2
			A7	A6	A5	A4	A3	A2	A1	A0	
P2*	Port 2	A0h	–	–	–	–	–	–	X1	X2	Note 2
P0M1#	Port 0 output mode 1	84h	–	(P0M1.6)	(P0M1.5)	(P0M1.4)	(P0M1.3)	–	–	–	00h
P0M2#	Port 0 output mode 2	85h	–	(P0M2.6)	(P0M2.5)	(P0M2.4)	(P0M2.3)	–	–	–	00h
P1M1#	Port 1 output mode 1	91h	(P1M1.7)	–	–	–	–	–	(P1M1.1)	(P1M1.0)	00h[1]
P1M2#	Port 1 output mode 2	92h	(P1M2.7)	–	–	–	–	–	(P1M2.1)	(P1M2.0)	00h[1]
P2M1#	Port 2 output mode 1	A4h	P2S	P1S	P0S	ENCLK	–	T0OE	(P2M1.1)	(P2M1.0)	00h

FUNCTIONAL DESCRIPTION

Details of P87LPC760 functions will be described in the following sections.

Enhanced CPU

The P87LPC760 uses an enhanced 80C51 CPU which runs at twice the speed of standard 80C51 devices. This means that the performance of the P87LPC760 running at 5 MHz is exactly the same as that of a standard 80C51 running at 10 MHz. A machine cycle consists of 6 oscillator cycles, and most instructions execute in 6 or 12 clocks. A user configurable option allows restoring standard 80C51 execution timing. In that case, a machine cycle becomes 12 oscillator cycles.

In the following sections, the term “CPU clock” is used to refer to the clock that controls internal instruction execution. This may sometimes be different from the externally applied clock, as in the case where the part is configured for standard 80C51 timing by means of the CLKR configuration bit or in the case where the clock is divided down via the setting of the DIVM register. These features are described in the Oscillator section.

Analog Functions

The P87LPC760 incorporates one Analog Comparator. In order to give the best analog function performance and to minimize power consumption, pins that are actually being used for analog functions must have the digital outputs and the digital inputs disabled.

Digital outputs are disabled by putting the port output into the Input Only (high impedance) mode as described in the I/O Ports section.

Digital inputs on port 0 may be disabled through the use of the PT0AD register. Each bit in this register corresponds to one pin of Port 0. Setting the corresponding bit in PT0AD disables that pin’s digital input. Port bits that have their digital inputs disabled will be read as 0 by any instruction that accesses the port.

Analog Comparators

An analog comparator is provided on the P87LPC760. Input and output options allow use of the comparator in a number of different configurations. Comparator operation is such that the output is a logical one (which may be read in a register and/or routed to a pin) when the positive input (one of two selectable pins) is greater than the negative input (selectable from a pin or an internal reference voltage). Otherwise the output is a zero. The comparator may be configured to cause an interrupt when the output value changes.

Comparator Configuration

The comparator has a control register, CMP1. The control register is shown in Figure 2.

The overall connections to the comparator are shown in Figure 3. There are eight possible configurations for the comparator, as determined by the control bits in the CMP1 register: CP1, CN1, and OE1. These configurations are shown in Figure 4. The comparator functions down to a V_{DD} of 3.0V.

When the comparator is first enabled, the comparator output and interrupt flag are not guaranteed to be stable for 10 microseconds. The comparator interrupt should not be enabled during that time, and the comparator interrupt flag must be cleared before the interrupt is enabled in order to prevent an immediate interrupt service.

CMP1 Address: ACh Reset Value: 00h

Not Bit Addressable

7	6	5	4	3	2	1	0
—	—	CE1	CP1	CN1	OE1	CO1	CMF1

BIT	SYMBOL	FUNCTION
CMP1.7, 6	—	Reserved for future use. Should not be set to 1 by user programs.
CMP1.5	CE1	Comparator enable. When set by software, the corresponding comparator function is enabled. Comparator output is stable 10 microseconds after CE1 is first set.
CMP1.4	CP1	Comparator positive input select. When 0, CIN1A is selected as the positive comparator input. When 1, CIN1B is selected as the positive comparator input.
CMP1.3	CN1	Comparator negative input select. When 0, the comparator reference pin CMPREF is selected as the negative comparator input. When 1, the internal comparator reference V_{ref} is selected as the negative comparator input.
CMP1.2	OE1	Output enable. When 1, the comparator output is connected to the CMP1 pin if the comparator is enabled (CE1 = 1). This output is asynchronous to the CPU clock.
CMP1.1	CO1	Comparator output, synchronized to the CPU clock to allow reading by software. Cleared when the comparator is disabled (CE1 = 0).
CMP1.0	CMF1	Comparator interrupt flag. This bit is set by hardware whenever the comparator output CO1 changes state. This bit will cause a hardware interrupt if enabled and of sufficient priority. Cleared by software and when the comparator is disabled (CE1 = 0).

SU01531

Figure 2. Comparator Control Register (CMP1)

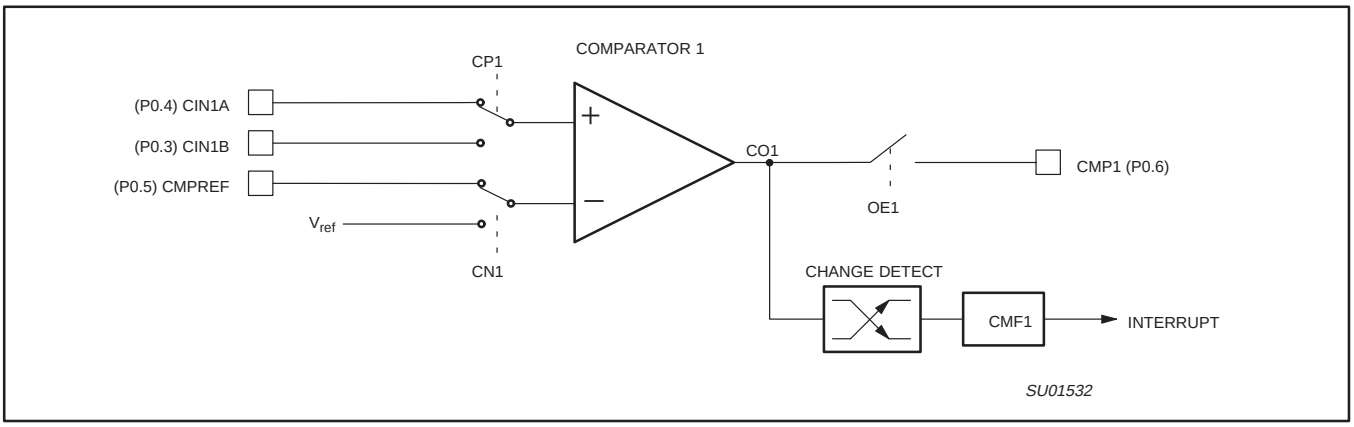


Figure 3. Comparator Input and Output Connections

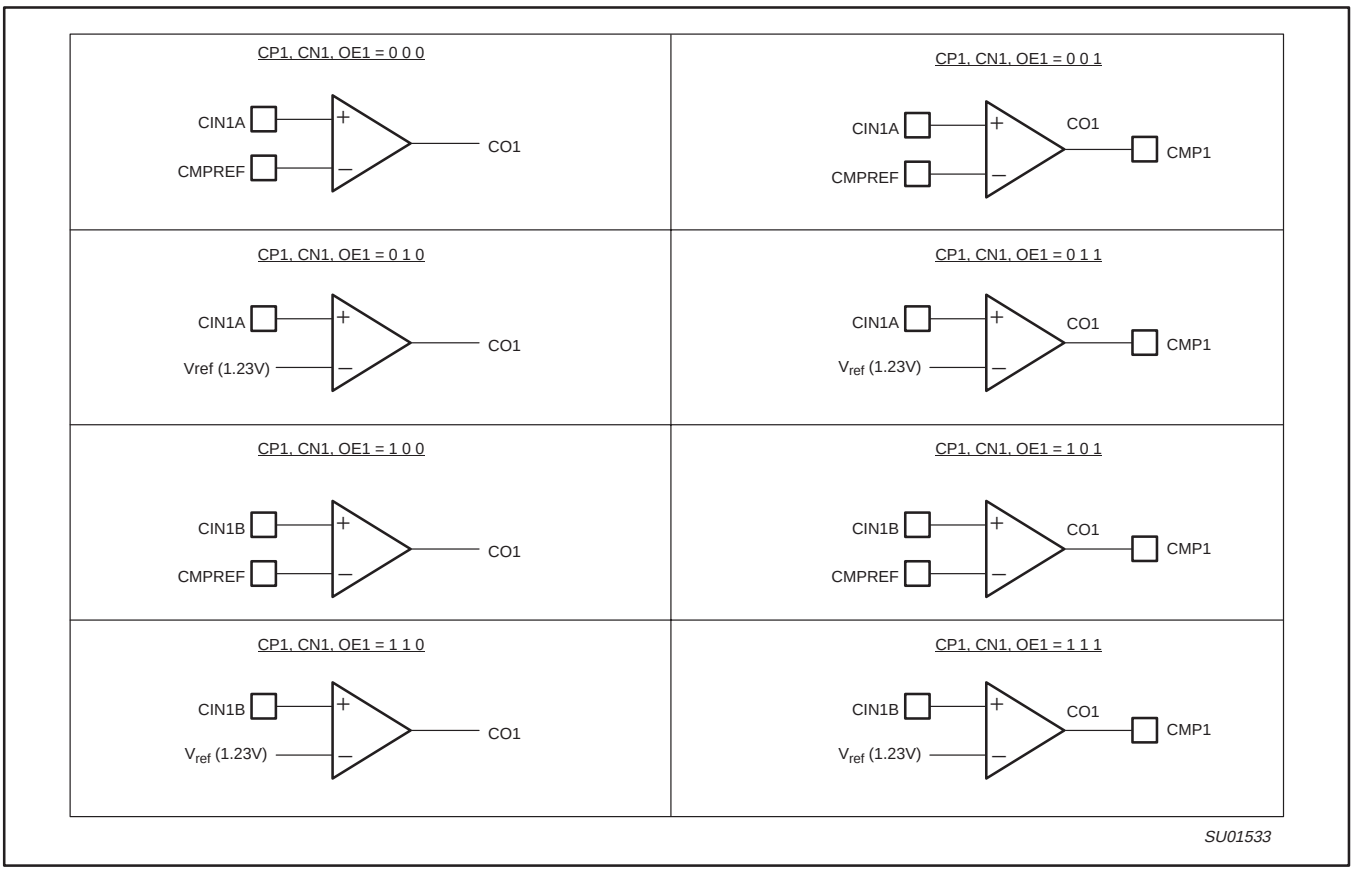


Figure 4. Comparator Configurations

I2CFG Address: C8h Reset Value: 00h

Bit Addressable

7	6	5	4	3	2	1	0
SLAVEN	MASTRQ	CLRTI	TIRUN	—	—	CT1	CT0

BIT	SYMBOL	FUNCTION
I2CFG.7	SLAVEN	Slave Enable. Writing a 1 this bit enables the slave functions of the I^2C subsystem. If SLAVEN and MASTRQ are 0, the I^2C hardware is disabled. This bit is cleared to 0 by reset and by an I^2C time-out.
I2CFG.6	MASTRQ	Master Request. Writing a 1 to this bit requests mastership of the I^2C bus. If a transmission is in progress when this bit is changed from 0 to 1, action is delayed until a stop condition is detected. A start condition is sent and DRDY is set (thus making ATN = 1 and generating an I^2C interrupt). When a master wishes to release mastership status of the I^2C, it writes a 1 to XSTP in I2CON. MASTRQ is cleared by an I^2C time-out.
I2CFG.5	CLRTI	Writing a 1 to this bit clears the Timer I overflow flag. This bit position always reads as a 0.
I2CFG.4	TIRUN	Writing a 1 to this bit lets Timer I run; a zero stops and clears it. Together with SLAVEN, MASTRQ, and MASTER, this bit determines operational modes as shown in Table 1.
I2CFG.2, 3	—	Reserved for future use. Should not be set to 1 by user programs.
I2CFG.1, 0	CT1, CT0	These two bits are programmed as a function of the CPU clock rate, to optimize the MIN HI and LO time of SCL when this device is a master on the I^2C. The time value determined by these bits controls both of these parameters, and also the timing for stop and start conditions.

SU01552

Figure 8. I^2C Configuration Register (I2CFG)

Regarding Software Response Time

Because the P87LPC760 can run at 20 MHz, and because the I^2C interface is optimized for high-speed operation, it is quite likely that an I^2C service routine will sometimes respond to DRDY (which is set at a rising edge of SCL) and write I2DAT before SCL has gone low again. If XDAT were applied directly to SDA, this situation would produce an I^2C protocol violation. The programmer need not worry about this possibility because XDAT is applied to SDA only when SCL is low.

Conversely, a program that includes an I^2C service routine may take a long time to respond to DRDY. Typically, an I^2C routine operates on a flag-polling basis during a message, with interrupts from other peripheral functions enabled. If an interrupt occurs, it will delay the response of the I^2C service routine. The programmer need not worry about this very much either, because the I^2C hardware stretches the SCL low time until the service routine responds. The only constraint on the response is that it must not exceed the Timer I time-out.

Values to be used in the CT1 and CT0 bits are shown in Table 2. To allow the I^2C bus to run at the maximum rate for a particular oscillator frequency, compare the actual oscillator rate to the f OSC max column in the table. The value for CT1 and CT0 is found in the first line of the table where CPU clock max is greater than or equal to the actual frequency.

Table 2 also shows the machine cycle count for various settings of CT1/CT0. This allows calculation of the actual minimum high and low times for SCL as follows:

$$\text{SCL min high/low time in microseconds} = \frac{6 * \text{Min Time Count}}{\text{CPU clock in MHz}}$$

For instance, at an 8 MHz frequency, with CT1/CT0 set to 1 0, the minimum SCL high and low times will be 5.25 μs.

Table 2 also shows the Timer I timeout period (given in machine cycles) for each CT1/CT0 combination. The timeout period varies because of the way in which minimum SCL high and low times are measured. When the I^2C interface is operating, Timer I is pre-loaded at every SCL transition with a value dependent upon CT1/CT0. The pre-load value is chosen such that a minimum SCL high or low time has elapsed when Timer I reaches a count of 008 (the actual value pre-loaded into Timer I is 8 minus the machine cycle count).

External Interrupt Inputs

The P87LPC760 has one individual interrupt input as well as the Keyboard Interrupt function. The latter is described separately in this section. The interrupt input are identical to those present on the standard 80C51 microcontroller.

The external source can be programmed to be level-activated or transition-activated by setting or clearing bit IT0 in Register TCON. If IT0 = 0, external interrupt 0 is triggered by a detected low at the INT0 pin. If IT0 = 1, external interrupt 0 is edge triggered. In this mode if successive samples of the INT0 pin show a high in one cycle and a low in the next cycle, interrupt request flag IE0 in TCON is set, causing an interrupt request.

Since the external interrupt pin is sampled once each machine cycle, an input high or low should hold for at least 6 CPU Clocks to ensure proper sampling. If the external interrupt is transition-activated, the external source has to hold the request pin high for at least one machine cycle, and then hold it low for at least one machine cycle. This is to ensure that the transition is detected and that interrupt request flag IE0 is set. IE0 is automatically cleared by the CPU when the service routine is called.

If the external interrupt is level-activated, the external source must hold the request active until the requested interrupt is actually generated. If the external interrupt is still asserted when the interrupt service routine is completed another interrupt will be generated. It is not necessary to clear the interrupt flag IE0 when the interrupt is level sensitive, it simply tracks the input pin level.

If the external interrupt is enabled when the P87LPC760 is put into Power Down or Idle mode, the interrupt will cause the processor to wake up and resume operation. Refer to the section on Power Reduction Modes for details.

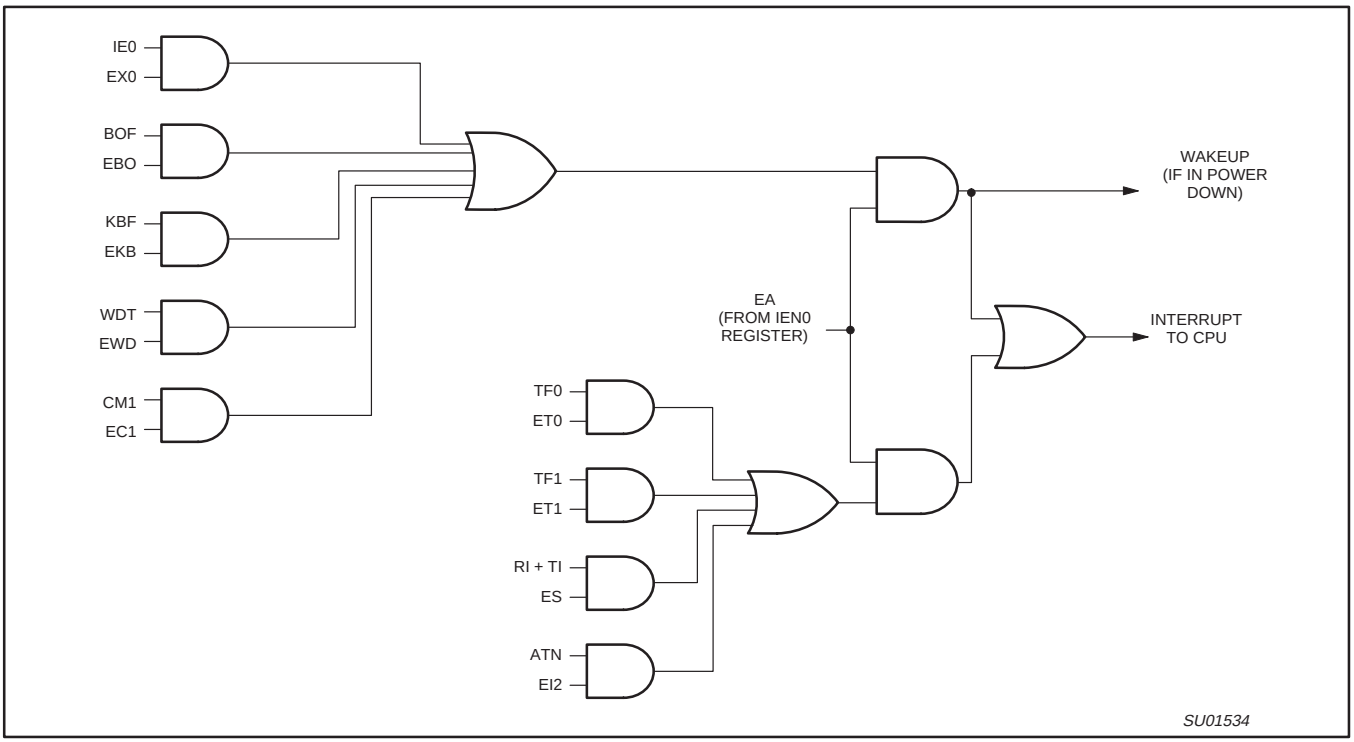


Figure 9. Interrupt Sources, Interrupt Enables, and Power Down Wakeup Sources

Oscillator

The P87LPC760 provides several user selectable oscillator options, allowing optimization for a range of needs from high precision to lowest possible cost. These are configured when the EPROM is programmed. Basic oscillator types that are supported include: low, medium, and high speed crystals, covering a range from 20 kHz to 20 MHz; ceramic resonators; and on-chip RC oscillator.

Low Frequency Oscillator Option

This option supports an external crystal in the range of 20 kHz to 100 kHz.

Table 5 shows capacitor values that may be used with a quartz crystal in this mode.

Table 5. Recommended oscillator capacitors for use with the low frequency oscillator option

Oscillator Frequency	V_{DD} = 2.7 to 4.5 V			V_{DD} = 4.5 to 6.0 V		
	Lower Limit	Optimal Value	Upper Limit	Lower Limit	Optimal Value	Upper Limit
20 kHz	15 pF	15 pF	33 pF	33 pF	33 pF	47 pF
32 kHz	15 pF	15 pF	33 pF	33 pF	33 pF	47 pF
100 kHz	15 pF	15 pF	33 pF	15 pF	15 pF	33 pF

Medium Frequency Oscillator Option

This option supports an external crystal in the range of 100 kHz to 4 MHz. Ceramic resonators are also supported in this configuration.

Table 6 shows capacitor values that may be used with a quartz crystal in this mode.

Table 6. Recommended oscillator capacitors for use with the medium frequency oscillator option

Oscillator Frequency	V_{DD} = 2.7 to 4.5 V		
	Lower Limit	Optimal Value	Upper Limit
100 kHz	33 pF	33 pF	47 pF
1 MHz	15 pF	15 pF	33 pF
4 MHz	15 pF	15 pF	33 pF

High Frequency Oscillator Option

This option supports an external crystal in the range of 4 to 20 MHz. Ceramic resonators are also supported in this configuration.

Table 7 shows capacitor values that may be used with a quartz crystal in this mode.

Table 7. Recommended oscillator capacitors for use with the high frequency oscillator option

Oscillator Frequency	V_{DD} = 2.7 to 4.5 V			V_{DD} = 4.5 to 6.0 V		
	Lower Limit	Optimal Value	Upper Limit	Lower Limit	Optimal Value	Upper Limit
4 MHz	15 pF	33 pF	47 pF	15 pF	33 pF	68 pF
8 MHz	15 pF	15 pF	33 pF	15 pF	33 pF	47 pF
16 MHz	–	–	–	15 pF	15 pF	33 pF
20 MHz	–	–	–	15 pF	15 pF	33 pF

On-Chip RC Oscillator Option

The on-chip RC oscillator option has a typical frequency of 6 MHz and can be divided down for slower operation through the use of the DIVM register. For on-chip oscillator tolerance see AC Electrical Characteristics table. A clock output on the X2/P2.0 pin may be enabled when the on-chip RC oscillator is used.

External Clock Input Option

In this configuration, the processor clock is input from an external source driving the X1/P2.1 pin. The rate may be from 0 Hz up to 20 MHz when V_{DD} is above 4.5 V and up to 10 MHz when V_{DD} is below 4.5 V. When the external clock input mode is used, the X2/P2.0 pin may be used as a standard port pin. A clock output on the X2/P2.0 pin may be enabled when the external clock input is used.

Clock Output

The P87LPC760 supports a clock output function when either the on-chip RC oscillator or external clock input options are selected. This allows external devices to synchronize to the P87LPC760. When enabled, via the ENCLK bit in the P2M1 register, the clock output appears on the X2/CLKOUT pin whenever the on-chip oscillator is running, including in Idle mode. The frequency of the clock output is 1/6 of the CPU clock rate. If the clock output is not needed in Idle mode, it may be turned off prior to entering Idle, saving additional power. The clock output may also be enabled when the external clock input option is selected.

For correct activation of Brownout Detect, the V_{DD} fall time must be no faster than 50 mV/µs. When V_{DD} is restored, is should not rise faster than 2 mV/µs in order to insure a proper reset.

The brownout voltage (2.5 V or 3.8 V) is selected via the BOV bit in the EPROM configuration register UCFG1. When unprogrammed (BOV = 1), the brownout detect voltage is 2.5 V. When programmed (BOV = 0), the brownout detect voltage is 3.8 V.

If the Brownout Detect function is not required in an application, it may be disabled, thus saving power. Brownout Detect is disabled by setting the control bit BOD in the AUXR1 register (AUXR1.6).

Power On Detection

The Power On Detect has a function similar to the Brownout Detect, but is designed to work as power comes up initially, before the power supply voltage reaches a level where Brownout Detect can work. When this feature is activated, the POF flag in the PCON register is set to indicate an initial power up condition. The POF flag will remain set until cleared by software.

Power Reduction Modes

The P87LPC760 supports Idle and Power Down modes of power reduction.

Idle Mode

The Idle mode leaves peripherals running in order to allow them to activate the processor when an interrupt is generated. Any enabled interrupt source or Reset may terminate Idle mode. Idle mode is entered by setting the IDL bit in the PCON register (see Figure 19).

Power Down Mode

The Power Down mode stops the oscillator in order to absolutely minimize power consumption. Power Down mode is entered by setting the PD bit in the PCON register (see Figure 19).

The processor can be made to exit Power Down mode via Reset or one of the interrupt sources shown in Table 5. This will occur if the interrupt is enabled and its priority is higher than any interrupt currently in progress.

In Power Down mode, the power supply voltage may be reduced to the RAM keep-alive voltage V_{RAM}. This retains the RAM contents at the point where Power Down mode was entered. SFR contents are not guaranteed after V_{DD} has been lowered to V_{RAM}, therefore it is recommended to wake up the processor via Reset in this case. V_{DD} must be raised to within the operating range before the Power Down mode is exited. Since the watchdog timer has a separate oscillator, it may reset the processor upon overflow if it is running during Power Down.

Note that if the Brownout Detect reset is enabled, the processor will be put into reset as soon as V_{DD} drops below the brownout voltage. If Brownout Detect is configured as an interrupt and is enabled, it will wake up the processor from Power Down mode when V_{DD} drops below the brownout voltage.

When the processor wakes up from Power Down mode, it will start the oscillator immediately and begin execution when the oscillator is stable. Oscillator stability is determined by counting 1024 CPU clocks after start-up when one of the crystal oscillator configurations is used, or 256 clocks after start-up for the internal RC or external clock input configurations.

Some chip functions continue to operate and draw power during Power Down mode, increasing the total power used during Power Down. These include the Brownout Detect, Watchdog Timer, and Comparator.

PCON Address: 87h

Not Bit Addressable

Reset Value:
- 30h for a Power On reset
- 20h for a Brownout reset
- 00h for other reset sources

7	6	5	4	3	2	1	0
SMOD1	SMOD0	BOF	POF	GF1	GF0	PD	IDL

BIT	SYMBOL	FUNCTION
PCON.7	SMOD1	When set, this bit doubles the UART baud rate for modes 1, 2, and 3.
PCON.6	SMOD0	This bit selects the function of bit 7 of the SCON SFR. When 0, SCON.7 is the SM0 bit. When 1, SCON.7 is the FE (Framing Error) flag.[1]
PCON.5	BOF	Brown Out Flag. Set automatically when a brownout reset or interrupt has occurred. Also set at power on. Cleared by software. Refer to the Power Monitoring Functions section for additional information.
PCON.4	POF	Power On Flag. Set automatically when a power-on reset has occurred. Cleared by software. Refer to the Power Monitoring Functions section for additional information.
PCON.3	GF1	General purpose flag 1. May be read or written by user software, but has no effect on operation.
PCON.2	GF0	General purpose flag 0. May be read or written by user software, but has no effect on operation.
PCON.1	PD	Power Down control bit. Setting this bit activates Power Down mode operation. Cleared when the Power Down mode is terminated (see text).
PCON.0	IDL	Idle mode control bit. Setting this bit activates Idle mode operation. Cleared when the Idle mode is terminated (see text).

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1. See Figure 31 for additional information.

Figure 19. Power Control Register (PCON)

Timer/Counters

The P87LPC760 has two general purpose counter/timers which are upward compatible with the standard 80C51 Timer 0 and Timer 1. Both can be configured to operate as timers or can be configured to be an event counter (see Figure 22). An option to automatically toggle the T0 pin upon timer overflow has been added.

In the “Timer” function, the register is incremented every machine cycle. Thus, one can think of it as counting machine cycles. Since a machine cycle consists of 6 CPU clock periods, the count rate is 1/6 of the CPU clock frequency. Refer to the section Enhanced CPU for a description of the CPU clock.

In the “Counter” function of Timer 0, the register is incremented in response to a 1-to-0 transition at its corresponding external input pin, T0. In this function, the external input is sampled once during every machine cycle. When the samples of the pin state show a high in one cycle and a low in the next cycle, the count is incremented. The new count value appears in the register during the cycle following the one in which the transition was detected. Since it takes 2 machine cycles (12 CPU clocks) to recognize a 1-to-0 transition, the maximum count rate is 1/6 of the CPU clock frequency. There are no restrictions on the duty cycle of the external input signal, but to ensure that a given level is sampled at least once before it changes, it should be held for at least one full machine cycle.

The “Timer” or “Counter” function of Timer 0 is selected by control bit C/$\overline{T}$ in the Special Function Register TMOD. In addition to the “Timer” or “Counter” selection, Timer 0 and Timer 1 have four operating modes, which are selected by bit-pairs (M1, M0) in TMOD. Modes 0, 1, and 2 are the same for both Timers/Counters. Mode 3 is different. The four operating modes are described in the following text.

TMOD Address: 89h Reset Value: 00h

Not Bit Addressable

7	6	5	4	3	2	1	0
–	–	M1	M0	GATE	C/$\overline{T}$	M1	M0
		T1		T0			

BIT	SYMBOL	FUNCTION
TMOD.7, 6	–	Reserved. Must be written with zeros only.
TMOD.5, 4	M1, M0	Mode Select for Timer 1 (see table below).
TMOD.3	GATE	Gating control for Timer 0. When set, Timer/Counter is enabled only while the $\overline{INT0}$ pin is high and the TR0 control pin is set. When cleared, Timer 0 is enabled when the TR0 control bit is set.
TMOD.2	C/$\overline{T}$	Timer or Counter Selector for Timer 0. Cleared for Timer operation (input from internal system clock.) Set for Counter operation (input from T0 input pin).
TMOD.1, 0	M1, M0	Mode Select for Timer 0 (see table below).
	M1, M0	Timer Mode
	0 0	8048 Timer “TLn” serves as 5-bit prescaler.
	0 1	16-bit Timer/Counter “THn” and “TLn” are cascaded; there is no prescaler.
	1 0	8-bit auto-reload Timer/Counter. THn holds a value which is loaded into TLn when it overflows.
	1 1	Timer 0 is a dual 8-bit Timer/Counter in this mode. TL0 is an 8-bit Timer/Counter controlled by the standard Timer 0 control bits. TH0 is an 8-bit timer only, controlled by the Timer 1 control bits (see text). Timer 1 in this mode is stopped.

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Figure 22. Timer/Counter Mode Control Register (TMOD)

Mode 0

Putting either Timer into Mode 0 makes it look like an 8048 Timer, which is an 8-bit Counter with a divide-by-32 prescaler. Figures 24 and 25 show Mode 0 operation.

In this mode, the Timer register is configured as a 13-bit register. As the count rolls over from all 1s to all 0s, it sets the Timer interrupt flag TFn. The count input is enabled to Timer 0 when TR0 = 1 and either GATE = 0 or INT0 = 1. (Setting GATE = 1 allows the Timer to be controlled by external input INT0, to facilitate pulse width measurements). TRn is a control bit in the Special Function Register TCON (Figure 23). The GATE bit is in the TMOD register (TMOD.3).

The 13-bit register consists of all 8 bits of THn and the lower 5 bits of TLn. The upper 3 bits of TLn are indeterminate and should be ignored. Setting the run flag (TRn) does not clear the registers.

Mode 0 operation is slightly different for Timer 0 and Timer 1. See Figures 24 and 25.

TCON Address: 88h Reset Value: 00h

Bit Addressable

7	6	5	4	3	2	1	0
TF1	TR1	TF0	TR0	–	–	IE0	IT0

BIT	SYMBOL	FUNCTION
TCON.7	TF1	Timer 1 overflow flag. Set by hardware on Timer/Counter overflow. Cleared by hardware when the interrupt is processed, or by software.
TCON.6	TR1	Timer 1 Run control bit. Set/cleared by software to turn Timer/Counter 1 on/off.
TCON.5	TF0	Timer 0 overflow flag. Set by hardware on Timer/Counter overflow. Cleared by hardware when the processor vectors to the interrupt routine, or by software.
TCON.4	TR0	Timer 0 Run control bit. Set/cleared by software to turn Timer/Counter 0 on/off.
TCON.3, 2	–	Reserved (must be 0).
TCON.1	IE0	Interrupt 0 Edge flag. Set by hardware when external interrupt 0 edge is detected. Cleared by hardware when the interrupt is processed, or by software.
TCON.0	IT0	Interrupt 0 Type control bit. Set/cleared by software to specify falling edge/low level triggered external interrupts.

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Figure 23. Timer/Counter Control Register (TCON)

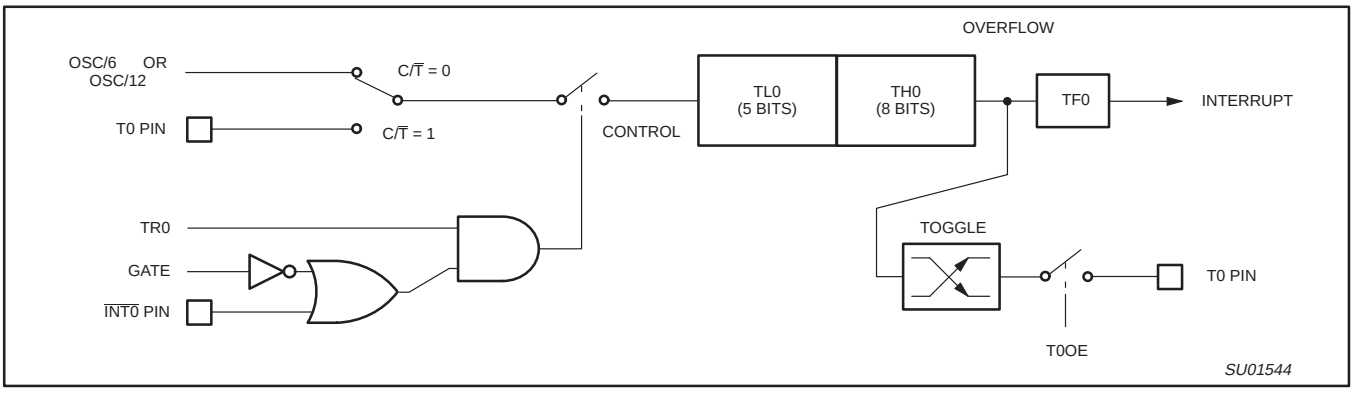

Figure 24. Timer/Counter 0 in Mode 0 (13-Bit Timer/Counter)

Timer Overflow Toggle Output
Timer 0 can be configured to automatically toggle a port output whenever a timer overflow occurs. The same device pins that is used for the T0 count inputs are also used for the timer toggle outputs. This function is enabled by control bit T0OE in the P2M1 register. The port outputs will be a logic 1 prior to the first timer overflow when this mode is turned on.

UART

The P87LPC760 includes an enhanced 80C51 UART. The baud rate source for the UART is timer 1 for modes 1 and 3, while the rate is fixed in modes 0 and 2. Because CPU clocking is different on the P87LPC760 than on the standard 80C51, baud rate calculation is somewhat different. Enhancements over the standard 80C51 UART include Framing Error detection and automatic address recognition.

The serial port is full duplex, meaning it can transmit and receive simultaneously. It is also receive-buffered, meaning it can commence reception of a second byte before a previously received byte has been read from the SBUF register. However, if the first byte still hasn't been read by the time reception of the second byte is complete, the first byte will be lost. The serial port receive and transmit registers are both accessed through Special Function Register SBUF. Writing to SBUF loads the transmit register, and reading SBUF accesses a physically separate receive register.

The serial port can be operated in 4 modes:

Mode 0
Serial data enters and exits through RxD. TxD outputs the shift clock. 8 bits are transmitted or received, LSB first. The baud rate is fixed at 1/6 of the CPU clock frequency.

Mode 1
10 bits are transmitted (through TxD) or received (through RxD): a start bit (logical 0), 8 data bits (LSB first), and a stop bit (logical 1). When data is received, the stop bit is stored in RB8 in Special Function Register SCON. The baud rate is variable and is determined by the Timer 1 overflow rate.

Mode 2
11 bits are transmitted (through TxD) or received (through RxD): start bit (logical 0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (logical 1). When data is transmitted, the 9th data bit (TB8 in SCON) can be assigned the value of 0 or 1. Or, for example, the parity bit (P, in the PSW) could be moved into TB8. When data is received, the 9th data bit goes into RB8 in Special Function Register SCON, while the stop bit is ignored. The baud rate is programmable to either 1/16 or 1/32 of the CPU clock frequency, as determined by the SMOD1 bit in PCON.

Mode 3
11 bits are transmitted (through TxD) or received (through RxD): a start bit (logical 0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (logical 1). In fact, Mode 3 is the same as Mode 2 in all respects except baud rate. The baud rate in Mode 3 is variable and is determined by the Timer 1 overflow rate.

In all four modes, transmission is initiated by any instruction that uses SBUF as a destination register. Reception is initiated in Mode 0 by the condition RI = 0 and REN = 1. Reception is initiated in the other modes by the incoming start bit if REN = 1

Serial Port Control Register (SCON)
The serial port control and status register is the Special Function Register SCON, shown in Figure 31. This register contains not only the mode selection bits, but also the 9th data bit for transmit and receive (TB8 and RB8), and the serial port interrupt bits (TI and RI).

The Framing Error bit (FE) allows detection of missing stop bits in the received data stream. The FE bit shares the bit position SCON.7 with the SM0 bit. Which bit appears in SCON at any particular time is determined by the SMOD0 bit in the PCON register. If SMOD0 = 0, SCON.7 is the SM0 bit. If SMOD0 = 1, SCON.7 is the FE bit. Once set, the FE bit remains set until it is cleared by software. This allows detection of framing errors for a group of characters without the need for monitoring it for every character individually.

SCON Address: 98h Reset Value: 00h

Bit Addressable

7	6	5	4	3	2	1	0
SM0/FE	SM1	SM2	REN	TB8	RB8	TI	RI

BIT	SYMBOL	FUNCTION
SCON.7	FE	Framing Error. This bit is set by the UART receiver when an invalid stop bit is detected. Must be cleared by software. The SMOD0 bit in the PCON register must be 1 for this bit to be accessible. See SM0 bit below.
SCON.7	SM0	With SM1, defines the serial port mode. The SMOD0 bit in the PCON register must be 0 for this bit to be accessible. See FE bit above.
SCON. 6	SM1	With SM0, defines the serial port mode (see table below).
	SM0, SM1	UART Mode — Baud Rate
	0 0	0: shift register — CPU clock/6
	0 1	1: 8-bit UART — Variable (see text)
	1 0	2: 9-bit UART — CPU clock/32 or CPU clock/16
	1 1	3: 9-bit UART — Variable (see text)
SCON.5	SM2	Enables the multiprocessor communication feature in Modes 2 and 3. In Mode 2 or 3, if SM2 is set to 1, then RI will not be activated if the received 9th data bit (RB8) is 0. In Mode 1, if SM2=1 then RI will not be activated if a valid stop bit was not received. In Mode 0, SM2 should be 0.
SCON.4	REN	Enables serial reception. Set by software to enable reception. Clear by software to disable reception.
SCON.3	TB8	The 9th data bit that will be transmitted in Modes 2 and 3. Set or clear by software as desired.
SCON.2	RB8	In Modes 2 and 3, is the 9th data bit that was received. In Mode 1, it SM2=0, RB8 is the stop bit that was received. In Mode 0, RB8 is not used.
SCON.1	TI	Transmit interrupt flag. Set by hardware at the end of the 8th bit time in Mode 0, or at the beginning of the stop bit in the other modes, in any serial transmission. Must be cleared by software.
SCON.0	RI	Receive interrupt flag. Set by hardware at the end of the 8th bit time in Mode 0, or halfway through the stop bit time in the other modes, in any serial reception (except see SM2). Must be cleared by software.

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Figure 31. Serial Port Control Register (SCON)

Baud Rates

The baud rate in Mode 0 is fixed: Mode 0 Baud Rate = CPU clock/6. The baud rate in Mode 2 depends on the value of bit SMOD1 in Special Function Register PCON. If SMOD1 = 0 (which is the value on reset), the baud rate is 1/32 of the CPU clock frequency. If SMOD1 = 1, the baud rate is 1/16 of the CPU clock frequency.

$$\text{Mode 2 Baud Rate} = \frac{1 + \text{SMOD1}}{32} \times \text{CPU clock frequency}$$

Using Timer 1 to Generate Baud Rates

When Timer 1 is used as the baud rate generator, the baud rates in Modes 1 and 3 are determined by the Timer 1 overflow rate and the value of SMOD1. The Timer 1 interrupt should be disabled in this application. The Timer itself can be configured for either “timer” or “counter” operation, and in any of its 3 running modes. In the most typical applications, it is configured for “timer” operation, in the auto-reload mode (high nibble of TMOD = 0010b). In that case the baud rate is given by the formula:

$$\text{Mode 1, 3 Baud Rate} = \frac{\text{CPU clock frequency}/\text{192 (or 96 if SMOD1 = 1)}}{256 - (\text{TH1})}$$

Tables 6 and 7 list various commonly used baud rates and how they can be obtained using Timer 1 as the baud rate generator.

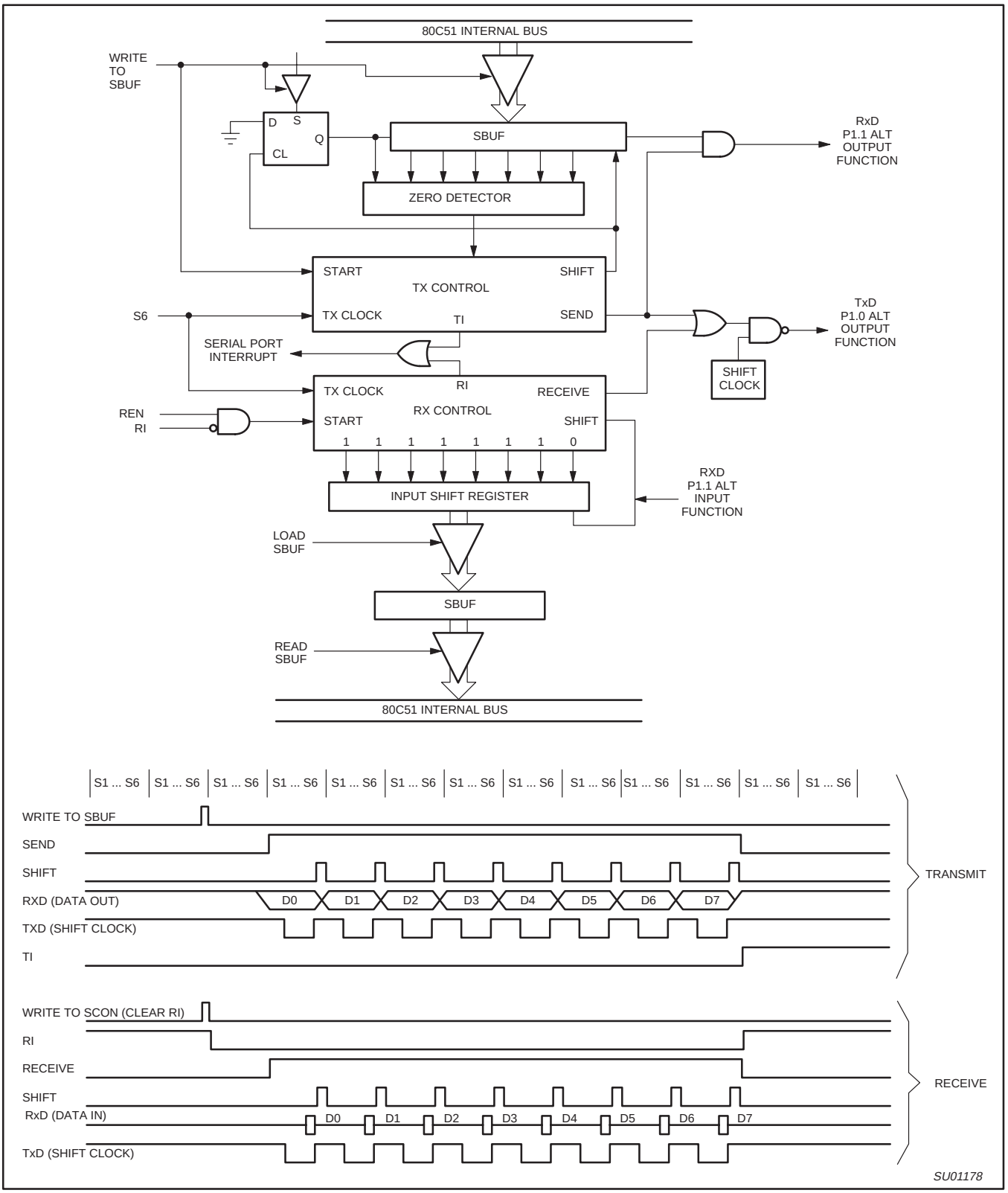

Figure 32. Serial Port Mode 0

More About UART Modes 2 and 3

Eleven bits are transmitted (through TxD), or received (through RxD): a start bit (0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (1). On transmit, the 9th data bit (TB8) can be assigned the value of 0 or 1. On receive, the 9the data bit goes into RB8 in SCON. The baud rate is programmable to either 1/16 or 1/32 of the CPU clock frequency in Mode 2. Mode 3 may have a variable baud rate generated from Timer 1.

Figures 34 and 35 show a functional diagram of the serial port in Modes 2 and 3. The receive portion is exactly the same as in Mode 1. The transmit portion differs from Mode 1 only in the 9th bit of the transmit shift register.

Transmission is initiated by any instruction that uses SBUF as a destination register. The “write to SBUF” signal also loads TB8 into the 9th bit position of the transmit shift register and flags the TX Control unit that a transmission is requested. Transmission commences at S1P1 of the machine cycle following the next rollover in the divide-by-16 counter. (Thus, the bit times are synchronized to the divide-by-16 counter, not to the “write to SBUF” signal.)

The transmission begins with activation of SEND, which puts the start bit at TxD. One bit time later, DATA is activated, which enables the output bit of the transmit shift register to TxD. The first shift pulse occurs one bit time after that. The first shift clocks a 1 (the stop bit) into the 9th bit position of the shift register. Thereafter, only zeros are clocked in. Thus, as data bits shift out to the right, zeros are clocked in from the left. When TB8 is at the output position of the shift register, then the stop bit is just to the left of TB8, and all positions to the left of that contain zeros. This condition flags the TX Control unit to do one last shift and then deactivate SEND and set TI. This occurs at the 11th divide-by-16 rollover after “write to SBUF.”

Reception is initiated by a detected 1-to-0 transition at RxD. For this purpose RxD is sampled at a rate of 16 times whatever baud rate has been established. When a transition is detected, the divide-by-16 counter is immediately reset, and 1FFH is written to the input shift register.

At the 7th, 8th, and 9th counter states of each bit time, the bit detector samples the value of R–D. The value accepted is the value that was seen in at least 2 of the 3 samples. If the value accepted during the first bit time is not 0, the receive circuits are reset and the unit goes back to looking for another 1-to-0 transition. If the start bit proves valid, it is shifted into the input shift register, and reception of the rest of the frame will proceed.

As data bits come in from the right, 1s shift out to the left. When the start bit arrives at the leftmost position in the shift register (which in Modes 2 and 3 is a 9-bit register), it flags the RX Control block to do one last shift, load SBUF and RB8, and set RI.

The signal to load SBUF and RB8, and to set RI, will be generated if, and only if, the following conditions are met at the time the final shift pulse is generated. 1. RI = 0, and 2. Either SM2 = 0, or the received 9th data bit = 1.

If either of these conditions is not met, the received frame is irretrievably lost, and RI is not set. If both conditions are met, the received 9th data bit goes into RB8, and the first 8 data bits go into SBUF. One bit time later, whether the above conditions were met or not, the unit goes back to looking for a 1-to-0 transition at the RxD input.

Multiprocessor Communications

UART modes 2 and 3 have a special provision for multiprocessor communications. In these modes, 9 data bits are received or transmitted. When data is received, the 9th bit is stored in RB8. The UART can be programmed such that when the stop bit is received, the serial port interrupt will be activated only if RB8 = 1. This feature is enabled by setting bit SM2 in SCON. One way to use this feature in multiprocessor systems is as follows:

When the master processor wants to transmit a block of data to one of several slaves, it first sends out an address byte which identifies the target slave. An address byte differs from a data byte in that the 9th bit is 1 in an address byte and 0 in a data byte. With SM2 = 1, no slave will be interrupted by a data byte. An address byte, however, will interrupt all slaves, so that each slave can examine the received byte and see if it is being addressed. The addressed slave will clear its SM2 bit and prepare to receive the data bytes that follow. The slaves that weren’t being addressed leave their SM2 bits set and go on about their business, ignoring the subsequent data bytes.

SM2 has no effect in Mode 0, and in Mode 1 can be used to check the validity of the stop bit, although this is better done with the Framing Error flag. In a Mode 1 reception, if SM2 = 1, the receive interrupt will not be activated unless a valid stop bit is received.

EPROM Characteristics

Programming of the EPROM on the P87LPC760 is accomplished with a serial programming method. Commands, addresses, and data are transmitted to and from the device on two pins after programming mode is entered. Serial programming allows easy implementation of In-System Programming of the P87LPC760 in an application board. Details of In-System Programming can be found in application note AN466.

The P87LPC760 contains three signature bytes that can be read and used by an EPROM programming system to identify the device. The signature bytes designate the device as an P87LPC760 manufactured by Philips. The signature bytes may be read by the user program at addresses FC30h, FC31h and FC60h with the MOVC instruction, using the DPTR register for addressing.

A special user data area is also available for access via the MOVC instruction at addresses FCE0h through FCFFh. This “customer code” space is programmed in the same manner as the main code EPROM and may be used to store a serial number, manufacturing date, or other application information.

32-Byte Customer Code Space

A small supplemental EPROM space is reserved for use by the customer in order to identify code revisions, store checksums, add a serial number to each device, or any other desired use. This area exists in the code memory space from addresses FCE0h through FCFFh. Code execution from this space is not supported, but it may be read as data through the use of the MOVC instruction with the appropriate addresses. The memory may be programmed at the same time as the rest of the code memory and UCFG bytes are programmed.

System Configuration Bytes

A number of user configurable features of the P87LPC760 must be defined at power up and therefore cannot be set by the program after start of execution. Those features are configured through the use of two EPROM bytes that are programmed in the same manner as the EPROM program space. The contents of the two configuration bytes, UCFG1 and UCFG2, are shown in Figures 39 and 40. The values of these bytes may be read by the program through the use of the MOVX instruction at the addresses shown in the figure.

UCFG1 Address: FD00h Unprogrammed Value: FFh

7	6	5	4	3	2	1	0
WDTE	RPD	PRHI	BOV	CLKR	FOSC2	FOSC1	FOSC0

BIT	SYMBOL	FUNCTION
UCFG1.7	WDTE	Watchdog timer enable. When programmed (0), disables the watchdog timer. The timer may still be used to generate an interrupt.
UCFG1.6	RPD	Reset pin disable. When 1 disables the reset function of pin P1.5, allowing it to be used as an input only port pin.
UCFG1.5	PRHI	Port reset high. When 1, ports reset to a high state. When 0, ports reset to a low state.
UCFG1.4	BOV	Brownout voltage select. When 1, the brownout detect voltage is 2.5V. When 0, the brownout detect voltage is 3.8V. This is described in the Power Monitoring Functions section.
UCFG1.3	CLKR	Clock rate select. When 0, the CPU clock rate is divided by 2. This results in machine cycles taking 12 CPU clocks to complete as in the standard 80C51. For full backward compatibility, this division applies to peripheral timing as well.
UCFG1.2–0	FOSC2–FSOC0	CPU oscillator type select. See Oscillator section for additional information. Combinations other than those shown below should not be used. They are reserved for future use.
	FOSC2–FOSC0	Oscillator Configuration
	1 1 1	External clock input on X1 (default setting for an unprogrammed part).
	0 1 1	Internal RC oscillator, 6 MHz. For tolerance, see AC Electrical Characteristics table.
	0 1 0	Low frequency crystal, 20 kHz to 100 kHz.
	0 0 1	Medium frequency crystal or resonator, 100 kHz to 4 MHz.
	0 0 0	High frequency crystal or resonator, 4 MHz to 20 MHz.

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Figure 39. EPROM System Configuration Byte 1 (UCFG1)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Operating temperature under bias	–55 to +125	°C
Storage temperature range	–65 to +150	°C
Voltage on $\overline{RST}/V_{PP}$ pin to V_{SS}	0 to +11.0	V
Voltage on any other pin to V_{SS}	–0.5 to V_{DD}+0.5V	V
Maximum I_{OL} per I/O pin	20	mA
Power dissipation (based on package heat transfer, not device power consumption)	1.5	W

NOTES:
1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions other than those described in the AC and DC Electrical Characteristics section of this specification are not implied.
2. This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.
3. Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to VSS unless otherwise noted.

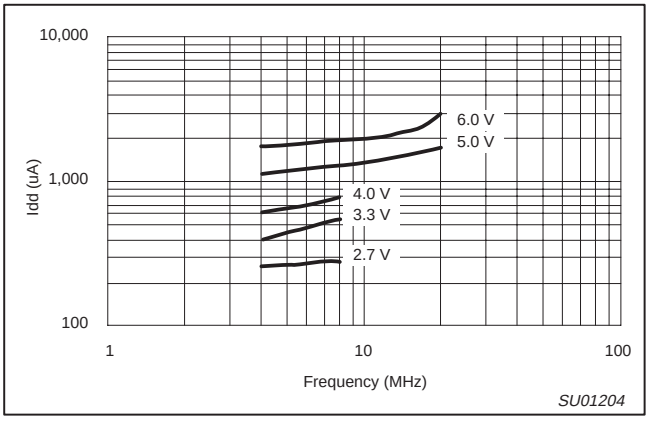


Figure 45. Typical Idd versus frequency (high frequency oscillator, 25 °C)

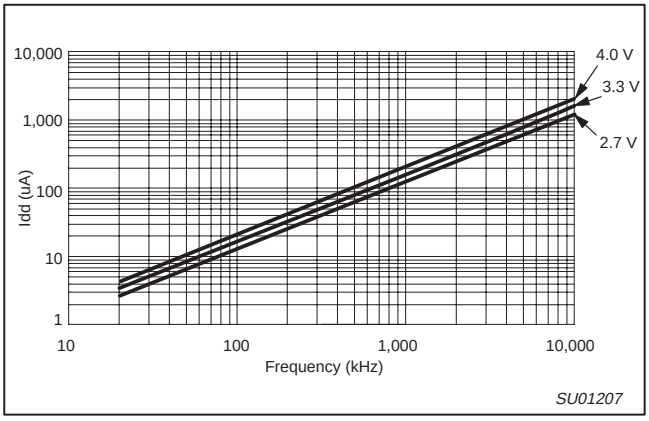


Figure 48. Typical Idle Idd versus frequency (external clock, 25 °C, LPEP=1)

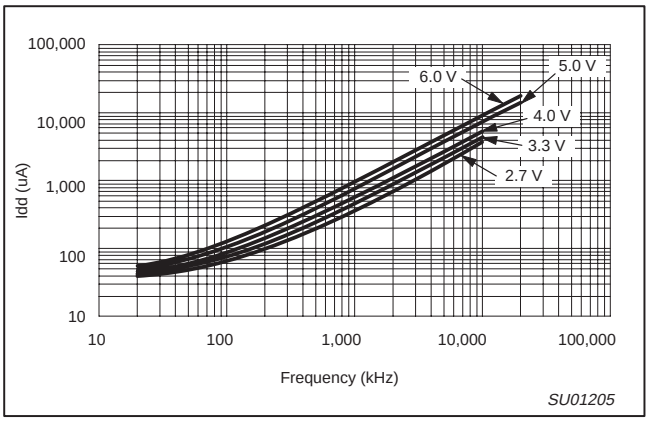


Figure 46. Typical Active Idd versus frequency (external clock, 25 °C, LPEP=0)

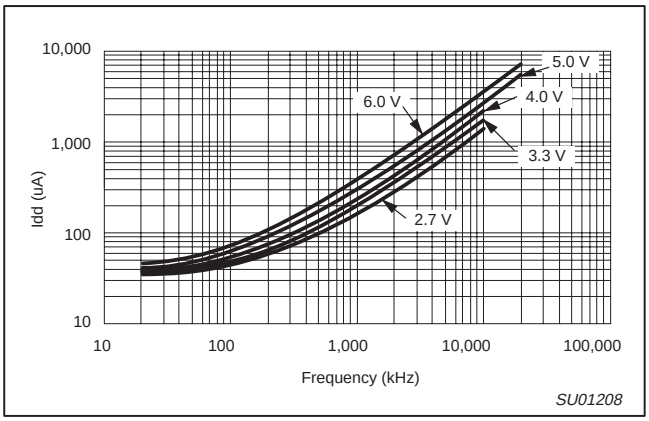


Figure 49. Typical Idle Idd versus frequency (external clock, 25 °C, LPEP=0)

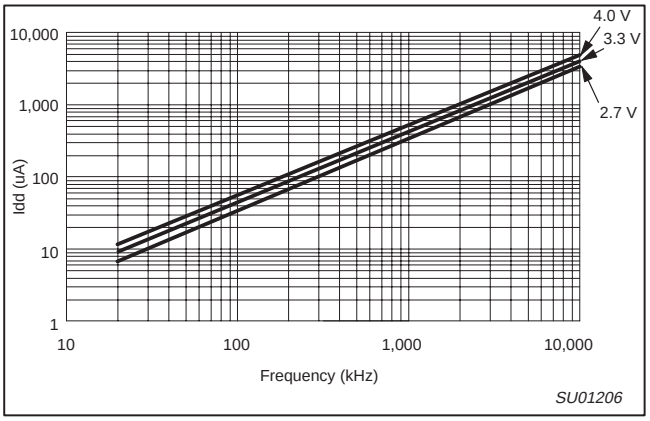
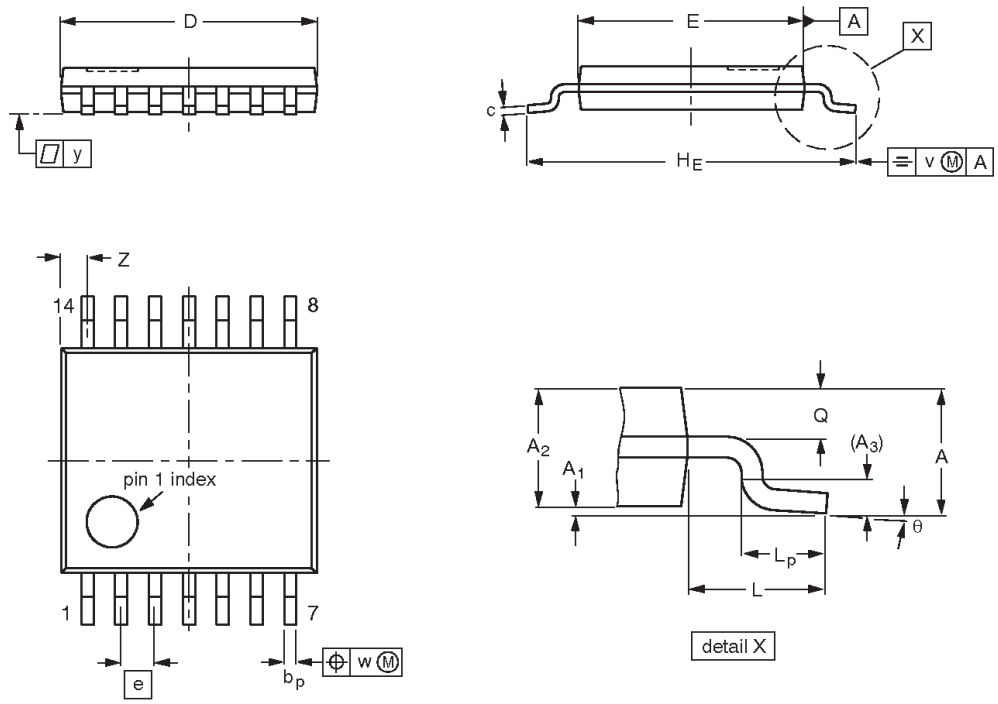
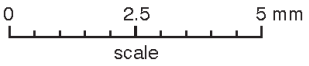


Figure 47. Typical Active Idd versus frequency (external clock, 25 °C, LPEP=1)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm SOT402-1





DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT402-1		MO-153				~~95-04-04~~ 99-12-27

Low power, low price, low pin count (14 pin) microcontroller with 1 kbyte OTP

P87LPC760

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specifications defined by Philips. This specification can be ordered using the code 9398 393 40011.

Data sheet status

Data sheet status[1]	Product status[2]	Definitions
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Changes will be communicated according to the Customer Product/Process Change Notification (CPCN) procedure SNW-SQ-650A.

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

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