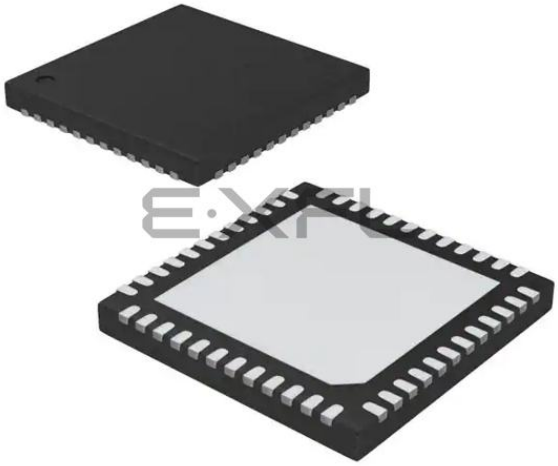

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	42MHz
Connectivity	EBI/EMI, I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	38
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 7x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	48-QFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/nano100nc2bn

LIST OF FIGURES

2 FEATURES

The equipped features are dependent on the product line and their sub products.

2.1 Nano100 Features – Base Line

- Core
  - ARM® Cortex™-M0 core running up to 42 MHz
  - One 24-bit system timer
  - Supports Low Power Sleep mode
  - Single-cycle 32-bit hardware multiplier
  - NVIC for the 32 interrupt inputs, each with 4-levels of priority
  - Serial Wire Debug supports with 2 watchpoints/4 breakpoints
- Brown-out
  - Built-in 2.5V/2.0V/1.7V BOD for wide operating voltage range operation
- Flash EPROM Memory
  - Runs up to 42 MHz with zero wait state for discontinuous address read access
  - 64K/32K/123K bytes application program memory (APROM)
  - 4 KB in system programming (ISP) loader program memory (LDROM)
  - Programmable data flash start address and memory size with 512 bytes page erase unit
  - In System Program (ISP)/In Application Program (IAP) to update on-chip Flash EPROM
- SRAM Memory
  - 16K/8K bytes embedded SRAM
  - Supports DMA mode
- DMA: Supports 8 channels: one VDMA channel, 6 PDMA channels and one CRC channel
  - VDMA
    - Memory-to-memory transfer
    - Supports block transfer with stride
    - Supports word/half-word/byte boundary address
    - Supports address direction: increment and decrement
  - PDMA
    - Peripheral-to-memory, memory-to-peripheral, and memory-to-memory transfer
    - Supports word boundary address
    - Supports word alignment transfer length in memory-to-memory mode
    - Supports word/half-word/byte alignment transfer length in peripheral-to-memory and memory-to-peripheral mode

- WDT can wake system up from Power-down mode

- Window Watchdog Timer(WWDT)
  - 6-bit down counter and 6-bit compare value to make the window period flexible
  - Selectable WWDT clock pre-scale counter to make WWDT time-out interval variable.

- RTC
  - Supports software compensation by setting frequency compensate register (FCR)
  - Supports RTC counter (second, minute, hour) and calendar counter (day, month, year)
  - Supports Alarm registers (second, minute, hour, day, month, year)
  - Selectable 12-hour or 24-hour mode
  - Automatic leap year recognition
  - Supports periodic time tick interrupt with 8 periodic options 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2 and 1 second
  - Wake system up from Power-down or Idle mode
  - Supports 80 bytes spare registers and a snoop pin to clear the content of these spare registers

- PWM/Capture
  - Supports 2 PWM module, each with two 16-bit PWM generators
  - Provides eight PWM outputs or four complementary paired PWM outputs
  - Each PWM generator equipped with one clock divider, one 8-bit prescaler, two clock selectors, and one Dead-Zone generator for complementary paired PWM
  - (Shared with PWM timers) with eight 16-bit digital capture timers provides eight rising/ falling/both capture inputs.
  - Supports Capture interrupt

- UART
  - Up to two 16-byte FIFO UART controllers
  - UART ports with flow control (TX, RX, CTSn and RTSn)
  - Supports IrDA (SIR) function
  - Supports LIN function
  - Supports RS-485 9 bit mode and direction control (Low Density Only)
  - Programmable baud rate generator
  - Supports PDMA mode
  - Wake system up from Power-down or Idle mode

- SPI
  - Up to 3 sets of SPI controller
  - Master up to 32 MHz, and Slave up to 16 MHz
  - Supports SPI/MICROWIRE Master/Slave mode

- Full duplex synchronous serial data transfer
- Variable length of transfer data from 4 to 32 bits
- MSB or LSB first data transfer
- RX and TX on both rising or falling edge of serial clock independently
- Two slave/device select lines when used as the master, and 1 slave/device select line when used as the slave
- Supports byte suspend mode in 32-bit transmission
- Supports two channel PDMA request, one for transmit and another for receive
- Supports three wire, no slave select signal, bi-direction interface
- Wake system up from Power-down or Idle mode

- I^2C
  - Up to two sets of I^2C device
  - Master/Slave up to 1Mbit/s
  - Bi-directional data transfer between masters and slaves
  - Multi-master bus (no central master)
  - Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
  - Serial clock synchronization allowing devices with different bit rates to communicate via one serial bus
  - Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer
  - Built-in 14-bit time-out counter will request the I^2C interrupt if the I^2C bus hangs up and timer-out counter overflows
  - Programmable clocks allowing for versatile rate control
  - Supports 7-bit addressing mode
  - Supports multiple address recognition (four slave addresses with mask option)
- I^2S
  - Interface with external audio CODEC
  - Operate as either Master or Slave mode
  - Capable of handling 8, 16, 24 and 32 bit word sizes
  - Supports Mono and stereo audio data
  - Supports I^2S and MSB justified data format
  - Provides two 8 word FIFO data buffers: one for transmitting and the other for receiving
  - Generates interrupt requests when buffer levels cross a programmable boundary
  - Supports two PDMA requests: one for transmitting and the other for receiving
- ADC
  - 12-bit SAR ADC up to 2Msps conversion rate

3.3.2 NuMicro™ Nano110 Pin Diagrams

3.3.2.1 NuMicro™ Nano110 LQFP 128-pin

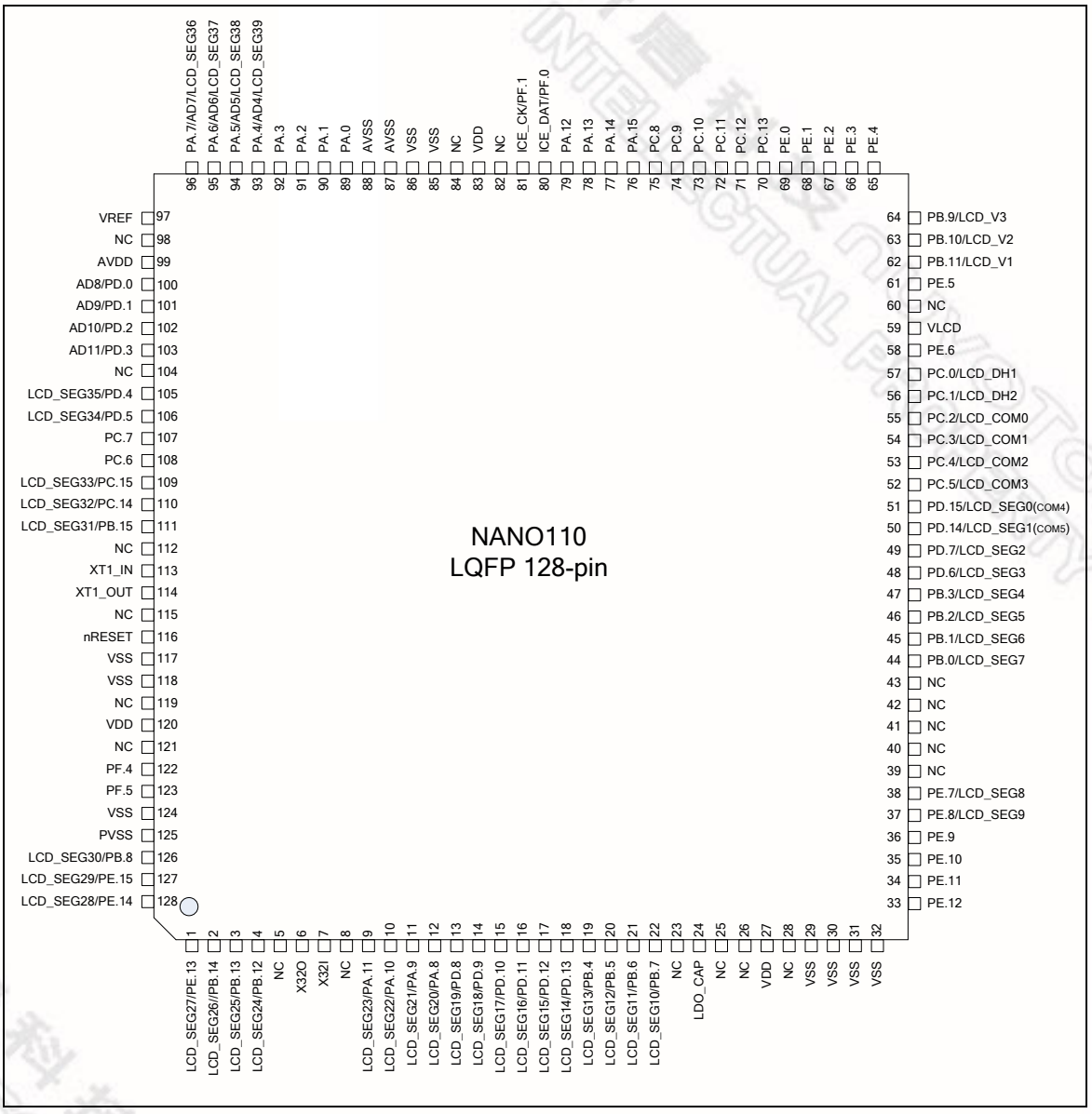


Figure 3-5 NuMicro™ Nano110 LQFP 128-pin Diagram

Pin No.			Pin Name	Pin Type	Description
LQFP 128-pin	LQFP 64-pin	LQFP/QFN 48-pin			
			AD0	**AI**	ADC analog input0
			SC2_CD	**I**	SmartCard2 card detect
90	45	33	PA.1	**I/O**	General purpose digital I/O pin
			AD1	**AI**	ADC analog input1
			EBI_AD12	**I/O**	EBI Address/Data bus bit12
91	46	34	PA.2	**I/O**	General purpose digital I/O pin
			AD2	**AI**	ADC analog input2
			EBI_AD11	**I/O**	EBI Address/Data bus bit11
			UART1_RXD	**I**	UART1 Data receiver input pin
92	47	35	PA.3	**I/O**	General purpose digital I/O pin
			AD3	**AI**	ADC analog input3
			EBI_AD10	**I/O**	EBI Address/Data bus bit10
			UART1_TXD	**O**	UART1 Data transmitter output pin
93	48	36	PA.4	**I/O**	General purpose digital I/O pin
			AD4	**AI**	ADC analog input4
			EBI_AD9	**I/O**	EBI Address/Data bus bit9
			SC2_PWR	**O**	SmartCard2 Power pin
			I2C0_SDA	**I/O**	I^2C0 data I/O pin
94	49	37	PA.5	**I/O**	General purpose digital I/O pin
			AD5	**AI**	ADC analog input5
			EBI_AD8	**I/O**	EBI Address/Data bus bit8
			SC2_RST	**O**	SmartCard2 RST pin
			I2C0_SCL	**I/O**	I^2C0 clock pin
95	50	38	PA.6	**I/O**	General purpose digital I/O pin
			AD6	**AI**	ADC analog input6
			EBI_AD7	**I/O**	EBI Address/Data bus bit7
			TC3	**I**	Timer3 capture input
			SC2_CLK	**O**	SmartCard2 clock pin(SC2_UART_TXD)
			PWM0_CH3	**O**	PWM0 Channel3 output
96			PA.7	**I/O**	General purpose digital I/O pin

Pin No.			Pin Name	Pin Type	Description
LQFP 128-pin	LQFP 64-pin	LQFP/QFN 48-pin			
104					NC
105			PD.4	**I/O**	General purpose digital I/O pin
			I2S_DI	**I**	I^2S data input
			SPI2_MISO1	**I/O**	SPI2 2nd MISO (Master In, Slave Out) pin
			SC1_CD	**I**	SmartCard1 card detect
106			PD.5	**I/O**	General purpose digital I/O pin
			I2S_DO	**O**	I^2S data output
			SPI2_MOSI1	**I/O**	SPI2 2nd MOSI (Master Out, Slave In) pin
107	53	41	PC.7	**I/O**	General purpose digital I/O pin
			DA1_OUT	**AO**	DAC 1 output
			EBI_AD5	**I/O**	EBI Address/Data bus bit5
			TC1	**I**	Timer1 capture input
			PWM0_CH1	**O**	PWM1 Channel1 output
108	54	42	PC.6	**I/O**	General purpose digital I/O pin
			DA0_OUT	**I**	DAC0 output
			EBI_AD4	**I/O**	EBI Address/Data bus bit4
			TC0	**I**	Timer0 capture input
			SC1_CD	**I**	SmartCard1 card detect pin
			PWM0_CH0	**O**	PWM0 Channel0 output
109	55		PC.15	**I/O**	General purpose digital I/O pin
			EBI_AD3	**I/O**	EBI Address/Data bus bit3
			TC0	**I**	Timer0 capture input
			PWM1_CH2	**O**	PWM1 Channel1 output
110	56		PC.14	**I/O**	General purpose digital I/O pin
			EBI_AD2	**I/O**	EBI Address/Data bus bit2
			PWM1_CH3	**I/O**	PWM1 Channel3 output
111	57	43	PB.15	**I/O**	General purpose digital I/O pin
			INT1	**I**	External interrupt1 input pin
			SNOOPER	**I**	Snooper pin
			SC1_CD	**I**	SmartCard1 card detect

Pin No.			Pin Name	Pin Type	Description
LQFP 128-pin	LQFP 64-pin	LQFP 48-pin			
10	7		PA.10	I/O	General purpose digital I/O pin
			I2C1_SDA	I/O	I^2C1 data I/O pin
			EBI_nWR	O	EBI write enable output pin
			SC0_PWR	O	SmartCard0 Power pin
			SPI2_MISO0	I/O	SPI2 1st MISO (Master In, Slave Out) pin
			LCD_SEG8	O	LCD segment output 8 at LQFP64
			LCD_SEG22	O	LCD segment output 22 at LQFP128
11	8		PA.9	I/O	General purpose digital I/O pin
			I2C0_SCL	I/O	I^2C0 clock pin
			SC0_DAT	I/O	SmartCard0 DATA pin(SC0_UART_RXD)
			SPI2_CLK	I/O	SPI2 serial clock pin
			LCD_SEG7	O	LCD segment output 7 at LQFP64
			LCD_SEG21	O	LCD segment output 21 at LQFP128
12	9		PA.8	I/O	General purpose digital I/O pin
			I2C0_SDA	I/O	I^2C0 data I/O pin
			SC0_CLK	O	SmartCard0 clock pin(SC0_UART_TXD)
			SPI2_SS0	I/O	SPI2 1st slave select pin
			LCD_SEG6	O	LCD segment output 6 at LQFP64
			LCD_SEG20	O	LCD segment output 20 at LQFP128
13			PD.8	I/O	General purpose digital I/O pin
			LCD_SEG19	O	LCD segment output 19 at LQFP128
14			PD.9	I/O	General purpose digital I/O pin
			LCD_SEG18	O	LCD segment output 18 at LQFP128
15			PD.10	I/O	General purpose digital I/O pin
			LCD_SEG17	O	LCD segment output 17 at LQFP128
16			PD.11	I/O	General purpose digital I/O pin
			LCD_SEG16	O	LCD segment output 16 at LQFP128
17			PD.12	I/O	General purpose digital I/O pin
			LCD_SEG15	O	LCD segment output 15 at LQFP128
18			PD.13	I/O	General purpose digital I/O pin

Pin No.			Pin Name	Pin Type	Description
LQFP 128-pin	LQFP 64-pin	LQFP 48-pin			
68			PE.1	**I/O**	General purpose digital I/O pin
			PWM1_CH3	**I/O**	PWM1 Channel3 output
			SPI0_SS0	**I/O**	SPI0 1st slave select pin
69			PE.0	**I/O**	General purpose digital I/O pin
			PWM1_CH2	**I/O**	PWM1 Channel2 output
			I2S_MCLK	**O**	I2S master clock output pin
70			PC.13	**I/O**	General purpose digital I/O pin
			SPI1_MOSI1	**I/O**	SPI1 2nd MOSI (Master Out, Slave In) pin
			PWM1_CH1	**O**	PWM1 Channel1 output
			SNOOPER	**I**	Snooper pin
			INT1	**I**	External interrupt 1
			I2C0_SCL	**O**	I2C0 clock pin
71			PC.12	**I/O**	General purpose digital I/O pin
			SPI1_MISO1	**I/O**	SPI1 2nd MISO (Master In, Slave Out) pin
			PWM1_CH0	**O**	PWM1 Channel0 output
			INT0	**I**	External interrupt0 input pin
			I2C0_SDA	**I/O**	I2C0 data I/O pin
72	33		PC.11	**I/O**	General purpose digital I/O pin
			SPI1_MOSI0	**I/O**	SPI1 1st MOSI (Master Out, Slave In) pin
			UART1_TXD	**O**	UART1 Data transmitter output pin
			LCD_SEG31	**O**	LCD segment output 31 at LQFP64
73	34		PC.10	**I/O**	General purpose digital I/O pin
			SPI1_MISO0	**I/O**	SPI1 1st MISO (Master In, Slave Out) pin
			UART1_RXD	**I**	UART1 Data receiver input pin
			LCD_SEG30	**O**	LCD segment output 30 at LQFP64
74	35		PC.9	**I/O**	General purpose digital I/O pin
			SPI1_CLK	**I/O**	SPI1 serial clock pin
			I2C1_SCL	**I/O**	I2C1 clock pin
			LCD_SEG29	**O**	LCD segment output 29 at LQFP64
75	36		PC.8	**I/O**	General purpose digital I/O pin

3.4.3 NuMicro™ Nano120 Pin Description

Pin No.			Pin Name	Pin Type	Description
LQFP 128	LQFP 64	LQFP 48			
1			PE.13	**I/O**	General purpose digital IO pin
2	1		PB.14	**I/O**	General purpose digital IO pin
			INT0	**I**	External interrupt0 input pin
			SC2_CD	**I**	SmartCard2 card detect
			SPI2_SS1	**I/O**	SPI2 2nd slave select pin
3	2		PB.13	**I/O**	General purpose digital IO pin
			EBI_AD1	**I/O**	EBI Address/Data bus bit1
4	3	1	PB.12	**I/O**	General purpose digital IO pin
			EBI_AD0	**I/O**	EBI Address/Data bus bit0
			FCLKO	**O**	Frequency Divider output pin
5					NC
6	4	2	X32O	**O**	External 32.768 kHz crystal output pin
7	5	3	X32I	**I**	External 32.768 kHz crystal input pin
8					NC
9	6	4	PA.11	**I/O**	General purpose digital IO pin
			I2C1_SCL	**I/O**	I2C 1 clock pin
			EBI_nRD	**O**	EBI read enable output pin
			SC0_RST	**O**	SmartCard0 RST pin
			SPI2_MOSI0	**I/O**	SPI2 1st MOSI (Master Out, Slave In) pin
10	7	5	PA.10	**I/O**	General purpose digital IO pin
			I2C1_SDA	**I/O**	I2C 1 data I/O pin
			EBI_nWR	**O**	EBI write enable output pin
			SC0_PWR	**O**	SmartCard0 Power pin
			SPI2_MISO0	**I/O**	SPI2 1st MISO (Master In, Slave Out) pin
11	8	6	PA.9	**I/O**	General purpose digital IO pin
			I2C0_SCL	**I/O**	I2C 0 clock pin
			SC0_DAT	**I/O**	SmartCard0 DATA pin(SC0_UART_RXD)
			SPI2_CLK	**I/O**	SPI2 serial clock pin

Pin No.			Pin Name	Pin Type	Description
LQFP 128-pin	LQFP 64-pin	LQFP 48-pin			
			LCD_SEG14	O	LCD segment output 14 at LQFP128
19	10		PB.4	I/O	General purpose digital I/O pin
			UART1_RXD	I	UART1 Data receiver input pin
			SC0_CD	I	SmartCard0 card detect pin
			SPI2_SS0	I/O	SPI2 1st slave select pin
			LCD_SEG5	O	LCD segment output 5 at LQFP64
			LCD_SEG13	O	LCD segment output 13 at LQFP128
20	11		PB.5	I/O	General purpose digital I/O pin
			UART1_TXD	O	UART1 Data transmitter output pin
			SC0_RST	O	SmartCard0 RST pin
			SPI2_CLK	I/O	SPI2 serial clock pin
			LCD_SEG4	O	LCD segment output 4 at LQFP64
			LCD_SEG12	O	LCD segment output 12 at LQFP128
21	12		PB.6	I/O	General purpose digital I/O pin
			UART1_RTSn	O	UART1 Request to Send output pin
			EBI_ALE	O	EBI address latch enable output pin
			SPI2_MISO0	I/O	SPI2 1st MISO (Master In, Slave Out) pin
			LCD_SEG3	O	LCD segment output 3 at LQFP64
			LCD_SEG11	O	LCD segment output 11 at LQFP128
22	13		PB.7	I/O	General purpose digital I/O pin
			UART1_CTSn	I	UART1 Clear to Send input pin
			EBI_nCS	O	EBI chip select enable output pin
			SPI2_MOSI0	I/O	SPI2 1st MOSI (Master Out, Slave In) pin
			LCD_SEG2	O	LCD segment output 2 at LQFP64
			LCD_SEG10	O	LCD segment output 10 at LQFP128
23					NC
24	14		LDO_CAP	P	LDO output pin
25					NC
26					NC
27	15		VDD	P	Power supply for I/O ports and LDO source

Pin No.			Pin Name	Pin Type	Description
LQFP 128-pin	LQFP 64-pin	LQFP 48-pin			
28					NC
29	16		VSS	P	Ground
30			VSS	P	Ground
31			VSS	P	Ground
32			VSS	P	Ground
33			PE.12	I/O	General purpose digital I/O pin
34			PE.11	I/O	General purpose digital I/O pin
35			PE.10	I/O	General purpose digital I/O pin
36			PE.9	I/O	General purpose digital I/O pin
37			PE.8	I/O	General purpose digital I/O pin
			LCD_SEG9	O	LCD segment output 9 at LQFP128
38			PE.7	I/O	General purpose digital I/O pin
			LCD_SEG8	O	LCD segment output 8 at LQFP128
39					NC
40	17		USB_VBUS	USB	POWER SUPPLY: From USB Host or HUB.
41	18		USB_VDD33_CAP	USB	Internal Power Regulator Output 3.3V Decoupling Pin
42	19		USB_D-	USB	USB Differential Signal D-
43	20		USB_D+	USB	USB Differential Signal D+
44	21		PB.0	I/O	General purpose digital I/O pin
			UART0_RXD	I	UART0 Data receiver input pin
			SPI1_MOSI0	I/O	SPI1 1st MOSI (Master Out, Slave In) pin
			LCD_SEG1	O	LCD segment output 1 at LQFP64 (or as LCD_COM5)
			LCD_SEG7	O	LCD segment output 7 at LQFP128
45	22		PB.1	I/O	General purpose digital I/O pin
			UART0_TXD	O	UART0 Data transmitter output pin
			SPI1_MISO0	I/O	SPI1 1st MISO (Master In, Slave Out) pin
			LCD_SEG0	O	LCD segment output 0 at LQFP64 (or as LCD_COM4)
			LCD_SEG6	O	LCD segment output 6 at LQFP128
46	23		PB.2	I/O	General purpose digital I/O pin

5.5 Analog to Digital Converter (ADC)

5.5.1 Overview

This chip contains one 12-bit successive approximation analog-to-digital converter (SAR A/D converter) with 12 external input channels and 6 internal channels. The A/D converter supports three operation modes: Single, Single-cycle Scan and Continuous Scan mode, and can be started by software and external STADC/PB.8 pin and timer event start.

Note that the I/O pins used as ADC analog input pins must be configured as input type and off digital function (GPIOA_OFFD) should be turned on before ADC function is enabled.

5.5.2 Features

- Analog input voltage range: 0~Vref (Max to 3.6V)
- Selectable 12-bits, 10-bits, 8-bits and 6-bits resolution
- Supports sampling time settings (in ADC_CLK unit) for channel 0~11 individually and channel 12~17 share the same one sampling time setting
- Supports two power-down modes:
  - Power-down mode
  - Standby mode
- Up to 12 external analog input channels (channel0 ~ channel11), and 6 internal channels (channel12~channel17) converting six voltage sources, including DAC0, DAC1, internal band-gap voltage, internal temperature sensor output, AVDD, and AVSS.
- Maximum ADC clock frequency is 42 MHz and each conversion is 19 clocks+ sampling time depending on the input resistance.
- Three operating modes
  - Single mode: A/D conversion is performed one time on a specified channel.
  - Single-cycle Scan mode: A/D conversion is performed one cycle on all specified channels with the sequence from the lowest numbered channel to the highest numbered channel.
  - Continuous Scan mode: A/D converter continuously performs Single-cycle scan mode until software stops A/D conversion.
- An A/D conversion can be started by:
  - Software write 1 to ADST bit
  - External pin STADC
  - Selects one from four timer events (TMR0, TMR1, TMR2 and TMR3) that enable ADC and transfer AD results by PDMA
- Conversion results held in data registers for each channel
- Conversion result can be compared with a specified value and user can select whether to generate an interrupt when conversion result is equal to the compare register setting.
- Supports Calibration and load Calibration words capability.

5.7 DMA Controller

5.7.1 Overview

The DMA controller contains six channel peripheral direct memory access (PDMA) controllers, a video direct memory access (VDMA) controller and a cyclic redundancy check (CRC) generator. The PDMA controller can transfer data to and from memory or transfer data to and from APB devices. The DMA has eight channels of DMA including one channel VDMA (Memory-to-Memory) and six channels PDMA (Peripheral-to-Memory or Memory-to-Peripheral or Memory-to-Memory) and a CRC controller. For channel0 VDMA, it supports block transfer from memory to memory. For PDMA channel (DMA CH1~CH6), there is one-word buffer as transfer buffer between the Peripherals APB devices and Memory. And for channel 0 VDMA, there is a two-word buffer.

Software can stop the DMA operation by disable PDMA [PDMACEN]/VDMA [VDMACEN]. Software can recognize the completion of a DMA operation by software polling or when it receives an internal DMA interrupt. The DMA controller can increase source or destination address, fixed or wrap around them as well.

The DMA controller also contains a cyclic redundancy check (CRC) generator that can perform CRC calculation with programmable polynomial settings. The CRC engine support CPU PIO mode and DMA transfer mode.

5.7.2 Features

Seven DMA channels and a CRC generator: 1 VDMA channel and 6 PDMA channels. Each channel can support a unidirectional transfer.

AMBA AHB master/slave interface compatible, for data transfer and register read/write.

Hardware round robin priority scheme.

- VDMA
  - Memory-to-memory transfer
  - Supports block transfer with stride
  - Supports word/half-word/byte boundary address
  - Supports address direction: increment and decrement
- PDMA
  - Peripheral-to-memory, memory-to-peripheral, and memory-to-memory transfer
  - Supports word boundary address
  - Supports word alignment transfer length in memory-to-memory mode
  - Supports word/half-word/byte alignment transfer length in peripheral-to-memory and memory-to-peripheral mode
  - Supports word/half-word/byte transfer data width from/to peripheral
  - Supports address direction: increment, fixed, and wrap around
- Cyclic Redundancy Check (CRC)
  - Supports four common polynomials CRC-CCITT, CRC-8, CRC-16, and CRC-32
    - CRC-CCITT: $X^{16} + X^{12} + X^5 + 1$
    - CRC-8: $X^8 + X^2 + X + 1$
    - CRC-16: $X^{16} + X^{15} + X^2 + 1$

5.14.2 Features

5.14.2.1 PWM Function:

- Two PWM controllers, each controller having 4 independent PWM outputs, CH0~CH3, or as 2 complementary PWM pairs, (CH0, CH1), (CH2, CH3) with 2 programmable dead-zone generators
- Up to 8 PWM channels or 4 PWM paired channels
- Up to 16 bits PWM counter width
- PWM Interrupt request synchronous with PWM period
- Single-shot or Continuous mode
- Four Dead-Zone generators

5.14.2.2 Capture Function:

- Timing control logic shared with PWM timer.
- 8 Capture input channels shared with 8 PWM output channels.
- Each channel supports one rising latch register (PWMx_CRLy), one falling latch register (PWMx_CFLy) and Capture interrupt flag (CAPIFy) where x=0~1,y=0~3.
- Eight 16-bit counters for eight capture channels or four 32-bit counter for four capture channels when cascade is enabled: when CH01CASKEN is set, the original 16-bit counter of channel 1 will combine with channel 0's 16 bit counter for channel 0 input capture counting and so does CH23CASKEN for channel 2, 3
- Supports PDMA transfer function for PWMx channel 0, 2

6 ARM® CORTEX™-M0 CORE

6.1 Overview

The Cortex™-M0 processor is a configurable, multistage, 32-bit RISC processor. It has an AMBA AHB-Lite interface and includes an NVIC component. It also has optional hardware debug functionality. The processor can execute Thumb code and is compatible with other Cortex-M profile processor. The profile supports two modes – Thread mode and Handler mode. Handler mode is entered as a result of an exception. An exception return can only be issued in Handler mode. Thread mode is entered on Reset, and can be entered as a result of an exception return. The following figure shows the functional controller of processor.

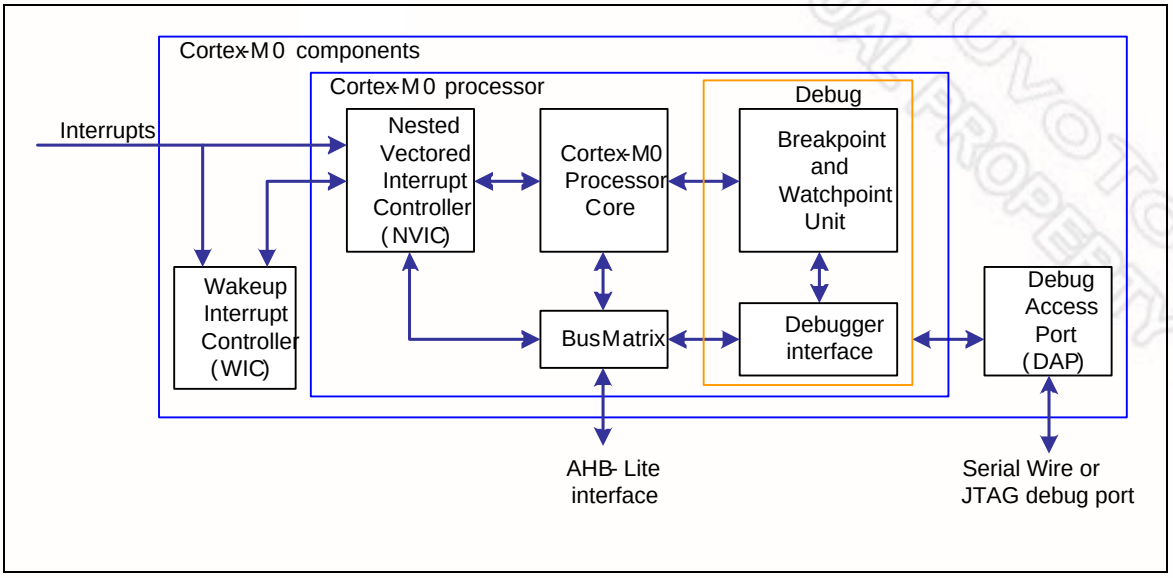
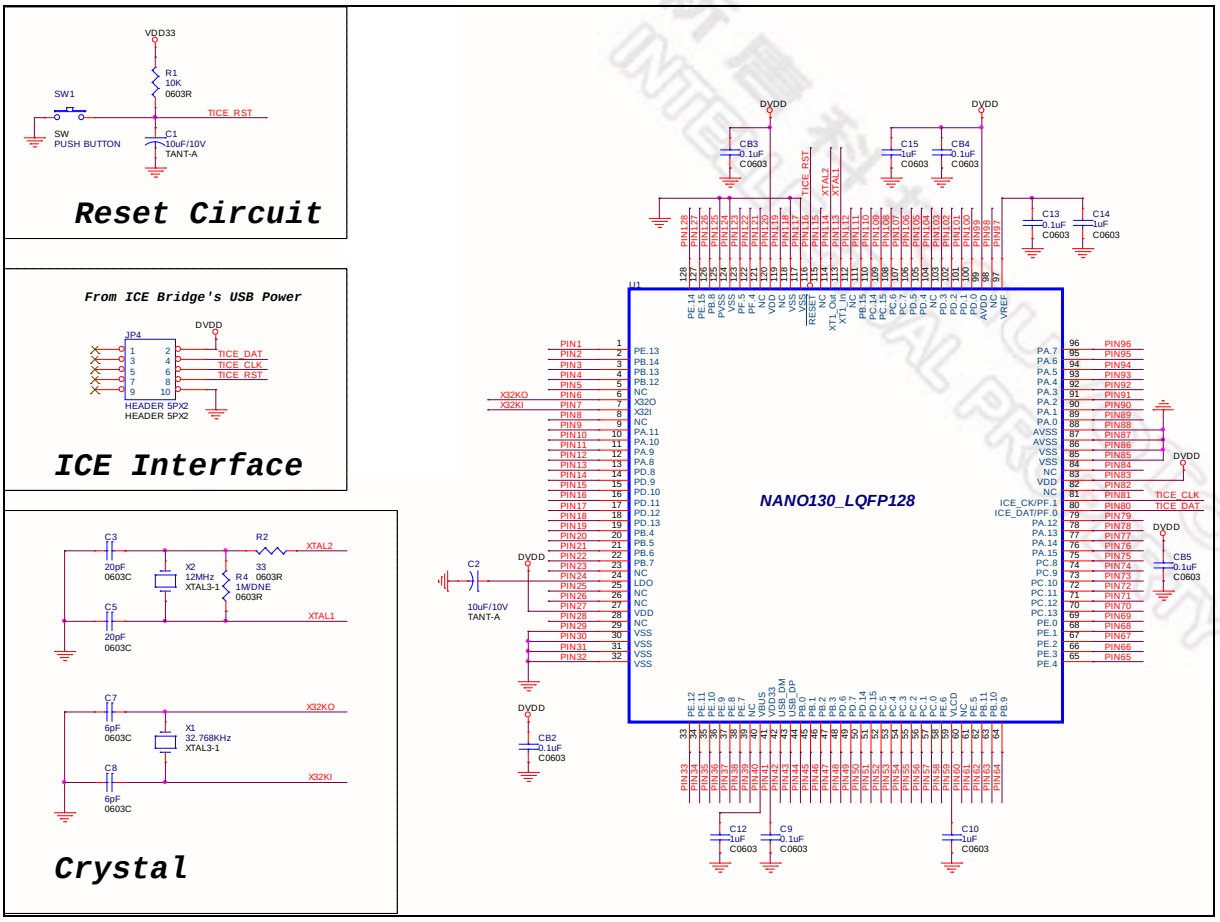


Figure 6-1 M0 Functional Block

6.2 Features

- A low gate count processor:
  - ARMv6-M Thumb® instruction set
  - Thumb-2 technology
  - ARMv6-M compliant 24-bit SysTick timer
  - A 32-bit hardware multiplier
  - Supports little-endian data accesses
  - Capable of deterministic, fixed-latency, interrupt handling
  - Load/store-multiples and multi-cycle-multiplies that can be abandoned and restarted to facilitate rapid interrupt handling
  - C Application Binary Interface compliant exception model. This is the ARMv6-M, C Application Binary Interface (C-ABI) compliant exception model that enables the use of pure C functions as interrupt handlers
  - Low Power Sleep mode entry using Wait For Interrupt (WFI), Wait For Event (WFE) instructions, or return from interrupt sleep-on-exit feature

7.4 Whole Chip Application Circuit



8 POWER COMSUMPTION

Part No	Test Condition		VDD	CPU Clock	Current
Nano100 (B) series 128 KB Flash 16 KB RAM	**Operating Mode:** CPU run while(1) in FLASH ROM Clock = 12 MHz Crystal Oscillator Disable all peripherial		3.3V	12 MHz	2.41mA 200uA/MHz
			1.8V	12 MHz	N/A
	Idle Mode: CPU stop Clock = 12 MHz Crystal Oscillator Disable all peripherial		3.3V	12 MHz	900uA 75uA/MHz
			1.8V	12 MHz	N/A
	RTC + LCD Mode: (RAM retention) (Power down with 32K and LCD enabled) CPU stop Clock = 32.768 kHz Crystal Oscillator Disable all peripherial except RTC and LCD circuit Without panel loading	C-type	3.3V	-	10uA
		Internal R-type (With 200kΩ Resistor ladder)			8.5uA
		External R-type (With 1MΩ Resistor ladder)			4.5uA
		C-type/R-type	1.8V	-	N/A
	RTC Mode: (RAM retention) (Power down with 32K enabled) CPU stop Clock = 32.768 kHz Crystal Oscillator Disable all peripherial except RTC circuit		3.3V	-	2.5uA
			1.8V	-	2.0uA
	Power-down Mode: (RAM retention) CPU and all clocks stop		3.3V	-	1uA
			1.8V	-	0.8uA
	Wake-Up from Power-down Mode		3.3V	7us	N/A

Note: Wake-up time: 7us from wake-up event to first CPU core valid clock; 10us from interrupt event to interrupt service routine first instruction.

9.3.3 External 32.768 kHz Crystal

PARAMETER	SYM.	SPECIFICATIONS				TEST CONDITION
		MIN.	TYP.	MAX.	UNIT	
Oscillator frequency	f_{LXT}		32.768		kHz	VDD = 1.8V ~ 3.6V
Temperature	T_{LXT}	-40	-	+85	°C	
Operating current	I_{LXT}		1.2		μA	VDD = 3.0V

9.3.4 Internal 12 MHz Oscillator

PARAMETER	SYM.	SPECIFICATIONS				TEST CONDITION
		MIN.	TYP.	MAX.	UNIT	
Supply voltage[1]	V_{HRC}		1.8		V	
Calibrated Internal Oscillator Frequency	F_{HRC}	11.88	12	12.12	MHz	25°C, V_{DD} = 3V
		11.76	12	12.24	MHz	-40°C~+85 °C, V_{DD} = 1.8V~3.6V
		11.97	12	12.03	MHz	-40°C~+85 °C, V_{DD} = 1.8V~3.6V Enable 32.768K crystal oscillator and set TRIM_SEL[1:0]=”10”
Operating current	I_{HRC}		450		μA	

Note: Internal oscillator operation voltage comes from LDO.

9.3.5 Internal 10 kHz Oscillator

PARAMETER	SYM.	SPECIFICATIONS				TEST CONDITION
		MIN.	TYP.	MAX.	UNIT	
Supply voltage[1]	V_{LRC}		1.8		V	
Center Frequency	F_{LRC}	7	10	13	kHz	25°C, V_{DD} = 3V
		5	10	15	kμHz	-40°C~+85 °C, V_{DD} = 1.8V~3.6V
Operating current	I_{LRC}		0.7		μA	V_{DD} = 3V

Note: Internal oscillator operation voltage comes from LDO.

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