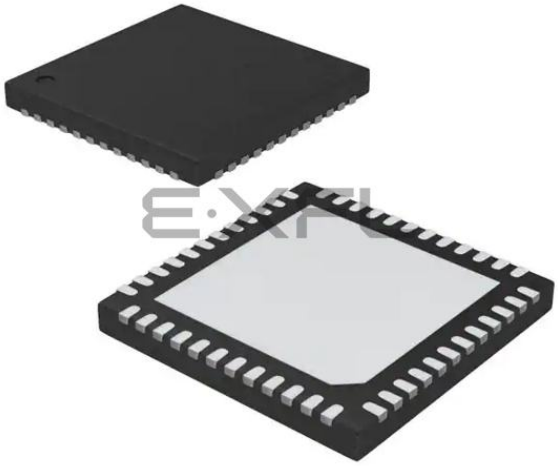


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	42MHz
Connectivity	EBI/EMI, I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	38
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 7x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	48-QFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/nano100nd2bn

LIST OF FIGURES

1 GENERAL DESCRIPTION

The Nano100 series ultra-low power 32-bit microcontroller is embedded with ARM® Cortex™-M0 core operated at a wide voltage range from 1.8V to 3.6V and runs up to 42 MHz frequency with 32K/64K/128K bytes embedded Flash and 8K/16K-byte embedded SRAM. Integrating LCD 4x40 or 6x38 (COM/Segment), USB 2.0 full-speed function, RTC, 12-bit SAR ADC, 12-bit DAC and provides high performance connectivity peripheral interfaces such as UART, SPI, I^2C, I^2S, GPIOs, EBI (External Bus Interface) for external memory-mapped device access and ISO-7816-3 for Smart card, the Nano100 series supports Brown-out Detector, Power-down mode with RAM retention and fast wake-up via many peripheral interfaces.

The Nano100 series provides low power voltage, low power consumption, low standby current, high integration peripherals, high-efficiency operation, fast wake-up function and the lowest cost 32-bit microcontrollers. The Nano100 series is suitable for a wide range of battery device applications such as:

- Portable Data Collector
- Portable Medical Monitor
- Portable RFID Reader
- Portable Barcode Scanner
- Security Alarm System
- System Supervisors
- Power Metering
- USB Accessories
- Smart Card Reader
- Wireless Game Control Device
- IPTV Remote Smart Keyboard
- Wireless Sensors Node Device (WSN)
- Wireless RF4CE Remote Control
- Wireless Audio
- Wireless Automatic Meter Reader (AMR)
- Electronic Toll Collection (ETC)

The Nano100 Base line, an ultra-low power 32-bit microcontroller with the embedded ARM® Cortex™-M0 core, operates at wide voltage range from 1.8V to 3.6V and runs up to 42 MHz frequency with 32K/64K/128K bytes embedded flash and 8K/16K bytes embedded SRAM. It integrates RTC, 12- channels 12-bit SAR ADC, 2-channels 12-bit DAC and provides high performance connectivity peripheral interfaces such as 2xUART, 3xSPI, $2xI^2C$, I^2S, GPIOs, EBI (External Bus Interface) for external memory-mapped device access and 3xISO-7816-3 for Smart card. The Nano100 Base line supports Brown-out Detector, Power-down mode with RAM retention and fast wake-up via many peripheral interfaces.

The Nano110 LCD line, an ultra-low power 32-bit microcontroller with the embedded ARM® Cortex™-M0 core, operates at wide voltage range from 1.8V to 3.6V and runs up to 42 MHz frequency with 32K/64K/128K bytes embedded flash and 8K/16K bytes embedded SRAM. It integrates LCD 4x40 or 6x38 (COM/Segment). RTC, 12-channels 12-bit SAR ADC, 2-channels 12-bit DAC and provides high performance connectivity peripheral interfaces such as 2xUART, 2xSPI, $2xI^2C$, I^2S, GPIOs, EBI (External Bus Interface) for external memory-mapped device access and 3xISO-7816-3 for Smart card. The Nano110 LCD line supports Brown-out Detector,

- Wake system up from Power-down mode

- SPI
  - Up to three sets of SPI controller
  - Master up to 32 MHz, and Slave up to 16 MHz
  - Supports SPI/MICROWIRE Master/Slave mode
  - Full duplex synchronous serial data transfer
  - Variable length of transfer data from 4 to 32 bits
  - MSB or LSB first data transfer
  - RX and TX on both rising or falling edge of serial clock independently
  - Two slave/device select lines when SPI controller is used as the master, and 1 slave/device select line when SPI controller is used as the slave
  - Supports byte suspend mode in 32-bit transmission
  - Supports two channel PDMA requests, one for transmit and another for receive
  - Supports three wire mode, no slave select signal, bi-direction interface
  - Wake system up from Power-down mode
- I^2C
  - Up to two sets of I^2C device
  - Master/Slave up to 1 Mbit/s
  - Bi-directional data transfer between masters and slaves
  - Multi-master bus (no central master)
  - Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
  - Serial clock synchronization allows devices with different bit rates to communicate via one serial bus
  - Serial clock synchronization used as a handshake mechanism to suspend and resume serial transfer
  - Built-in 14-bit time-out counter requesting the I^2C interrupt if the I^2C bus hangs up and timer-out counter overflows
  - Programmable clocks allowing for versatile rate control
  - Supports 7-bit addressing mode
  - Supports multiple address recognition (four slave addresses with mask option)
- I^2S
  - Interface with external audio CODEC
  - Operated as either Master or Slave mode
  - Capable of handling 8, 16, 24 and 32 bit word sizes
  - Supports Mono and stereo audio data
  - Supports I^2S and MSB justified data format
  - Provides two 8 word FIFO data buffers: one for transmitting and the other for

2.2 Nano110 Features – LCD Line

- Core
  - ARM® Cortex™-M0 core running up to 42 MHz
  - One 24-bit system timer
  - Supports Low Power Sleep mode
  - Single-cycle 32-bit hardware multiplier
  - NVIC for the 32 interrupt inputs, each with 4-levels of priority
  - Serial Wire Debug supports with 2 watchpoints/4 breakpoints
- Brown-out
  - Built-in 2.5V/2.0V/1.7V BOD for wide operating voltage range operation
- Flash EPROM Memory
  - Runs up to 42 MHz with zero wait state for discontinuous address read access.
  - 64K/32K/123K bytes application program memory (APROM)
  - 4 KB In System Programming (ISP) loader program memory (LDROM)
  - Programmable data flash start address and memory size with 512 bytes page erase unit
  - In System Program (ISP)/In Application Program (IAP) to update on chip Flash EPROM
- SRAM Memory
  - 16K/8K bytes embedded SRAM
  - Supports DMA mode
- DMA : Supports 8 channels: one VDMA channel,6 PDMA channels, and one CRC channel
  - VDMA
    - Memory-to-memory transfer
    - Supports block transfer with stride
    - Supports word/half-word/byte boundary address
    - Supports address direction: increment and decrement
  - PDMA
    - Peripheral-to-memory, memory-to-peripheral, and memory-to-memory transfer
    - Supports word boundary address
    - Supports word alignment transfer length in memory-to-memory mode
    - Supports word/half-word/byte alignment transfer length in peripheral-to-memory and memory-to-peripheral mode
    - Supports word/half-word/byte transfer data width from/to peripheral
    - Supports address direction: increment, fixed, and wrap around
  - CRC

2.4 Nano130 Features – Advanced Line

- Core
  - ARM® Cortex™-M0 core running up to 42 MHz
  - One 24-bit system timer
  - Supports Low Power Sleep mode
  - Single-cycle 32-bit hardware multiplier
  - NVIC for the 32 interrupt inputs, each with 4-levels of priority
  - Serial Wire Debug supports with 2 watchpoints/4 breakpoints
- Brown-out
  - Built-in 2.5V/2.0V/1.7V BOD for wide operating voltage range operation
- Flash EPROM Memory
  - Runs up to 42 MHz with zero wait state for discontinuous address read access.
  - 64K/32K/123K bytes application program memory (APROM)
  - 4KB in system programming (ISP) loader program memory (LDROM)
  - Programmable data flash start address and memory size with 512 bytes page erase unit
  - In System Program (ISP)/In Application Program (IAP) to update on chip Flash EPROM
- SRAM Memory
  - 16K/8K bytes embedded SRAM
  - Supports DMA mode
- DMA : Supports 8 channels: one VDMA channel,6 PDMA channels, and one CRC 28egiste
  - VDMA
    - Memory-to-memory transfer
    - Supports block transfer with stride
    - Supports word/half-word/byte boundary address
    - Supports address direction: increment and decrement
  - PDMA
    - Peripheral-to-memory, memory-to-peripheral, and memory-to-memory transfer
    - Supports word boundary address
    - Supports word alignment transfer length in memory-to-memory mode
    - Supports word/half-word/byte alignment transfer length in peripheral-to-memory and memory-to-peripheral mode
    - Supports word/half-word/byte transfer data width from/to peripheral
    - Supports address direction: increment, fixed, and wrap around
  - CRC

- LCD driver for up to 4 COM x 40 SEG or 6 COM x 38 SEG
- Supports Static,1/2 bias and 1/3 bias voltage
- Four display modes: Static, 1/2 duty, 1/3 duty, 1/4 duty, 1/5 duty and 1/6 duty.
- Selectable LCD frequency by frequency divider
- Configurable frame frequency
- Internal Charge pump, adjustable contrast adjustment
- Configurable Charge pump frequency
- Blinking capability
- Supports R-type/C-type method
- LCD frame interrupt

- USB 2.0 Full-speed Device
  - One set of USB 2.0 FS Device 12 Mbps
  - On-chip USB Transceiver
  - Provides 1 interrupt source with 4 interrupt events
  - Supports Control, Bulk In/Out, Interrupt and Isochronous transfers
  - Auto suspend function when no bus signaling for 3 ms
  - Provides 8 programmable endpoints
  - Includes 512 Bytes internal SRAM as USB buffer
  - Provides remote wake-up capability
- EBI (External bus interface)
  - Accessible space: 64 KB in 8-bit mode or 128 KB in 16-bit mode
  - Supports 8bit/16bit data width
  - Supports byte write in 16-bit data width mode
- One built-in temperature sensor with 1℃ resolution
- 96-bit unique ID
- 128-bit unique customer ID
- Operating Temperature: -40℃~85℃
- Packages:
  - All Green package (RoHS)
  - LQFP 128-pin(14x14) / 64-pin (7x7)

3 PARTS INFORMATION LIST AND PIN CONFIGURATION

3.1 NuMicro™ Nano100 Series Selection Code

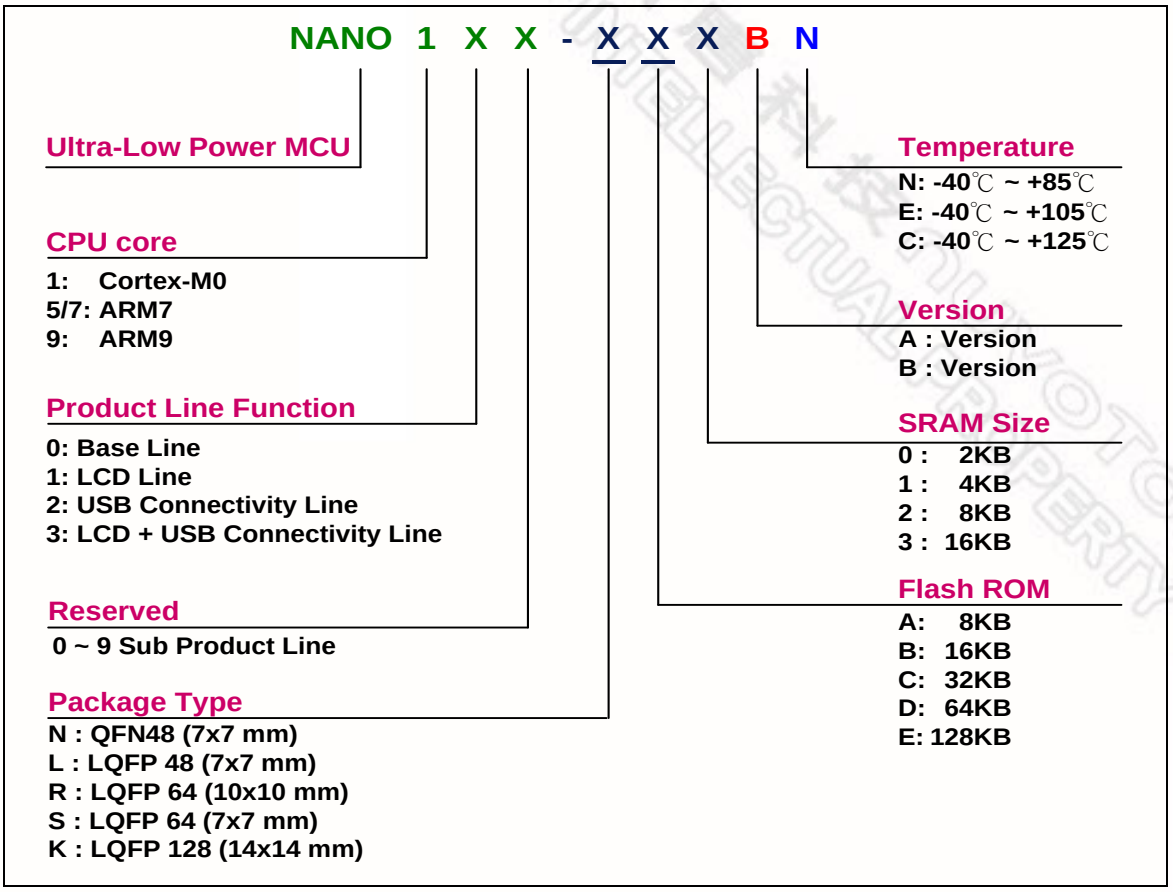


Figure 3-1 NuMicro™ Nano100 Series Selection Code

3.3.2.2 NuMicro™ Nano110 LQFP 64-pin

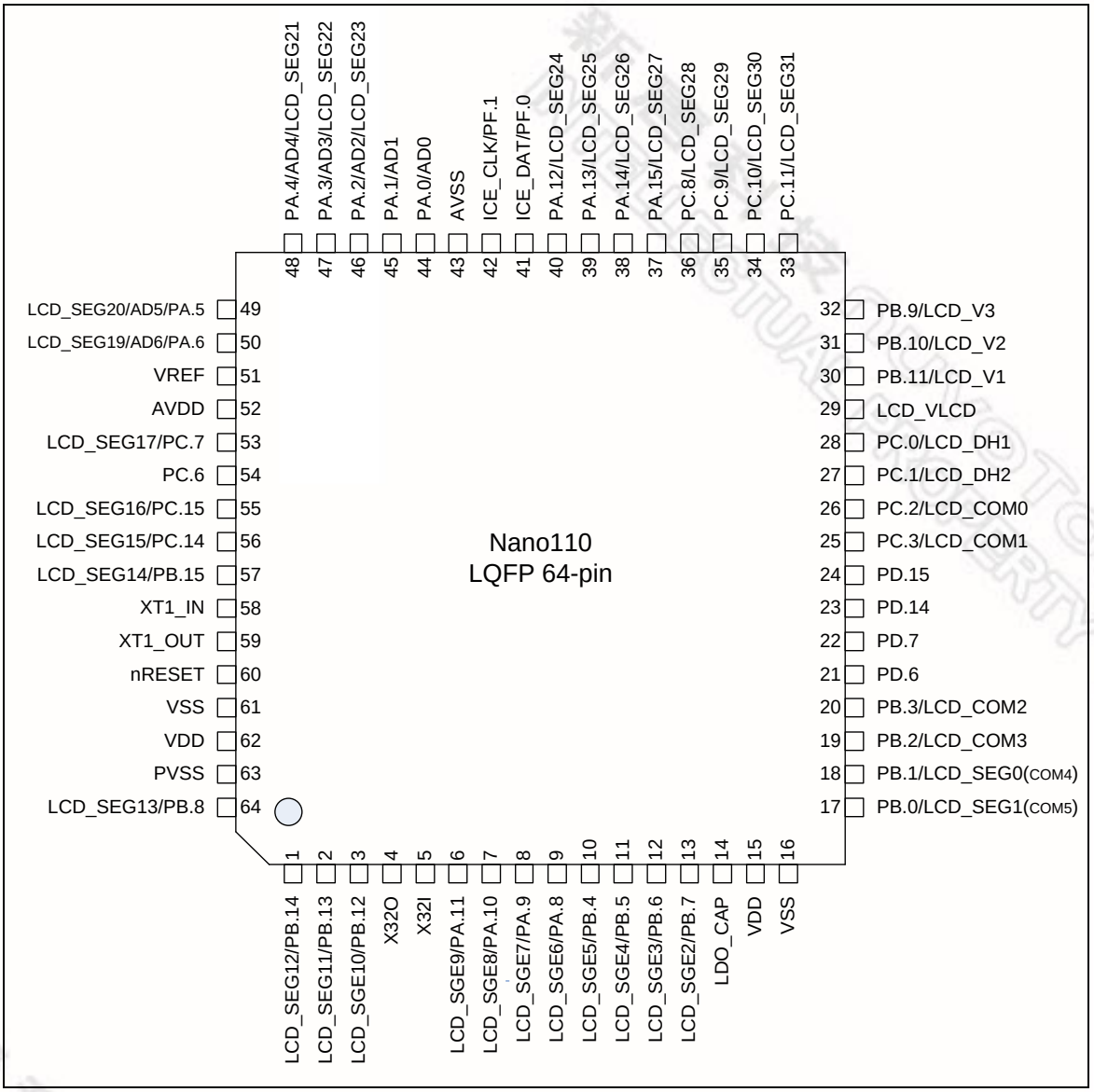


Figure 3-6 NuMicro™ Nano110 LQFP 64-pin Diagram

3.3.3.2 NuMicro™ Nano120 LQFP 64-pin

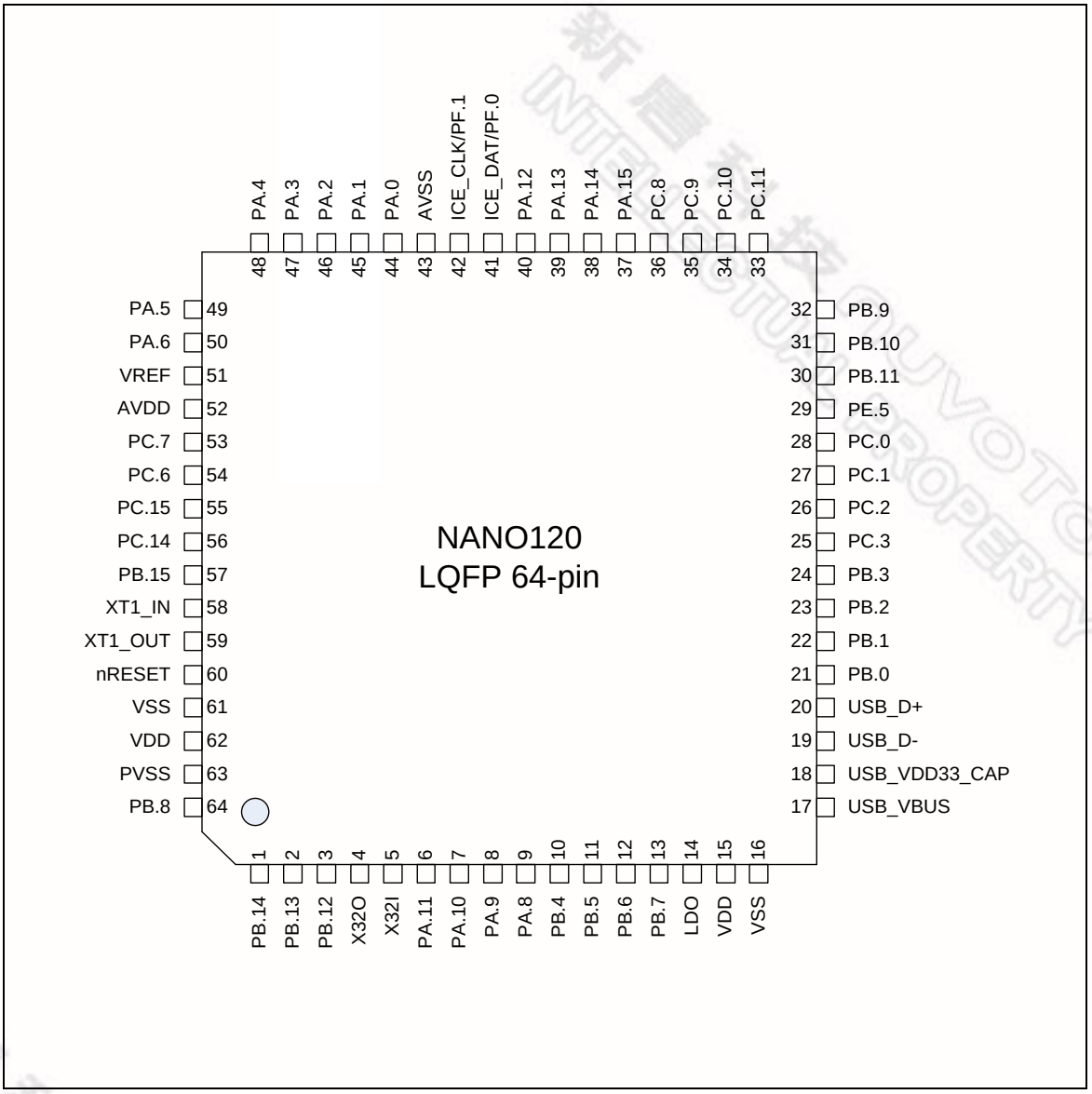


Figure 3-8 NuMicro™ Nano120 LQFP 64-pin Diagram

3.3.4.2 NuMicro™ Nano130 LQFP 64-pin

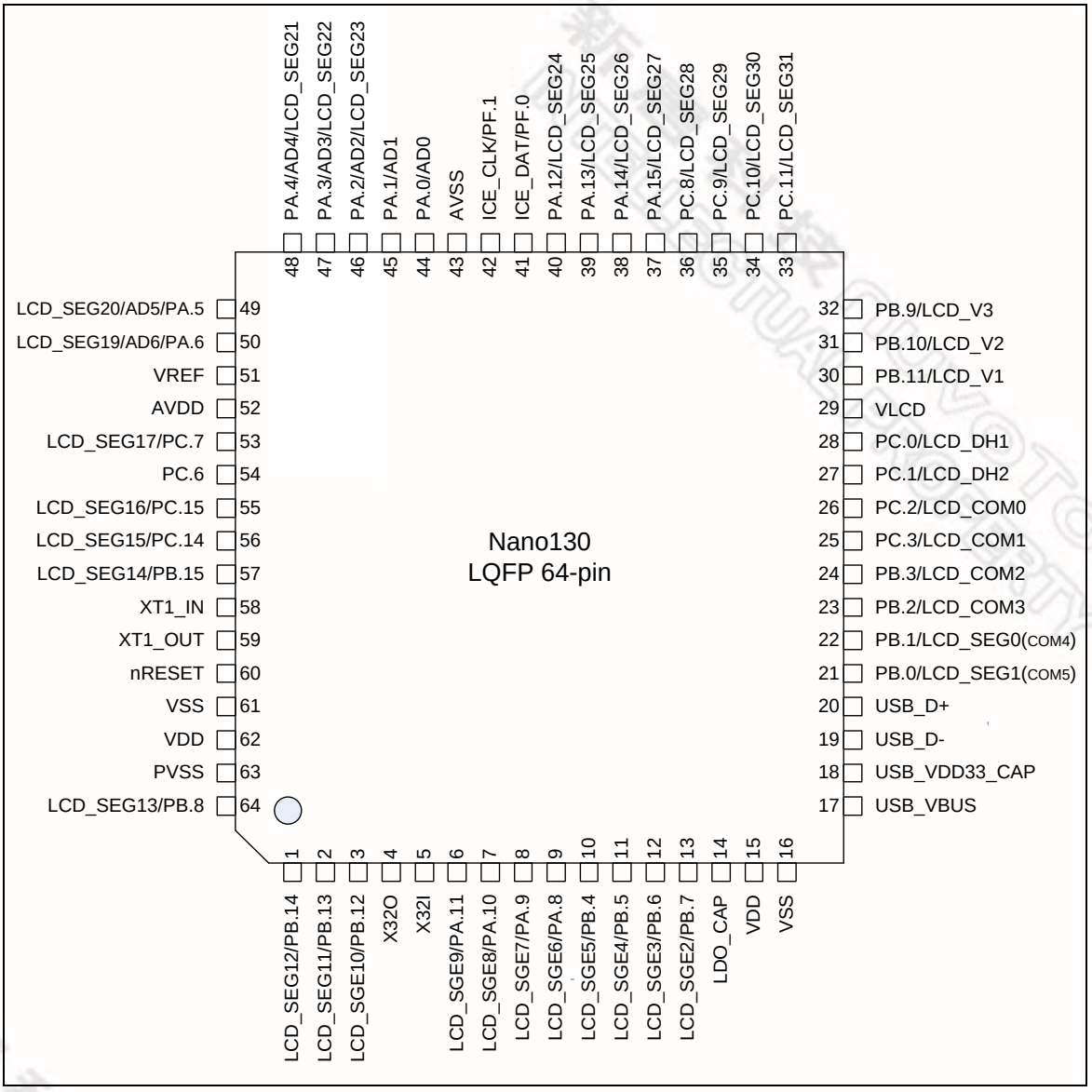


Figure 3-11 NuMicro™ Nano130 LQFP 64-pin Diagram

3.4 Pin Description

3.4.1 NuMicro™ Nano100 Pin Description

Pin No.			Pin Name	Pin Type	Description
LQFP 128-pin	LQFP 64-pin	LQFP/QFN 48-pin			
1			PE.13	**I/O**	General purpose digital I/O pin
2	1		PB.14	**I/O**	General purpose digital I/O pin
			INT0	**I**	External interrupt0 input pin
			SC2_CD	**I**	SmartCard2 card detect pin
			SPI2_SS1	**I/O**	SPI2 2nd slave select pin
3	2		PB.13	**I/O**	General purpose digital I/O pin
			EBI_AD1	**I/O**	EBI Address/Data bus bit1
4	3	1	PB.12	**I/O**	General purpose digital I/O pin
			EBI_AD0	**I/O**	EBI Address/Data bus bit0
			FCLKO	**O**	Frequency Divider output pin
5					NC
6	4	2	X32O	**O**	External 32.768 kHz crystal output pin
7	5	3	X32I	**I**	External 32.768 kHz crystal input pin
8					NC
9	6	4	PA.11	**I/O**	General purpose digital I/O pin
			I2C1_SCL	**I/O**	I2C1 clock pin
			EBI_nRD	**O**	EBI read enable output pin
			SC0_RST	**O**	SmartCard0 RST pin
			SPI2_MOSI0	**I/O**	SPI2 1st MOSI (Master Out, Slave In) pin
10	7	5	PA.10	**I/O**	General purpose digital I/O pin
			I2C1_SDA	**I/O**	I2C1 data I/O pin
			EBI_nWR	**O**	EBI write enable output pin
			SC0_PWR	**O**	SmartCard0 Power pin
			SPI2_MISO0	**I/O**	SPI2 1st MISO (Master In, Slave Out) pin
11	8	6	PA.9	**I/O**	General purpose digital I/O pin
			I2C0_SCL	**I/O**	I2C0 clock pin
			SC0_DAT	**I/O**	SmartCard0 DATA pin(SC0_UART_RXD)

Pin No.			Pin Name	Pin Type	Description
LQFP 128-pin	LQFP 64-pin	LQFP/QFN 48-pin			
			SPI2_CLK	**I/O**	SPI2 serial clock pin
12	9	7	PA.8	**I/O**	General purpose digital I/O pin
			I2C0_SDA	**I/O**	I^2C0 data I/O pin
			SC0_CLK	**O**	SmartCard0 clock pin(SC0_UART_TXD)
			SPI2_SS0	**I/O**	SPI2 1st slave select pin
13			PD.8	**I/O**	General purpose digital I/O pin
14			PD.9	**I/O**	General purpose digital I/O pin
15			PD.10	**I/O**	General purpose digital I/O pin
16			PD.11	**I/O**	General purpose digital I/O pin
17			PD.12	**I/O**	General purpose digital I/O pin
18			PD.13	**I/O**	General purpose digital I/O pin
19	10	8	PB.4	**I/O**	General purpose digital I/O pin
			UART1_RXD	**I**	UART1 Data receiver input pin
			SC0_CD	**I**	SmartCard0 card detect pin
			SPI2_SS0	**I/O**	SPI2 1st slave select pin
20	11	9	PB.5	**I/O**	General purpose digital I/O pin
			UART1_TXD	**O**	UART1 Data transmitter output pin
			SC0_RST	**O**	SmartCard0 RST pin
			SPI2_CLK	**I/O**	SPI2 serial clock pin
21	12		PB.6	**I/O**	General purpose digital I/O pin
			UART1_RTSn	**O**	UART1 Request to Send output pin
			EBI_ALE	**O**	EBI address latch enable output pin
			SPI2_MISO0	**I/O**	SPI2 1st MISO (Master In, Slave Out) pin
22	13		PB.7	**I/O**	General purpose digital I/O pin
			UART1_CTSn	**I**	UART1 Clear to Send input pin
			EBI_nCS	**O**	EBI chip select enable output pin
			SPI2_MOSI0	**I/O**	SPI2 1st MOSI (Master Out, Slave In) pin
23					NC
24	14	10	LDO_CAP	**P**	LDO output pin
25					NC

3.4.2 NuMicro™ Nano110 Pin Description

Pin No.			Pin Name	Pin Type	Description
LQFP 128-pin	LQFP 64-pin	LQFP 48-pin			
1			PE.13	**I/O**	General purpose digital I/O pin
			LCD_SEG27	**O**	LCD segment output 27 at LQFP128
2	1		PB.14	**I/O**	General purpose digital I/O pin
			INT0	**I**	External interrupt0 input pin
			SC2_CD	**I**	SmartCard2 card detect
			SPI2_SS1	**I/O**	SPI2 2nd slave select pin
			LCD_SEG12	**O**	LCD segment output 12 at LQFP64
			LCD_SEG26	**O**	LCD segment output 26 at LQFP128
3	2		PB.13	**I/O**	General purpose digital I/O pin
			EBI_AD1	**I/O**	EBI Address/Data bus bit1
			LCD_SEG11	**O**	LCD segment output 11 at LQFP64
			LCD_SEG25	**O**	LCD segment output 25 at LQFP128
4	3		PB.12	**I/O**	General purpose digital I/O pin
			EBI_AD0	**I/O**	EBI Address/Data bus bit0
			FCLKO	**O**	Frequency Divider output pin
			LCD_SEG10	**O**	LCD segment output 10 at LQFP64
			LCD_SEG24	**O**	LCD segment output 24 at LQFP128
5					NC
6	4		X32O	**O**	External 32.768 kHz crystal output pin
7	5		X32I	**I**	External 32.768 kHz crystal input pin
8					NC
9	6		PA.11	**I/O**	General purpose digital I/O pin
			I2C1_SCL	**I/O**	I^2C1 clock pin
			EBI_nRD	**O**	EBI read enable output pin
			SC0_RST	**O**	SmartCard0 RST pin
			SPI2_MOSI0	**I/O**	SPI2 1st MOSI (Master Out, Slave In) pin
			LCD_SEG9	**O**	LCD segment output 9 at LQFP64
			LCD_SEG23	**O**	LCD segment output 23 at LQFP128

Pin No.			Pin Name	Pin Type	Description
LQFP 128-pin	LQFP 64-pin	LQFP 48-pin			
			LCD_SEG14	O	LCD segment output 14 at LQFP128
19	10		PB.4	I/O	General purpose digital I/O pin
			UART1_RXD	I	UART1 Data receiver input pin
			SC0_CD	I	SmartCard0 card detect pin
			SPI2_SS0	I/O	SPI2 1st slave select pin
			LCD_SEG5	O	LCD segment output 5 at LQFP64
			LCD_SEG13	O	LCD segment output 13 at LQFP128
20	11		PB.5	I/O	General purpose digital I/O pin
			UART1_TXD	O	UART1 Data transmitter output pin
			SC0_RST	O	SmartCard0 RST pin
			SPI2_CLK	I/O	SPI2 serial clock pin
			LCD_SEG4	O	LCD segment output 4 at LQFP64
			LCD_SEG12	O	LCD segment output 12 at LQFP128
21	12		PB.6	I/O	General purpose digital I/O pin
			UART1_RTSn	O	UART1 Request to Send output pin
			EBI_ALE	O	EBI address latch enable output pin
			SPI2_MISO0	I/O	SPI2 1st MISO (Master In, Slave Out) pin
			LCD_SEG3	O	LCD segment output 3 at LQFP64
			LCD_SEG11	O	LCD segment output 11 at LQFP128
22	13		PB.7	I/O	General purpose digital I/O pin
			UART1_CTSn	I	UART1 Clear to Send input pin
			EBI_nCS	O	EBI chip select enable output pin
			SPI2_MOSI0	I/O	SPI2 1st MOSI (Master Out, Slave In) pin
			LCD_SEG2	O	LCD segment output 2 at LQFP64
			LCD_SEG10	O	LCD segment output 10 at LQFP128
23					NC
24	14		LDO_CAP	P	LDO output pin
25					NC
26					NC
27	15		VDD	P	Power supply for I/O ports and LDO source

Pin No.			Pin Name	Pin Type	Description
LQFP 128-pin	LQFP 64-pin	LQFP 48-pin			
10	7		PA.10	I/O	General purpose digital I/O pin
			I2C1_SDA	I/O	I^2C1 data I/O pin
			EBI_nWR	O	EBI write enable output pin
			SC0_PWR	O	SmartCard0 Power pin
			SPI2_MISO0	I/O	SPI2 1st MISO (Master In, Slave Out) pin
			LCD_SEG8	O	LCD segment output 8 at LQFP64
			LCD_SEG22	O	LCD segment output 22 at LQFP128
11	8		PA.9	I/O	General purpose digital I/O pin
			I2C0_SCL	I/O	I^2C0 clock pin
			SC0_DAT	I/O	SmartCard0 DATA pin(SC0_UART_RXD)
			SPI2_CLK	I/O	SPI2 serial clock pin
			LCD_SEG7	O	LCD segment output 7 at LQFP64
			LCD_SEG21	O	LCD segment output 21 at LQFP128
12	9		PA.8	I/O	General purpose digital I/O pin
			I2C0_SDA	I/O	I^2C0 data I/O pin
			SC0_CLK	O	SmartCard0 clock pin(SC0_UART_TXD)
			SPI2_SS0	I/O	SPI2 1st slave select pin
			LCD_SEG6	O	LCD segment output 6 at LQFP64
			LCD_SEG20	O	LCD segment output 20 at LQFP128
13			PD.8	I/O	General purpose digital I/O pin
			LCD_SEG19	O	LCD segment output 19 at LQFP128
14			PD.9	I/O	General purpose digital I/O pin
			LCD_SEG18	O	LCD segment output 18 at LQFP128
15			PD.10	I/O	General purpose digital I/O pin
			LCD_SEG17	O	LCD segment output 17 at LQFP128
16			PD.11	I/O	General purpose digital I/O pin
			LCD_SEG16	O	LCD segment output 16 at LQFP128
17			PD.12	I/O	General purpose digital I/O pin
			LCD_SEG15	O	LCD segment output 15 at LQFP128
18			PD.13	I/O	General purpose digital I/O pin

Pin No.			Pin Name	Pin Type	Description
LQFP 128-pin	LQFP 64-pin	LQFP 48-pin			
28					NC
29	16		VSS	P	Ground
30			VSS	P	Ground
31			VSS	P	Ground
32			VSS	P	Ground
33			PE.12	I/O	General purpose digital I/O pin
34			PE.11	I/O	General purpose digital I/O pin
35			PE.10	I/O	General purpose digital I/O pin
36			PE.9	I/O	General purpose digital I/O pin
37			PE.8	I/O	General purpose digital I/O pin
			LCD_SEG9	O	LCD segment output 9 at LQFP128
38			PE.7	I/O	General purpose digital I/O pin
			LCD_SEG8	O	LCD segment output 8 at LQFP128
39					NC
40	17		USB_VBUS	USB	POWER SUPPLY: From USB Host or HUB.
41	18		USB_VDD33_CAP	USB	Internal Power Regulator Output 3.3V Decoupling Pin
42	19		USB_D-	USB	USB Differential Signal D-
43	20		USB_D+	USB	USB Differential Signal D+
44	21		PB.0	I/O	General purpose digital I/O pin
			UART0_RXD	I	UART0 Data receiver input pin
			SPI1_MOSI0	I/O	SPI1 1st MOSI (Master Out, Slave In) pin
			LCD_SEG1	O	LCD segment output 1 at LQFP64 (or as LCD_COM5)
			LCD_SEG7	O	LCD segment output 7 at LQFP128
45	22		PB.1	I/O	General purpose digital I/O pin
			UART0_TXD	O	UART0 Data transmitter output pin
			SPI1_MISO0	I/O	SPI1 1st MISO (Master In, Slave Out) pin
			LCD_SEG0	O	LCD segment output 0 at LQFP64 (or as LCD_COM4)
			LCD_SEG6	O	LCD segment output 6 at LQFP128
46	23		PB.2	I/O	General purpose digital I/O pin

5.9 FLASH Memory Controller (FMC)

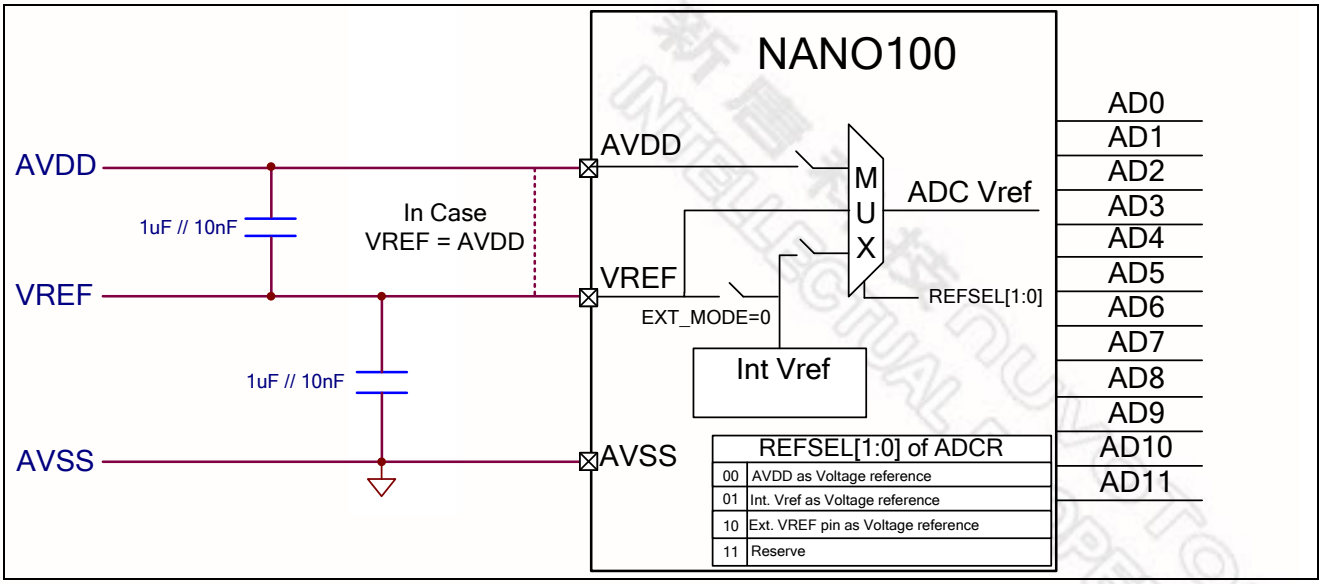
5.9.1 Overview

This chip is equipped with 32K/64K/123K bytes on-chip embedded Flash EPROM for application program memory (APROM) that can be updated through ISP/IAP procedure. In System Programming (ISP) function enables user to update program memory when chip is soldered on PCB. After chip powered on Cortex-M0 CPU fetches code from APROM or LDROM decided by boot select (CBS) in Config0. By the way, this chip also provides DATA Flash Region, the data flash is shared with original program memory and its start address is configurable and defined by user in Config1. The data flash size is defined by user application request.

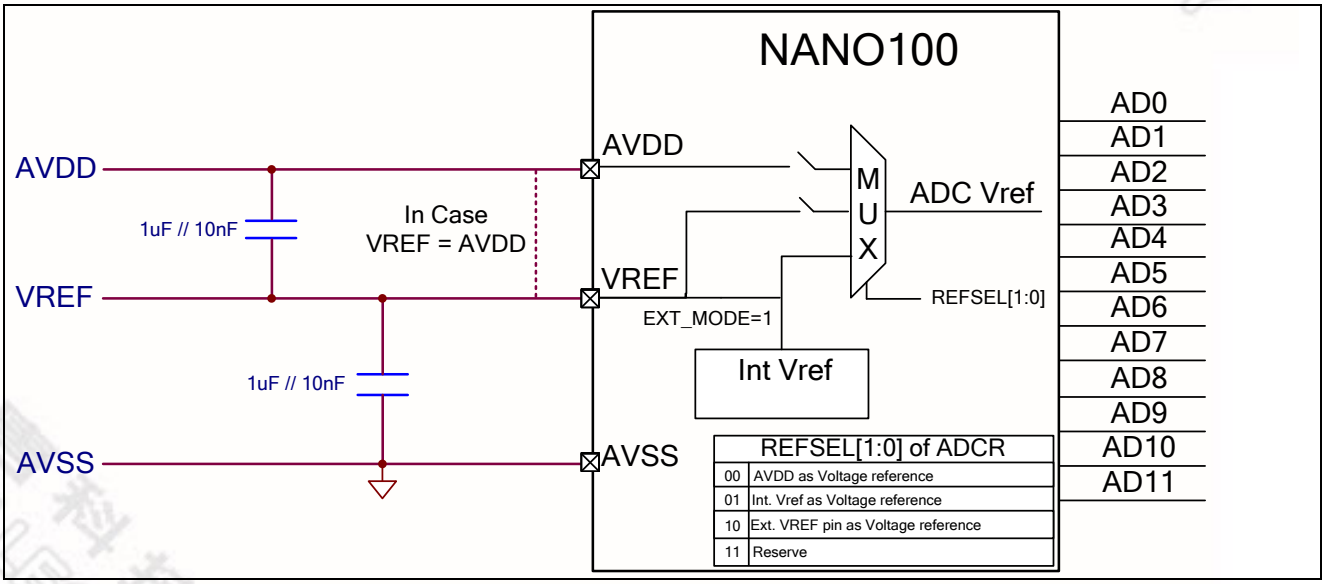
5.9.2 Features

- AHB interface compatible
- Run up to 42 MHz with zero wait state for discontinuous address read access
- 32/64/123KB application program memory (APROM)
- 4KB in system programming (ISP) loader program memory (LDROM)
- Programmable data flash start address and memory size with 512 bytes page erase unit
- In System Program (ISP)/In Application Program (IAP) to update on chip Flash EPROM

7.2.1.2 Vref Pin



7.2.1.3 Int Vref



PARAMETER	SYM.	SPECIFICATIONS				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
	I_{DD24}		68		uA	V_{DD} = 1.8V at 32.768 kHz all IP and PLL disabled
Operating Current Run Mode at IRC 10 kHz, HCLK = 10 kHz	I_{DD25}		70		uA	V_{DD} = 3.6V at 10 kHz all IP enabled and PLL disabled
	I_{DD26}		68		uA	V_{DD} = 3.6V at 10 kHz all IP and PLL disabled
	I_{DD27}		65		uA	V_{DD} = 1.8V at 10 kHz all IP enabled and PLL disabled
	I_{DD28}		62		uA	V_{DD} = 1.8V at 10 kHz all IP and PLL disabled
Operating Current Idle Mode at XTAL 12 MHz, HCLK = 42 MHz	I_{IDLE1}		14.5		mA	V_{DD}= 3.6V at 42 MHz all IP and PLL enabled [*5]
	I_{IDLE2}		4.6		mA	V_{DD}=3.6V at 42 MHz all IP disabled and PLL enabled
	I_{IDLE3}		13.8		mA	V_{DD} = 1.8V at 42MHz all IP and PLL enabled [*5]
	I_{IDLE4}		4.5		mA	V_{DD} = 1.8V at 42 MHz all IP disabled and PLL enabled
Operating Current Idle Mode at XTAL 12 MHz, HCLK = 32 MHz	I_{IDLE5}		11.6		mA	V_{DD}= 3.6V at 32 MHz all IP and PLL enabled [*5]
	I_{IDLE6}		3.6		mA	V_{DD}=3.6V at 32 MHz all IP disabled and PLL enabled
	I_{IDLE7}		11.1		mA	V_{DD} = 1.8V at 32MHz all IP and PLL enabled [*5]
	I_{IDLE8}		3.6		mA	V_{DD} = 1.8V at 32 MHz all IP disabled and PLL enabled
Operating Current Idle Mode at XTAL 12 MHz, HCLK = 12 MHz	I_{IDLE9}		4.7		mA	V_{DD} = 3.6V at 12 MHz, all IP enabled and PLL disabled
	I_{IDLE10}		0.99		mA	V_{DD} = 3.6V at 12 MHz, all IP and PLL disabled
	I_{IDLE11}		4.6		mA	V_{DD} = 1.8V at 12 MHz, all IP enabled and PLL disabled