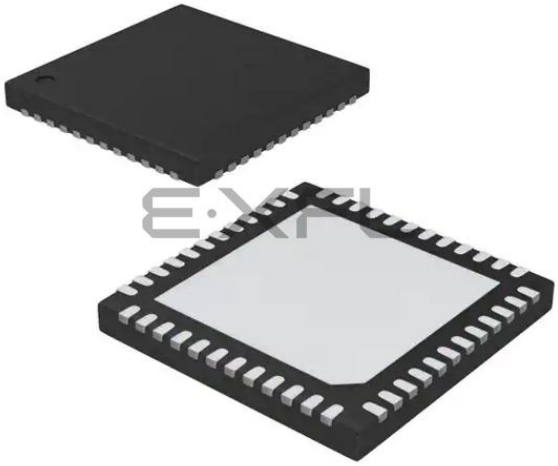

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	42MHz
Connectivity	EBI/EMI, I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	38
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 7x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	48-QFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/nano100nd3bn

Table of Contents

- Supports hardware warm reset sequence process
- Supports hardware deactivation sequence process
- Supports hardware auto deactivation sequence when detect the card is removal
- Supports UART mode (Half Duplex)

- EBI (External bus interface) support
  - Accessible space: 64 KB in 8-bit mode or 128 KB in 16-bit mode
  - Supports 8bit/16bit data width
  - Supports byte write in 16-bit Data Width mode
- One built-in temperature sensor with 1℃ resolution
- 96-bit unique ID
- 128-bit unique customer ID
- Operating Temperature: -40℃~85℃
- Packages:
  - All Green package (RoHS)
  - LQFP 128-pin(14x14) / 64-pin(7x7) / 48-pin(7x7) / QFN 48-pin(7x7)

- Supports UART mode (Half Duplex)

- LCD
  - LCD driver for up to 4 COM x 40 SEG or 6 COM x 38 SEG
  - Supports Static,1/2 bias and 1/3 bias voltage
  - Four display modes; Static, 1/2 duty, 1/3 duty,1/4 duty, 1/5 duty and 1/6 duty.
  - Selectable LCD frequency by frequency divider
  - Configurable frame frequency
  - Internal Charge pump, adjustable contrast adjustment
  - Configurable Charge pump frequency
  - Blinking capability
  - Supports R-type/C-type method
  - LCD frame interrupt
- One built-in temperature sensor with 1℃ resolution
- 96-bit unique ID
- 128-bit unique customer ID
- Operating Temperature: -40℃~85℃
- Packages:
  - All Green package (RoHS)
  - LQFP 128-pin(14x14) / 64-pin(10x10) / 64-pin(7x7)

3 PARTS INFORMATION LIST AND PIN CONFIGURATION

3.1 NuMicro™ Nano100 Series Selection Code

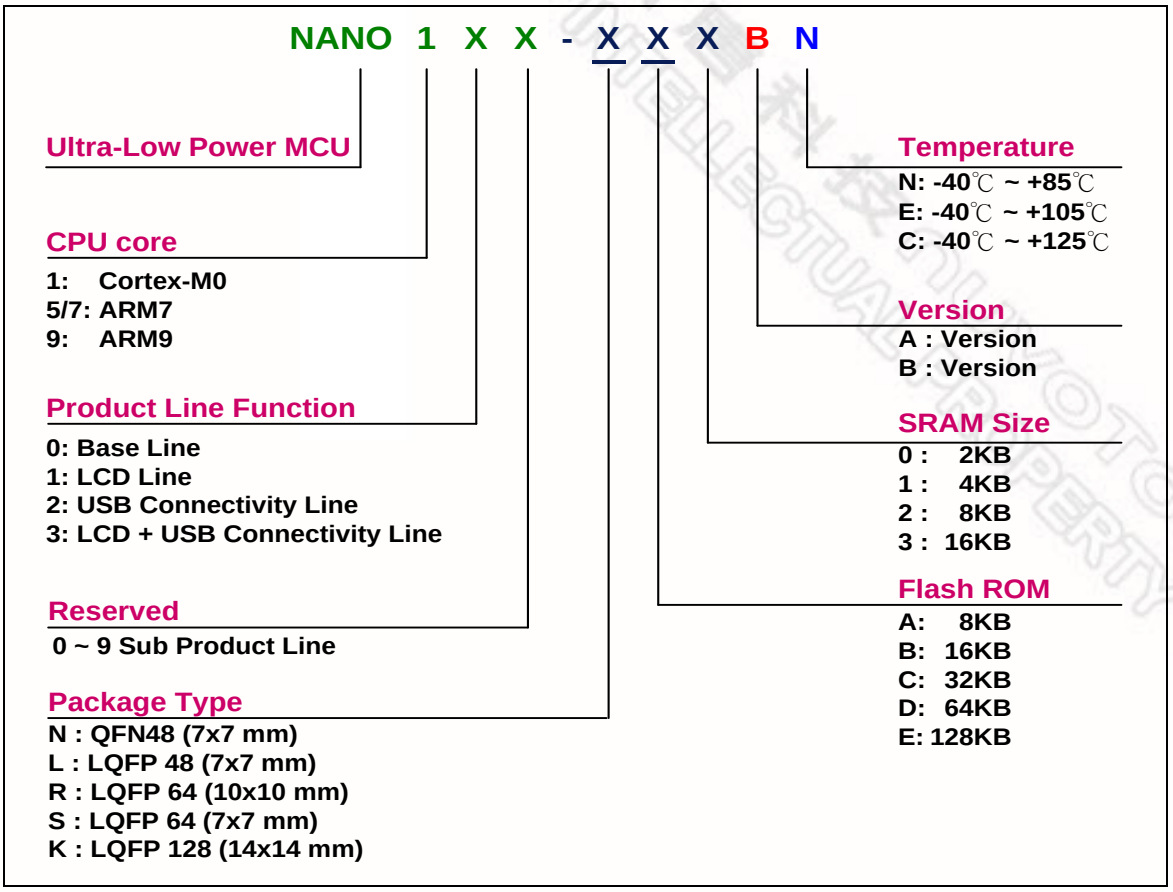


Figure 3-1 NuMicro™ Nano100 Series Selection Code

3.3.1.3 NuMicro™ Nano100 LQFP/QFN 48-pin

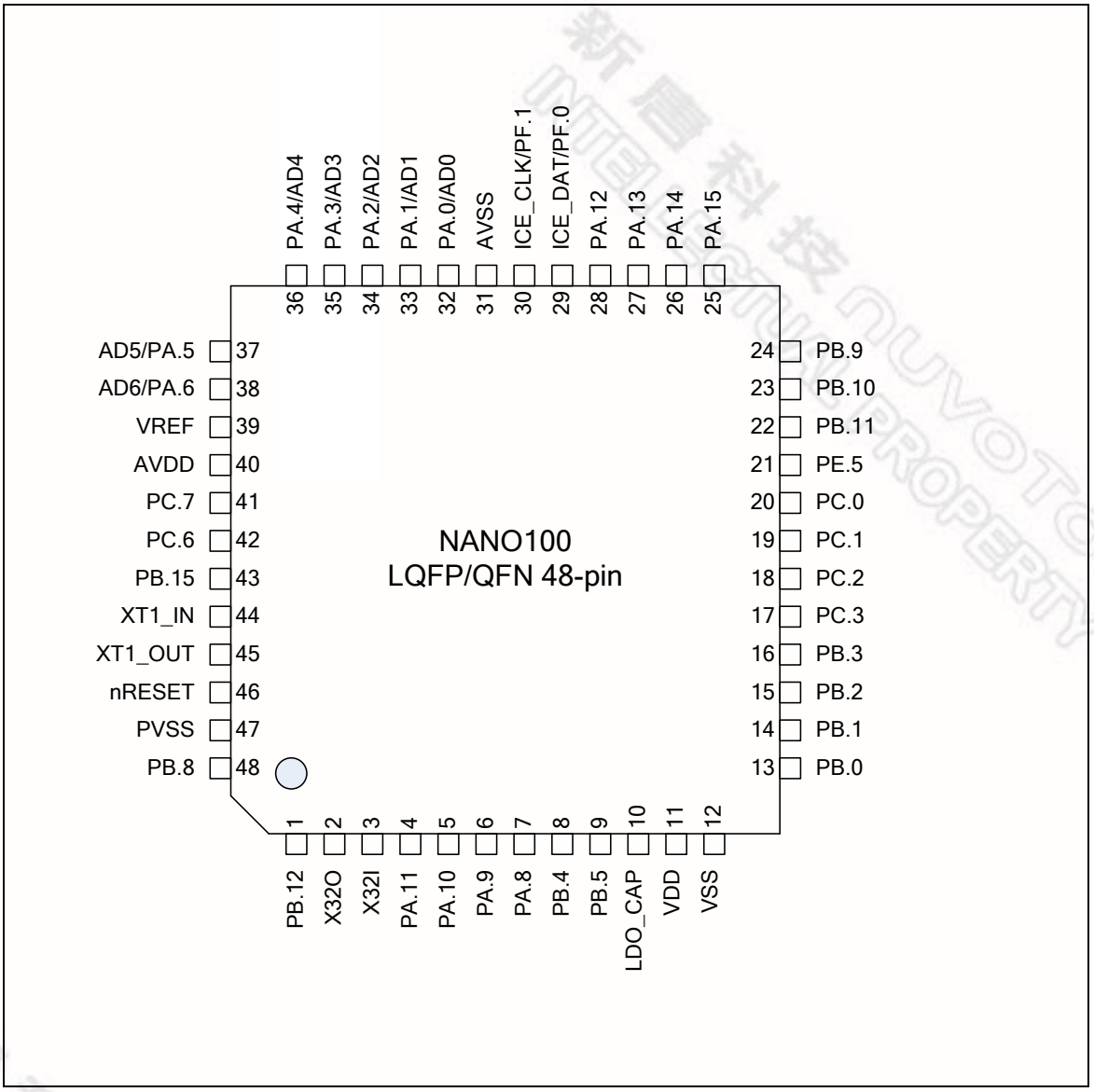


Figure 3-4 NuMicro™ Nano100 LQFP 48-pin Diagram

3.3.2 NuMicro™ Nano110 Pin Diagrams

3.3.2.1 NuMicro™ Nano110 LQFP 128-pin

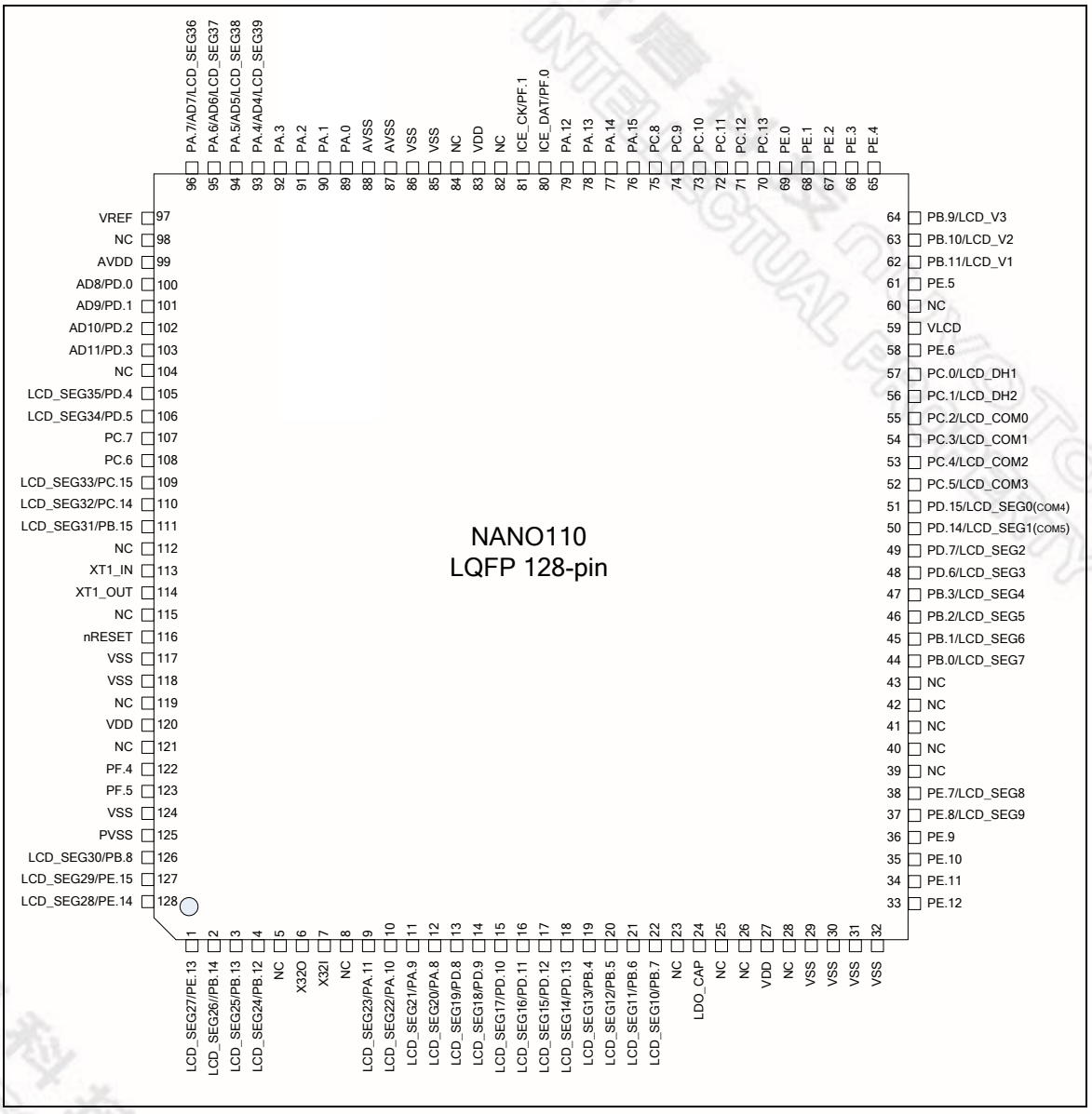


Figure 3-5 NuMicro™ Nano110 LQFP 128-pin Diagram

3.3.3 NuMicro™ Nano120 Pin Diagrams

3.3.3.1 NuMicro™ Nano120 LQFP 128-pin

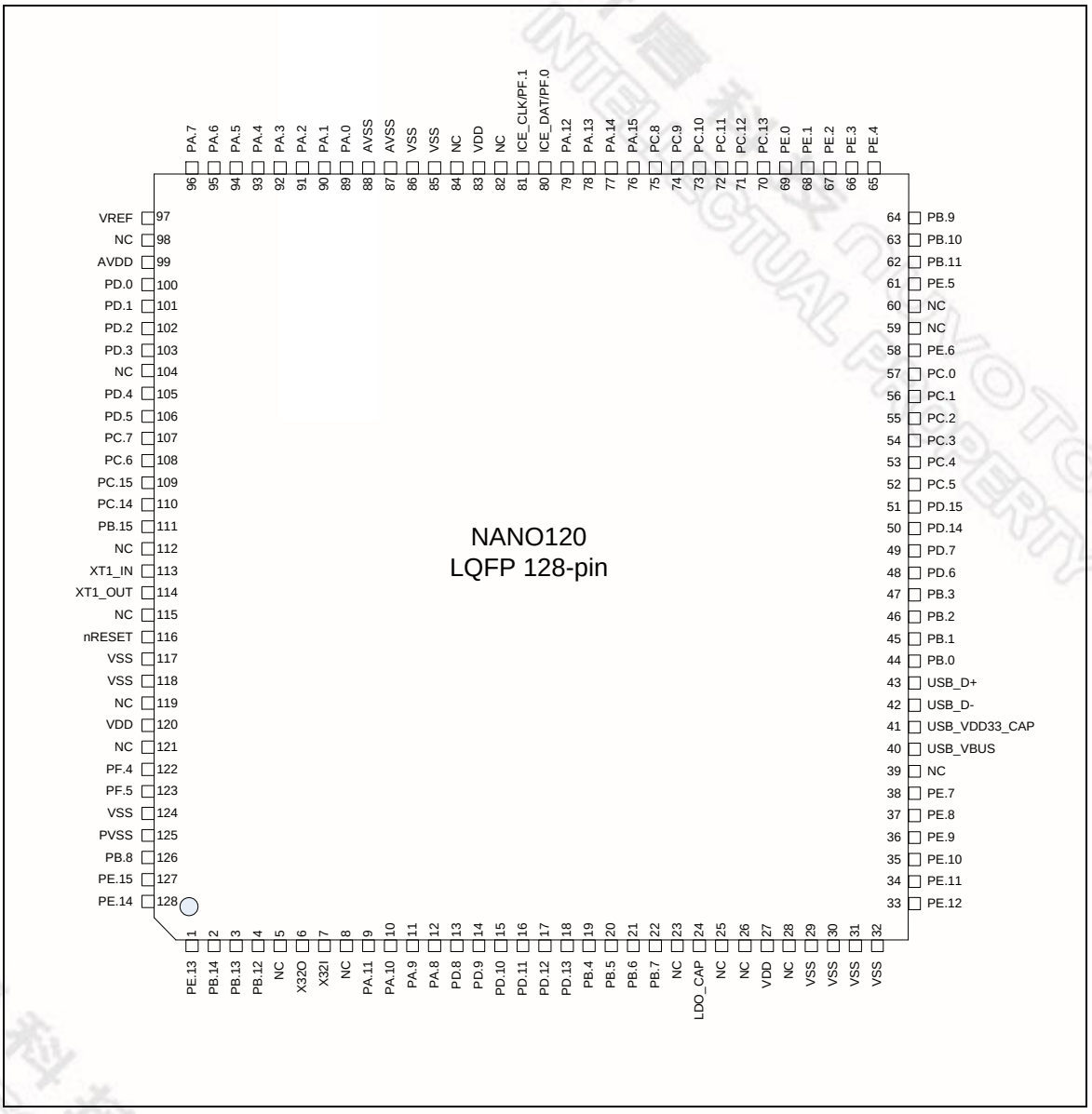


Figure 3-7 NuMicro™ Nano120 LQFP 128-pin Diagram

3.3.3.2 NuMicro™ Nano120 LQFP 64-pin

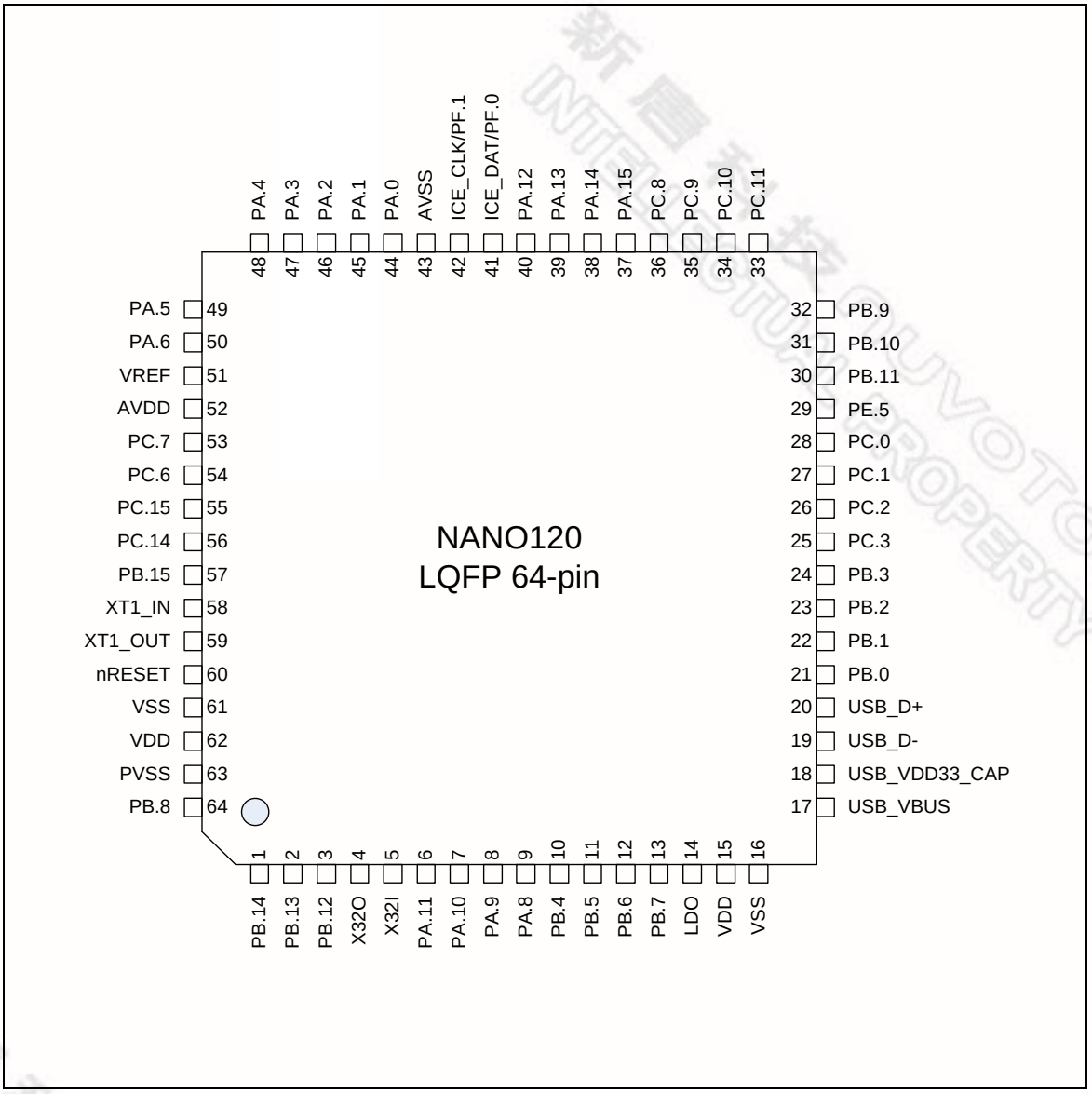


Figure 3-8 NuMicro™ Nano120 LQFP 64-pin Diagram

Pin No.			Pin Name	Pin Type	Description
LQFP 128-pin	LQFP 64-pin	LQFP/QFN 48-pin			
			EBI_nWRH	**O**	EBI high byte write enable output pin
			SPI1_SS0	**I/O**	SPI1 1st slave select pin
48	21		PD.6	**I/O**	General purpose digital I/O pin
49	22		PD.7	**I/O**	General purpose digital I/O pin
50	23		PD.14	**I/O**	General purpose digital I/O pin
51	24		PD.15	**I/O**	General purpose digital I/O pin
52			PC.5	**I/O**	General purpose digital I/O pin
			SPI0_MOSI1	**I/O**	SPI0 2nd MOSI (Master Out, Slave In) pin
53			PC.4	**I/O**	General purpose digital I/O pin
			SPI0_MISO1	**I/O**	SPI0 2nd MISO (Master In, Slave Out) pin
54	25	17	PC.3	**I/O**	General purpose digital I/O pin
			SPI0_MOSI0	**I/O**	SPI0 1st MOSI (Master Out, Slave In) pin
			I2S_DO	**O**	I2S data output
			SC1_RST	**O**	SmartCard1 RST pin
55	26	18	PC.2	**I/O**	General purpose digital I/O pin
			SPI0_MISO0	**I/O**	SPI0 1st MISO (Master In, Slave Out) pin
			I2S_DI	**I**	I2S data input
			SC1_PWR	**O**	SmartCard1 PWR pin
56	27	19	PC.1	**I/O**	General purpose digital I/O pin
			SPI0_CLK	**I/O**	SPI0 serial clock pin
			I2S_BCLK	**I/O**	I2S bit clock pin
			SC1_DAT	**I/O**	SmartCard1 DATA pin(SC1_UART_RXD)
57	28	20	PC.0 / MCLKO	**I/O**	General purpose digital I/O pin / Module clock output pin
			SPI0_SS0	**I/O**	SPI0 1st slave select pin
			I2S_LRCLK	**I/O**	I2S left right channel clock
			SC1_CLK	**O**	SmartCard1 clock pin(SC1_UART_TXD)
58			PE.6	**I/O**	General purpose digital I/O pin
59					NC
60					NC

Pin No.			Pin Name	Pin Type	Description
LQFP 128-pin	LQFP 64-pin	LQFP/QFN 48-pin			
61	29	21	PE.5	I/O	General purpose digital I/O pin
			PWM1_CH1	I/O	PWM1 Channel1 output
62	30	22	PB.11	I/O	General purpose digital I/O pin
			PWM1_CH0	I/O	PWM1 Channel0 output
			TM3	O	Timer3 external counter input
			SC2_DAT	I/O	SmartCard2 DATA pin(SC2_UART_RXD)
			SPI0_MISO0	I/O	SPI0 1st MISO (Master In, Slave Out) pin
63	31	23	PB.10	I/O	General purpose digital I/O pin
			SPI0_SS1	I/O	SPI0 2nd slave select pin
			TM2	O	Timer2 external counter input
			SC2_CLK	O	SmartCard2 clock pin(SC2_UART_TXD)
			SPI0_MOSI0	I/O	SPI0 1st MOSI (Master Out, Slave In) pin
64	32	24	PB.9	I/O	General purpose digital I/O pin
			SPI1_SS1	I/O	SPI1 2nd slave select pin
			TM1	O	Timer1 external counter input
			SC2_RST	O	SmartCard2 RST pin
			INT0	I	External interrupt0 input pin
65			PE.4	I/O	General purpose digital I/O pin
			SPI0_MOSI0	I/O	SPI0 1st MOSI (Master Out, Slave In) pin
66			PE.3	I/O	General purpose digital I/O pin
			SPI0_MISO0	I/O	SPI0 1st MISO (Master In, Slave Out) pin
67			PE.2	I/O	General purpose digital I/O pin
			SPI0_CLK	I/O	SPI0 serial clock pin
68			PE.1	I/O	General purpose digital I/O pin.
			PWM1_CH3	I/O	PWM1 Channel3 output
			SPI0_SS0	I/O	SPI0 1st slave select pin
69			PE.0	I/O	General purpose digital I/O pin
			PWM1_CH2	I/O	PWM1 Channel2 output
			I2S_MCLK	O	I2S master clock output pin
70			PC.13	I/O	General purpose digital I/O pin

Pin No.			Pin Name	Pin Type	Description
LQFP 128-pin	LQFP 64-pin	LQFP 48-pin			
			LCD_SEG14	O	LCD segment output 14 at LQFP128
19	10		PB.4	I/O	General purpose digital I/O pin
			UART1_RXD	I	UART1 Data receiver input pin
			SC0_CD	I	SmartCard0 card detect pin
			SPI2_SS0	I/O	SPI2 1st slave select pin
			LCD_SEG5	O	LCD segment output 5 at LQFP64
			LCD_SEG13	O	LCD segment output 13 at LQFP128
20	11		PB.5	I/O	General purpose digital I/O pin
			UART1_TXD	O	UART1 Data transmitter output pin
			SC0_RST	O	SmartCard0 RST pin
			SPI2_CLK	I/O	SPI2 serial clock pin
			LCD_SEG4	O	LCD segment output 4 at LQFP64
			LCD_SEG12	O	LCD segment output 12 at LQFP128
21	12		PB.6	I/O	General purpose digital I/O pin
			UART1_RTSn	O	UART1 Request to Send output pin
			EBI_ALE	O	EBI address latch enable output pin
			SPI2_MISO0	I/O	SPI2 1st MISO (Master In, Slave Out) pin
			LCD_SEG3	O	LCD segment output 3 at LQFP64
			LCD_SEG11	O	LCD segment output 11 at LQFP128
22	13		PB.7	I/O	General purpose digital I/O pin
			UART1_CTSn	I	UART1 Clear to Send input pin
			EBI_nCS	O	EBI chip select enable output pin
			SPI2_MOSI0	I/O	SPI2 1st MOSI (Master Out, Slave In) pin
			LCD_SEG2	O	LCD segment output 2 at LQFP64
			LCD_SEG10	O	LCD segment output 10 at LQFP128
23					NC
24	14		LDO_CAP	P	LDO output pin
25					NC
26					NC
27	15		VDD	P	Power supply for I/O ports and LDO source

Pin No.			Pin Name	Pin Type	Description
LQFP 128-pin	LQFP 64-pin	LQFP 48-pin			
28					NC
29	16		VSS	P	Ground
30			VSS	P	Ground
31			VSS	P	Ground
32			VSS	P	Ground
33			PE.12	I/O	General purpose digital I/O pin
			UART1_CTSn	I	UART1 Clear to Send input pin
34			PE.11	I/O	General purpose digital I/O pin
			UART1_RTSn	O	UART1 Request to Send output pin
35			PE.10	I/O	General purpose digital I/O pin
			UART1_TXD	O	UART1 Data transmitter output pin
36			PE.9	I/O	General purpose digital I/O pin
			UART1_RXD	I	UART1 Data receiver input pin
37			PE.8	I/O	General purpose digital I/O pin
			LCD_SEG9	O	LCD segment output 9 at LQFP128
38			PE.7	I/O	General purpose digital I/O pin
			LCD_SEG8	O	LCD segment output 8 at LQFP128
39					NC
40					NC
41					NC
42					NC
43					NC
44	17		PB.0	I/O	General purpose digital I/O pin
			UART0_RXD	I	UART0 Data receiver input pin
			SPI1_MOSI0	I/O	SPI1 1st MOSI (Master Out, Slave In) pin
			LCD_SEG1	O	LCD segment output 1 at LQFP64 (or as LD_COM5)
			LCD_SEG7	O	LCD segment output 7 at LQFP128
45	18		PB.1	I/O	General purpose digital I/O pin
			UART0_TXD	O	UART0 Data transmitter output pin

Pin No.			Pin Name	Pin Type	Description
LQFP 128-pin	LQFP 64-pin	LQFP 48-pin			
10	7		PA.10	I/O	General purpose digital I/O pin
			I2C1_SDA	I/O	I^2C1 data I/O pin
			EBI_nWR	O	EBI write enable output pin
			SC0_PWR	O	SmartCard0 Power pin
			SPI2_MISO0	I/O	SPI2 1st MISO (Master In, Slave Out) pin
			LCD_SEG8	O	LCD segment output 8 at LQFP64
			LCD_SEG22	O	LCD segment output 22 at LQFP128
11	8		PA.9	I/O	General purpose digital I/O pin
			I2C0_SCL	I/O	I^2C0 clock pin
			SC0_DAT	I/O	SmartCard0 DATA pin(SC0_UART_RXD)
			SPI2_CLK	I/O	SPI2 serial clock pin
			LCD_SEG7	O	LCD segment output 7 at LQFP64
			LCD_SEG21	O	LCD segment output 21 at LQFP128
12	9		PA.8	I/O	General purpose digital I/O pin
			I2C0_SDA	I/O	I^2C0 data I/O pin
			SC0_CLK	O	SmartCard0 clock pin(SC0_UART_TXD)
			SPI2_SS0	I/O	SPI2 1st slave select pin
			LCD_SEG6	O	LCD segment output 6 at LQFP64
			LCD_SEG20	O	LCD segment output 20 at LQFP128
13			PD.8	I/O	General purpose digital I/O pin
			LCD_SEG19	O	LCD segment output 19 at LQFP128
14			PD.9	I/O	General purpose digital I/O pin
			LCD_SEG18	O	LCD segment output 18 at LQFP128
15			PD.10	I/O	General purpose digital I/O pin
			LCD_SEG17	O	LCD segment output 17 at LQFP128
16			PD.11	I/O	General purpose digital I/O pin
			LCD_SEG16	O	LCD segment output 16 at LQFP128
17			PD.12	I/O	General purpose digital I/O pin
			LCD_SEG15	O	LCD segment output 15 at LQFP128
18			PD.13	I/O	General purpose digital I/O pin

5 FUNCTIONAL DESCRIPTION

5.1 Memory Organization

5.1.1 Overview

The Nano100 provides 4G-byte addressing space. The memory locations assigned to each on-chip modules are shown in following. The detailed register definition, memory space, and programming detailed will be described in the following sections for each on-chip module. The Nano100 series only supports little-endian data format.

5.1.2 Memory Map

The memory locations assigned to each on-chip controllers are shown in the following table.

Address Space	Token	Modules
Flash & SRAM Memory Space		
0x0000_0000 – 0x0001_FFFF	FLASH_BA	FLASH Memory Space (128KB)
0x2000_0000 – 0x2000_3FFF	SRAM_BA	SRAM Memory Space (16KB)
0x6000_0000 --- 0x6001_FFFF	EXTMEM_BA	External Memory Space(128KB)
AHB Modules Space (0x5000_0000 – 0x501F_FFFF)		
0x5000_0000 – 0x5000_01FF	GCR_BA	System Management Control Registers
0x5000_0200 – 0x5000_02FF	CLK_BA	Clock Control Registers
0x5000_0300 – 0x5000_03FF	INT_BA	Interrupt Multiplexer Control Registers
0x5000_4000 – 0x5000_7FFF	GPIO_BA	GPIO Control Registers
0x5000_8000 – 0x5000_BFFF	DMA_BA	DMA Control Registers
0x5000_C000 – 0x5000_FFFF	FMC_BA	Flash Memory Control Registers
0x5001_0000 – 0x5001_03FF	EBI_BA	External Bus Interface Control Registers
APB1 Modules Space (0x4000_0000 ~ 0x400F_FFFF)		
0x4000_4000 – 0x4000_7FFF	WDT_BA	Watchdog Timer Control Registers
0x4000_8000 – 0x4000_BFFF	RTC_BA	Real Time Clock (RTC) Control Register
0x4001_0000 – 0x4001_3FFF	TMR01_BA	Timer0 and Timer1 Control Registers
0x4002_0000 – 0x4002_3FFF	I2C0_BA	I^2C0 Interface Control Registers
0x4003_0000 – 0x4003_3FFF	SPI0_BA	SPI0 with Master/Slave function Control Registers
0x4004_0000 – 0x4004_3FFF	PWM0_BA	PWM0 Control Registers
0x4005_0000 – 0x4005_3FFF	UART0_BA	UART0 Control Registers
0x4006_0000 – 0x4006_3FFF	USBD_BA	USB FS device Controller Registers
0x400A_0000 – 0x400A_3FFF	DAC_BA	Digital-Analog-Converter (DAC) Control Registers
0x400B_0000 – 0x400B_3FFF	LCD_BA	LCD Control Registers

5.11.2 Features

- Acts as Master or Slave mode
- Bidirectional data transfer between masters and slaves
- Multi-master bus (no central master)
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer
- One built-in 14-bit time-out counter requesting the I^2C interrupt if the I^2C bus hangs up and timer-out counter overflows.
- Programmable clock divider allows versatile rate control
- Supports 7-bit addressing mode
- Supports multiple address recognition (Two slave addresses with mask option)
- Supports Power-down wake-up function

5.17 SPI

5.17.1 Overview

The Serial Peripheral Interface (SPI) is a synchronous serial data communication protocol. Devices communicate in Master/Slave mode with 4-wire bi-direction interface. It is used to perform a serial-to-parallel conversion on data received from a peripheral device, and a parallel-to-serial conversion on data transmitted to a peripheral device. The SPI controller can be configured as a master or a slave devicee.

The SPI controller supports wake-up function. When this chip stays in power-down mode, it can be waked up chip by off-chip device.

This controller supports variable serial clock function for special application and 2-bit transfer mode to connect 2 off-chip slave devices at the same time. The SPI controller also supports PDMA function to access the data buffer.

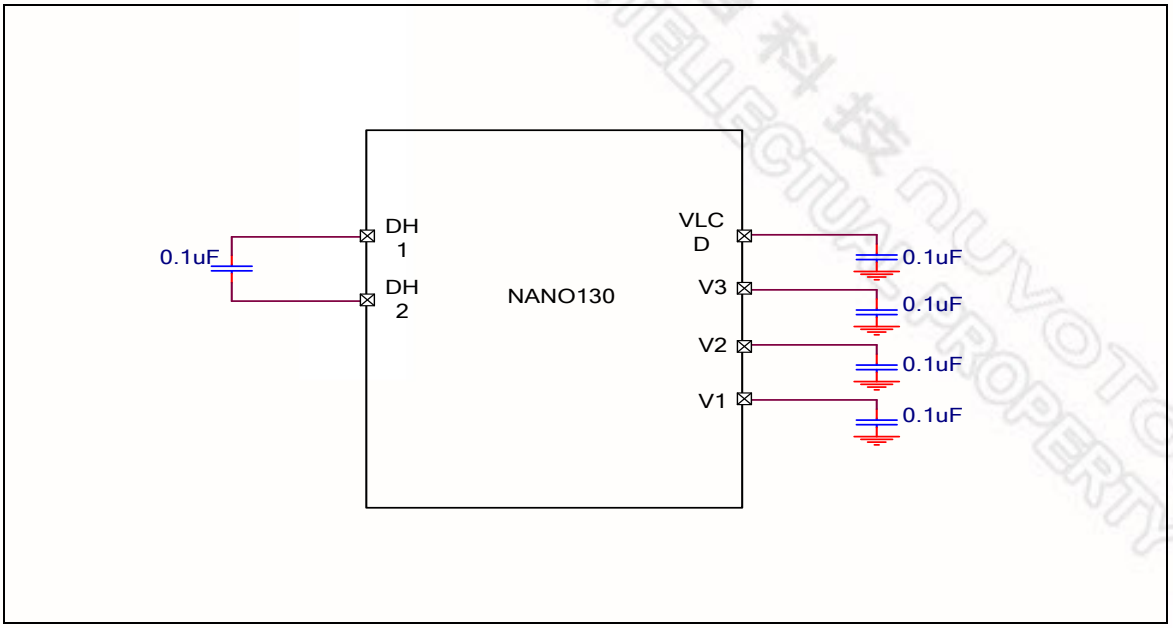
5.17.2 Features

- Supports Master (max. 32 MHz) or Slave (max. 16 MHz) mode operation
- Supports 1 bit and 2 bit transfer mode
- Support Dual IO transfer mode
- Configurable bit length of a transaction from 8 to 32-bit
- Supports MSB first or LSB first transfer sequence
- Two slave select lines supported in Master mode
- Configurable byte or word suspend mode
- Supports byte re-ordering function
- Supports variable serial clock in Master mode
- Provide separate 8-level depth transmit and receive FIFO buffer
- Supports wake-up function
- Supports PDMA transfer
- Supports three wires, no slave select signal, bi-direction interface

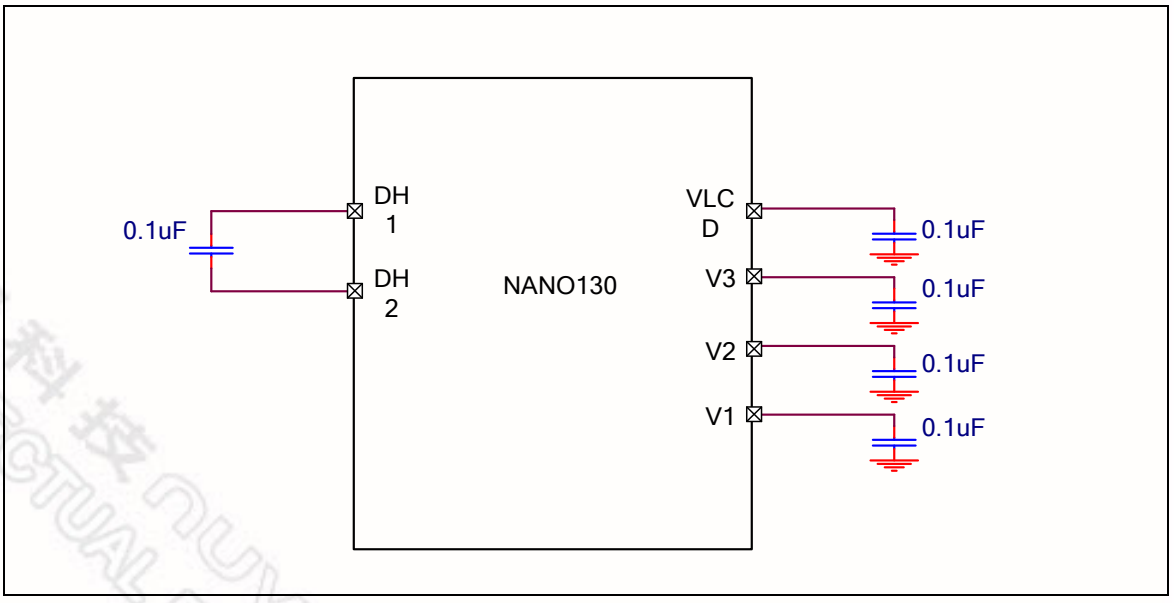
7 APPLICATION CIRCUIT

7.1 LCD Charge Pump

7.1.1 C-type 1/3 Bias



7.1.2 C-type 1/2 Bias



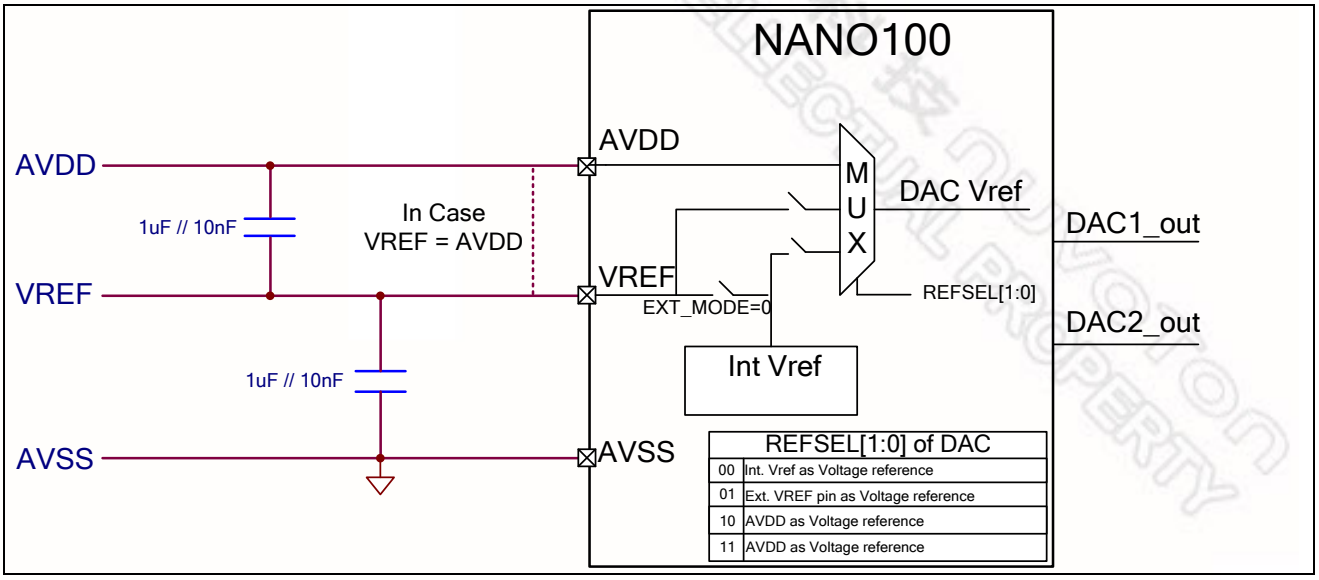
7.1.3 Internal R-type

Nano110/130 series MCUs also support external R-type mode (bypass internal R) to reduce current consumption. For external R-type application, VLCD is normally connected to system VDD, or it can be connected to VDD through an external variable resistor (VR) which is used for adjusting LCD contrast.

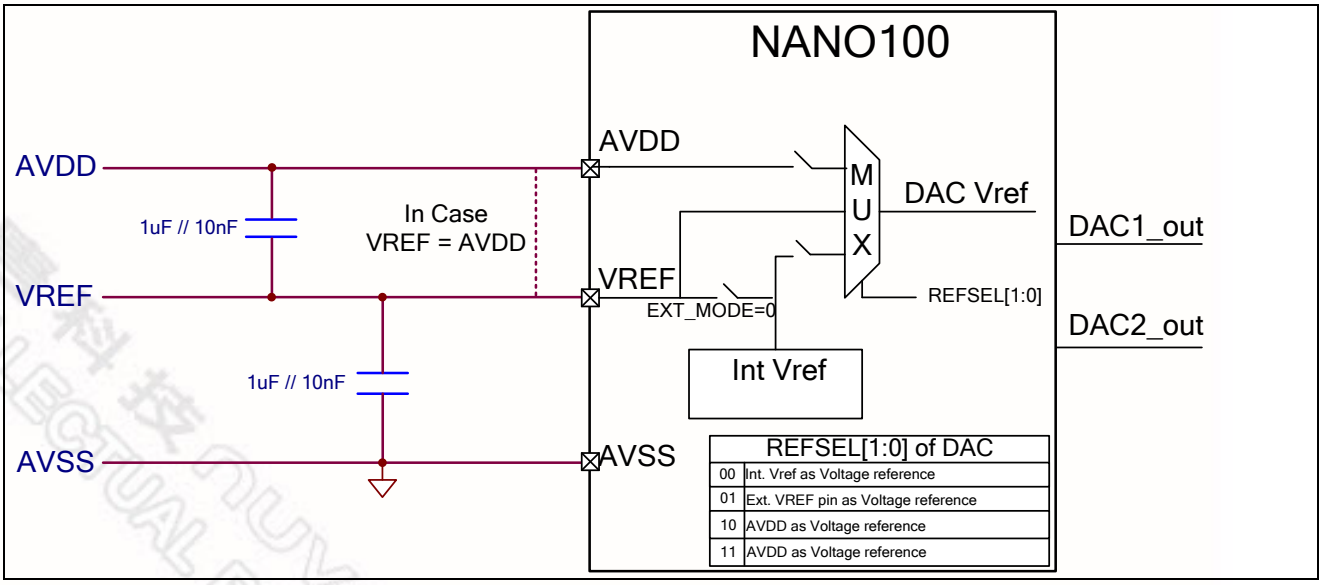
7.3 DAC Application Circuit

7.3.1 Voltage Reference Source

7.3.1.1 AVDD

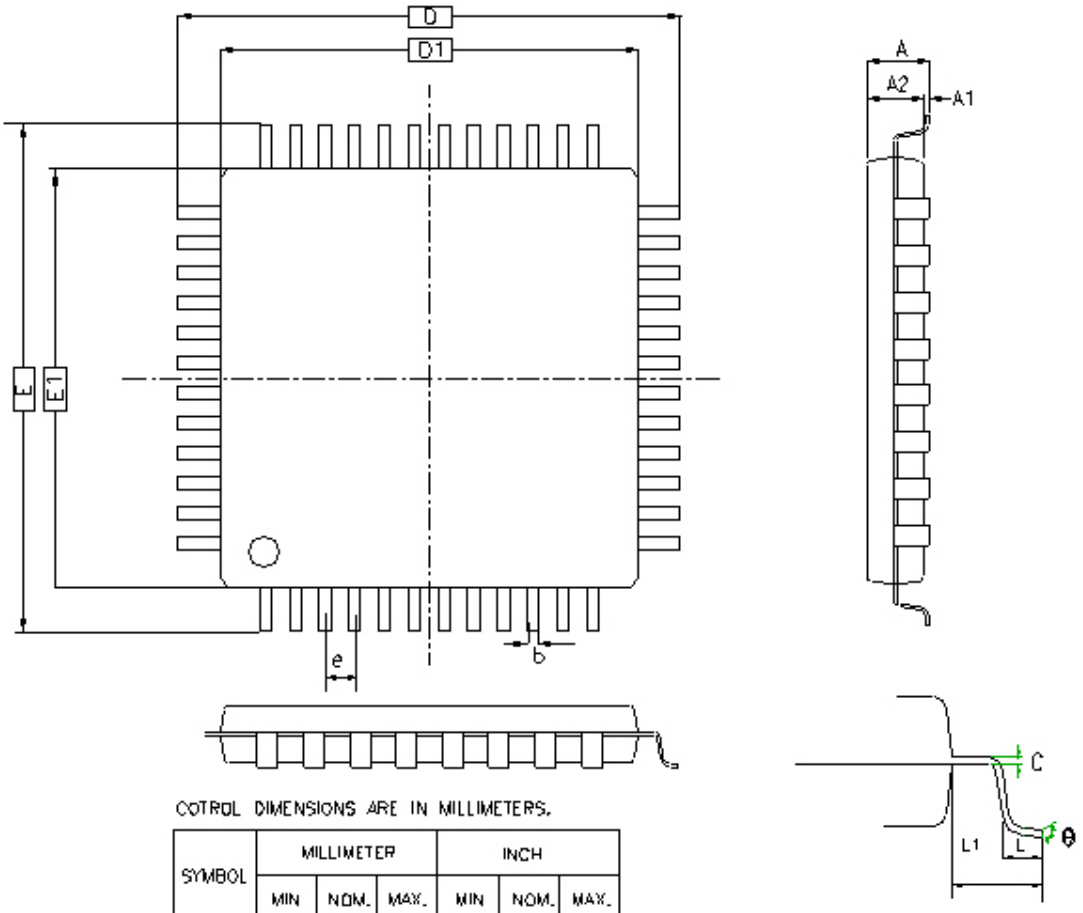


7.3.1.2 Vref Pin



PARAMETER	SYM.	SPECIFICATIONS				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
	I_{IDLE12}		0.94		mA	V_{DD} = 1.8V at 12 MHz, all IP and PLL disabled
Operating Current Idle Mode at IRC 12 MHz, HCLK = 12 MHz	I_{IDLE13}		5.9		mA	V_{DD} = 3.6V at 12 MHz, all IP enabled and PLL disabled
	I_{IDLE14}		1.3		mA	V_{DD} = 3.6V at 12 MHz, all IP and PLL disabled
	I_{IDLE15}		4.9		mA	V_{DD} = 1.8V at 12 MHz, all IP enabled and PLL disabled
	I_{IDLE16}		1.3		mA	V_{DD} = 1.8V at 12 MHz, all IP and PLL disabled
Operating Current Idle Mode at XTAL 4 MHz, HCLK = 4 MHz	I_{IDLE17}		2.7		mA	V_{DD} = 3.6V at 4 MHz, all IP enabled and PLL disabled
	I_{IDLE18}		0.66		mA	V_{DD} = 3.6V at 4 MHz, all IP and PLL disabled
	I_{IDLE19}		2.7		mA	V_{DD} = 1.8V at 4 MHz, all IP enabled and PLL disabled
	I_{IDLE20}		0.64		mA	V_{DD} = 1.8V at 4 MHz, all IP and PLL disabled
Operating Current Idle Mode at XTAL 32.768 kHz, HCLK = 32.768 kHz	I_{IDLE21}		78		uA	V_{DD} = 3.6V at 32.768 kHz all IP enabled and PLL disabled
	I_{IDLE22}		69		uA	V_{DD} = 3.6V at 32.768 kHz all IP and PLL disabled
	I_{IDLE23}		72		uA	V_{DD} = 1.8V at 32.768 kHz all IP enabled and PLL disabled
	I_{IDLE24}		63		uA	V_{DD} = 1.8V at 32.768 kHz all IP and PLL disabled
Operating Current Idle Mode at IRC 10 kHz, HCLK = 10 kHz	I_{IDLE25}		69		uA	V_{DD} = 3.6V at 10 kHz all IP enabled and PLL disabled
	I_{IDLE26}		66		uA	V_{DD} = 3.6V at 10 kHz all IP and PLL disabled
	I_{IDLE27}		63		uA	V_{DD} = 1.8V at 10 kHz all IP enabled and PLL disabled

10.4 LQFP48 (7x7x1.4 mm footprint 2.0 mm)



COTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN	NOM.	MAX.	MIN	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A1	0.05	0.10	0.15	0.002	0.004	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D1	6.90	7.00	7.10	0.272	0.276	0.280
E1	6.90	7.00	7.10	0.272	0.276	0.280
e	0.35	0.50	0.65	0.014	0.020	0.280
D	8.9	9.00	9.10	0.350	0.354	0.358
E	8.9	9.00	9.10	0.350	0.354	0.358
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	—	1.00	—	—	0.039	—
C	0.09	—	0.20	0.0035	—	0.0079
θ	0°	—	7°	0°	—	7°
b	0.17	0.22	0.27	0.007	0.0087	0.011