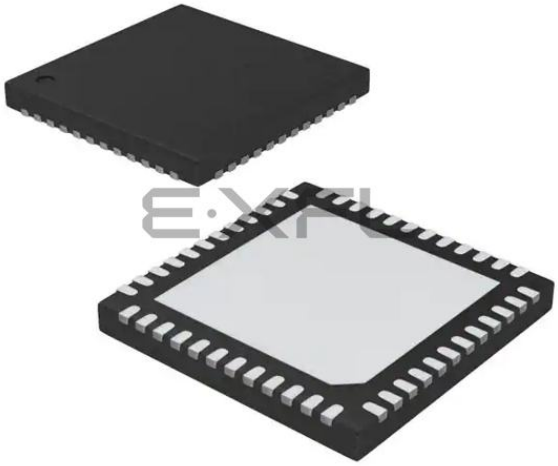

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	42MHz
Connectivity	EBI/EMI, I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	38
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 7x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	48-QFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/nano100ne3bn

2.2 Nano110 Features – LCD Line

- Core
  - ARM® Cortex™-M0 core running up to 42 MHz
  - One 24-bit system timer
  - Supports Low Power Sleep mode
  - Single-cycle 32-bit hardware multiplier
  - NVIC for the 32 interrupt inputs, each with 4-levels of priority
  - Serial Wire Debug supports with 2 watchpoints/4 breakpoints
- Brown-out
  - Built-in 2.5V/2.0V/1.7V BOD for wide operating voltage range operation
- Flash EPROM Memory
  - Runs up to 42 MHz with zero wait state for discontinuous address read access.
  - 64K/32K/123K bytes application program memory (APROM)
  - 4 KB In System Programming (ISP) loader program memory (LDROM)
  - Programmable data flash start address and memory size with 512 bytes page erase unit
  - In System Program (ISP)/In Application Program (IAP) to update on chip Flash EPROM
- SRAM Memory
  - 16K/8K bytes embedded SRAM
  - Supports DMA mode
- DMA : Supports 8 channels: one VDMA channel,6 PDMA channels, and one CRC channel
  - VDMA
    - Memory-to-memory transfer
    - Supports block transfer with stride
    - Supports word/half-word/byte boundary address
    - Supports address direction: increment and decrement
  - PDMA
    - Peripheral-to-memory, memory-to-peripheral, and memory-to-memory transfer
    - Supports word boundary address
    - Supports word alignment transfer length in memory-to-memory mode
    - Supports word/half-word/byte alignment transfer length in peripheral-to-memory and memory-to-peripheral mode
    - Supports word/half-word/byte transfer data width from/to peripheral
    - Supports address direction: increment, fixed, and wrap around
  - CRC

2.4 Nano130 Features – Advanced Line

- Core
  - ARM® Cortex™-M0 core running up to 42 MHz
  - One 24-bit system timer
  - Supports Low Power Sleep mode
  - Single-cycle 32-bit hardware multiplier
  - NVIC for the 32 interrupt inputs, each with 4-levels of priority
  - Serial Wire Debug supports with 2 watchpoints/4 breakpoints
- Brown-out
  - Built-in 2.5V/2.0V/1.7V BOD for wide operating voltage range operation
- Flash EPROM Memory
  - Runs up to 42 MHz with zero wait state for discontinuous address read access.
  - 64K/32K/123K bytes application program memory (APROM)
  - 4KB in system programming (ISP) loader program memory (LDROM)
  - Programmable data flash start address and memory size with 512 bytes page erase unit
  - In System Program (ISP)/In Application Program (IAP) to update on chip Flash EPROM
- SRAM Memory
  - 16K/8K bytes embedded SRAM
  - Supports DMA mode
- DMA : Supports 8 channels: one VDMA channel,6 PDMA channels, and one CRC 28egiste
  - VDMA
    - Memory-to-memory transfer
    - Supports block transfer with stride
    - Supports word/half-word/byte boundary address
    - Supports address direction: increment and decrement
  - PDMA
    - Peripheral-to-memory, memory-to-peripheral, and memory-to-memory transfer
    - Supports word boundary address
    - Supports word alignment transfer length in memory-to-memory mode
    - Supports word/half-word/byte alignment transfer length in peripheral-to-memory and memory-to-peripheral mode
    - Supports word/half-word/byte transfer data width from/to peripheral
    - Supports address direction: increment, fixed, and wrap around
  - CRC

- Supports four common polynomials CRC-CCITT, CRC-8, CRC-16, and CRC-32
  - CRC-CCITT: $X^{16} + X^{12} + X^5 + 1$
  - CRC-8: $X^8 + X^2 + X + 1$
  - CRC-16: $X^{16} + X^{15} + X^2 + 1$
  - CRC-32: $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$

- Clock Control
  - Flexible selection for different applications
  - Built-in 12MHz OSC, can be trimmed to 0.25% deviation within all temperature range when turning on auto-trim function (system must have external 32.768 kHz crystal input) otherwise 12 MHz OSC has 2 % deviation within all temperarure range.
  - Low power 10 kHz OSC for watchdog and low power system operation
  - Supports one PLL, up to 120 MHz, for high performance system operation and USB application (48 MHz).
  - External 4~24 MHz crystal input for precise timing operation
  - External 32.768 kHz crystal input for RTC function and low power system operation
- GPIO
  - Three I/O modes:
    - Push-Pull output
    - Open-Drain output
    - Input only with high impendence
  - All inputs with Schmitt trigger
  - I/O pin configured as interrupt source with edge/level setting
  - Supports High Driver and High Sink I/O mode
  - Supports input 5V tolerance (except ADC and DAC shared pins)
- Timer
  - Supports 4 sets of 32-bit timers with 24-bit up-timer and one 8-bit pre-scale counter
  - Independent Clock Source for each timer
  - Provides one-shot,periodic, output toggle and continuous operation modes
  - Supports internal trigger event to ADC, DAC and PDMA module
  - Wake system up from Power-down mode
- Watchdog Timer
  - Clock Source is from LIRC. (Internal 10 kHz Low Speed Oscillator Clock)
  - Selectable time-out period from 1.6ms ~ 26sec (depends on clock source)
  - Interrupt or reset selectable on watchdog time-out

3.2 NuMicro™ Nano100 Products Selection Guide

3.2.1 NuMicro™ Nano100 Base Line Selection Guide

Part No.	Flash (Kbytes)	SRAM (Kbytes)	Data Flash	ISP ROM (Kbytes)	I/O	Timer (32-bit)	Connectivity				I2S	PWM (16-bit	ADC (12-bit)	RTC	EBI	IRC 10KHz 12MHz	PDMA	LCD	DAC (12-bit)	ISO-7816-3	ISP ICP	Package
							UART	SPI	I2C	USB												
NANO100NC2BN	32K	8K	Configurable	4K	up to 38	4x32-bit	4	3	2	-	1	0	7	V	-	V	8	-	2	2	V	QFN48*
NANO100ND2BN	64K	8K	Configurable	4K	up to 38	4x32-bit	4	3	2	-	1	6	7	V	-	V	8	-	2	2	V	QFN48*
NANO100ND3BN	64K	16K	Configurable	4K	up to 38	4x32-bit	4	3	2	-	1	6	7	V	-	V	8	-	2	2	V	QFN48*
NANO100NE3BN	128K	16K	Configurable	4K	up to 38	4x32-bit	4	3	2	-	1	6	7	V	-	V	8	-	2	2	V	QFN48*
NANO100LC2BN	32K	8K	Configurable	4K	up to 38	4x32-bit	4	3	2	-	1	6	7	V	-	V	8	-	2	2	V	LQFP48
NANO100LD2BN	64K	8K	Configurable	4K	up to 38	4x32-bit	4	3	2	-	1	6	7	V	-	V	8	-	2	2	V	LQFP48
NANO100LD3BN	64K	16K	Configurable	4K	up to 38	4x32-bit	4	3	2	-	1	6	7	V	-	V	8	-	2	2	V	LQFP48
NANO100LE3BN	128K	16K	Configurable	4K	up to 38	4x32-bit	4	3	2	-	1	6	7	V	-	V	8	-	2	2	V	LQFP48
NANO100SC2BN	32K	8K	Configurable	4K	up to 52	4x32-bit	5	3	2	-	1	8	7	V	-	V	8	-	2	3	V	LQFP64
NANO100SD2BN	64K	8K	Configurable	4K	up to 52	4x32-bit	5	3	2	-	1	8	7	V	-	V	8	-	2	3	V	LQFP64
NANO100SD3BN	64K	16K	Configurable	4K	up to 52	4x32-bit	5	3	2	-	1	8	7	V	-	V	8	-	2	3	V	LQFP64
NANO100SE3BN	128K	16K	Configurable	4K	up to 52	4x32-bit	5	3	2	-	1	8	7	V	-	V	8	-	2	3	V	LQFP64
NANO100KD3BN	64K	16K	Configurable	4K	up to 86	4x32-bit	5	3	2	-	1	8	12	V	V	V	8	-	2	3	V	LQFP128
NANO100KE3BN	128K	16K	Configurable	4K	up to 86	4x32-bit	5	3	2	-	1	8	12	V	V	V	8	-	2	3	V	LQFP128

QFN*48* : 7x7, pitch 0.5 mm ; LQFP48 : 7x7, pitch 0.5 mm ; LQFP64 : 7x7, pitch 0.4 mm ; LQFP128 : 14x14, pitch 0.4 mm

Table 3-1 Nano100 Base Line Selection Table

3.2.2 NuMicro™ Nano110 LCD Line Selection Guide

Part No.	Flash (Kbytes)	SRAM (Kbytes)	Data Flash	ISP ROM (Kbytes)	I/O	Timer (32-bit)	Connectivity				I2S	PWM (16-bit	ADC (12-bit)	RTC	EBI	IRC 10KHz 12MHz	PDMA	LCD	DAC (12-bit)	ISO-7816-3	ISP ICP	Package
							UART	SPI	I2C	USB												
NANO110SC2BN	32K	8K	Configurable	4K	up to 51	4x32-bit	5	3	2	-	1	7	7	V	-	V	8	4x31, 6x29	2	3	V	LQFP64
NANO110SD2BN	64K	8K	Configurable	4K	up to 51	4x32-bit	5	3	2	-	1	7	7	V	-	V	8	4x31, 6x29	2	3	V	LQFP64
NANO110SD3BN	64K	16K	Configurable	4K	up to 51	4x32-bit	5	3	2	-	1	7	7	V	-	V	8	4x31, 6x29	2	3	V	LQFP64
NANO110SE3BN	128K	16K	Configurable	4K	up to 51	4x32-bit	5	3	2	-	1	7	7	V	-	V	8	4x31, 6x29	2	3	V	LQFP64
NANO110RC2BN	32K	8K	Configurable	4K	up to 51	4x32-bit	5	3	2	-	1	7	7	V	-	V	8	4x31, 6x29	2	3	V	LQFP64*
NANO110RD2BN	64K	8K	Configurable	4K	up to 51	4x32-bit	5	3	2	-	1	7	7	V	-	V	8	4x31, 6x29	2	3	V	LQFP64*
NANO110RD3BN	64K	16K	Configurable	4K	up to 51	4x32-bit	5	3	2	-	1	7	7	V	-	V	8	4x31, 6x29	2	3	V	LQFP64*
NANO110RE3BN	128K	16K	Configurable	4K	up to 51	4x32-bit	5	3	2	-	1	7	7	V	-	V	8	4x31, 6x29	2	3	V	LQFP64*
NANO110KC2BN	32K	8K	Configurable	4K	up to 86	4x32-bit	5	3	2	-	1	8	12	V	V	V	8	4x40, 6x38	2	3	V	LQFP128
NANO110KD2BN	64K	8K	Configurable	4K	up to 86	4x32-bit	5	3	2	-	1	8	12	V	V	V	8	4x40, 6x38	2	3	V	LQFP128
NANO110KD3BN	64K	16K	Configurable	4K	up to 86	4x32-bit	5	3	2	-	1	8	12	V	V	V	8	4x40, 6x38	2	3	V	LQFP128
NANO110KE3BN	128K	16K	Configurable	4K	up to 86	4x32-bit	5	3	2	-	1	8	12	V	V	V	8	4x40, 6x38	2	3	V	LQFP128

LQFP64 : 7x7, pitch 0.4 mm ; LQFP64* : 10x10, pitch 0.5 mm ; LQFP128 : 14x14, pitch 0.4 mm

Table 3-2 Nano110 LCD Line Selection Table

3.2.3 NuMicro™ Nano120 USB Connectivity Line Selection Guide

Part No.	Flash (Kbytes)	SRAM (Kbytes)	Data Flash	ISP ROM (Kbytes)	I/O	Timer (32-bit)	Connectivity				I2S	PWM (16-bit	ADC (12-bit)	RTC	EBI	IRC 10KHz 12MHz	PDMA	LCD	DAC (12-bit)	ISO-7816-3	ISP ICP	Package
							UART	SPI	I2C	USB												
NANO120LC2BN	32K	8K	Configurable	4K	up to 34	4x32-bit	4	3	2	1	1	4	7	V	-	V	8	-	2	2	V	LQFP48
NANO120LD2BN	64K	8K	Configurable	4K	up to 34	4x32-bit	4	3	2	1	1	4	7	V	-	V	8	-	2	2	V	LQFP48
NANO120LD3BN	64K	16K	Configurable	4K	up to 34	4x32-bit	4	3	2	1	1	4	7	V	-	V	8	-	2	2	V	LQFP48
NANO120LE3BN	128K	16K	Configurable	4K	up to 34	4x32-bit	4	3	2	1	1	4	7	V	-	V	8	-	2	2	V	LQFP48
NANO120SC2BN	32K	8K	Configurable	4K	up to 48	4x32-bit	5	3	2	1	1	8	7	V	-	V	8	-	2	3	V	LQFP64
NANO120SD2BN	64K	8K	Configurable	4K	up to 48	4x32-bit	5	3	2	1	1	8	7	V	-	V	8	-	2	3	V	LQFP64
NANO120SD3BN	64K	16K	Configurable	4K	up to 48	4x32-bit	5	3	2	1	1	8	7	V	-	V	8	-	2	3	V	LQFP64
NANO120SE3BN	128K	16K	Configurable	4K	up to 48	4x32-bit	5	3	2	1	1	8	7	V	-	V	8	-	2	3	V	LQFP64
NANO120KD3BN	64K	16K	Configurable	4K	up to 86	4x32-bit	5	3	2	1	1	8	8	V	V	V	8	-	2	3	V	LQFP128
NANO120KE3BN	128K	16K	Configurable	4K	up to 86	4x32-bit	5	3	2	1	1	8	8	V	V	V	8	-	2	3	V	LQFP128

LQFP48 : 7x7, pitch 0.5 mm ; LQFP64 : 7x7, pitch 0.4 mm ; LQFP128 : 14x14, pitch 0.4 mm

Table 3-3 Nano120 USB Connectivity Line Selection Table

3.3 Pin Configuration

3.3.1 NuMicro™ Nano100 Pin Diagrams

3.3.1.1 NuMicro™ Nano100 LQFP 128-pin

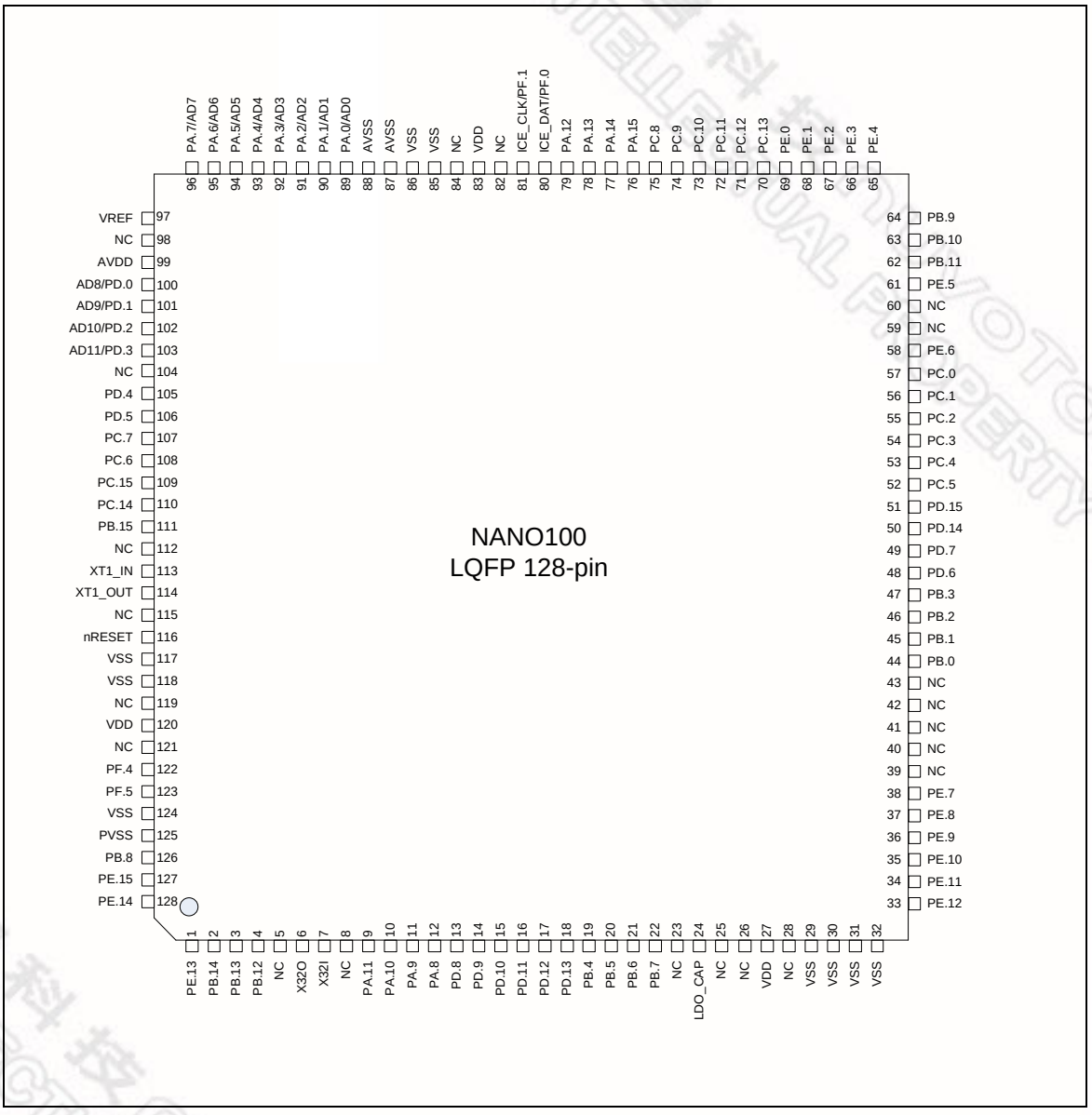


Figure 3-2 NuMicro™ Nano100 LQFP 128-pin Diagram

Pin No.			Pin Name	Pin Type	Description
LQFP 128-pin	LQFP 64-pin	LQFP/QFN 48-pin			
26					NC
27	15	11	VDD	**P**	Power supply for I/O ports and LDO source
28					NC
29	16	12	VSS	**P**	Ground
30			VSS	**P**	Ground
31			VSS	**P**	Ground
32			VSS	**P**	Ground
33			PE.12	**I/O**	General purpose digital I/O pin
34			PE.11	**I/O**	General purpose digital I/O pin
35			PE.10	**I/O**	General purpose digital I/O pin
36			PE.9	**I/O**	General purpose digital I/O pin
37			PE.8	**I/O**	General purpose digital I/O pin
38			PE.7	**I/O**	General purpose digital I/O pin
39					NC
40					NC
41					NC
42					NC
43					NC
44	17	13	PB.0	**I/O**	General purpose digital I/O pin
			UART0_RXD	**I**	UART0 Data receiver input pin
			SPI1_MOSI0	**I/O**	SPI1 1st MOSI (Master Out, Slave In) pin
45	18	14	PB.1	**I/O**	General purpose digital I/O pin
			UART0_TXD	**O**	UART0 Data transmitter output pin
			SPI1_MISO0	**I/O**	SPI1 1st MISO (Master In, Slave Out) pin
46	19	15	PB.2	**I/O**	General purpose digital I/O pin
			UART0_RTSn	**O**	UART0 Request to Send output pin
			EBI_nWRL	**O**	EBI low byte write enable output pin
			SPI1_CLK	**I/O**	SPI1 serial clock pin
47	20	16	PB.3	**I/O**	General purpose digital I/O pin
			UART0_CTSn	**I**	UART0 Clear to Send input pin

Pin No.			Pin Name	Pin Type	Description
LQFP 128-pin	LQFP 64-pin	LQFP/QFN 48-pin			
61	29	21	PE.5	I/O	General purpose digital I/O pin
			PWM1_CH1	I/O	PWM1 Channel1 output
62	30	22	PB.11	I/O	General purpose digital I/O pin
			PWM1_CH0	I/O	PWM1 Channel0 output
			TM3	O	Timer3 external counter input
			SC2_DAT	I/O	SmartCard2 DATA pin(SC2_UART_RXD)
			SPI0_MISO0	I/O	SPI0 1st MISO (Master In, Slave Out) pin
63	31	23	PB.10	I/O	General purpose digital I/O pin
			SPI0_SS1	I/O	SPI0 2nd slave select pin
			TM2	O	Timer2 external counter input
			SC2_CLK	O	SmartCard2 clock pin(SC2_UART_TXD)
			SPI0_MOSI0	I/O	SPI0 1st MOSI (Master Out, Slave In) pin
64	32	24	PB.9	I/O	General purpose digital I/O pin
			SPI1_SS1	I/O	SPI1 2nd slave select pin
			TM1	O	Timer1 external counter input
			SC2_RST	O	SmartCard2 RST pin
			INT0	I	External interrupt0 input pin
65			PE.4	I/O	General purpose digital I/O pin
			SPI0_MOSI0	I/O	SPI0 1st MOSI (Master Out, Slave In) pin
66			PE.3	I/O	General purpose digital I/O pin
			SPI0_MISO0	I/O	SPI0 1st MISO (Master In, Slave Out) pin
67			PE.2	I/O	General purpose digital I/O pin
			SPI0_CLK	I/O	SPI0 serial clock pin
68			PE.1	I/O	General purpose digital I/O pin.
			PWM1_CH3	I/O	PWM1 Channel3 output
			SPI0_SS0	I/O	SPI0 1st slave select pin
69			PE.0	I/O	General purpose digital I/O pin
			PWM1_CH2	I/O	PWM1 Channel2 output
			I2S_MCLK	O	I2S master clock output pin
70			PC.13	I/O	General purpose digital I/O pin

Pin No.			Pin Name	Pin Type	Description
LQFP 128-pin	LQFP 64-pin	LQFP 48-pin			
10	7		PA.10	I/O	General purpose digital I/O pin
			I2C1_SDA	I/O	I^2C1 data I/O pin
			EBI_nWR	O	EBI write enable output pin
			SC0_PWR	O	SmartCard0 Power pin
			SPI2_MISO0	I/O	SPI2 1st MISO (Master In, Slave Out) pin
			LCD_SEG8	O	LCD segment output 8 at LQFP64
			LCD_SEG22	O	LCD segment output 22 at LQFP128
11	8		PA.9	I/O	General purpose digital I/O pin
			I2C0_SCL	I/O	I^2C0 clock pin
			SC0_DAT	I/O	SmartCard0 DATA pin(SC0_UART_RXD)
			SPI2_CLK	I/O	SPI2 serial clock pin
			LCD_SEG7	O	LCD segment output 7 at LQFP64
			LCD_SEG21	O	LCD segment output 21 at LQFP128
12	9		PA.8	I/O	General purpose digital I/O pin
			I2C0_SDA	I/O	I^2C0 data I/O pin
			SC0_CLK	O	SmartCard0 clock pin(SC0_UART_TXD)
			SPI2_SS0	I/O	SPI2 1st slave select pin
			LCD_SEG6	O	LCD segment output 6 at LQFP64
			LCD_SEG20	O	LCD segment output 20 at LQFP128
13			PD.8	I/O	General purpose digital I/O pin
			LCD_SEG19	O	LCD segment output 19 at LQFP128
14			PD.9	I/O	General purpose digital I/O pin
			LCD_SEG18	O	LCD segment output 18 at LQFP128
15			PD.10	I/O	General purpose digital I/O pin
			LCD_SEG17	O	LCD segment output 17 at LQFP128
16			PD.11	I/O	General purpose digital I/O pin
			LCD_SEG16	O	LCD segment output 16 at LQFP128
17			PD.12	I/O	General purpose digital I/O pin
			LCD_SEG15	O	LCD segment output 15 at LQFP128
18			PD.13	I/O	General purpose digital I/O pin

Pin No.			Pin Name	Pin Type	Description
LQFP 128-pin	LQFP 64-pin	LQFP 48-pin			
			LCD_SEG29	**O**	LCD segment output 29 at LQFP128
128			PE.14	**I/O**	General purpose digital I/O pin
			LCD_SEG28	**O**	LCD segment output 28 at LQFP128

Note:

1. Pin Type: I = Digital Input, O=Digital Output; AI=Analog Input; AO= Analog Output; P=Power Pin; AP=Analog Power;
2. * : Output voltage for ADC/LCD shared pins cannot be higher than VDD because these pins are without 5V tolerance.

Pin No.			Pin Name	Pin Type	Description
LQFP 128	LQFP 64	LQFP 48			
12	9	7	PA.8	**I/O**	General purpose digital IO pin
			I2C0_SDA	**I/O**	I^2C 0 data I/O pin
			SC0_CLK	**O**	SmartCard0 clock pin(SC0_UART_TXD)
			SPI2_SS0	**I/O**	SPI2 1st slave select pin
13			PD.8	**I/O**	General purpose digital IO pin
14			PD.9	**I/O**	General purpose digital IO pin
15			PD.10	**I/O**	General purpose digital IO pin
16			PD.11	**I/O**	General purpose digital IO pin
17			PD.12	**I/O**	General purpose digital IO pin
18			PD.13	**I/O**	General purpose digital IO pin
19	10	8	PB.4	**I/O**	General purpose digital IO pin
			UART1_RXD	**I**	UART1 Data receiver input pin
			SC0_CD	**I**	SmartCard0 card detect pin
			SPI2_SS0	**I/O**	SPI2 1st slave select pin
20	11	9	PB.5	**I/O**	General purpose digital IO pin
			UART1_TXD	**O**	UART1 Data transmitter output pin
			SC0_RST	**O**	SmartCard0 RST pin
			SPI2_CLK	**I/O**	SPI2 serial clock pin
21	12		PB.6	**I/O**	General purpose digital IO pin
			UART1_nRTS	**O**	UART1 Request to Send output pin
			EBI_ALE	**O**	EBI address latch enable output pin
			SPI2_MISO0	**I/O**	SPI2 1st MISO (Master In, Slave Out) pin
22	13		PB.7	**I/O**	General purpose digital IO pin
			UART1_nCTS	**I**	UART1 Clear to Send input pin
			EBI_nCS	**O**	EBI chip select enable output pin
			SPI2_MOSI0	**I/O**	SPI2 1st MOSI (Master Out, Slave In) pin
23					NC
24	14	10	LDO_CAP	**P**	LDO output pin
25					NC
26					NC

Pin No.			Pin Name	Pin Type	Description
LQFP 128	LQFP 64	LQFP 48			
			EBI_nWRH	**O**	EBI high byte write enable output pin
			SPI1_SS0	**I/O**	SPI1 1st slave select pin
48			PD.6	**I/O**	General purpose digital IO pin
49			PD.7	**I/O**	General purpose digital IO pin
50			PD.14	**I/O**	General purpose digital IO pin
51			PD.15	**I/O**	General purpose digital IO pin
52			PC.5	**I/O**	General purpose digital IO pin
			SPI0_MOSI1	**I/O**	SPI0 2nd MOSI (Master Out, Slave In) pin
53			PC.4	**I/O**	General purpose digital IO pin
			SPI0_MISO1	**I/O**	SPI0 2nd MISO (Master In, Slave Out) pin
54	25	21	PC.3	**I/O**	General purpose digital IO pin
			SPI0_MOSI0	**I/O**	SPI0 1st MOSI (Master Out, Slave In) pin
			I2S_DO	**O**	I2S data output
			SC1_RST	**O**	SmartCard1 RST pin
55	26	22	PC.2	**I/O**	General purpose digital IO pin
			SPI0_MISO0	**I/O**	SPI0 1st MISO (Master In, Slave Out) pin
			I2S_DI	**I**	I2S data input
			SC1_PWR	**O**	SmartCard1 PWR pin
56	27	23	PC.1	**I/O**	General purpose digital IO pin
			SPI0_CLK	**I/O**	SPI0 serial clock pin
			I2S_BCLK	**I/O**	I2S bit clock pin
			SC1_DAT	**I/O**	SmartCard1 DATA pin(SC1_UART_RXD)
57	28	24	PC.0 / MCLKO	**I/O**	General purpose digital IO pin / Module clock output pin
			SPI0_SS0	**I/O**	SPI0 1st slave select pin
			I2S_LRCLK	**I/O**	I2S left right channel clock
			SC1_CLK	**O**	SmartCard1 clock pin(SC1_UART_TXD)
58			PE.6	**I/O**	General purpose digital IO pin
59					NC
60					NC

Pin No.			Pin Name	Pin Type	Description
LQFP 128-pin	LQFP 64-pin	LQFP 48-pin			
			DA1_OUT	**AO**	DAC 1 output
			EBI_AD5	**I/O**	EBI Address/Data bus bit5
			TC1	**I**	Timer1 capture input
			PWM0_CH1	**O**	PWM1 Channel1 output
			LCD_SEG17*	**AO**	LCD segment output 17 at LQFP64
108	54		PC.6	**I/O**	General purpose digital I/O pin
			DA0_OUT	**I**	DAC0 output
			EBI_AD4	**I/O**	EBI Address/Data bus bit4
			TC0	**I**	Timer0 capture input
			SC1_CD		SmartCard1 card detect pin
			PWM0_CH0	**O**	PWM0 Channel0 output
109	55		PC.15	**I/O**	General purpose digital I/O pin
			EBI_AD3	**I/O**	EBI Address/Data bus bit3
			TC0	**I**	Timer0 capture input
			PWM1_CH2	**O**	PWM1 Channel1 output
			LCD_SEG16	**AO**	LCD segment output 16 at LQFP64
			LCD_SEG33	**AO**	LCD segment output 33 at LQFP128
110	56		PC.14	**I/O**	General purpose digital I/O pin
			EBI_AD2	**I/O**	EBI Address/Data bus bit2
			PWM1_CH3	**I/O**	PWM1 Channel3 output
			LCD_SEG15	**AO**	LCD segment output 15 at LQFP64
			LCD_SEG32	**AO**	LCD segment output 32 at LQFP128
111	57		PB.15	**I/O**	General purpose digital I/O pin
			INT1	**I**	External interrupt1 input pin
			SNOOPER	**I**	Snooper pin
			SC1_CD	**I**	SmartCard1 card detect
			LCD_SEG14	**AO**	LCD segment output 14 at LQFP64
			LCD_SEG31	**AO**	LCD segment output 31 at LQFP128
112					NC
113	58		XT1_IN	**O**	External 4~24 MHz crystal output pin

Pin No.			Pin Name	Pin Type	Description
LQFP 128-pin	LQFP 64-pin	LQFP 48-pin			
			PF.3	**I/O**	General purpose digital I/O pin
114	59		XT1_OUT	**I**	External 4~24 MHz crystal input pin
			PF.2	**I/O**	General purpose digital I/O pin
115					NC
116	60		nRESET	**I**	External reset input: Low active, set this pin low reset chip to initial state. With internal pull-up.
117	61		VSS	**P**	Ground
118			VSS	**P**	Ground
119					NC
120	62		VDD	**P**	Power supply for I/O ports and LDO source for internal PLL and digital circuit
121					NC
122			PF.4	**I/O**	General purpose digital I/O pin
			I2C0_SDA	**I/O**	I^2C0 data I/O pin
123			PF.5	**I/O**	Digital GPI/O pin
			I2C0_SCL	**I/O**	I^2C0 clock pin
124			VSS	**P**	Ground
125	63		PVSS	**I/O**	PLL Ground
126	64		PB.8	**I/O**	General purpose digital I/O pin
			STADC	**I**	ADC external trigger input.
			TM0	**I**	Timer0 external counter input
			INT0	**I**	External interrupt0 input pin
			SC2_PWR	**O**	SmartCard2 Power pin
			LCD_SEG13	**AO**	LCD segment output 13 at LQFP64
			LCD_SEG30	**AO**	LCD segment output 30 at LQFP128
127			PE.15	**I/O**	General purpose digital I/O pin
			LCD_SEG29	**O**	LCD segment output 29 at LQFP128
128			PE.14	**I/O**	General purpose digital I/O pin
			LCD_SEG28	**O**	LCD segment output 28 at LQFP128

Note:

1. Pin Type: I=Digital Input, O=Digital Output; AI=Analog Input; AO=Analog Output; P=Power Pin; AP=Analog Power
2. * : Output voltage for ADC/LCD shared pins cannot be higher than VDD because these pins are without 5V tolerance.

4.2 Nano110 Block Diagram

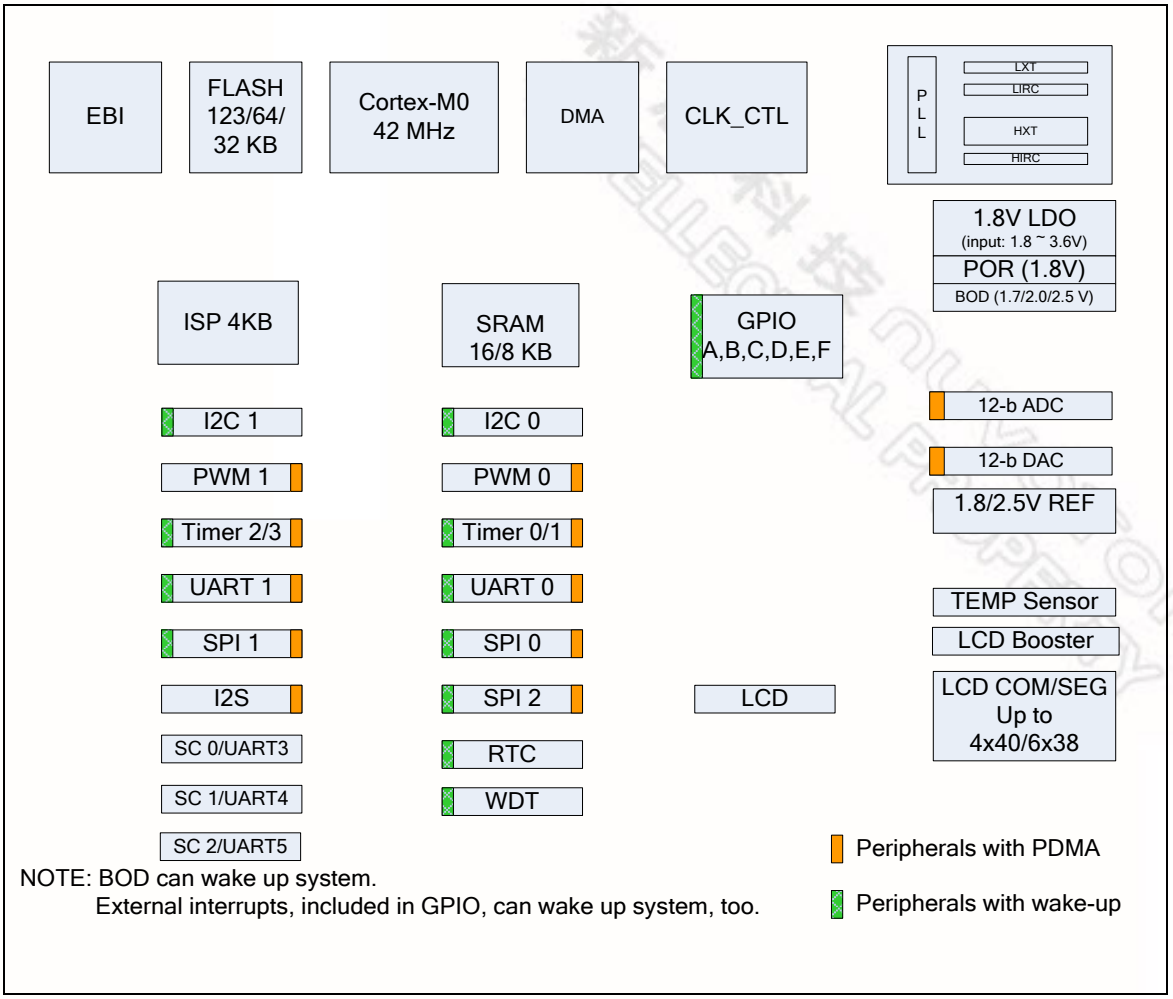


Figure 4-2 NuMicro™ Nano110 Block Diagram

5.8 External Bus Interface

5.8.1 Overview

This chip is equipped with an external bus interface (EBI) to access external device. To save the connections between external device and this chip, EBI support address bus and data bus multiplex mode. Also, address latch enable (ALE) signal is used to differentiate the address and data cycle.

5.8.2 Features

- External devices with max. 64 Kbytes size (8-bit data width)/128 Kbytes (16-bit data width) supported
- Supports variable external bus base clock (MCLK)
- Supports 8-bit or 16-bit data width
- Supports variable data access time (tACC), address latch enable time (tALE) and address hold time (tAHD)
- Address bus and data bus multiplex mode supported to save the address pins
- Configurable idle cycle supported for different access condition: Write command finish (W2X), Read-to-Read (R2R), Read-to-Write (R2W)
- Supports PDMA and VDMA transfer

5.9 FLASH Memory Controller (FMC)

5.9.1 Overview

This chip is equipped with 32K/64K/123K bytes on-chip embedded Flash EPROM for application program memory (APROM) that can be updated through ISP/IAP procedure. In System Programming (ISP) function enables user to update program memory when chip is soldered on PCB. After chip powered on Cortex-M0 CPU fetches code from APROM or LDROM decided by boot select (CBS) in Config0. By the way, this chip also provides DATA Flash Region, the data flash is shared with original program memory and its start address is configurable and defined by user in Config1. The data flash size is defined by user application request.

5.9.2 Features

- AHB interface compatible
- Run up to 42 MHz with zero wait state for discontinuous address read access
- 32/64/123KB application program memory (APROM)
- 4KB in system programming (ISP) loader program memory (LDROM)
- Programmable data flash start address and memory size with 512 bytes page erase unit
- In System Program (ISP)/In Application Program (IAP) to update on chip Flash EPROM

5.18 Timer Controller

5.18.1 Overview

This chip is equipped with four timer modules including TIMER0, TIMER1, TIMER2 and TIMER3 (TIMER0/1 is at APB1 and TIMER2/3 is at APB2), which allow user to easily implement a counting scheme or timing control for applications. The timer can perform functions like frequency measurement, event counting, interval measurement, clock generation, delay timing, and so on. The timer can generate an interrupt signal upon timeout, or provide the current value of count during operation.

5.18.2 Features

- Independent Clock Source for each Timer (TMRx_CLK, x= 0, 1,2,3)
- Time-out period = (Period of timer clock input) * (8-bit pre-scale counter + 1) * (24-bit TCMP)
- Counting cycle time = (1 / TMRx_CLK) * (2^8) * (2^24)
- Internal 8-bit pre-scale counter
- Internal 24-bit up counter is readable through TDR (Timer Data Register)
- Supports One-shot, Periodic,Output Toggle and Countinuous Counting Operation mode
- Supports external pin capture for interval measurement
- Supports external pin capture for timer counter reset
- Supports Inter-Timer trigger
- Supports Internal trigger event to ADC, DAC and PDMA

8 POWER COMSUMPTION

Part No	Test Condition		VDD	CPU Clock	Current
Nano100 (B) series 128 KB Flash 16 KB RAM	**Operating Mode:** CPU run while(1) in FLASH ROM Clock = 12 MHz Crystal Oscillator Disable all peripherial		3.3V	12 MHz	2.41mA 200uA/MHz
			1.8V	12 MHz	N/A
	Idle Mode: CPU stop Clock = 12 MHz Crystal Oscillator Disable all peripherial		3.3V	12 MHz	900uA 75uA/MHz
			1.8V	12 MHz	N/A
	RTC + LCD Mode: (RAM retention) (Power down with 32K and LCD enabled) CPU stop Clock = 32.768 kHz Crystal Oscillator Disable all peripherial except RTC and LCD circuit Without panel loading	C-type	3.3V	-	10uA
		Internal R-type (With 200kΩ Resistor ladder)			8.5uA
		External R-type (With 1MΩ Resistor ladder)			4.5uA
		C-type/R-type	1.8V	-	N/A
	RTC Mode: (RAM retention) (Power down with 32K enabled) CPU stop Clock = 32.768 kHz Crystal Oscillator Disable all peripherial except RTC circuit		3.3V	-	2.5uA
			1.8V	-	2.0uA
	Power-down Mode: (RAM retention) CPU and all clocks stop		3.3V	-	1uA
			1.8V	-	0.8uA
	Wake-Up from Power-down Mode		3.3V	7us	N/A

Note: Wake-up time: 7us from wake-up event to first CPU core valid clock; 10us from interrupt event to interrupt service routine first instruction.

9 ELECTRICAL CHARACTERISTIC

SYMBOL	PARAMETER	MIN	MAX	UNIT
DC Power Supply	V_{DD}–V_{SS}	-0.3	+4.0	V
Input Voltage on 5V Tolerance Pin	V_{IN}	V_{SS} -0.3	V_{DD} +3.7	V
Input Voltage on Any Other Pin without 5V Tolerance Pin	V_{IN}	V_{SS} -0.3	V_{DD} +0.3	V
Oscillator Frequency	$1/t_{CLCL}$	4	24	MHz
Operating Temperature	T_A	-40	+85	°C
Storage Temperature	T_{ST}	-55	+150	°C
Maximum Current into VDD		-	150	mA
Maximum Current out of VSS		-	150	mA
Maximum Current sunk by a I/O Pin		-	25	mA
Maximum Current Sourced by a I/O Pin		-	25	mA
Maximum Current Sunk by Total I/O Pins		-	100	mA
Maximum Current Sourced by Total I/O Pins		-	100	mA

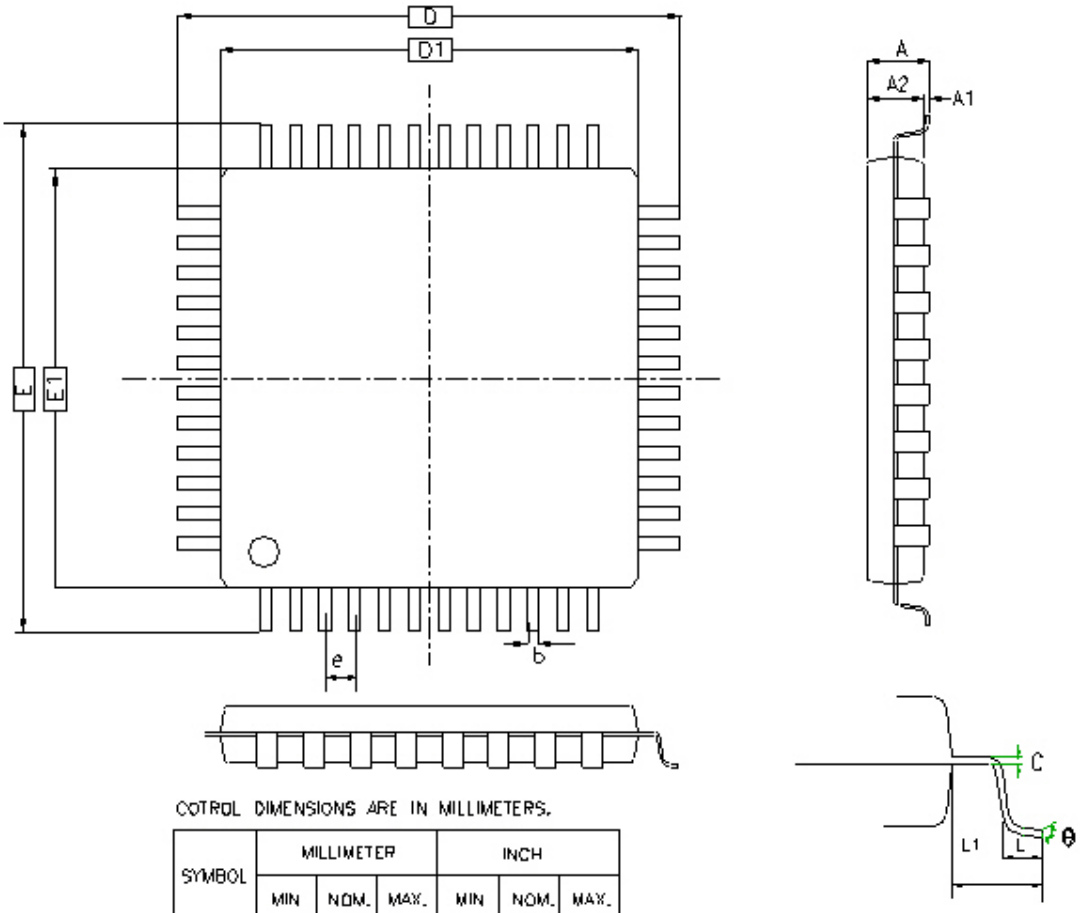
9.1 Absolute Maximum Ratings

Note : Output voltage for ADC/LCD shared pins cannot be higher than VDD because these pins are without 5V tolerance.

(LQFP64 : LCD_SEG17, LCD_SEG19, LCD_SEG20, LCD_SEG21, LCD_SEG22, LCD_SEG23)

(LQFP128 : LCD_SEG36, LCD_SEG37, LCD_SEG38, LCD_SEG39)

10.4 LQFP48 (7x7x1.4 mm footprint 2.0 mm)



COTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN	NOM.	MAX.	MIN	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A1	0.05	0.10	0.15	0.002	0.004	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D1	6.90	7.00	7.10	0.272	0.276	0.280
E1	6.90	7.00	7.10	0.272	0.276	0.280
e	0.35	0.50	0.65	0.014	0.020	0.280
D	8.9	9.00	9.10	0.350	0.354	0.358
E	8.9	9.00	9.10	0.350	0.354	0.358
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	—	1.00	—	—	0.039	—
C	0.09	—	0.20	0.0035	—	0.0079
θ	0°	—	7°	0°	—	7°
b	0.17	0.22	0.27	0.007	0.0087	0.011