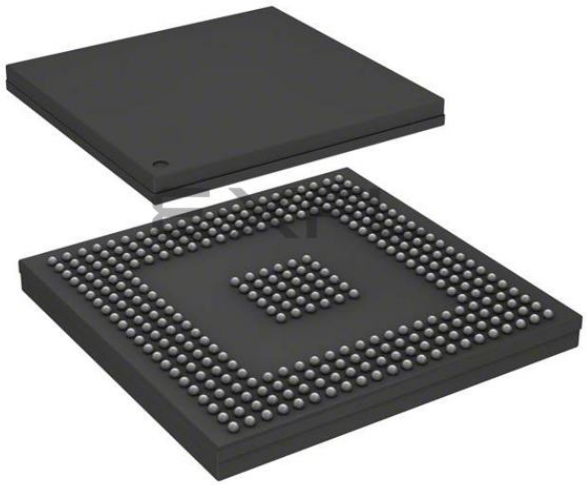

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	e200z6
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, EBI/EMI, Ethernet, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	220
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.35V ~ 1.65V
Data Converters	A/D 40x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	324-BBGA
Supplier Device Package	324-PBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5534mvz80

The MPC5500 family of parts contains many new features coupled with high performance CMOS technology to provide significant performance improvement over the MPC565.

The host processor core of the MPC5534 also includes an instruction set enhancement allowing variable length encoding (VLE). This allows optional encoding of mixed 16- and 32-bit instructions. With this enhancement, it is possible to significantly reduce the code size footprint.

The MPC5534 has a single-level memory hierarchy consisting of 64-kilobytes (KB) on-chip SRAM and one megabyte (MB) of internal flash memory. Both the SRAM and the flash memory can hold instructions and data. The external bus interface (EBI) supports most standard memories used with the MPC5*xx* family.

The MPC5534 does not support arbitration with other masters on the external bus. The MPC5534 must be the only master on the external bus, or act as a slave-only device.

The complex input/output timer functions of the MPC5534 are performed by an enhanced time processor unit (eTPU) engine. The eTPU engine controls 32 hardware channels. The eTPU has been enhanced over the TPU by providing: 24-bit timers, double-action hardware channels, variable number of parameters per channel, angle clock hardware, and additional control and arithmetic instructions. The eTPU is programmed using a high-level programming language.

The less complex timer functions of the MPC5534 are performed by the enhanced modular input/output system (eMIOS). The eMIOS' 24 hardware channels are capable of single-action, double-action, pulse-width modulation (PWM), and modulus-counter operations. Motor control capabilities include edge-aligned and center-aligned PWM.

Off-chip communication is performed by a suite of serial protocols including controller area networks (FlexCANs), enhanced deserial/serial peripheral interfaces (DSPIs), and enhanced serial communications interfaces (eSCIs).

The MCU has an on-chip enhanced queued dual analog-to-digital converter (eQADC) with a 5 V conversion range. The 324 package has 40-channels; the 208 package has 34 channels.

The system integration unit (SIU) performs several chip-wide configuration functions. Pad configuration and general-purpose input and output (GPIO) are controlled from the SIU. External interrupts and reset control are also determined by the SIU. The internal multiplexer sub-block (IMUX) provides multiplexing of eQADC trigger sources and external interrupt signal multiplexing.

3 Electrical Characteristics

This section contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications for the MCU.

3.1 Maximum Ratings

Table 2. Absolute Maximum Ratings [1]

Spec	Characteristic	Symbol	Min.	Max.	Unit
1	1.5 V core supply voltage [2]	V_{DD}	–0.3	1.7	V
2	Flash program/erase voltage	V_{PP}	–0.3	6.5	V
4	Flash read voltage	V_{FLASH}	–0.3	4.6	V
5	SRAM standby voltage	V_{STBY}	–0.3	1.7	V
6	Clock synthesizer voltage	V_{DDSYN}	–0.3	4.6	V
7	3.3 V I/O buffer voltage	V_{DD33}	–0.3	4.6	V
8	Voltage regulator control input voltage	V_{RC33}	–0.3	4.6	V
9	Analog supply voltage (reference to V_{SSA})	V_{DDA}	–0.3	5.5	V
10	I/O supply voltage (fast I/O pads) [3]	V_{DDE}	–0.3	4.6	V
11	I/O supply voltage (slow and medium I/O pads) [3]	V_{DDEH}	–0.3	6.5	V
12	DC input voltage [4] V_{DDEH} powered I/O pads V_{DDE} powered I/O pads	V_{IN}	 –1.0 [5] –1.0 [5]	 6.5 [6] 4.6 [7]	V
13	Analog reference high voltage (reference to V_{RL})	V_{RH}	–0.3	5.5	V
14	V_{SS} to V_{SSA} differential voltage	$V_{SS} – V_{SSA}$	–0.1	0.1	V
15	V_{DD} to V_{DDA} differential voltage	$V_{DD} – V_{DDA}$	$–V_{DDA}$	V_{DD}	V
16	V_{REF} differential voltage	$V_{RH} – V_{RL}$	–0.3	5.5	V
17	V_{RH} to V_{DDA} differential voltage	$V_{RH} – V_{DDA}$	–5.5	5.5	V
18	V_{RL} to V_{SSA} differential voltage	$V_{RL} – V_{SSA}$	–0.3	0.3	V
19	V_{DDEH} to V_{DDA} differential voltage	$V_{DDEH} – V_{DDA}$	$–V_{DDA}$	V_{DDEH}	V
20	V_{DDF} to V_{DD} differential voltage	$V_{DDF} – V_{DD}$	–0.3	0.3	V
21	V_{RC33} to V_{DDSYN} differential voltage spec has been moved to Table 9 DC Electrical Specifications, Spec 43a.				
22	V_{SSSYN} to V_{SS} differential voltage	$V_{SSSYN} – V_{SS}$	–0.1	0.1	V
23	V_{RCVSS} to V_{SS} differential voltage	$V_{RCVSS} – V_{SS}$	–0.1	0.1	V
24	Maximum DC digital input current [8] (per pin, applies to all digital pins) [4]	I_{MAXD}	–2	2	mA
25	Maximum DC analog input current [9] (per pin, applies to all analog pins)	I_{MAXA}	–3	3	mA
26	Maximum operating temperature range [10] Die junction temperature	T_J	T_L	150.0	°C
27	Storage temperature range	T_{STG}	–55.0	150.0	°C

At a known board temperature, the junction temperature is estimated using the following equation:

$$T_J = T_B + (R_{\theta JB} \times P_D)$$

where:

T_J = junction temperature (^oC)

T_B = board temperature at the package perimeter ($^oC/W$)

$R_{\theta JB}$ = junction-to-board thermal resistance ($^oC/W$) per JESD51-8

P_D = power dissipation in the package (W)

When the heat loss from the package case to the air does not factor into the calculation, an acceptable value for the junction temperature is predictable. Ensure the application board is similar to the thermal test condition, with the component soldered to a board with internal planes.

The thermal resistance is expressed as the sum of a junction-to-case thermal resistance plus a case-to-ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

where:

$R_{\theta JA}$ = junction-to-ambient thermal resistance ($^oC/W$)

$R_{\theta JC}$ = junction-to-case thermal resistance ($^oC/W$)

$R_{\theta CA}$ = case-to-ambient thermal resistance ($^oC/W$)

$R_{\theta JC}$ is device related and is not affected by other factors. The thermal environment can be controlled to change the case-to-ambient thermal resistance, $R_{\theta CA}$. For example, change the air flow around the device, add a heat sink, change the mounting arrangement on the printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device. This description is most useful for packages with heat sinks where 90% of the heat flow is through the case to heat sink to ambient. For most packages, a better model is required.

A more accurate two-resistor thermal model can be constructed from the junction-to-board thermal resistance and the junction-to-case thermal resistance. The junction-to-case thermal resistance describes when using a heat sink or where a substantial amount of heat is dissipated from the top of the package. The junction-to-board thermal resistance describes the thermal performance when most of the heat is conducted to the printed circuit board. This model can be used to generate simple estimations and for computational fluid dynamics (CFD) thermal models.

To determine the junction temperature of the device in the application on a prototype board, use the thermal characterization parameter (Ψ_{JT}) to determine the junction temperature by measuring the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

where:

T_T = thermocouple temperature on top of the package (^oC)

Ψ_{JT} = thermal characterization parameter ($^oC/W$)

P_D = power dissipation in the package (W)

3.5 ESD (Electromagnetic Static Discharge) Characteristics

Table 5. ESD Ratings [1, 2]

Characteristic	Symbol	Value	Unit
ESD for human body model (HBM)		2000	V
HBM circuit description	R1	1500	Ω
	C	100	pF
ESD for field induced charge model (FDCM)		500 (all pins)	V
		750 (corner pins)	
Number of pulses per pin: Positive pulses (HBM) Negative pulses (HBM)	 — —	 1 1	 — —
Interval of pulses	—	1	second

1 All ESD testing conforms to CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.

2 Device failure is defined as: 'If after exposure to ESD pulses, the device does not meet the device specification requirements, which includes the complete DC parametric and functional testing at room temperature and hot temperature.

3.6 Voltage Regulator Controller (V_{RC}) and Power-On Reset (POR) Electrical Specifications

The following table lists the V_{RC} and POR electrical specifications:

Table 6. V_{RC} and POR Electrical Specifications

Spec	Characteristic		Symbol	Min.	Max.	Units
1	1.5 V (V_{DD}) POR [1]	Negated (ramp up) Asserted (ramp down)	V_{POR15}	1.1 1.1	1.35 1.35	V
2	3.3 V (V_{DDSYN}) POR [1]	Asserted (ramp up) Negated (ramp up) Asserted (ramp down) Negated (ramp down)	V_{POR33}	0.0 2.0 2.0 0.0	0.30 2.85 2.85 0.30	V
3	$\overline{\text{RESET}}$ pin supply (V_{DDEH6}) POR [1, 2]	Negated (ramp up) Asserted (ramp down)	V_{POR5}	2.0 2.0	2.85 2.85	V
4	V_{RC33} voltage	Before V_{RC} allows the pass transistor to start turning on	V_{TRANS_START}	1.0	2.0	V
5		When V_{RC} allows the pass transistor to completely turn on [3, 4]	V_{TRANS_ON}	2.0	2.85	V
6		When the voltage is greater than the voltage at which the V_{RC} keeps the 1.5 V supply in regulation [5, 6]	$V_{VRC33REG}$	3.0	—	V
7	Current can be sourced by V_{RCCTL} at Tj:	–40° C 25° C 150° C	I_{VRCCTL} [7]	11.0 9.0 7.5	— — —	mA mA mA
8	Voltage differential during power up such that: V_{DD33} can lag V_{DDSYN} or V_{DDEH6} before V_{DDSYN} and V_{DDEH6} reach the V_{POR33} and V_{POR5} minimums respectively.		V_{DD33_LAG}	—	1.0	V

Table 9. DC Electrical Specifications ($T_A = T_L$ to T_H) (continued)

Spec	Characteristic	Symbol	Min	Max.	Unit
27a	Operating current 1.5 V supplies @ 82 MHz: [6, 7] V_{DD} (including V_{DDF} max current) @1.65 V high use [8, 9, 10, 11, 12] V_{DD} (including V_{DDF} max current) @1.35 V high use [8, 9, 10, 11, 12]	 I_{DD} I_{DD}	 — —	 250 180	 mA mA
27b	Operating current 1.5 V supplies @ 68 MHz: [13, 14] V_{DD} (including V_{DDF} max current) @1.65 V high use [15, 16, 17] V_{DD} (including V_{DDF} max current) @1.35 V high use [15, 16, 17]	 I_{DD} I_{DD}	 — —	 210 160	 mA mA
27c	Operating current 1.5 V supplies @ 42 MHz: [13, 14] V_{DD} (including V_{DDF} max current) @1.65 V high use [15, 16, 17] V_{DD} (including V_{DDF} max current) @1.35 V high use [15, 16, 17]	 I_{DD} I_{DD}	 — —	 130 110	 mA mA
27d	Refer to Figure 2 for an interpolation of this data.[18] I_{DD_STBY} @ 25° C V_{STBY} @ 0.8 V V_{STBY} @ 1.0 V V_{STBY} @ 1.2 V I_{DD_STBY} @ 60° C V_{STBY} @ 0.8 V V_{STBY} @ 1.0 V V_{STBY} @ 1.2 V I_{DD_STBY} @ 150° C (Tj) V_{STBY} @ 0.8 V V_{STBY} @ 1.0 V V_{STBY} @ 1.2 V	 I_{DD_STBY} I_{DD_STBY} I_{DD_STBY} I_{DD_STBY} I_{DD_STBY} I_{DD_STBY} I_{DD_STBY} I_{DD_STBY} I_{DD_STBY}	 — — — — — — — — —	 20 30 50 70 100 200 1200 1500 2000	 µA µA µA µA µA µA µA µA µA
28	Operating current 3.3 V supplies @ f_{MAX} MHz V_{DD33} [19] V_{FLASH} V_{DDSYN}	 I_{DD_33} I_{VFLASH} I_{DDSYN}	 — — —	 2 + (values derived from procedure of footnote [19]) 10 15	 mA mA mA
29	Operating current 5.0 V supplies (12 MHz ADCLK): V_{DDA} (V_{DDA0} + V_{DDA1}) Analog reference supply current (V_{RH}, V_{RL}) V_{PP}	 I_{DD_A} I_{REF} I_{PP}	 — — —	 20.0 1.0 25.0	 mA mA mA
30	Operating current V_{DDE} supplies: [20] V_{DDEH1} V_{DDE2} V_{DDE3} V_{DDEH4} V_{DDE5} V_{DDEH6} V_{DDE7} V_{DDEH8} V_{DDEH9}	 I_{DD1} I_{DD2} I_{DD3} I_{DD4} I_{DD5} I_{DD6} I_{DD7} I_{DD8} I_{DD9}	 — — — — — — — — —	 Refer to footnote [20]	 mA mA mA mA mA mA mA mA mA

3.8.2 I/O Pad V_{DD33} Current Specifications

The power consumption of the V_{DD33} supply dependents on the usage of the pins on all I/O segments. The power consumption is the sum of all input and output pin V_{DD33} currents for all I/O segments. The output pin V_{DD33} current can be calculated from Table 11 based on the voltage, frequency, and load on all fast (pad_fc) pins. The input pin V_{DD33} current can be calculated from Table 11 based on the voltage, frequency, and load on all pad_sh and pad_mh pins. Use linear scaling to calculate pin currents for voltage, frequency, and load parameters that fall outside the values given in Table 11.

Table 11. V_{DD33} Pad Average DC Current ($T_A = T_L$ to T_H) [1]

Spec	Pad Type	Symbol	Frequency (MHz)	Load [2] (pF)	V_{DD33} (V)	V_{DDE} (V)	Drive Select	Current (mA)
Inputs								
1	Slow	I_{33_SH}	66	0.5	3.6	5.5	NA	0.003
2	Medium	I_{33_MH}	66	0.5	3.6	5.5	NA	0.003
Outputs								
3	Fast	I_{33_FC}	66	10	3.6	3.6	00	0.35
4			66	20	3.6	3.6	01	0.53
5			66	30	3.6	3.6	10	0.62
6			66	50	3.6	3.6	11	0.79
7			66	10	3.6	1.98	00	0.35
8			66	20	3.6	1.98	01	0.44
9			66	30	3.6	1.98	10	0.53
10			66	50	3.6	1.98	11	0.70
11			56	10	3.6	3.6	00	0.30
12			56	20	3.6	3.6	01	0.45
13			56	30	3.6	3.6	10	0.52
14			56	50	3.6	3.6	11	0.67
15			56	10	3.6	1.98	00	0.30
16			56	20	3.6	1.98	01	0.37
17			56	30	3.6	1.98	10	0.45
18			56	50	3.6	1.98	11	0.60
19			40	10	3.6	3.6	00	0.21
20			40	20	3.6	3.6	01	0.31
21			40	30	3.6	3.6	10	0.37
22			40	50	3.6	3.6	11	0.48
23			40	10	3.6	1.98	00	0.21
24			40	20	3.6	1.98	01	0.27
25			40	30	3.6	1.98	10	0.32
26			40	50	3.6	1.98	11	0.42

1 These values are estimated from simulation and not tested. Currents apply to output pins for the fast pads only and to input pins for the slow and medium pads only.

2 All loads are lumped.

Table 16 shows the FLASH_BIU settings versus frequency of operation. Refer to the device reference manual for definitions of these bit fields.

Table 16. FLASH_BIU Settings vs. Frequency of Operation[1]

Target Maximum Frequency (MHz)	APC	RWSC	WWSC	DPFEN [2]	IPFEN [2]	PFLIM [3]	BFEN [2]
Up to and including 27 MHz [4, 5]	0b000	0b000	0b01	0b0 0b1	0b0 0b1	0b000 to 0b010	0b0 0b1
Up to and including 52 MHz [6]	0b001	0b001	0b01	0b0 0b1	0b0 0b1	0b000 to 0b010	0b0 0b1
Up to and including 77 MHz [7]	0b010	0b010	0b01	0b0 0b1	0b0 0b1	0b000 to 0b010	0b0 0b1
Up to and including 82 MHz [8]	0b011[9]	0b011[9]	0b01	0b0 0b1	0b0 0b1	0b000 to 0b010	0b0 0b1
Reset values:	0b111	0b111	0b11	0b0	0b0	0b000	0b0

1 Illegal combinations exist. Use entries from the same row in this table.
2 For maximum flash performance, set to 0b1.
3 For maximum flash performance, set to 0b010.
4 27 MHz parts allow for 25 MHz system clock + 2% frequency modulation (FM).
5 The APC, RWSC, and WWSC combination requires setting the PRD bit to 1 in the flash MCR register.
6 52 MHz parts allow for 50 MHz system clock + 2% FM.
7 77 MHz parts allow for 75 MHz system clock + 2% FM.
8 82 MHz parts allow for 80 MHz system clock + 2% FM.
9 For frequencies up to and including 80 MHz, if VDD is within ±5% of 1.5 V, then APC = RWSC = 0b010 is a valid setting.

3.12 AC Specifications

3.12.1 Pad AC Specifications

Table 17. Pad AC Specifications (V_{DDEH} = 5.0 V, V_{DDE} = 1.8 V) [1]

Spec	Pad	SRC / DSC (binary)	Out Delay [2, 3, 4] (ns)	Rise / Fall [4, 5] (ns)	Load Drive (pF)
1	Slow high voltage (SH)	11	26	15	50
			82	60	200
		01	75	40	50
			137	80	200
		00	377	200	50
			476	260	200

Table 18. Derated Pad AC Specifications (V_{DDEH} = 3.3 V, V_{DDE} = 3.3 V) [1] (continued)

Spec	Pad	SRC/DSC (binary)	Out Delay [2, 3, 4] (ns)	Rise / Fall [3, 5] (ns)	Load Drive (pF)
3	Fast	00	3.2	2.4	10
		01		2.2	20
		10		2.1	30
		11		2.1	50
4	Pullup/down (3.6 V max)	—	—	7500	50
5	Pullup/down (5.5 V max)	—	—	9500	50

1 These are worst-case values that are estimated from simulation (not tested). The values in the table are simulated at: V_{DD} = 1.35–1.65 V; V_{DDE} = 3.0–3.6 V; V_{DDEH} = 3.0–3.6 V; V_{DD33} and V_{DDSYN} = 3.0–3.6 V; and $T_A = T_L$ to T_H.

2 This parameter is supplied for reference and guaranteed by design (not tested).

3 The output delay, and the rise and fall, are calculated to 20% or 80% of the respective signal.

4 The output delay is shown in Figure 4. To calculate the output delay with respect to the system clock, add a maximum of one system clock to the output delay.

5 This parameter is guaranteed by characterization rather than 100% tested.

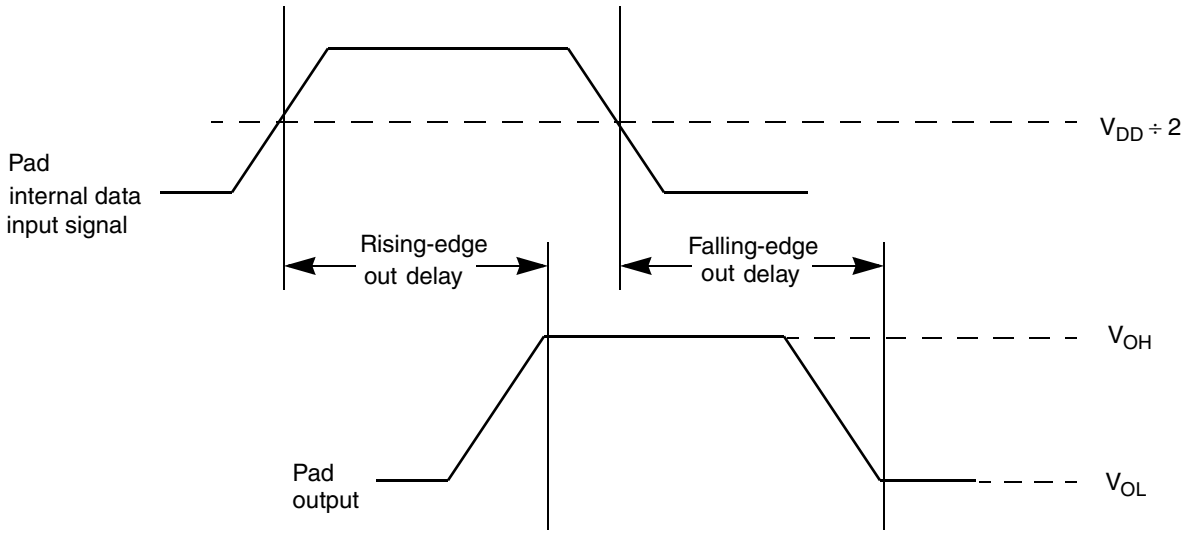


Figure 4. Pad Output Delay

3.13 AC Timing

3.13.1 Reset and Configuration Pin Timing

Table 19. Reset and Configuration Pin Timing [1]

Spec	Characteristic	Symbol	Min.	Max.	Unit
1	$\overline{\text{RESET}}$ pulse width	t_{RPW}	10	—	t_{CYC}
2	$\overline{\text{RESET}}$ glitch detect pulse width	t_{GPW}	2	—	t_{CYC}

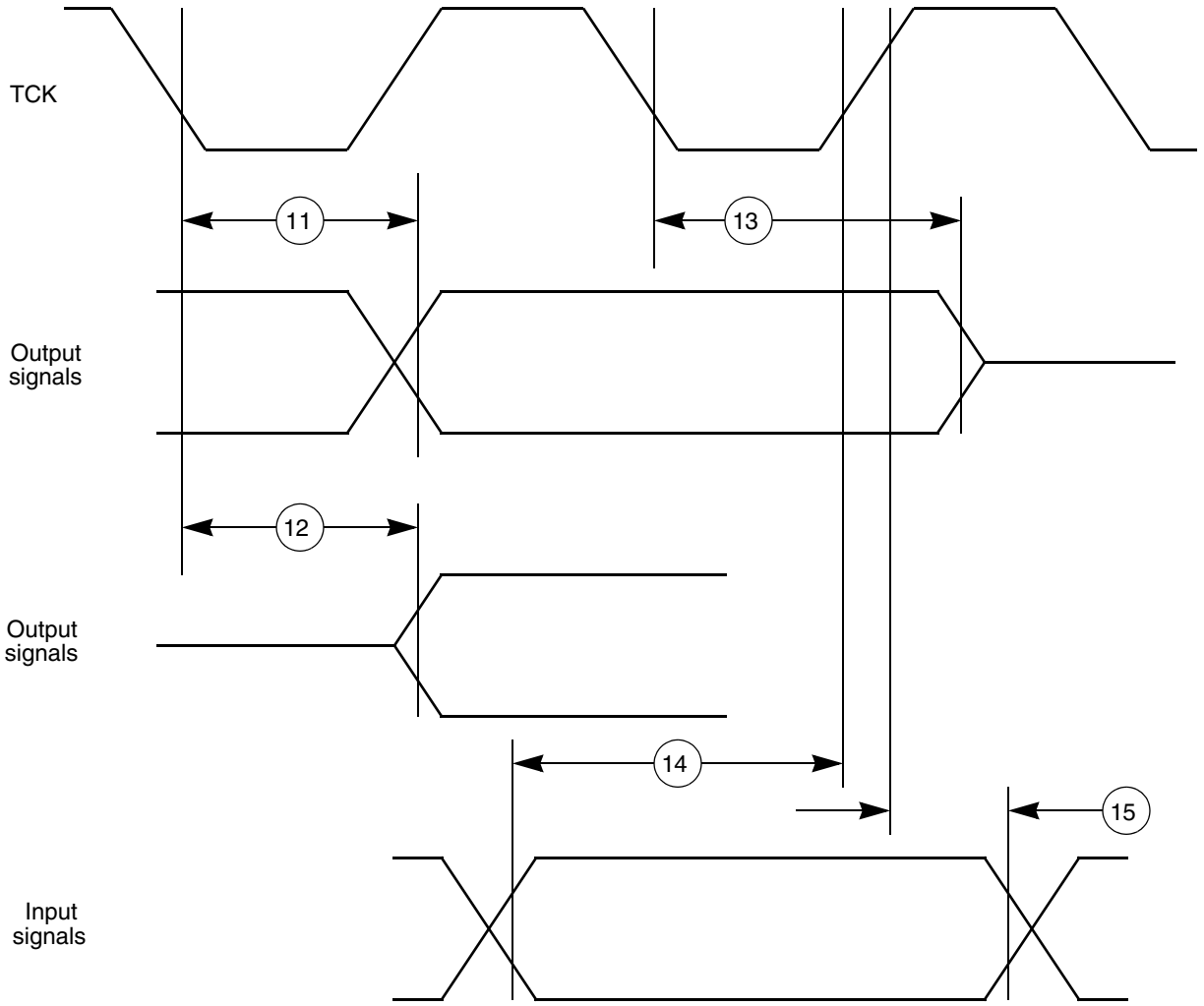


Figure 9. JTAG Boundary Scan Timing

3.13.4 External Bus Interface (EBI) Timing

Table 22 lists the timing information for the external bus interface (EBI).

Table 22. External Bus Operation Timing[1, 2]

Spec	Characteristic and Description	Symbol	External Bus Frequency [3]						Unit	Notes
			20 MHz		33 MHz		40 MHz			
			Min.	Max	Min.	Max	Min.	Max		
1	CLKOUT period	T_C	24.4	—	17.5	—	14.9	—	ns	Signals are measured at 50% V_{DDE}.
2	CLKOUT duty cycle	t_{CDC}	45%	55%	45%	55%	45%	55%	T_C	
3	CLKOUT rise time	t_{CRT}	—	—[4]	—	—	—	—[4]	ns	
4	CLKOUT fall time	t_{CFT}	—	—[4]	—	—[4]	—	—[4]	ns	
5[5]	CLKOUT positive edge to output signal *invalid* or Hi-Z (hold time) External bus interface $\overline{CS}$[0:3] ADDR[8:31] DATA[0:15] RD_$\overline{WR}$ $\overline{BDIP}$ $\overline{WE}$/$\overline{BE}$[0:1] $\overline{OE}$ $\overline{TS}$ $\overline{TA}$	t_{COH}	1.0[6] 1.5	—	1.0[6] 1.5	—	1.0[6] 1.5	—	ns	EBTS = 0 EBTS = 1 Hold time selectable via SIU_ECCR [EBTS] bit.
5	Calibration bus interface CAL_$\overline{CS}$[0, 2:3] CAL_ADDR[10:30] CAL_DATA[0:15] CAL_RD_$\overline{WR}$ CAL_$\overline{WE}$[0:1] CAL_$\overline{OE}$ CAL_$\overline{TS}$	t_{CCOH}	1.0 [6] 1.5	—	1.0 [6] 1.5	—	1.0 [6] 1.5	—	ns	EBTS = 0 EBTS = 1 Hold time selectable via SIU_ECCR [EBTS] bit.
6[5]	CLKOUT positive edge to output signal *valid* (output delay) External bus interface $\overline{CS}$[0:3] ADDR[8:31] DATA[0:15] RD_$\overline{WR}$ $\overline{BDIP}$ $\overline{WE}$/$\overline{BE}$[0:1] $\overline{OE}$ $\overline{TS}$ $\overline{TA}$	t_{COV}	—	10.0[6] 11.0	—	10.0[6] 11.0	—	10.0[6] 11.0	ns	EBTS = 0 EBTS = 1 Output valid time selectable via SIU_ECCR [EBTS] bit.

[3] Speed is the nominal maximum frequency. Max speed is the maximum speed allowed including frequency modulation (FM). 42 MHz parts allow for 40 MHz system clock + 2% FM; 68 MHz parts allow for a 66 MHz system clock + 2% FM, and 82 MHz parts allow for 80 MHz system clock + 2% FM.

[4] Refer to fast pad timing in Table 17 and Table 18 (different values for 1.8 V and 3.3 V).

[5] Available on the 324 package only; not available on the 208 package.

[6] EBTS = 0 timings are tested and valid at V_{DDE} = 2.25–3.6 V only; EBTS = 1 timings are tested and valid at V_{DDE} = 1.6–3.6 V.

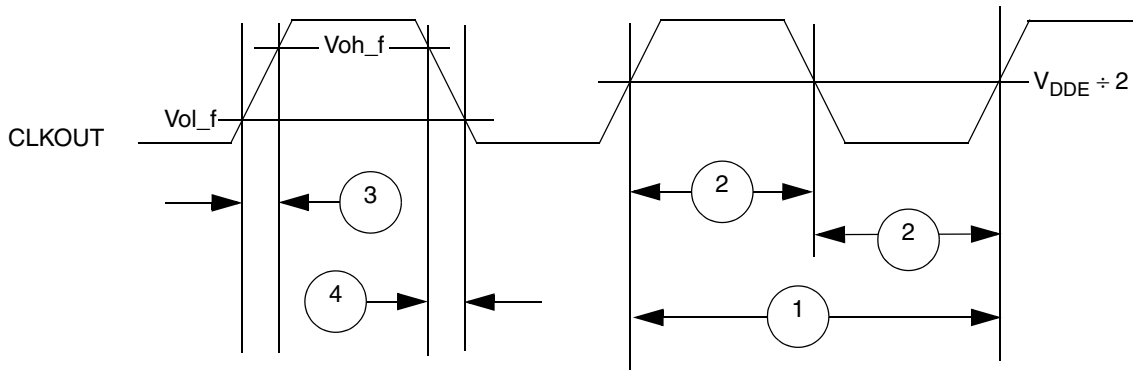


Figure 12. CLKOUT Timing

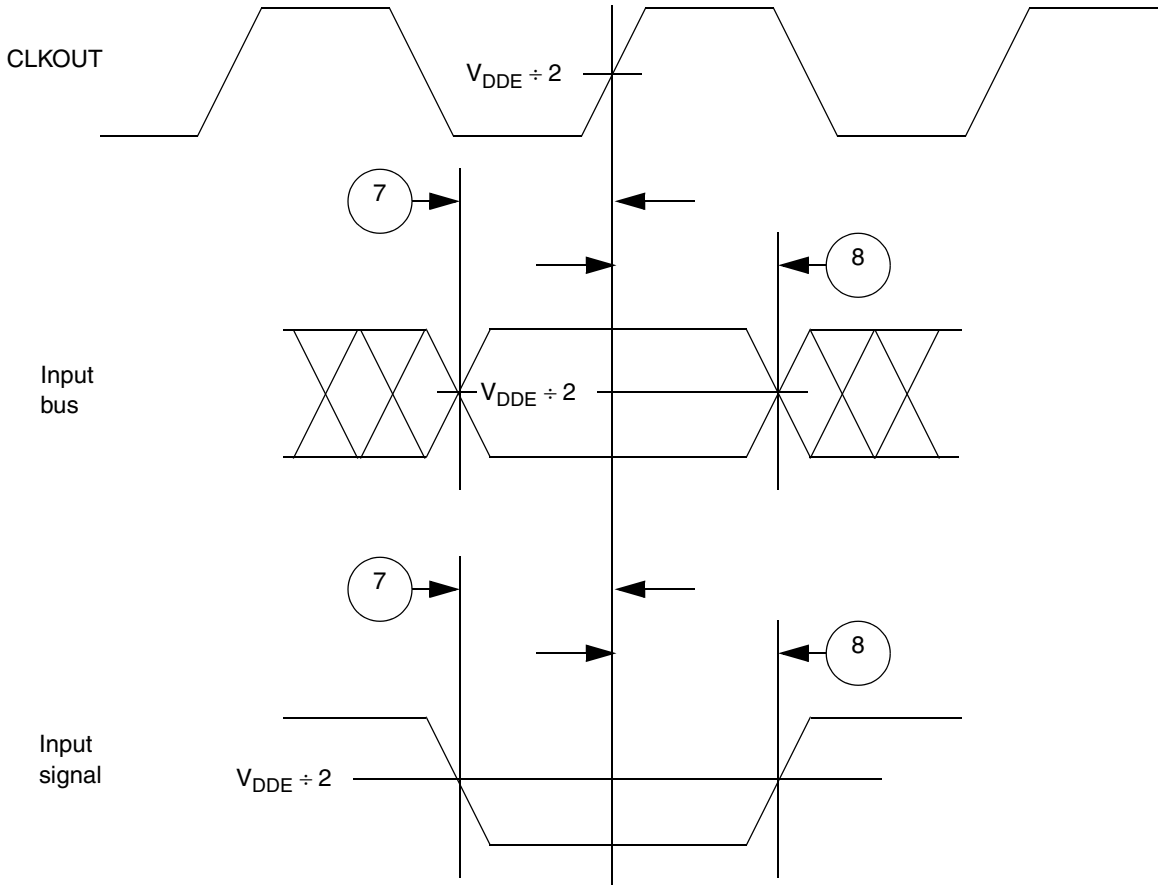


Figure 14. Synchronous Input Timing

3.13.5 External Interrupt Timing (IRQ Signals)

Table 23. External Interrupt Timing [1]

Spec	Characteristic	Symbol	Min.	Max.	Unit
1	IRQ pulse-width low	t_{IPWL}	3	—	t_{CYC}
2	IRQ pulse-width high	T_{IPWH}	3	—	t_{CYC}
3	IRQ edge-to-edge time [2]	t_{ICYC}	6	—	t_{CYC}

[1] IRQ timing specified at: V_{DDEH} = 3.0–5.25 V and $T_A = T_L$ to T_H.

[2] Applies when IRQ signals are configured for rising-edge or falling-edge events, but not both.

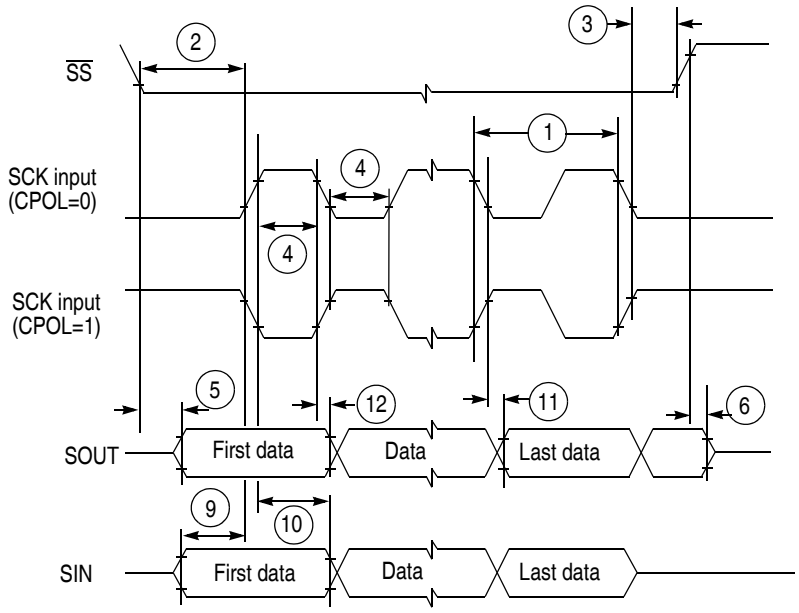


Figure 20. DSPI Classic SPI Timing—Slave, CPHA = 0

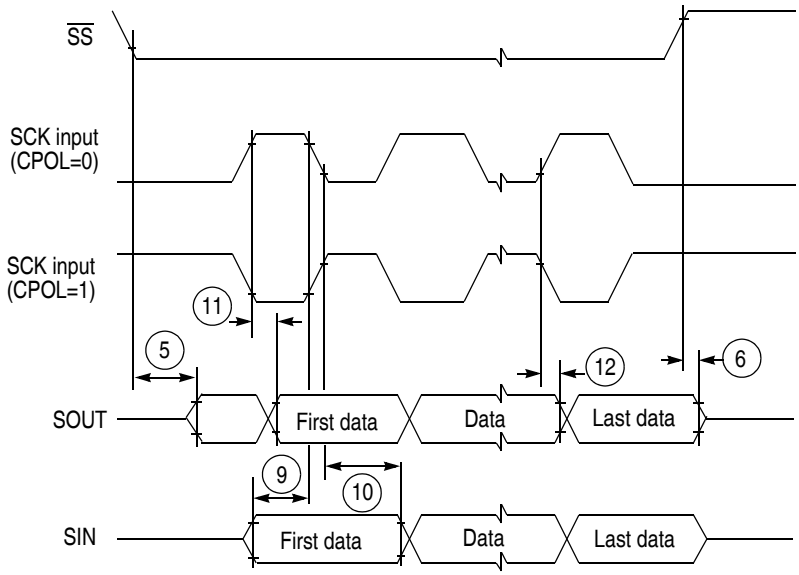


Figure 21. DSPI Classic SPI Timing—Slave, CPHA = 1

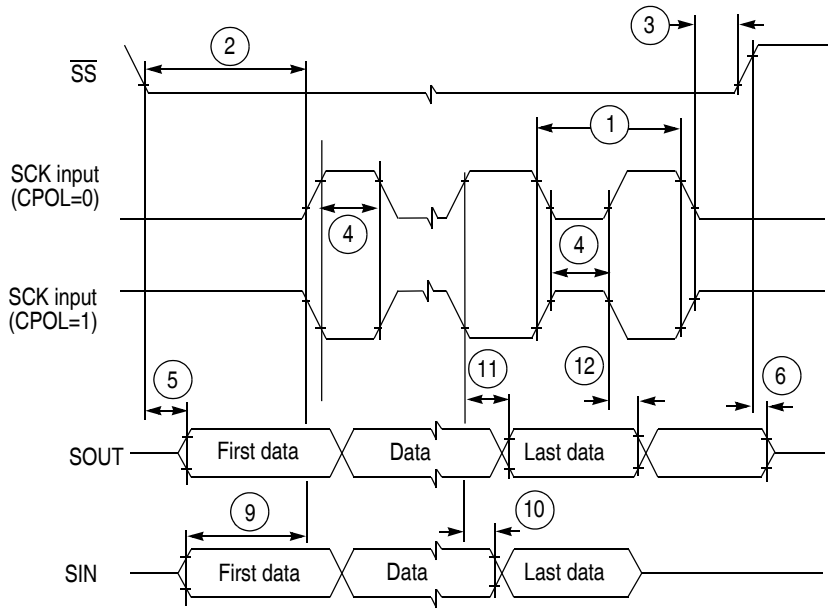


Figure 24. DSPI Modified Transfer Format Timing—Slave, CPHA = 0

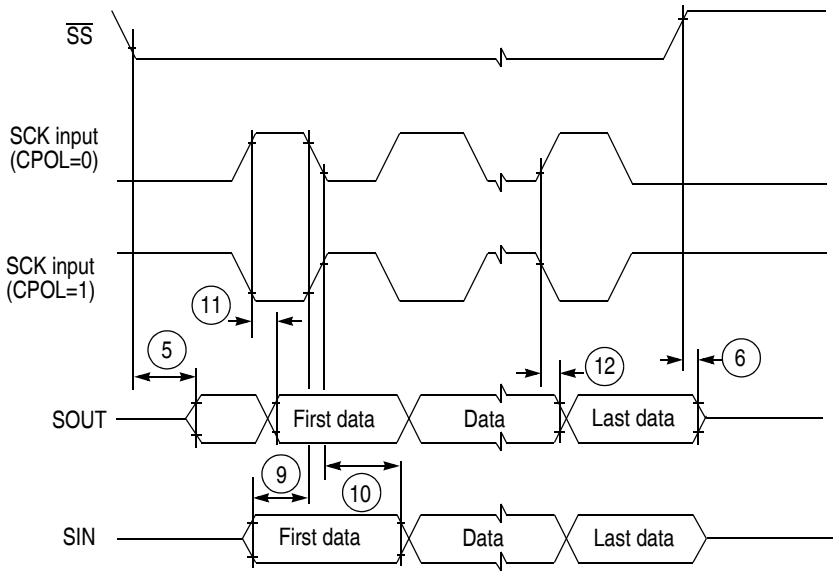


Figure 25. DSPI Modified Transfer Format Timing—Slave, CPHA = 1

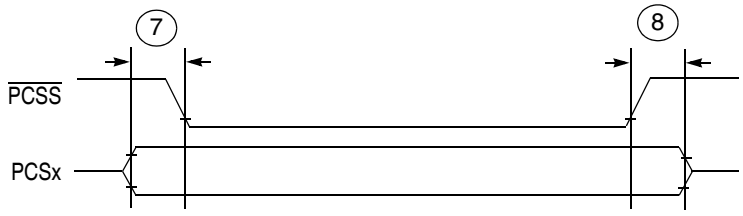
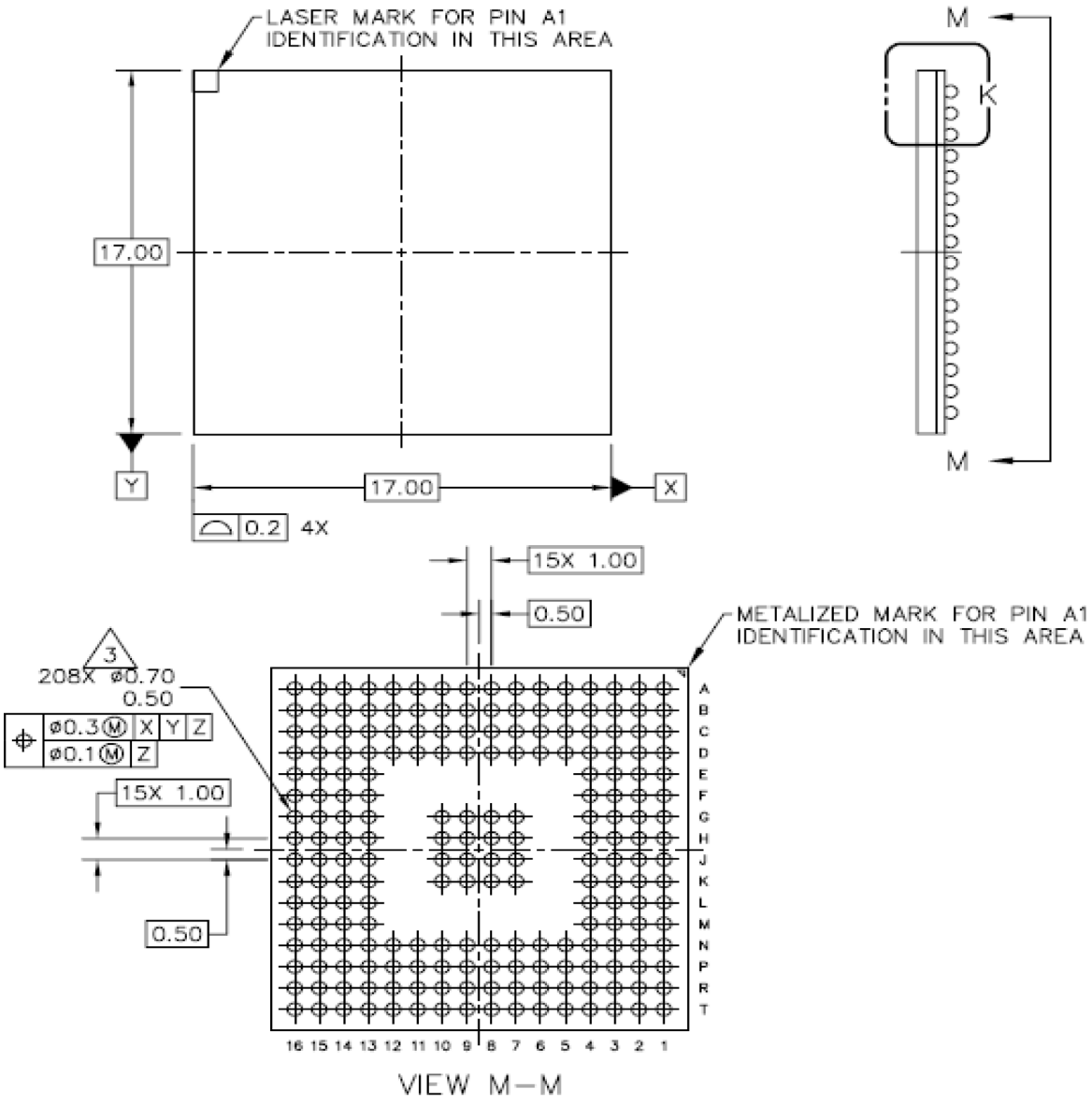


Figure 26. DSPI PCS Strobe (PCSS) Timing

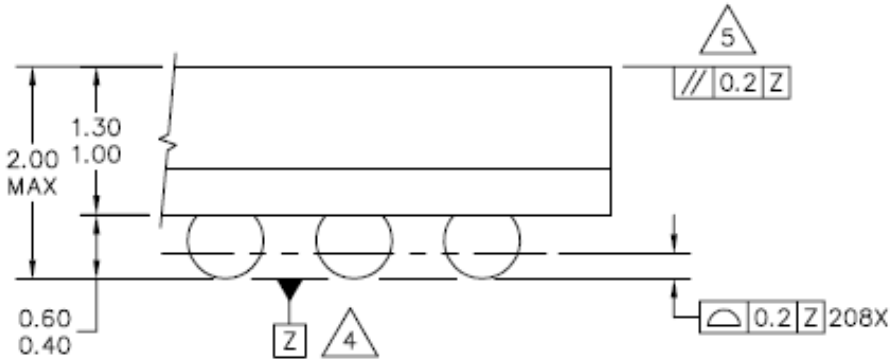
4.3 MPC5534 208-Pin Package Dimensions

The package drawings of the MPC5534 208-pin MAP BGA are shown in Figure 30.



© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: 208 I/O MAP BGA, 17 X 17 PKG, 1–MM PITCH	DOCUMENT NO: 98ARS23882W	REV: D
	CASE NUMBER: 1159A–01	02 AUG 2005
	STANDARD: JEDEC MO–151 AAF–1	

Figure 30. MPC5534 208-Pin Package



DETAIL K
(ROTATED 90° CLOCKWISE)

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO DATUM PLANE Z.
4. DATUM Z (SEATING PLANE) IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: 208 I/O MAP BGA, 17 X 17 PKG, 1–MM PITCH	DOCUMENT NO: 98ARS23882W	REV: D
	CASE NUMBER: 1159A–01	02 AUG 2005
	STANDARD: JEDEC MO–151 AAF–1	

Figure 30. MPC5534 208 MAP BGA Package (continued)

NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.
4. DATUM A, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE	
TITLE: PBGA, 324 I/O, 23 X 23 PKG, 1 MM PITCH (OMPAC)	DOCUMENT NO: 98ASS23840W	REV: D
	CASE NUMBER: 1158–03	26 APR 2006
	STANDARD: JEDEC MS–034 AAJ–1	

Figure 31. MPC5534 324 TEPBGA Package (continued)

5 Revision History for the MPC5534 Data Sheet

The history of revisions made to this data sheet are described in this section. The changes are divided into each revision of this document.

The substantive changes incorporated in MPC5534 Data Sheet revision 4.0 to produce revision 5.0 are:

- Text changes
- Table and figure changes

Within each group, the changes are listed in sequential page number order.

5.1 Changes Between Revisions 5.0 and 6.0

Location	Description of Changes
Section 3.7, "Power-Up/Down Sequencing	Added the following paragraph in Section 3.7, "Power-Up/Down Sequencing. During initial power ramp-up, when vstby is 0.6v or above. a typical current of 1-3mA and maximum of 4mA may be seen until VDD is applied. This current will not reoccur until Vstby is lowered below Vstby min specification.
	Moved Figure 2"ISTBY Worst-case Specifications" to Section 3.7, "Power-Up/Down Sequencing

5.2 Changes Between Revisions 4.0 and 5.0

The following table lists the substantive text changes made to paragraphs.

Table 28. Text Changes Between Rev. 4.0 and 5.0

Location	Description of Changes
Title page:	
	Changed the Revision number from 4.0 to 5.0. Changed the date format to DD MMM YYYY. Made the same changes in the lower left corner of the back page.
Section 3.2.1, "General Notes for Specifications at Maximum Junction Temperature	
	Updated the address of Semiconductor Equipment and Materials International 3081 Zanker Rd. San Jose, CA., 95134 (408) 943-6900
Table 16 on page 24	
	Added footnote 9: For frequencies up to and including 80 MHz, if VDD is within ±5% of 1.5 V, then APC = RWSC = 0b010 is a valid setting.
4 Mechanicals:	
	Added the following NOTE before the 208 and 324 BGA Maps: NOTE The MPC5500 devices are pin compatible for software portability and use the primary function names to label the pins in the BGA diagram. Although some devices do not support all the primary functions shown in the BGA diagram, the muxed and GPIO signals on those pins remain available. See the signals chapter in the device reference manual for the signal muxing.

The following table describes the changes made to information in tables and figures, and is presented in sequential page number order.

Table 30. Table and Figure Changes Between Rev. 3.0 and 4.0

Location	Description of Changes
Figure 1, MPC5500 Family Part Numbers:	
	• Removed the 2 in the tape and reel designator in both the graphic and in the Tape and Reel Status text. • Changed Qualification Status by adding ', general market flow' to the M designator, and added an 'S' designator with the description of 'Fully spec. qualified, automotive flow.
Table 1, Orderable Part Numbers:	
	• Footnote 1 added that reads: All devices are PPC5534, rather than MPC5534 or SPC5534, until product qualifications are complete. Not all configurations are available in the PPC parts. • Reordered rows to group devices by lead-free package types in descending frequency order, and leaded package types. • Footnote 2 added that reads:' The lowest ambient operating temperature is referenced by T_L; the highest ambient operating temperature is referenced by T_H.' • Footnote 3 added that reads: 'Speed is the nominal maximum frequency. Max speed is the maximum speed allowed including frequency modulation (FM). 42 MHz parts allow for 40 MHz system clock + 2% FM; 68 MHz parts allow for 66 MHz system clock + 2% FM, and 82 MHz parts allow for 80 MHz system clock + 2% FM.'
Table 2, Absolute Maximum Ratings:	
	• Deleted Spec 3, "Flash core voltage." • Spec 12 "DC Input Voltage": Deleted from second line'. . .except for eTPUB[15] and SINB (DSPI_B_SIN)' leaving V_{DDEH} powered I/O pads. Deleted third line 'V_{DDEH} powered by I/O pads (eTPUB[15] and SINB), including the min. and max values of -0.3 and 6.5 respectively, and deleted old footnote 7. • Spec 12 "DC Input Voltage": Added footnote 8 to second line "V_{DDE} powered I/O pads" that reads: 'Internal structures hold the input voltage less than the maximum voltage on all pads powered by the V_{DDE} supplies, if the maximum injection current specification is met (s mA for all pins) and V_{DDE} is within the operating voltage specifications. • Spec 14, column 2, changed: 'V_{SS} differential voltage' to 'V_{SS} to V_{SSA} differential voltage.' • Spec 15, column 2, changed: 'V_{DD} differential voltage' to 'V_{DD} to V_{DDA} differential voltage.' • Spec 21, Added the name of the spec, '*V_{RC33} to V_{DDSYN} differential voltage,'* as well as the name and cross reference to Table 9, *DC Electrical Specifications*, to which the Spec was moved. • Spec 28 "Maximum Solder Temperature": Added two lines: Lead free (PbFree) and Leaded (SnPb) with maximum values of 260 C and 245 C respectively. • Footnote 1, added: 'any of' between 'beyond' and 'the listed maxima.' • Deleted footnote 2: 'Absolute maximum voltages are currently maximum burn-in voltages. Absolute maximum specifications for device stress have not yet been determined.'Spec 26 "Maximum Operating Temperature Range": replaced -40 C with. • Footnote 6 (now footnote 5): Changed the end of the last sentence as follows; "Internal structures hold the input voltage greater than -1.0 V if the injection current limit of 2 mA is met. Keep the negative DC voltage greater than -0.6 V on eTPU[15] and on SINB during the internal power-on reset (POR) state."
Table 3, MPC5534 Thermal Characteristics:	
	Changed for production purposes, footnote 1 from: Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other *components on the board*, and board thermal resistance. to: Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other *board components*, and board thermal resistance.

Table 30. Table and Figure Changes Between Rev. 3.0 and 4.0 (continued)

Location	Description of Changes
Table 12, FMPLL Electrical Characteristics:	• Spec 1, footnote 1 in column 2: *'PLL reference frequency range*': Added that reads 'Nominal crystal and external reference values are worst-case not more than 1%. The device operates correctly if the frequency remains within ± 5% of the specification limit. This tolerance range allows for a slight frequency drift of the crystals over time. The designer must thoroughly understand the drift margin of the source clock.' • Spec 1, footnote 2 in column 1: Changed to: 'The 8–20 MHz crystal or external reference values have PLLCFG[2] pulled low' and applies to spec 1, column 2, crystal reference and external reference. • Spec 21, column 2: Changed $f_{ref\_crystal}$ to f_{ref} in ICO frequency equation, and added the same equation but substituted f_{ref_ext} for f_{ref} for the external reference clock, giving: $f_{ico} = [f_{ref\_crystal} \times (MFD + 4)] \div (PREDIV + 1)$ $f_{ico} = [f_{ref\_ext} \times (MFD + 4)] \div (PREDIV + 1)$ • Spec 21: Changed column 5 from 'f_{SYS}' MHz' to: 'f_{MAX}'. • Spec 22: Changed column 4, *Max Value* from f_{MAX} to 20, and added footnote 17 to read, 'Maximum value for dual controller (1:1) mode is ($f_{MAX} \div 2$) and the predivider set to 1 (FMPLL_SYNCR[PREDIV] = 0b001).'
Table 13, eQADC Conversion Specifications: Changed '(Operating)' to '($T_A = T_L - T_H$)' to the table title.	
Table 14, Flash Program and Erase Specifications*:*	• Added ($T_A = T_L - T_H$) to the table title. • Spec 8, 128 KB block pre-program and erase time, Max column value from 15,000 to 7,500. • Moved footnote 1 from the table title to directly after the 'Typical' in the column 5 header. • Footnote 2: Changed from: 'Initial factory condition: ≤ 100 program/erase cycles, 25 ^oC, typical supply voltage, 80 MHz minimum system frequency.' To: 'Initial factory condition: ≤ 100 program/erase cycles, 25 ^oC, using a typical supply voltage measured at a minimum system frequency of 80 MHz.'
Table 15, Flash EEPROM Module Life:	• Replaced (Full Temperature Range) with ($T_A = T_L - T_H$) in the table title. • Spec 1b, Min. column value changed from 10,000 to 1,000.
Table 16, FLash BIU Settings vs. Frequency of Operations:	• 'Added footnote 1 to the end of the table title, The footnote reads: 'Illegal combinations exist. Use entries from the same row in this table.' • Moved footnote 2:' For maximum flash performance, set to 0b11' to the 'DPFEN' column header. • Deleted the x-refs in the 'DPFEN' column for the rows. • Created a x-ref for footnote 2 and inserted in the 'IPFEN' column header. • Deleted the x-refs in the 'IPFEN' column for the rows. • Added to the PFLIM binary values a leading 0 so that 0bxx became 0b0xx. • Moved footnote 3:' For maximum flash performance, set to 0b110' to the 'PFLIM' column header. • Deleted the x-refs in the 'PFLIM' column for the rows. • Moved footnote 4:' For maximum flash performance, set to 0b1' to the 'BFEN' column header. • Deleted the x-refs in the 'BFEN' column for the rows. • Added footnotes 4, 6, 7, and 8: -- footnote 4 27 MHz parts allow for 25 MHz system clock + 2% frequency modulation (FM). -- footnote 5 52 MHz parts allow for 50 MHz system clock + 2% FM. -- footnote 6 77 MHz parts allow for 75 MHz system clock + 2% FM. -- footnote 7 82 MHz parts allow for 80 MHz system clock + 2% FM.