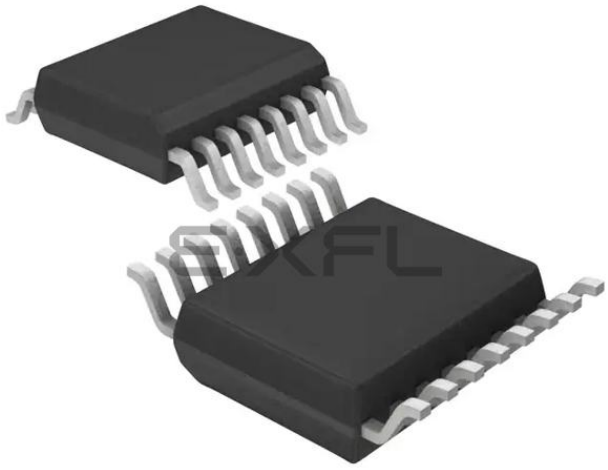
Renesas Electronics America Inc - R5F1054AASP#30 Datasheet



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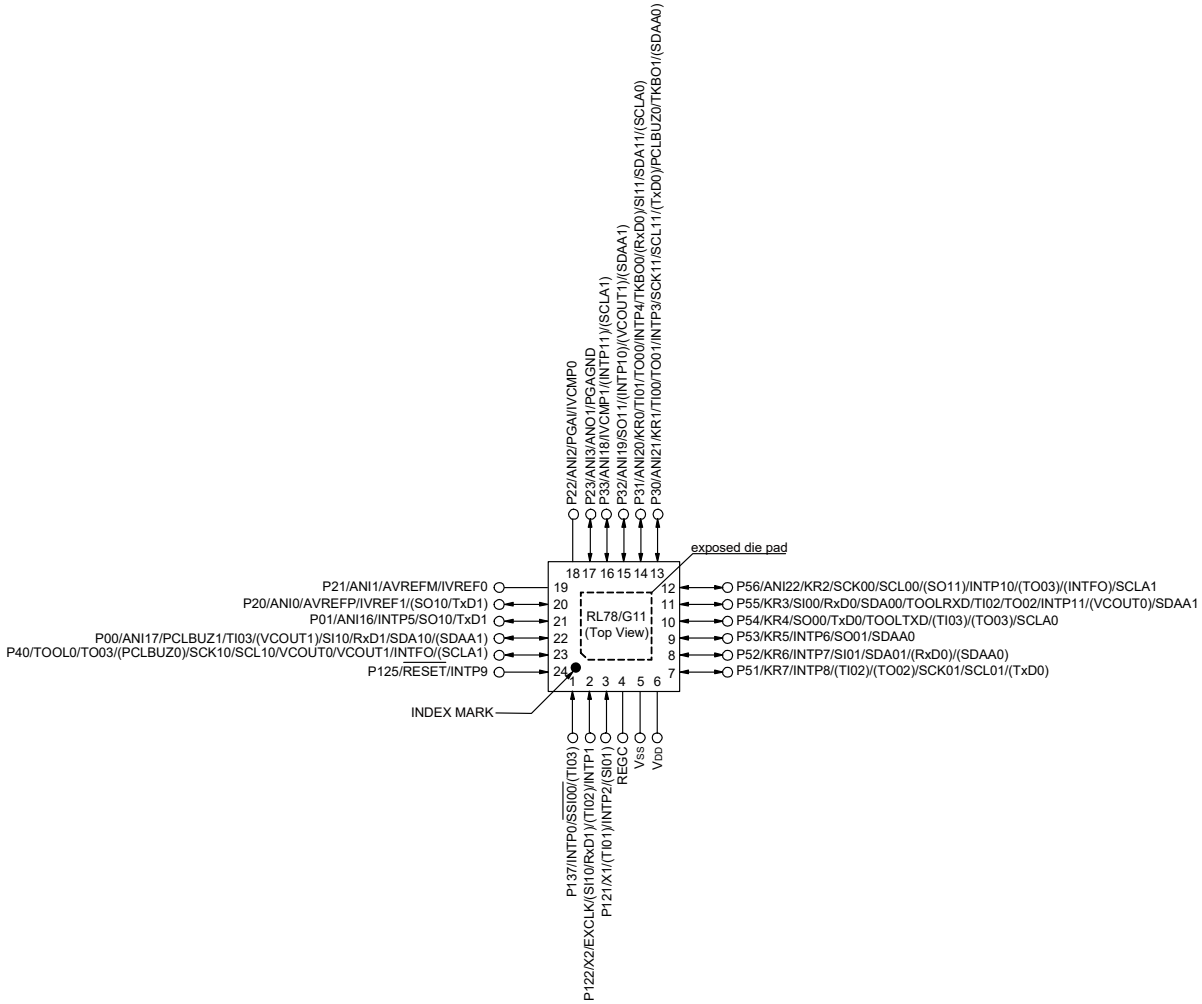
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	RL78
Core Size	16-Bit
Speed	24MHz
Connectivity	CSI, I²C, UART/USART
Peripherals	LVD, POR, WDT
Number of I/O	13
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	1.5K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 8x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	16-SSOP (0.173", 4.40mm Width)
Supplier Device Package	16-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f1054aasp-30

1.3.4 24-pin products

<R> • 24-pin plastic HWQFN (4 × 4 mm, 0.5 mm pitch)



Caution Connect the REGC pin to Vss pin via a capacitor (0.47 to 1 μF).

Remark 1. For pin identification, see **1.4 Pin Identification**.

Remark 2. It is recommended to connect an exposed die pad to Vss.

Remark 3. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0 to 3 (PIOR0 to PIOR3).

2.2 Oscillator Characteristics

2.2.1 X1 characteristics

(T_A = -40 to +85°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Resonator	Resonator	Conditions	MIN.	TYP.	MAX.	Unit
X1 clock oscillation frequency (f_X) Note	Ceramic resonator/ crystal resonator	2.7 V ≤ V_{DD} ≤ 5.5 V	1.0		20.0	MHz
		2.4 V ≤ V_{DD} < 2.7 V	1.0		16.0	
		1.8 V ≤ V_{DD} < 2.4 V	1.0		8.0	
		1.6 V ≤ V_{DD} < 1.8 V	1.0		4.0	

Note Indicates only permissible oscillator frequency ranges. Refer to **2.4 AC Characteristics** for instruction execution time. Request evaluation by the manufacturer of the oscillator circuit mounted on a board to check the oscillator characteristics.

Caution **Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.**

Remark When using the X1 oscillator, refer to **6.4 System Clock Oscillator** in the RL78/G11 User's Manual.

2.2.2 On-chip oscillator characteristics

(T_A = -40 to +85°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Oscillators	Parameters	Conditions		MIN.	TYP.	MAX.	Unit
High-speed on-chip oscillator clock frequency Notes 1, 2	f_{IH}	2.7 V ≤ V_{DD} ≤ 5.5 V		1		24	MHz
		2.4 V ≤ V_{DD} ≤ 5.5 V		1		16	
		1.8 V ≤ V_{DD} ≤ 5.5 V		1		8	
		1.6 V ≤ V_{DD} ≤ 5.5 V		1		4	
High-speed on-chip oscillator clock frequency accuracy		T_A = -20 to +85°C	1.8 V ≤ V_{DD} ≤ 5.5 V	-1		1	%
			1.6 V ≤ V_{DD} < 1.8 V	-5		5	
		T_A = -40 to -20°C	1.8 V ≤ V_{DD} ≤ 5.5 V	-1.5		1.5	%
			1.6 V ≤ V_{DD} < 1.8 V	-5.5		5.5	
Middle-speed on-chip oscillator oscillation frequency Note 2	f_{IM}			1		4	MHz
Middle-speed on-chip oscillator oscillation frequency accuracy				-12		+12	%
<R> Temperature drift of Middle-speed on-chip oscillator oscillation frequency accuracy	D_{IMT}				0.008		%/°C
<R> Voltage drift of Middle-speed on-chip oscillator oscillation frequency accuracy	D_{IMV}	T_A = 25°C	2.1 V ≤ V_{DD} ≤ 5.5 V		0.02		%/V
			2.0 V ≤ V_{DD} < 2.1 V		-12		
			1.6 V ≤ V_{DD} < 2.0 V		10		
Low-speed on-chip oscillator clock frequency Note 2	f_{IL}				15		kHz
Low-speed on-chip oscillator clock frequency accuracy				-15		+15	%

Note 1. High-speed on-chip oscillator frequency is selected with bits 0 to 3 of the option byte (000C2H) and bits 0 to 2 of the HOCODIV register.

Note 2. This only indicates the oscillator characteristics. Refer to **2.4 AC Characteristics** for instruction execution time.

(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) **(3/5)**

<R>

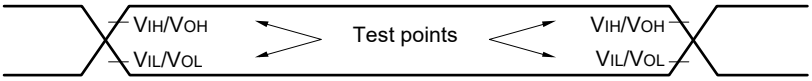
Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH1}	P00, P01, P30 to P33, P40, and P51 to P56	Normal mode	0.8 EV_{DD}		EV_{DD}	V
	V_{IH2}	P00, P30 to P32, P40, P51 to P56	TTL mode 4.0 V ≤ EV_{DD} ≤ 5.5 V	2.2		EV_{DD}	V
			TTL mode 3.3 V ≤ EV_{DD} < 4.0 V	2.0		EV_{DD}	V
			TTL mode 1.6 V ≤ EV_{DD} < 3.3 V	1.5		EV_{DD}	V
	V_{IH3}	P20 to P23 (digital input)		0.7 V_{DD}		V_{DD}	V
	V_{IH4}	P121, P122, P125, P137, EXCLK, $\overline{RESET}$		0.8 V_{DD}		V_{DD}	V
Input voltage, low	V_{IL1}	P00, P01, P30 to P33, P40, and P51 to P56	Normal mode	0		0.2 EV_{DD}	V
	V_{IL2}	P00, P30 to P32, P40, P51 to P56	TTL mode 4.0 V ≤ EV_{DD} ≤ 5.5 V	0		0.8	V
			TTL mode 3.3 V ≤ EV_{DD} < 4.0 V	0		0.5	V
			TTL mode 1.6 V ≤ EV_{DD} < 3.3 V	0		0.32	V
	V_{IH3}	P20 to P23 (digital input)		0		0.3 V_{DD}	V
	V_{IH4}	P121, P122, P125, P137, EXCLK, $\overline{RESET}$		0		0.2 V_{DD}	V

Caution The maximum value of V_{IH} of pins P00, P01, P20, P30 to P33, P40 and P51 to P56 is V_{DD} or EV_{DD}, even in the N-ch open-drain mode.
(P20: V_{DD}
P00, P01, P30 to P33, P40, P51 to P56: EV_{DD})

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

2.5 Peripheral Functions Characteristics

AC Timing Test Points



(5) During communication at same potential (simplified I²C mode)

(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LP (Low-power main) mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLr clock frequency	f_{SCL}	2.7 V ≤ EV_{DD} ≤ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ		1000 Note 1		400 Note 1		250 Note 1		400 Note 1	kHz
		1.8 V ≤ EV_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ		400 Note 1							
		1.8 V ≤ EV_{DD} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ		300 Note 1		300 Note 1		250 Note 1		300 Note 1	
		1.7 V ≤ EV_{DD} < 1.8 V, C_b = 100 pF, R_b = 5 kΩ		250 Note 1		250 Note 1		250 Note 1		250 Note 1	
		1.6 V ≤ EV_{DD} < 1.8 V, C_b = 100 pF, R_b = 5 kΩ		—							
Hold time when SCLr = "L"	t_{LOW}	2.7 V ≤ EV_{DD} ≤ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ	475		1150		1150		1150		ns
		1.8 V ≤ EV_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	1150								
		1.8 V ≤ EV_{DD} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ	1550		1550		1550		1550		
		1.7 V ≤ EV_{DD} < 1.8 V, C_b = 100 pF, R_b = 5 kΩ	1850		1850		1850		1850		
		1.6 V ≤ EV_{DD} < 1.8 V, C_b = 100 pF, R_b = 5 kΩ	—								
Hold time when SCLr = "H"	t_{HIGH}	2.7 V ≤ EV_{DD} ≤ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ	475		1150		1150		1150		ns
		1.8 V ≤ EV_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	1150								
		1.8 V ≤ EV_{DD} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ	1550		1550		1550		1550		
		1.7 V ≤ EV_{DD} < 1.8 V, C_b = 100 pF, R_b = 5 kΩ	1850		1850		1850		1850		
		1.6 V ≤ EV_{DD} < 1.8 V, C_b = 100 pF, R_b = 5 kΩ	—								
Data setup time (reception)	$t_{SU:DAT}$	2.7 V ≤ EV_{DD} ≤ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ	1/f_{MCK} + 85 Note 2		1/f_{MCK} + 145 Note 2		1/f_{MCK} + 145 Note 2		1/f_{MCK} + 145 Note 2		ns
		1.8 V ≤ EV_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	1/f_{MCK} + 145 Note 2								
		1.8 V ≤ EV_{DD} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ	1/f_{MCK} + 230 Note 2		1/f_{MCK} + 230 Note 2		1/f_{MCK} + 230 Note 2		1/f_{MCK} + 230 Note 2		
		1.7 V ≤ EV_{DD} < 1.8 V, C_b = 100 pF, R_b = 5 kΩ	1/f_{MCK} + 290 Note 2		1/f_{MCK} + 290 Note 2		1/f_{MCK} + 290 Note 2		1/f_{MCK} + 290 Note 2		
		1.6 V ≤ EV_{DD} < 1.8 V, C_b = 100 pF, R_b = 5 kΩ	—		—		—				
Data hold time (transmission)	$t_{HD:DAT}$	2.7 V ≤ EV_{DD} ≤ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ	0	305	0	305	0	305	0	305	ns
		1.8 V ≤ EV_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ		355		355		355		355	
		1.8 V ≤ EV_{DD} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ		405		405		405		405	
		1.7 V ≤ EV_{DD} < 1.8 V, C_b = 100 pF, R_b = 5 kΩ									
		1.6 V ≤ EV_{DD} < 1.8 V, C_b = 100 pF, R_b = 5 kΩ	—	—							

Note 6. The smaller maximum transfer rate derived by using f_{MCK}/6 or the following expression is the valid maximum transfer rate.
Expression for calculating the transfer rate when 1.8 V ≤ EV_{DD} < 3.3 V and 1.6 V ≤ V_b ≤ 2.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides

Note 7. This value as an example is calculated when the conditions described in the “Conditions” column are met.
Refer to Note 6 above to calculate the maximum transfer rate under conditions of the customer.

Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (EV_{DD} tolerance) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

Note 1. Transfer rate in the SNOOZE mode: MAX. 1 Mbps

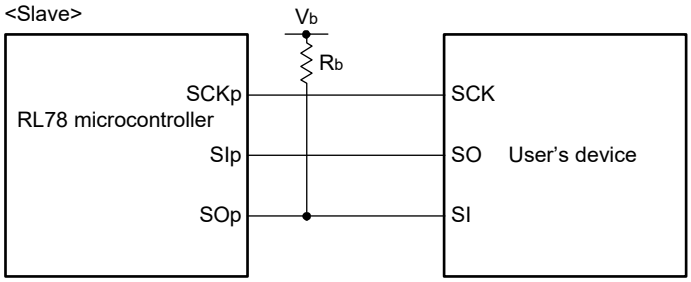
Note 2. Use it with $EV_{DD} \geq V_b$.

Note 3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 4. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Caution Select the TTL input buffer for the SIp pin and SCKp pin and the N-ch open drain output (EV_{DD} tolerance) mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

CSI mode connection diagram (during communication at different potential)



Remark 1. R_b[Ω]: Communication line (SOp) pull-up resistance, C_b[F]: Communication line (SOp) load capacitance, V_b[V]: Communication line voltage

Remark 2. p: CSI number (p = 00 to 03), m: Unit number (m = 0), n: Channel number (n = 0 to 3), g: PIM and POM numbers (g = 0, 2, 3 to 5 and 12)

Remark 3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03))

Remark The maximum value of C_b (communication line capacitance) and the value of R_b (communication line pull-up resistor) at that time in each mode are as follows.

Standard mode: C_b = 400 pF, R_b = 2.7 kΩ

2.6.2 Temperature sensor characteristics/internal reference voltage characteristic

(T_A = -40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Temperature sensor output voltage	V_{TMPS25}	Setting ADS register = 80H, T_A = +25°C		1.05		V
Internal reference voltage	V_{BGR}	Setting ADS register = 81H	1.38	1.45	1.5	V
Temperature coefficient	F_{VTMPS}	Temperature sensor that depends on the temperature		-3.6		mV/°C
Operation stabilization wait time	t_{AMP}	2.4 V ≤ V_{DD} ≤ 5.5 V	5			μs
		1.8 V ≤ V_{DD} < 2.4 V	10			μs

2.6.3 D/A converter characteristics

(T_A = -40 to +85°C, 1.6 V ≤ EV_{SS} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES					8	bit
Overall error	AINL	Rload = 4 MΩ	1.8 V ≤ V_{DD} ≤ 5.5 V			±2.5	LSB
		Rload = 8 MΩ	1.8 V ≤ V_{DD} ≤ 5.5 V			±2.5	LSB
Settling time	t_{SET}	Cload = 20 pF	2.7 V ≤ V_{DD} ≤ 5.5 V			3	μs
			1.6 V ≤ V_{DD} < 2.7 V			6	μs

2.6.7 LVD circuit characteristics

(1) LVD Detection Voltage of Reset Mode and Interrupt Mode

(T_A = -40 to +85°C, $V_{PDR} \leq EV_{DD} \leq V_{DD} \leq$ 5.5 V, V_{SS} = 0 V)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	Supply voltage level	V_{LVD0}	Power supply rise time	3.98	4.06	4.14	V
			Power supply fall time	3.90	3.98	4.06	V
		V_{LVD1}	Power supply rise time	3.68	3.75	3.82	V
			Power supply fall time	3.60	3.67	3.74	V
		V_{LVD2}	Power supply rise time	3.07	3.13	3.19	V
			Power supply fall time	3.00	3.06	3.12	V
		V_{LVD3}	Power supply rise time	2.96	3.02	3.08	V
			Power supply fall time	2.90	2.96	3.02	V
		V_{LVD4}	Power supply rise time	2.86	2.92	2.97	V
			Power supply fall time	2.80	2.86	2.91	V
		V_{LVD5}	Power supply rise time	2.76	2.81	2.87	V
			Power supply fall time	2.70	2.75	2.81	V
		V_{LVD6}	Power supply rise time	2.66	2.71	2.76	V
			Power supply fall time	2.60	2.65	2.70	V
		V_{LVD7}	Power supply rise time	2.56	2.61	2.66	V
			Power supply fall time	2.50	2.55	2.60	V
		V_{LVD8}	Power supply rise time	2.45	2.50	2.55	V
			Power supply fall time	2.40	2.45	2.50	V
		V_{LVD9}	Power supply rise time	2.05	2.09	2.13	V
			Power supply fall time	2.00	2.04	2.08	V
		V_{LVD10}	Power supply rise time	1.94	1.98	2.02	V
			Power supply fall time	1.90	1.94	1.98	V
		V_{LVD11}	Power supply rise time	1.84	1.88	1.91	V
			Power supply fall time	1.80	1.84	1.87	V
		V_{LVD12}	Power supply rise time	1.74	1.77	1.81	V
			Power supply fall time	1.70	1.73	1.77	V
		V_{LVD13}	Power supply rise time	1.64	1.67	1.70	V
			Power supply fall time	1.60	1.63	1.66	V
Minimum pulse width		t_{LW}		300			µs
Detection delay time						300	µs

3.3 DC Characteristics

3.3.1 Pin characteristics

(T_A = -40 to +105°C, 2.4 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = 0 V) **(1/5)**

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
<R> Output current, high Note 1	I_{OH1}	Per pin for P00, P01, P30 to P33, P40, and P51 to P56				-3.0 Note 2	mA
		Total of P00, P01, and P40 (When duty ≤ 70% Note 3)	4.0 V ≤ EV_{DD} ≤ 5.5 V			-12.5	mA
			2.7 V ≤ EV_{DD} < 4.0 V			-10.0	mA
			2.4 V ≤ EV_{DD} < 2.7 V			-5.0	mA
		Total of P30 to P33, and P51 to P56 (When duty ≤ 70% Note 3)	4.0 V ≤ EV_{DD} ≤ 5.5 V			-30.0	mA
			2.7 V ≤ EV_{DD} < 4.0 V			-19.0	mA
			2.4 V ≤ EV_{DD} < 2.7 V			-10.0	mA
		Total of all pins (When duty ≤ 70% Note 3)				-42.5	mA
	I_{OH2}	Per pin for P20 to P23				-0.1 Note 2	mA
		Total of all pins (When duty ≤ 70% Note 3)	2.4 V ≤ V_{DD} ≤ 5.5 V			-0.4	mA

Note 1. Value of current at which the device operation is guaranteed even if the current flows from the V_{DD} pin to an output pin.

Note 2. Do not exceed the total current value.

Note 3. Specification under conditions where the duty factor ≤ 70%.
The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = (I_{OH} × 0.7)/(n × 0.01)
  <Example> Where n = 80% and I_{OH} = -10.0 mA
  Total output current of pins = (-10.0 × 0.7)/(80 × 0.01) ≈ -8.7 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor.
A current higher than the absolute maximum rating must not flow into one pin.

Caution **P00, P01, P20, P30 to P33, P40 and P51 to P56 do not output high level in N-ch open-drain mode.**

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

3.3.2 Supply current characteristics

(T_A = -40 to +105°C, 2.4 V ≤ EV_{DD} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) **(1/3)**

Parameter	Symbol	Conditions					MIN.	TYP.	MAX.	Unit
Supply current Note 1	I_{DD1}	Operating mode	Basic operation	HS (high-speed main) mode	f_{HOCO} = 48 MHz Note 3, f_{IH} = 24 MHz Note 3	V_{DD} = 5.0 V			1.7		mA
						V_{DD} = 3.0 V			1.7		
					f_{HOCO} = 24 MHz Note 3, f_{IH} = 24 MHz Note 3	V_{DD} = 5.0 V			1.4		
						V_{DD} = 3.0 V			1.4		
			Normal operation	HS (high-speed main) mode	f_{HOCO} = 48 MHz Note 3, f_{IH} = 24 MHz Note 3	V_{DD} = 5.0 V			3.5	7.3	mA
						V_{DD} = 3.0 V			3.5	7.3	
					f_{HOCO} = 24 MHz Note 3, f_{IH} = 24 MHz Note 3	V_{DD} = 5.0 V			3.2	6.7	
						V_{DD} = 3.0 V			3.2	6.7	
					f_{HOCO} = 16 MHz Note 3, f_{IH} = 16 MHz Note 3	V_{DD} = 5.0 V			2.4	4.9	
						V_{DD} = 3.0 V			2.4	4.9	
			Normal operation	HS (high-speed main) mode	f_{MX} = 20 MHz Note 2	V_{DD} = 5.0 V	Square wave input		2.7	5.7	mA
							Resonator connection		2.8	5.8	
						V_{DD} = 3.0 V	Square wave input		2.7	5.7	
							Resonator connection		2.8	5.8	
					f_{MX} = 10 MHz Note 2	V_{DD} = 5.0 V	Square wave input		1.8	3.4	
							Resonator connection		1.9	3.5	
						V_{DD} = 3.0 V	Square wave input		1.8	3.4	
							Resonator connection		1.9	3.5	
			Normal operation	Subsystem clock operation	f_{IL} = 15 kHz, T_A = -40°C Note 4				1.8	5.9	μA
					f_{IL} = 15 kHz, T_A = +25°C Note 4				1.9	5.9	
					f_{IL} = 15 kHz, T_A = +85°C Note 4				2.3	8.7	
					f_{IL} = 15 kHz, T_A = +105°C Note 4				3.0	20.9	

Note 1. Total current flowing into V_{DD} and EV_{DD}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}. The MAX values include the peripheral operating current. However, these values do not include the current flowing into the A/D converter, comparator, Programmable gain amplifier, LVD circuit, I/O ports, and on-chip pull-up/pull-down resistors, and the current flowing during data flash rewrite.

Note 2. When the high-speed on-chip oscillator clock, middle-speed on-chip oscillator clock and low-speed on-chip oscillator clock are stopped.

Note 3. When the high-speed system clock, middle-speed on-chip oscillator clock and low-speed on-chip oscillator clock are stopped.

Note 4. When the high-speed system clock, high-speed on-chip oscillator clock and middle-speed on-chip oscillator clock are stopped.

Remark 1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

Remark 2. f_{IH}: High-speed on-chip oscillator clock frequency (24 MHz max.)

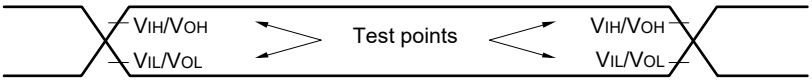
Remark 3. f_{IM}: Middle-speed on-chip oscillator clock frequency (4 MHz max.)

Remark 4. f_{IL}: Low-speed on-chip oscillator clock frequency

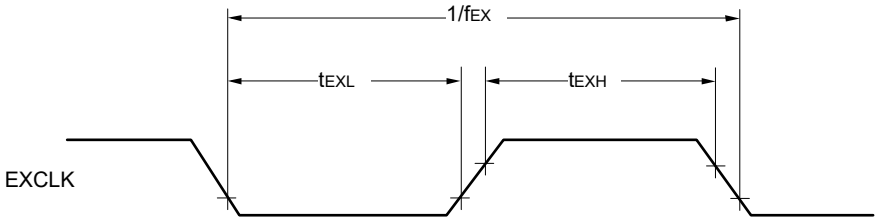
Remark 5. f_{SUB}: Subsystem clock frequency (Low-speed on-chip oscillator clock frequency)

Remark 6. Except subsystem clock operation, temperature condition of the TYP. value is T_A = 25°C

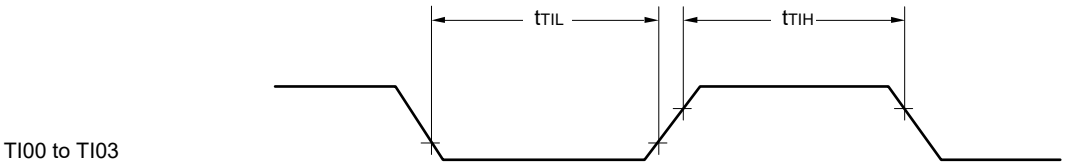
AC Timing Test Points

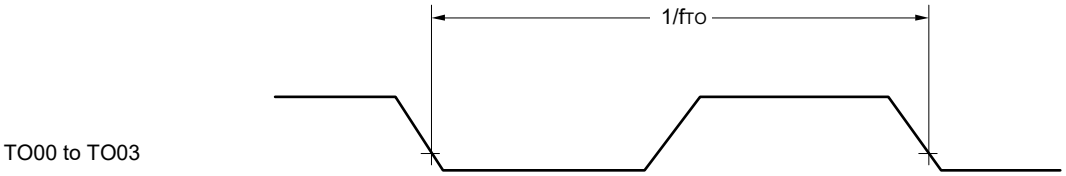


External System Clock Timing



TI/TO Timing





3.5.1 Serial array unit

(1) during communication at same potential (UART mode)

When P01, P30, P31 and P54 are used as TxDq pin

(T_A = -40 to +105°C, 2.4 V ≤ EV_{DD} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
Transfer rate		Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} = 24 MHz		$f_{MCK}/12$ Notes 1, 2	bps
				2.0	Mbps

Note 1. Transfer rate in the SNOOZE mode is 4800 bps only.

Note 2. The maximum operating frequencies of the CPU/peripheral hardware clock (f_{CLK}) are:
HS (high-speed main) mode:
2.4 V ≤ EV_{DD} ≤ 2.7 V: MAX. 1.3 Mbps

Caution Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

When P20 is used as TxD1 pin

(T_A = -40 to +105°C, 2.4 V ≤ EV_{DD} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
Transfer rate		4.0 V ≤ V_{DD} ≤ 5.5 V		$f_{MCK}/16$ Note	bps
		Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} = 24 MHz		1.5	Mbps
		2.7 V ≤ V_{DD} ≤ 5.5 V		$f_{MCK}/20$ Note	bps
		Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} = 24 MHz		1.2	Mbps
		2.4 V ≤ V_{DD} ≤ 5.5 V		$f_{MCK}/16$ Note	bps
		Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} = 16 MHz		1.0	Mbps

<R> **Note** Transfer rate in the SNOOZE mode is 4800 bps only. When f_{HOCO} = 48 MHz, SNOOZE mode is not supported.

Note 6. The smaller maximum transfer rate derived by using f_{MCK}/6 or the following expression is the valid maximum transfer rate.
Expression for calculating the transfer rate when 2.4 V ≤ EV_{DD} < 3.3 V and 1.6 V ≤ V_b ≤ 2.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\} \times 3} \text{ [bps]}$$

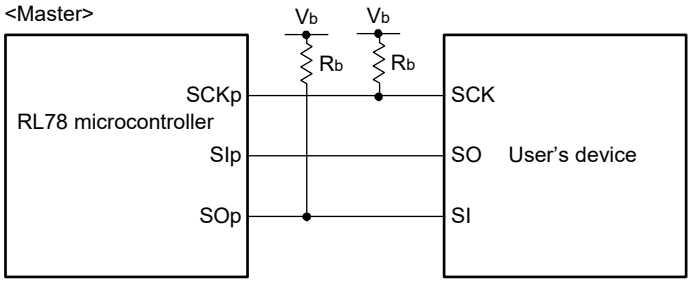
$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides

Note 7. This value as an example is calculated when the conditions described in the “Conditions” column are met.
Refer to Note 6 above to calculate the maximum transfer rate under conditions of the customer.

Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (EV_{DD} tolerance) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

CSI mode connection diagram (during communication at different potential)



Remark 1. R_b[Ω]: Communication line (SCKp, SOp) pull-up resistance, C_b[F]: Communication line (SCKp, SOp) load capacitance, V_b[V]: Communication line voltage

Remark 2. p: CSI number (p = 00, 01, 10 and 11), m: Unit number (m = 0), n: Channel number (n = 0 to 3), g: PIM and POM numbers (g = 0, 2, 3 to 5 and 12)

Remark 3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03))

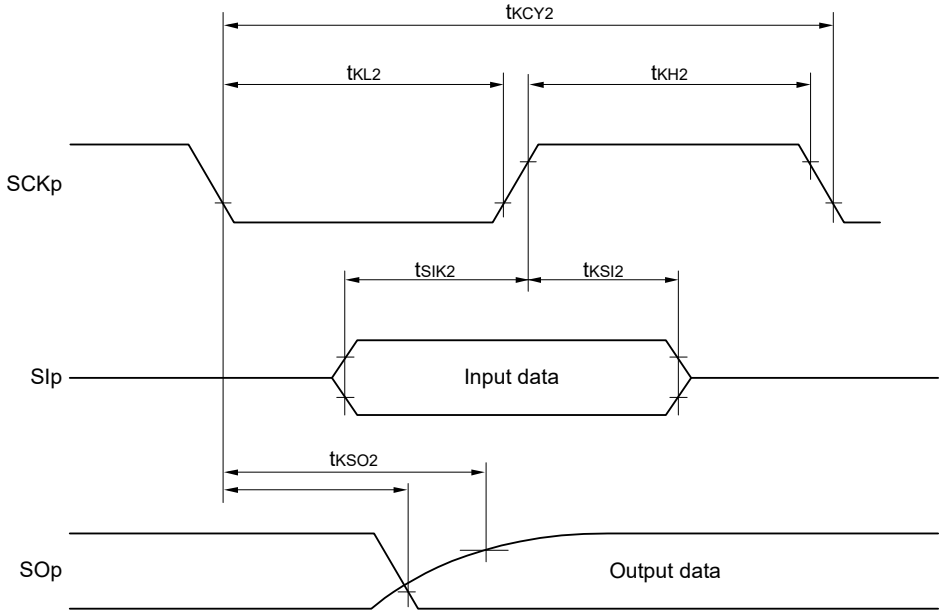
(7) Communication at different potential (1.8 V, 2.5 V, 3.0 V) (CSI mode) (slave mode, SCKp... external clock input)

(T_A = -40 to +105°C, 2.4 V ≤ EV_{DD} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

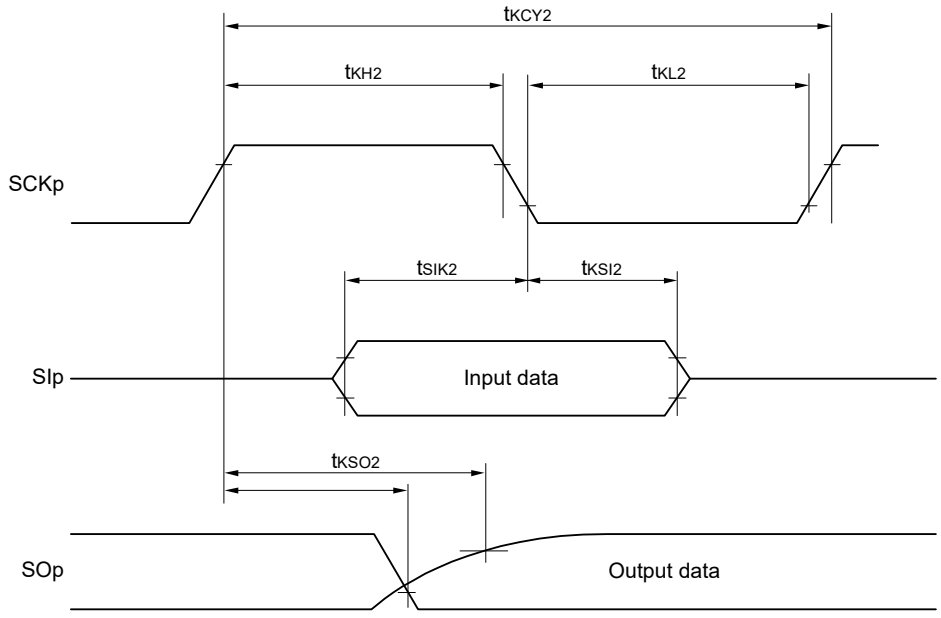
Parameter	Symbol	Conditions		HS (high-speed main) Mode		Unit
				MIN.	MAX.	
SCKp cycle time Note 1	t_{KCY2}	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V	20 MHz < f_{MCK} ≤ 24 MHz	24/f_{MCK}		ns
			8 MHz < f_{MCK} ≤ 20 MHz	20/f_{MCK}		ns
			4 MHz < f_{MCK} ≤ 8 MHz	16/f_{MCK}		ns
			f_{MCK} ≤ 4 MHz	12/f_{MCK}		ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V	20 MHz < f_{MCK} ≤ 24 MHz	32/f_{MCK}		ns
			16 MHz < f_{MCK} ≤ 20 MHz	28/f_{MCK}		ns
			8 MHz < f_{MCK} ≤ 16 MHz	24/f_{MCK}		ns
			4 MHz < f_{MCK} ≤ 8 MHz	16/f_{MCK}		ns
			f_{MCK} ≤ 4 MHz	12/f_{MCK}		ns
		2.4 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2	20 MHz < f_{MCK} ≤ 24 MHz	72/f_{MCK}		ns
			16 MHz < f_{MCK} ≤ 20 MHz	64/f_{MCK}		ns
			8 MHz < f_{MCK} ≤ 16 MHz	52/f_{MCK}		ns
			4 MHz < f_{MCK} ≤ 8 MHz	32/f_{MCK}		ns
			f_{MCK} ≤ 4 MHz	20/f_{MCK}		ns
SCKp high-/low-level width	t_{KH2}, t_{KL2}	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V		t_{KCY2}/2 - 24		ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V		t_{KCY2}/2 - 36		ns
		2.4 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2		t_{KCY2}/2 - 100		ns
SIp setup time (to SCKp↑) Note 3	t_{SIK2}	2.7 V ≤ EV_{DD} ≤ 5.5 V, 2.3 V ≤ V_b ≤ 4.0 V		1/f_{MCK} + 40		ns
		2.4 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2		1/f_{MCK} + 60		ns
SIp hold time (from SCKp↑) Note 4	t_{KSI2}			1/f_{MCK} + 62		ns
Delay time from SCKp↓ to SOp output Note 5	t_{KSO2}	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V C_b = 30 pF, R_b = 1.4 kΩ			2/f_{MCK} + 240	ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V C_b = 30 pF, R_b = 2.7 kΩ			2/f_{MCK} + 428	ns
		2.4 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2 C_b = 30 pF, R_b = 5.5 kΩ			2/f_{MCK} + 1146	ns

(**Notes**, **Caution** and **Remarks** are listed on the next page.)

CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Remark p: CSI number (p = 00, 01, 10 and 11), m: Unit number (m = 0), n: Channel number (n = 0 to 3), g: PIM and POM numbers (g = 0, 2, 3 to 5 and 12)

3.6.7 LVD circuit characteristics

(1) LVD Detection Voltage of Reset Mode and Interrupt Mode

(T_A = -40 to +105°C, $V_{PDR} \leq EV_{DD} = V_{DD} \leq$.5.5 V, V_{SS} = 0 V)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	Supply voltage level	V_{LVD0}	Power supply rise time	3.90	4.06	4.22	V
			Power supply fall time	3.83	3.98	4.13	V
		V_{LVD1}	Power supply rise time	3.60	3.75	3.90	V
			Power supply fall time	3.53	3.67	3.81	V
		V_{LVD2}	Power supply rise time	3.01	3.13	3.25	V
			Power supply fall time	2.94	3.06	3.18	V
		V_{LVD3}	Power supply rise time	2.90	3.02	3.14	V
			Power supply fall time	2.85	2.96	3.07	V
		V_{LVD4}	Power supply rise time	2.81	2.92	3.03	V
			Power supply fall time	2.75	2.86	2.97	V
		V_{LVD5}	Power supply rise time	2.71	2.81	2.92	V
			Power supply fall time	2.64	2.75	2.86	V
		V_{LVD6}	Power supply rise time	2.61	2.71	2.81	V
			Power supply fall time	2.55	2.65	2.75	V
		V_{LVD7}	Power supply rise time	2.51	2.61	2.71	V
			Power supply fall time	2.45	2.55	2.65	V
Minimum pulse width		t_{LW}		300			μs
Detection delay time						300	μs

(2) LVD Detection Voltage of Interrupt & Reset Mode

(T_A = -40 to +105°C, $V_{PDR} \leq EV_{DD} \leq V_{DD} \leq$ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Interrupt and reset mode	V_{LVDD0}	V_{POC0}, V_{POC1}, V_{POC2} = 0, 1, 1, falling reset voltage		2.64	2.75	2.86	V
	V_{LVDD1}	LVIS0, LVIS1 = 1, 0	Rising release reset voltage	2.81	2.92	3.03	V
			Falling interrupt voltage	2.75	2.86	2.97	V
	V_{LVDD2}	LVIS0, LVIS1 = 0, 1	Rising release reset voltage	2.90	3.02	3.14	V
			Falling interrupt voltage	2.85	2.96	3.07	V
	V_{LVDD3}	LVIS0, LVIS1 = 0, 0	Rising release reset voltage	3.90	4.06	4.22	V
			Falling interrupt voltage	3.83	3.98	4.13	V

3.6.8 Power supply voltage rising slope characteristics

(T_A = -40 to +105°C, V_{SS} = 0 V)

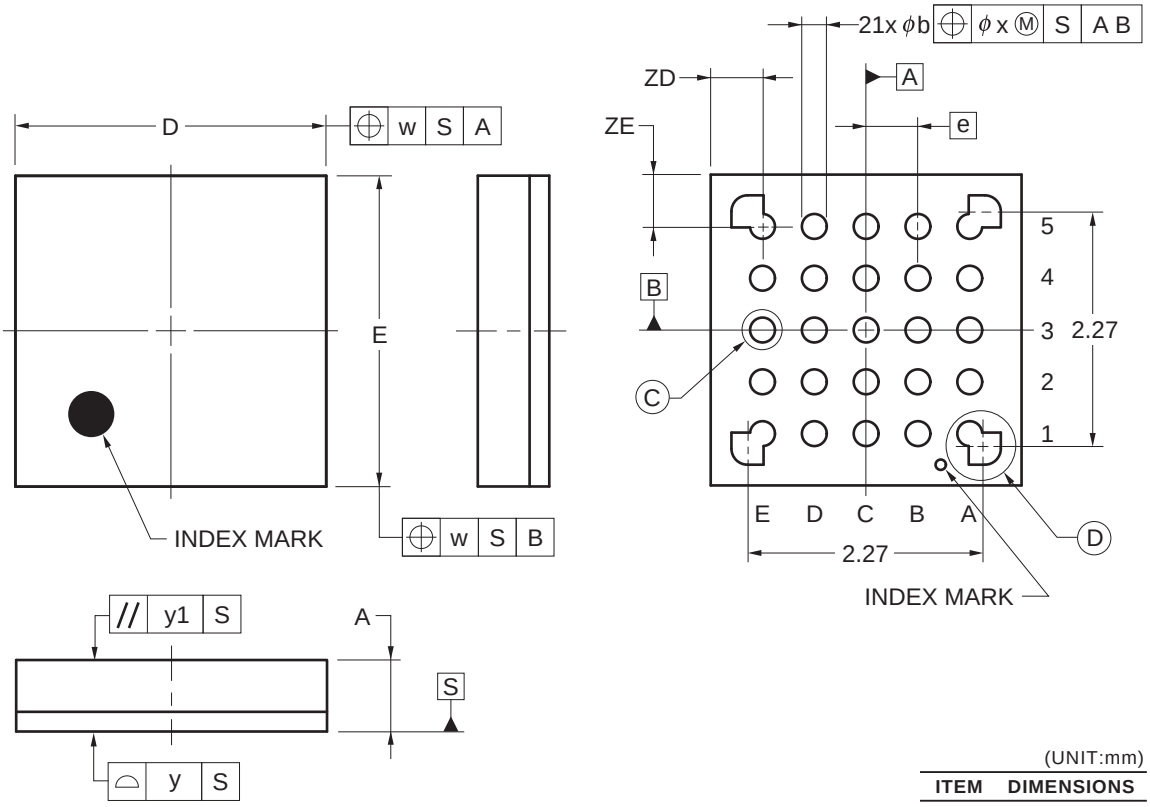
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Power supply voltage rising slope	S_{VDD}				54	V/ms

Caution Make sure to keep the internal reset state by the LVD circuit or an external reset until V_{DD} reaches the operating voltage range shown in 3.4 AC Characteristics.

4.5 25-pin products

R5F1058AGLA, R5F1058AALA

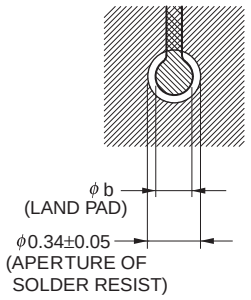
JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-WFLGA25-3x3-0.50	PWLG0025KA-A	P25FC-50-2N2-2	0.01



(UNIT:mm)

ITEM	DIMENSIONS
D	3.00±0.10
E	3.00±0.10
w	0.20
e	0.50
A	0.69±0.07
b	0.24±0.05
x	0.05
y	0.08
y1	0.20
ZD	0.50
ZE	0.50

DETAIL OF Ⓒ PART



DETAIL OF Ⓓ PART