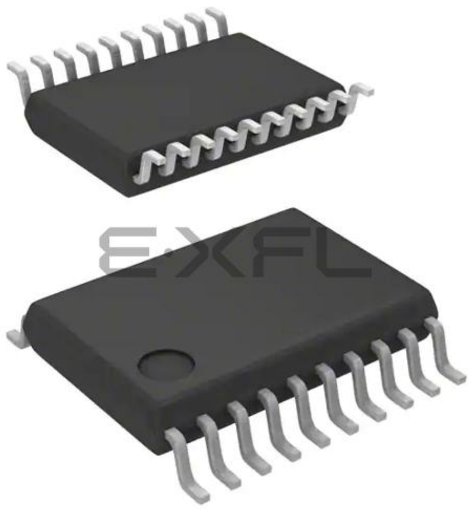
Renesas Electronics America Inc - R5F1056AASP#50 Datasheet



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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

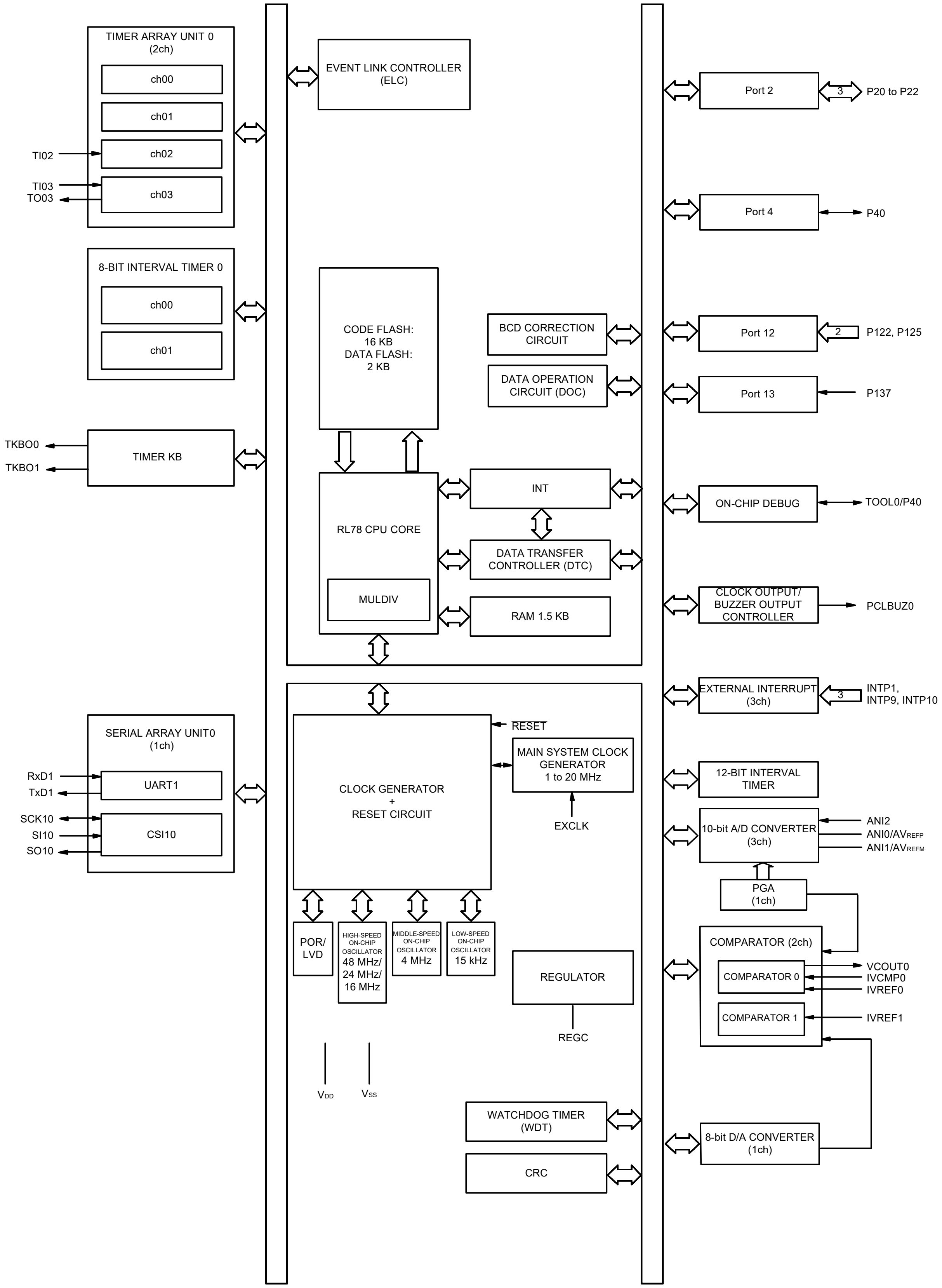
Details	
Product Status	Active
Core Processor	RL78
Core Size	16-Bit
Speed	24MHz
Connectivity	CSI, I²C, UART/USART
Peripherals	LVD, POR, WDT
Number of I/O	17
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	1.5K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 10x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-LSSOP (0.173", 4.40mm Width)
Supplier Device Package	20-LSSOP
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f1056aasp-50

1.4 Pin Identification

ANI0 to ANI3, ANI16 to ANI22 : Analog input
ANO1 : Analog output
AV$_{\text{REFM}}$: A/D converter reference potential (- side) input
AV$_{\text{REFP}}$: A/D converter reference potential (+ side) input
EV$_{\text{DD}}$: Power supply
EXCLK : External clock input (main system clock)
INTP0 to INTP11 : External interrupt input
INTFO : Interrupt Flag output
IVCMP0, IVCMP1 : Comparator input
IVREF0, IVREF1 : Comparator reference input
KR0 to KR7 : Key return
PGAI, PGAGND : PGA Input
P00 to P01 : Port 0
P20 to P23 : Port 2
P30 to P33 : Port 3
P40 : Port 4
P51 to P56 : Port 5
P121, P122, P125 : Port 12
P137 : Port 13
PCLBUZ0, PCLBUZ1 : Programmable clock output/buzzer output
REGC : Regulator capacitance
$\overline{\text{RESET}}$: Reset
RxD0, RxD1 : Receive data
SCK00, SCK01, SCK10, SCK11 : Serial clock input/output
SCLA0, SCLA1 : Serial clock input/output
SCL00, SCL01, SCL10, SCL11 : Serial clock output
SDAA0, SDAA1 : Serial data input/output
SDA00, SDA01, SDA10, SDA11 : Serial data input/output
SI00, SI01, SI10, SI11 : Serial data input
SO00, SO01, SO10, SO11 : Serial data output
$\overline{\text{SSI00}}$: Serial interface chip select input
TI00 to TI03 : Timer input
TKBO0, TKBO1 : TMKB output
TO00 to TO03 : Timer output
TOOL0 : Data input/output for tool
TOOLRXD, TOOLTXD : Data input/output for external device
TxD0, TxD1 : Transmit data
VCOUT0, VCOUT1 : Comparator output
V$_{\text{DD}}$: Power supply
V$_{\text{SS}}$: Ground
X1, X2 : Crystal oscillator (main system clock)

1.5 Block Diagram

1.5.1 10-pin products



(2/2)

Item		10-pin	16-pin	20-pin	24-pin	25-pin
		R5F1051A	R5F1054A	R5F1056A	R5F1057A	R5F1058A
Clock output/buzzer output		1		2		
<R>		• 2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (Main system clock: f_{MAIN} = 20 MHz operation) • 117 Hz, 234 Hz, 469 Hz, 938 Hz, 1.875 kHz, 3.75 kHz, 7.5 kHz, 15 kHz (subsystem clock: f_{IL} = 15 kHz operation)				
10-bit resolution A/D converter	External	3 channels	8 channels	10 channels	11 channels	
	Internal	1 channel				
8-bit D/A converter		1 channel	2 channels			
Comparator (Window Comparator)		1 channel	2 channels			
PGA		1 channel				
Data Operation Circuit (DOC)		Comparison, addition, and subtraction of 16-bit data				
<R> Serial interface		[10-pin products] • CSI: 1 channel/UART: 1 channel [16-pin products] • CSI: 2 channels/UART: 2 channels/simplified I^{2}C: 1 channel [20-pin products] • CSI: 3 channel/UART: 2 channel/simplified I^{2}C: 3 channel [24-pin, 25-pin products] • CSI: 4 channels/UART: 2 channel/simplified I^{2}C: 4 channels				
	I^{2}C bus	None	1 channel	2 channels		
Data transfer controller (DTC)		13 sources	22 sources	23 sources	24 sources	
Event link controller (ELC)		Event input: 11 Event trigger output: 3	Event input: 16 Event trigger output: 4	Event input: 17 Event trigger output: 4	Event input: 18 Event trigger output: 4	
Vectored interrupt sources	Internal	20	24	25		
	External	3	9	10	13	
Key interrupt		None	3	5	8	
Reset		• Reset by $\overline{\text{RESET}}$ pin • Internal reset by watchdog timer • Internal reset by power-on-reset • Internal reset by voltage detector • Internal reset by illegal instruction execution • Internal reset by RAM parity error • Internal reset by illegal-memory access				
Power-on-reset circuit		• Power-on-reset: 1.51 ± 0.04V (T_A = -40 to +85°C) 1.51 ± 0.06V (T_A = +85 to +105°C) • Power-down-reset: 1.50 ± 0.04 V (T_A = -40 to +85°C) 1.51 ± 0.06V (T_A = +85 to +105°C)				
Voltage detector	Power on	1.67 V to 4.06 V (14 stages)				
	Power down	1.63 V to 3.98 V (14 stages)				
On-chip debug function		Provided (Disable to tracing)				
Power supply voltage		V_{DD} = 1.6 to 5.5 V				
Operating ambient temperature		T_A = -40 to +85°C (Consumer applications) T_A = -40 to +105°C (Industrial applications)				

2.2 Oscillator Characteristics

2.2.1 X1 characteristics

(TA = -40 to +85°C, 1.6 V ≤ VDD ≤ 5.5 V, VSS = 0 V)

Resonator	Resonator	Conditions	MIN.	TYP.	MAX.	Unit
X1 clock oscillation frequency (fx) Note	Ceramic resonator/ crystal resonator	2.7 V ≤ VDD ≤ 5.5 V	1.0		20.0	MHz
		2.4 V ≤ VDD < 2.7 V	1.0		16.0	
		1.8 V ≤ VDD < 2.4 V	1.0		8.0	
		1.6 V ≤ VDD < 1.8 V	1.0		4.0	

Note Indicates only permissible oscillator frequency ranges. Refer to **2.4 AC Characteristics** for instruction execution time. Request evaluation by the manufacturer of the oscillator circuit mounted on a board to check the oscillator characteristics.

Caution Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.

Remark When using the X1 oscillator, refer to **6.4 System Clock Oscillator** in the RL78/G11 User's Manual.

2.2.2 On-chip oscillator characteristics

(TA = -40 to +85°C, 1.6 V ≤ VDD ≤ 5.5 V, VSS = 0 V)

Oscillators	Parameters	Conditions		MIN.	TYP.	MAX.	Unit
High-speed on-chip oscillator clock frequency Notes 1, 2	fIH	2.7 V ≤ VDD ≤ 5.5 V		1		24	MHz
		2.4 V ≤ VDD ≤ 5.5 V		1		16	
		1.8 V ≤ VDD ≤ 5.5 V		1		8	
		1.6 V ≤ VDD ≤ 5.5 V		1		4	
High-speed on-chip oscillator clock frequency accuracy		TA = -20 to +85°C	1.8 V ≤ VDD ≤ 5.5 V	-1		1	%
			1.6 V ≤ VDD < 1.8 V	-5		5	
		TA = -40 to -20°C	1.8 V ≤ VDD ≤ 5.5 V	-1.5		1.5	%
			1.6 V ≤ VDD < 1.8 V	-5.5		5.5	
Middle-speed on-chip oscillator oscillation frequency Note 2	fIM			1		4	MHz
Middle-speed on-chip oscillator oscillation frequency accuracy				-12		+12	%
<R> Temperature drift of Middle-speed on-chip oscillator oscillation frequency accuracy	DIMT				0.008		%/°C
<R> Voltage drift of Middle-speed on-chip oscillator oscillation frequency accuracy	DIMV	TA = 25°C	2.1 V ≤ VDD ≤ 5.5 V		0.02		%/V
			2.0 V ≤ VDD < 2.1 V		-12		
			1.6 V ≤ VDD < 2.0 V		10		
Low-speed on-chip oscillator clock frequency Note 2	fIL				15		kHz
Low-speed on-chip oscillator clock frequency accuracy				-15		+15	%

Note 1. High-speed on-chip oscillator frequency is selected with bits 0 to 3 of the option byte (000C2H) and bits 0 to 2 of the HOCODIV register.

Note 2. This only indicates the oscillator characteristics. Refer to **2.4 AC Characteristics** for instruction execution time.

(T_A = -40 to +85°C, 1.6 V $\leq$ EV_{DD} $\leq$ V_{DD} $\leq$ 5.5 V, V_{SS} = 0 V) **(4/4)**

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Supply current Note 1	I_{DD3} Note 2	STOP mode Note 3	T_A = -40°C		0.19	0.51	μA
			T_A = +25°C		0.25	0.51	
			T_A = +50°C		0.28	1.10	
			T_A = +70°C		0.38	1.90	
			T_A = +85°C		0.60	3.30	

Note 1. Total current flowing into V_{DD} and EV_{DD}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}. The MAX values include the peripheral operating current. However, these values do not include the current flowing into the A/D converter, comparator, Programmable gain amplifier, LVD circuit, I/O ports, and on-chip pull-up/pull-down resistors, and the current flowing during data flash rewrite.

Note 2. The values do not include the current flowing into the 12-bit interval timer and watchdog timer.

Note 3. For the setting of the current values when operating the subsystem clock in STOP mode, see the current values when operating the subsystem clock in HALT mode.

(2) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output, corresponding CSI00 only)

(T_A = -40 to +85°C, 2.7 V $\leq$ EV_{DD} $\leq$ V_{DD} $\leq$ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LP (Low-power main) mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t_{KCY1}	$t_{KCY1} \geq 2/f_{CLK}$	83.3		250		2000		500		ns
SCKp high-/low-level width	t_{KL1}	4.0 V $\leq$ EV_{DD} $\leq$ 5.5 V	$t_{KCY1}/2$ - 7		$t_{KCY1}/2$ - 50		$t_{KCY1}/2$ - 50		$t_{KCY1}/2$ - 50		ns
		2.7 V $\leq$ EV_{DD} $\leq$ 5.5 V	$t_{KCY1}/2$ - 10								ns
SIp setup time (to SCKp↑) Note 1	t_{SIK1}	4.0 V $\leq$ EV_{DD} $\leq$ 5.5 V	23		110		110		110		ns
		2.7 V $\leq$ EV_{DD} $\leq$ 5.5 V	33								ns
SIp hold time (from SCKp↑) Note 2	t_{KSI1}		10		10		10		10		ns
Delay time from SCKp↓ to SOp output Note 3	t_{KSO1}	C = 20 pF Note 4		10		20		20		20	ns

Note 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 4. C is the load capacitance of the SCKp and SOp output lines.

Caution **Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).**

Remark 1. p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM and POM numbers (g = 5)

Remark 2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,
n: Channel number (mn = 00))

(8) Communication at different potential (1.8 V, 2.5 V, 3.0 V) (CSI mode) (master mode, SCKp... internal clock output)

(T_A = -40 to +85°C, 1.8 V ≤ EV_{DD} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) **(1/2)**

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LP (Low-power main) mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t_{KCY1}	t_{KCY1} ≥ 4/f_{CLK}	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	300		1150		1150		1150		ns
			2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	500								ns
			1.8 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note, C_b = 30 pF, R_b = 5.5 kΩ	1150								ns
SCKp high-level width	t_{KH1}	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ		t_{KCY1}/2 - 75		t_{KCY1}/2 - 75		t_{KCY1}/2 - 75		t_{KCY1}/2 - 75		ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		t_{KCY1}/2 - 170		t_{KCY1}/2 - 170		t_{KCY1}/2 - 170		t_{KCY1}/2 - 170		ns
		1.8 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note, C_b = 30 pF, R_b = 5.5 kΩ		t_{KCY1}/2 - 458		t_{KCY1}/2 - 458		t_{KCY1}/2 - 458		t_{KCY1}/2 - 458		ns
SCKp low-level width	t_{KL1}	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ		t_{KCY1}/2 - 12		t_{KCY1}/2 - 50		t_{KCY1}/2 - 50		t_{KCY1}/2 - 50		ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		t_{KCY1}/2 - 18								
		1.8 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note, C_b = 30 pF, R_b = 5.5 kΩ		t_{KCY1}/2 - 50								ns

Note Use it with EV_{DD} ≥ V_b.

Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (EV_{DD} tolerance) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

(**Remarks** are listed on the page after the next page.)

(8) Communication at different potential (1.8 V, 2.5 V, 3.0 V) (CSI mode) (master mode, SCKp... internal clock output)

(T_A = -40 to +85°C, $1.8\ V \le EV_{DD} \le V_{DD} \le 5.5\ V$, V_{SS} = 0 V) (2/2)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LP (Low-power main) mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SIp setup time (to SCKp↑) Note 1	t_{SIK1}	$4.0\ V \le EV_{DD} \le 5.5\ V$, $2.7\ V \le V_b \le 4.0\ V$, C_b = 30 pF, R_b = 1.4 kΩ	81		479		479		479		ns
		$2.7\ V \le EV_{DD} < 4.0\ V$, $2.3\ V \le V_b \le 2.7\ V$, C_b = 30 pF, R_b = 2.7 kΩ	177								
		$1.8\ V \le EV_{DD} < 3.3\ V$, $1.6\ V \le V_b \le 2.0\ V$ Note 3, C_b = 30 pF, R_b = 5.5 kΩ	479								
SIp hold time (from SCKp↑) Note 1	t_{KSI1}	$4.0\ V \le EV_{DD} \le 5.5\ V$, $2.7\ V \le V_b \le 4.0\ V$, C_b = 30 pF, R_b = 1.4 kΩ	19		19		19		19		ns
		$2.7\ V \le EV_{DD} < 4.0\ V$, $2.3\ V \le V_b \le 2.7\ V$, C_b = 30 pF, R_b = 2.7 kΩ									
		$1.8\ V \le EV_{DD} < 3.3\ V$, $1.6\ V \le V_b \le 2.0\ V$ Note 3, C_b = 30 pF, R_b = 5.5 kΩ									
Delay time from SCKp↓ to SOp output Note 1	t_{KSO1}	$4.0\ V \le EV_{DD} \le 5.5\ V$, $2.7\ V \le V_b \le 4.0\ V$, C_b = 30 pF, R_b = 1.4 kΩ		100		100		100		100	ns
		$2.7\ V \le EV_{DD} < 4.0\ V$, $2.3\ V \le V_b \le 2.7\ V$, C_b = 30 pF, R_b = 2.7 kΩ		195		195		195		195	ns
		$1.8\ V \le EV_{DD} < 3.3\ V$, $1.6\ V \le V_b \le 2.0\ V$ Note 3, C_b = 30 pF, R_b = 5.5 kΩ		483		483		483		483	ns
SIp setup time (to SCKp↓) Note 2	t_{SIK1}	$4.0\ V \le EV_{DD} \le 5.5\ V$, $2.7\ V \le V_b \le 4.0\ V$, C_b = 30 pF, R_b = 1.4 kΩ	44		110		110		110		ns
		$2.7\ V \le EV_{DD} < 4.0\ V$, $2.3\ V \le V_b \le 2.7\ V$, C_b = 30 pF, R_b = 2.7 kΩ									
		$1.8\ V \le EV_{DD} < 3.3\ V$, $1.6\ V \le V_b \le 2.0\ V$ Note 3, C_b = 30 pF, R_b = 5.5 kΩ	110								
SIp hold time (from SCKp↓) Note 2	t_{KSI1}	$4.0\ V \le EV_{DD} \le 5.5\ V$, $2.7\ V \le V_b \le 4.0\ V$, C_b = 30 pF, R_b = 1.4 kΩ	19		19		19		19		ns
		$2.7\ V \le EV_{DD} < 4.0\ V$, $2.3\ V \le V_b \le 2.7\ V$, C_b = 30 pF, R_b = 2.7 kΩ									
		$1.8\ V \le EV_{DD} < 3.3\ V$, $1.6\ V \le V_b \le 2.0\ V$ Note 3, C_b = 30 pF, R_b = 5.5 kΩ									
Delay time from SCKp↑ to SOp output Note 2	t_{KSO1}	$4.0\ V \le EV_{DD} \le 5.5\ V$, $2.7\ V \le V_b \le 4.0\ V$, C_b = 30 pF, R_b = 1.4 kΩ		25		25		25		25	ns
		$2.7\ V \le EV_{DD} < 4.0\ V$, $2.3\ V \le V_b \le 2.7\ V$, C_b = 30 pF, R_b = 2.7 kΩ									
		$1.8\ V \le EV_{DD} < 3.3\ V$, $1.6\ V \le V_b \le 2.0\ V$ Note 3, C_b = 30 pF, R_b = 5.5 kΩ									

Note 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.

Note 2. When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 3. Use it with $EV_{DD} \ge V_b$.

Caution **Select the TTL input buffer for the SIp pin and the N-ch open drain output (EV_{DD} tolerance) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.**

(**Remarks** are listed on the next page.)

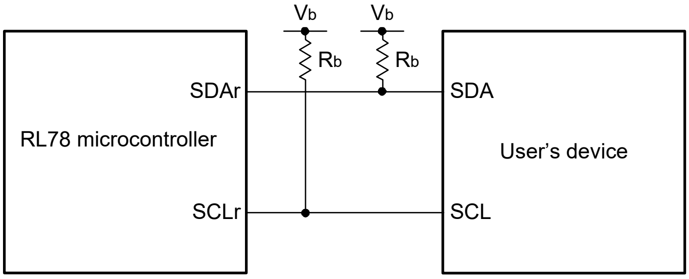
Note 1. The value must be equal to or less than $f_{MCK}/4$.

Note 2. Use it with $EV_{DD} \geq V_b$.

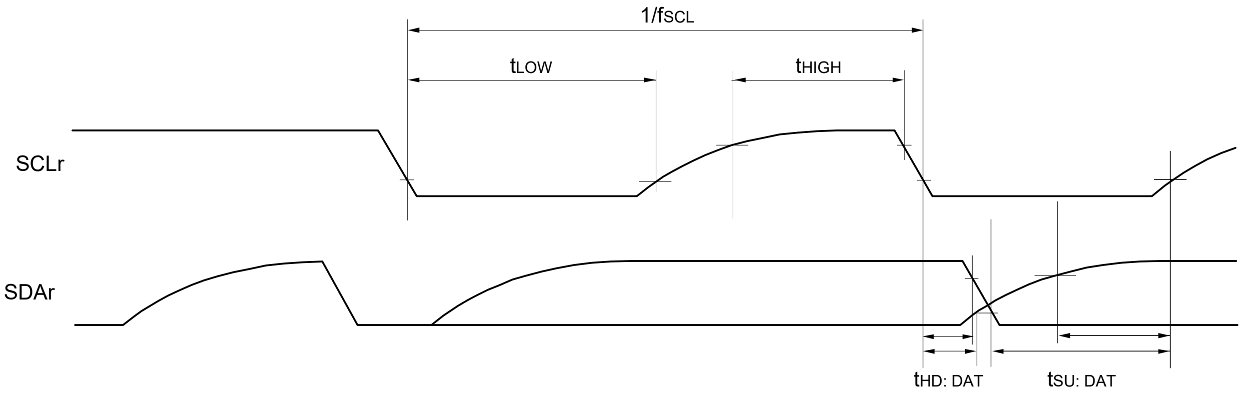
Note 3. Set the f_{MCK} value to keep the hold time of SCLr = “L” and SCLr = “H”.

Caution **Select the TTL input buffer and the N-ch open drain output (EV_{DD} tolerance) mode for the SDAr pin and the N-ch open drain output (EV_{DD} tolerance) mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.**

Simplified I²C mode connection diagram (during communication at different potential)



Simplified I²C mode serial transfer timing (during communication at different potential)



Remark 1. R_b[Ω]: Communication line (SDAr, SCLr) pull-up resistance, C_b[F]: Communication line (SDAr, SCLr) load capacitance, V_b[V]: Communication line voltage

Remark 2. r: IIC number (r = 00, 01, 10 and 11), g: PIM, POM number (g = 0, 3 and 5)

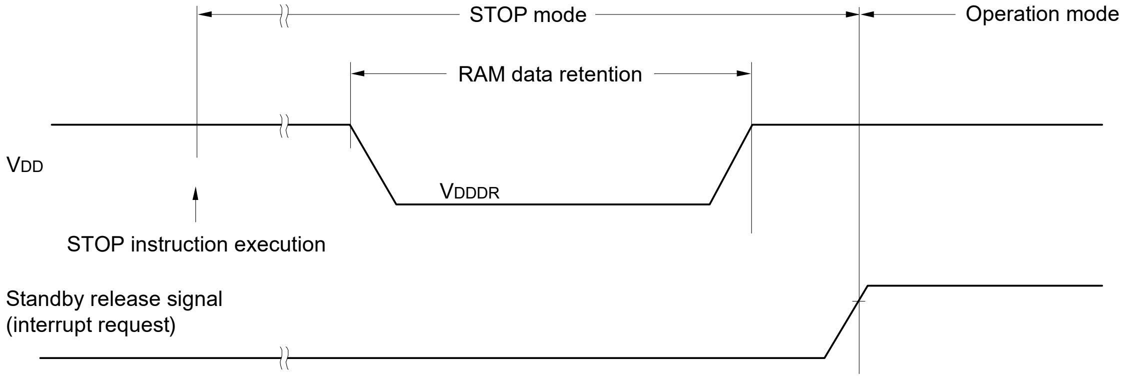
Remark 3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0),
n: Channel number (n = 0 to 3), mn = 00 to 03)

2.7 RAM Data Retention Characteristics

(T_A = -40 to +85°C, 1.8 V ≤ EV_{DD} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.46 [Note]		5.5	V

Note The value depends on the POR detection voltage. When the voltage drops, the RAM data is retained before a POR reset is effected, but RAM data is not retained when a POR reset is effected.



2.8 Flash Memory Programming Characteristics

(T_A = -40 to +85°C, 1.8 V ≤ EV_{DD} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
System clock frequency	f_{CLK}			1		24	MHz
Number of code flash rewrites Notes 1, 2, 3	C_{erwr}	Retained for 20 years	T_A = 85°C	1,000			Times
Number of data flash rewrites Notes 1, 2, 3		Retained for 1 year	T_A = 25°C		1,000,000		
		Retained for 5 years	T_A = 85°C	100,000			
		Retained for 20 years	T_A = 85°C	10,000			

Note 1. 1 erase + 1 write after the erase is regarded as 1 rewrite. The retaining years are until next rewrite after the rewrite.

Note 2. When using flash memory programmer and Renesas Electronics self-programming library

Note 3. These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.

3.3 DC Characteristics

3.3.1 Pin characteristics

(T_A = -40 to +105°C, 2.4 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = 0 V) **(1/5)**

<R>

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, high Note 1	I_{OH1}	Per pin for P00, P01, P30 to P33, P40, and P51 to P56				-3.0 Note 2	mA
		Total of P00, P01, and P40 (When duty ≤ 70% Note 3)	4.0 V ≤ EV_{DD} ≤ 5.5 V			-12.5	mA
			2.7 V ≤ EV_{DD} < 4.0 V			-10.0	mA
			2.4 V ≤ EV_{DD} < 2.7 V			-5.0	mA
		Total of P30 to P33, and P51 to P56 (When duty ≤ 70% Note 3)	4.0 V ≤ EV_{DD} ≤ 5.5 V			-30.0	mA
			2.7 V ≤ EV_{DD} < 4.0 V			-19.0	mA
			2.4 V ≤ EV_{DD} < 2.7 V			-10.0	mA
		Total of all pins (When duty ≤ 70% Note 3)				-42.5	mA
	I_{OH2}	Per pin for P20 to P23				-0.1 Note 2	mA
		Total of all pins (When duty ≤ 70% Note 3)	2.4 V ≤ V_{DD} ≤ 5.5 V			-0.4	mA

Note 1. Value of current at which the device operation is guaranteed even if the current flows from the V_{DD} pin to an output pin.

Note 2. Do not exceed the total current value.

Note 3. Specification under conditions where the duty factor ≤ 70%.
The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = (I_{OH} × 0.7)/(n × 0.01)

<Example> Where n = 80% and I_{OH} = -10.0 mA
Total output current of pins = (-10.0 × 0.7)/(80 × 0.01) ≈ -8.7 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor.
A current higher than the absolute maximum rating must not flow into one pin.

Caution **P00, P01, P20, P30 to P33, P40 and P51 to P56 do not output high level in N-ch open-drain mode.**

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

When P20 is used as SO10 pin

(T_A = -40 to +105°C, 2.7 V ≤ EV_{DD} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		Unit
				MIN.	MAX.	
SCKp cycle time	t_{KCY1}	t_{KCY1} ≥ $4/f_{CLK}$	2.7 V ≤ V_{DD} ≤ 5.5 V	1000		ns
			2.4 V ≤ V_{DD} ≤ 5.5 V	1200		ns
SCKp high-/low-level width	t_{KH1}, t_{KL1}	4.0 V ≤ V_{DD} ≤ 5.5 V		$t_{KCY1}/2 - 24$		ns
		2.4 V ≤ V_{DD} ≤ 5.5 V		$t_{KCY1}/2 - 76$		ns
SIp setup time (to SCKp↑) Note 1	t_{SIK1}	2.7 V ≤ V_{DD} ≤ 5.5 V		66		ns
		2.4 V ≤ V_{DD} ≤ 5.5 V		133		ns
SIp hold time (from SCKp↑) Note 2	t_{KSI1}			38		ns
Delay time from SCKp↓ to SOp output Note 3	t_{KSO1}	C = 30 pF Note 4			180	ns

Note 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes “to SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 4. C is the load capacitance of the SCKp and SOp output lines.

Caution **Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).**

Remark 1. p: CSI number (p = 00, 01, 10 and 11), m: Unit number (m = 0), n: Channel number (n = 0 to 3), g: PIM and POM numbers (g = 0, 2, 3 to 5 and 12)

Remark 2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,
n: Channel number (mn = 00 to 03))

When P20 is used as SO10 pin
(T_A = -40 to +105°C, 2.4 V ≤ EV_{DD} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		Unit
				MIN.	MAX.	
SCKp cycle time Note 4	t_{KCY2}	4.0 V ≤ V_{DD} ≤ 5.5 V	f_{MCK} > 20 MHz	20/f_{MCK}		ns
			f_{MCK} ≤ 20 MHz	18/f_{MCK}		ns
		2.7 V ≤ V_{DD} < 4.0 V	f_{MCK} > 16 MHz	20/fMCK and 1000		ns
			f_{MCK} ≤ 16 MHz	18/f_{MCK}		ns
		2.4 V ≤ V_{DD} < 2.7 V		18/f_{MCK} and 1200		ns
SCKp high-/low-level width	t_{KH2}, t_{KL2}	4.0 V ≤ V_{DD} ≤ 5.5 V		t_{KCY2}/2 - 14		ns
	t_{KH2}, t_{KL2}	2.7 V ≤ V_{DD} < 4.0 V		t_{KCY2}/2 - 16		ns
		2.4 V ≤ V_{DD} < 2.7 V		t_{KCY2}/2 - 36		ns
SIp setup time (to SCKp↑) Note 1	t_{SIK2}	2.7 V ≤ V_{DD} ≤ 5.5 V		1/f_{MCK} + 40		ns
		2.4 V ≤ V_{DD} < 2.7 V		1/f_{MCK} + 60		ns
SIp hold time (from SCKp↑) Note 1	t_{KSI2}			1/f_{MCK} + 62		ns
Delay time from SCKp↓ to SOp output Note 2	t_{KSO2}	C = 30 pF Note 3	2.7 V ≤ V_{DD} ≤ 5.5 V		2/f_{MCK} + 190	ns
			2.4 V ≤ V_{DD} < 2.7 V		2/f_{MCK} + 250	ns

Note 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 3. C is the load capacitance of the SOp output lines.

Note 4. The maximum transfer rate when using the SNOOZE mode is 1 Mbps.

Caution **Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).**

Remark 1. p: CSI number (p = 00, 01, 10 and 11), m: Unit number (m = 0), n: Channel number (n = 0 to 3), g: PIM and POM numbers (g = 0, 2, 3 to 5 and 12)

Remark 2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,
n: Channel number (mn = 00 to 03))

Note 6. The smaller maximum transfer rate derived by using $f_{MCK}/6$ or the following expression is the valid maximum transfer rate.
Expression for calculating the transfer rate when $2.4\ \text{V} \leq EV_{DD} < 3.3\ \text{V}$ and $1.6\ \text{V} \leq V_b \leq 2.0\ \text{V}$

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln (1 - \frac{1.5}{V_b})\} \times 3}\ [\text{bps}]$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln (1 - \frac{1.5}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100\ [\%]$$

* This value is the theoretical value of the relative difference between the transmission and reception sides

Note 7. This value as an example is calculated when the conditions described in the “Conditions” column are met.
Refer to Note 6 above to calculate the maximum transfer rate under conditions of the customer.

Caution **Select the TTL input buffer for the RxDq pin and the N-ch open drain output (EV_{DD} tolerance) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.**

(6) Communication at different potential (1.8 V, 2.5 V, 3.0 V) (CSI mode) (master mode, SCKp... internal clock output)

(T_A = -40 to +105°C, 2.4 V ≤ EV_{DD} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) **(1/2)**

Parameter	Symbol	Conditions		HS (high-speed main) Mode		Unit
				MIN.	MAX.	
SCKp cycle time	t_{KCY1}	t_{KCY1} ≥ 4/f_{CLK}	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	600		ns
			2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	1000		ns
			2.4 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ	2300		ns
SCKp high-level width	t_{KH1}	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ		t_{KCY1}/2 - 150		ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		t_{KCY1}/2 - 340		ns
		2.4 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ		t_{KCY1}/2 - 916		ns
SCKp low-level width	t_{KL1}	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ		t_{KCY1}/2 - 24		ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		t_{KCY1}/2 - 36		ns
		2.4 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ		t_{KCY1}/2 - 100		ns

Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (EV_{DD} tolerance) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

(**Remarks** are listed on the page after the next page.)

(8) Communication at different potential (1.8 V, 2.5 V, 3.0 V) (simplified I^{2}C mode)

(T_A = -40 to +105°C, 2.4 V ≤ EV_{DD} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
SCLr clock frequency	f_{SCL}	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 50 pF, R_b = 2.7 kΩ		400 Note 1	kHz
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 50 pF, R_b = 2.7 kΩ		400 Note 1	kHz
		4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 2.8 kΩ		100 Note 1	kHz
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ		100 Note 1	kHz
		2.4 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2, C_b = 100 pF, R_b = 5.5 kΩ		100 Note 1	kHz
Hold time when SCLr = "L"	t_{LOW}	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 50 pF, R_b = 2.7 kΩ	1200		ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 50 pF, R_b = 2.7 kΩ	1200		ns
		4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 2.8 kΩ	4600		ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ	4600		ns
		2.4 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2, C_b = 100 pF, R_b = 5.5 kΩ	4650		ns
Hold time when SCLr = "H"	t_{HIGH}	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 50 pF, R_b = 2.7 kΩ	620		ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 50 pF, R_b = 2.7 kΩ	500		ns
		4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 2.8 kΩ	2700		ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ	2400		ns
		2.4 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2, C_b = 100 pF, R_b = 5.5 kΩ	1830		ns
Data setup time (reception)	$t_{SU:DAT}$	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 50 pF, R_b = 2.7 kΩ	1/f_{MCK} + 340 Note 3		ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 50 pF, R_b = 2.7 kΩ	1/f_{MCK} + 340 Note 3		ns
		4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 2.8 kΩ	1/f_{MCK} + 760 Note 3		ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ	1/f_{MCK} + 760 Note 3		ns
		2.4 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2, C_b = 100 pF, R_b = 5.5 kΩ	1/f_{MCK} + 570 Note 3		ns
Data hold time (transmission)	$t_{HD:DAT}$	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 50 pF, R_b = 2.7 kΩ	0	770	ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 50 pF, R_b = 2.7 kΩ	0	770	ns
		4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 2.8 kΩ	0	1420	ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ	0	1420	ns
		2.4 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2, C_b = 100 pF, R_b = 5.5 kΩ	0	1215	ns

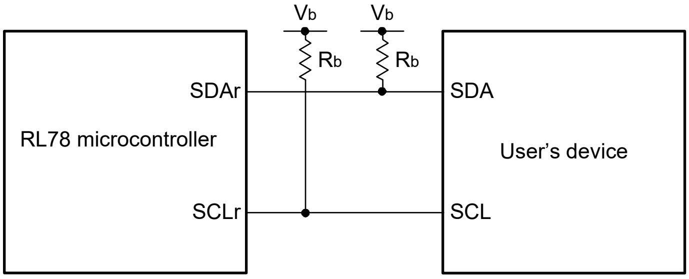
Note 1. The value must be equal to or less than $f_{MCK}/4$.

Note 2. Use it with $EV_{DD} \geq V_b$.

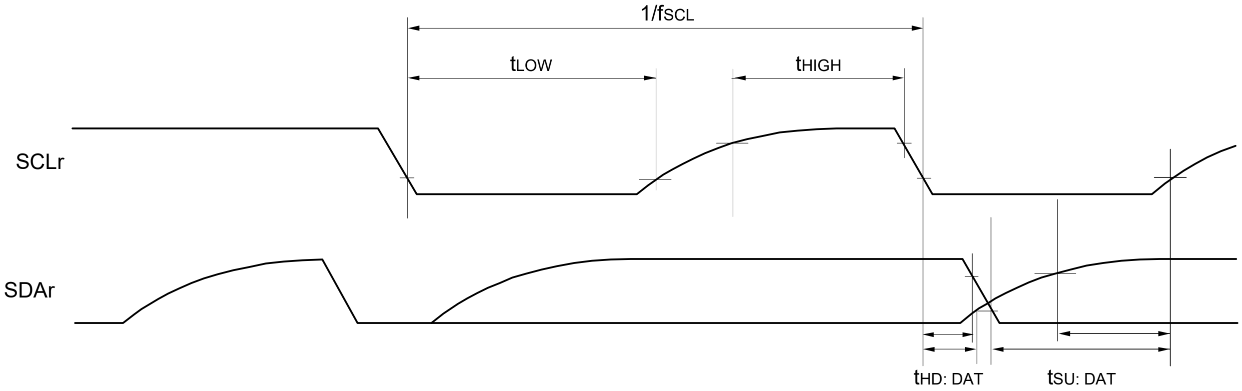
Note 3. Set the f_{MCK} value to keep the hold time of SCLr = “L” and SCLr = “H”.

Caution **Select the TTL input buffer and the N-ch open drain output (EV_{DD} tolerance) mode for the SDAr pin and the N-ch open drain output (EV_{DD} tolerance) mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.**

Simplified I²C mode connection diagram (during communication at different potential)



Simplified I²C mode serial transfer timing (during communication at different potential)



Remark 1. R_b[Ω]: Communication line (SDAr, SCLr) pull-up resistance, C_b[F]: Communication line (SDAr, SCLr) load capacitance, V_b[V]: Communication line voltage

Remark 2. r: IIC number (r = 00, 01, 10 and 11), g: PIM, POM number (g = 0, 3 and 5)

Remark 3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0), n: Channel number (n = 0 to 3), mn = 00 to 03)

3.6.5 PGA

(T_A = -40 to +105°C, 2.7 V ≤ EV_{DD} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input offset voltage	V_{IOPGA}					±10	mV
Input voltage range	V_{IPGA}			0		0.9 × V_{DD}/Gain	V
Output voltage range	V_{IOHPGA}			0.93 × V_{DD}			V
	V_{IOLPGA}					0.07 × V_{DD}	V
Gain error		x4, x8				±1	%
		x16				±1.5	%
		x32				±2	%
Slew rate	SR_{RPGA}	Rising When V_{IN} = 0.1V_{DD}/gain to 0.9V_{DD}/gain. 10 to 90% of output voltage amplitude	4.0 V ≤ V_{DD} ≤ 5.5 V (Other than x32)	3.5			V/μs
			4.0 V ≤ V_{DD} ≤ 5.5 V (x32)	3.0			
			2.7 V ≤ V_{DD} ≤ 4.0V	0.5			
	SR_{FPGA}	Falling When V_{IN}= 0.1V_{DD}/gain to 0.9V_{DD}/gain. 90 to 10% of output voltage amplitude	4.0 V ≤ V_{DD} ≤ 5.5 V (Other than x32)	3.5			
			4.0 V ≤ V_{DD} ≤ 5.5 V (x32)	3.0			
			2.7 V ≤ V_{DD} ≤ 4.0V	0.5			
Reference voltage stabilization wait time[Note]	t_{PGA}	x4, x8				5	μs
		x16, x32				10	μs

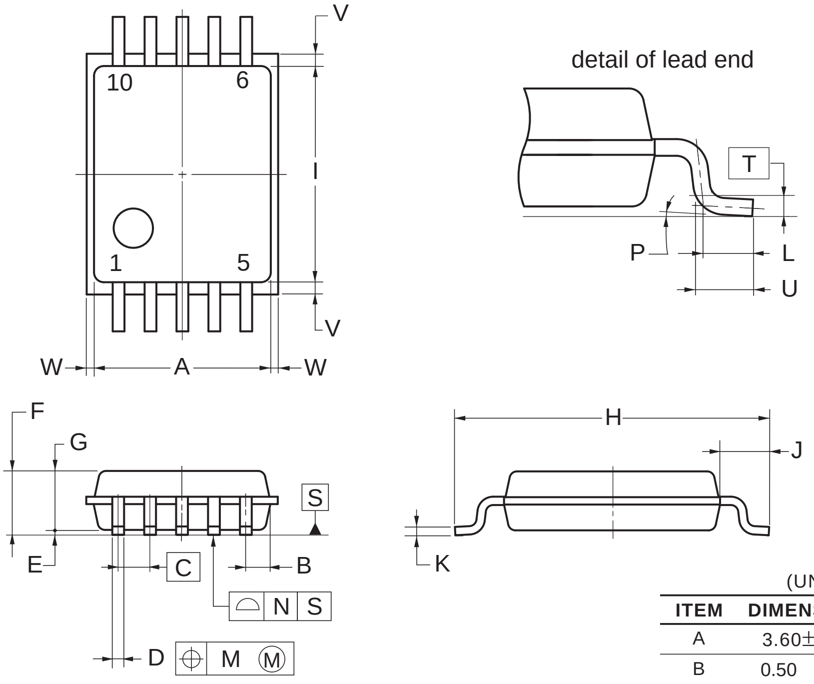
Note Time required until a state is entered where the DC and AC specifications of the PGA are satisfied after the PGA operation has been enabled (PGAEN = 1).

4. PACKAGE DRAWINGS

4.1 10-pin products

R5F1051AGSP, R5F1051AASP

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LSSOP10-4.4x3.6-0.65	PLSP0010JA-A	P10MA-65-CAC-2	0.05



(UNIT:mm)

ITEM	DIMENSIONS
A	3.60±0.10
B	0.50
C	0.65 (T.P.)
D	0.24±0.08
E	0.10±0.05
F	1.45 MAX.
G	1.20±0.10
H	6.40±0.20
I	4.40±0.10
J	1.00±0.20
K	$0.17^{+0.08}_{-0.07}$
L	0.50
M	0.13
N	0.10
P	$3^\circ\,{}^{+5^\circ}_{-3^\circ}$
T	0.25 (T.P.)
U	0.60±0.15
V	0.25 MAX.
W	0.15 MAX.

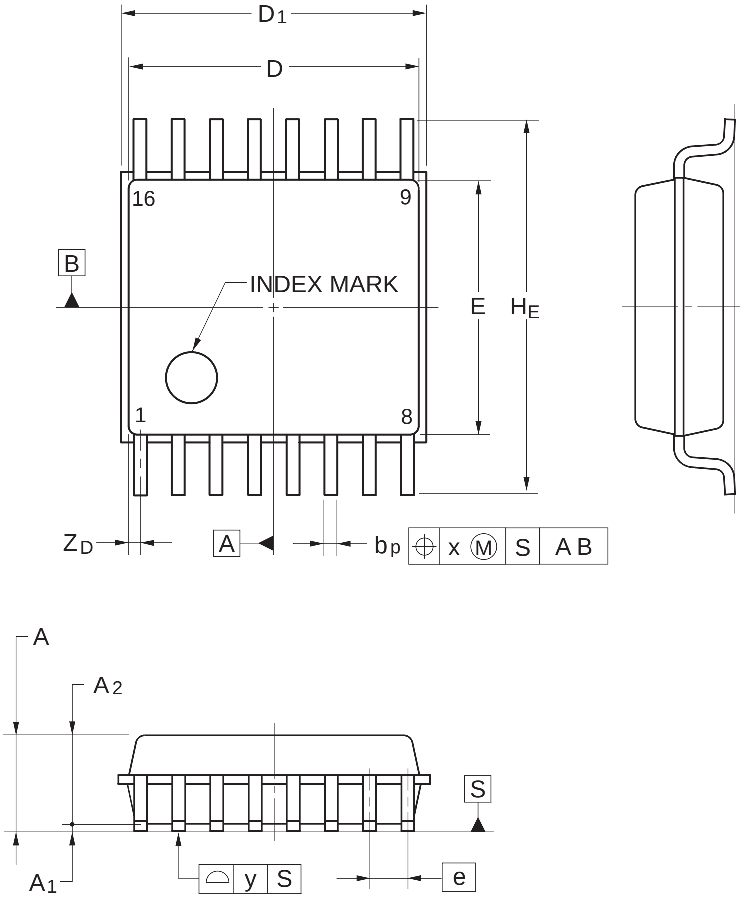
NOTE

Each lead centerline is located within 0.13 mm of its true position (T.P.) at maximum material condition.

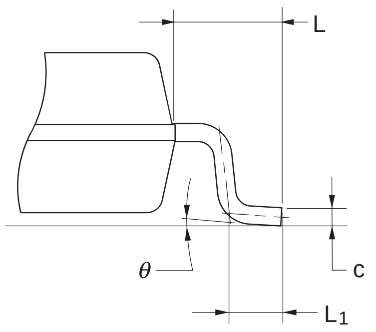
4.2 16-pin products

R5F1054AGSP, R5F1054AASP

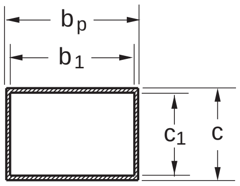
JEITA Package code	RENESAS code	Previous code	MASS(TYP.)[g]
P-SSOP16-4.4x5-0.65	PRSP0016JC-B	P16MA-65-FAB	0.08



detail of lead end



Terminal cross section



Referance Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	4.85	5.00	5.15
D_1	5.05	5.20	5.35
E	4.20	4.40	4.60
A_2	—	1.50	—
A_1	0.075	0.125	0.175
A	—	—	1.725
b_p	0.17	0.24	0.32
b_1	—	0.22	—
c	0.14	0.17	0.20
c_1	—	0.15	—
θ	0°	—	8°
H_E	6.20	6.40	6.60
e	—	0.65	—
x	—	—	0.13
y	—	—	0.10
Z_D	—	0.225	—
L	0.35	0.50	0.65
L_1	—	1.00	—