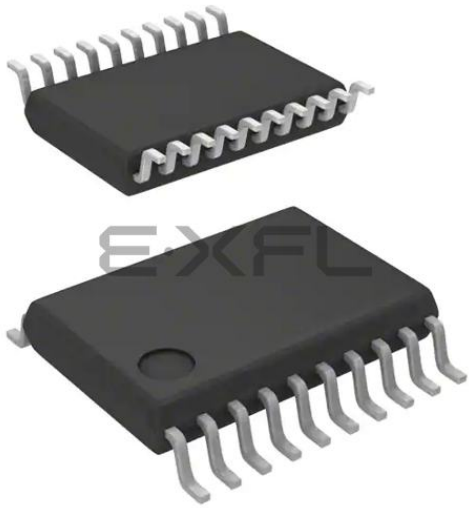

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	RL78
Core Size	16-Bit
Speed	24MHz
Connectivity	CSI, I²C, UART/USART
Peripherals	LVD, POR, WDT
Number of I/O	17
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	1.5K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 10x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	20-LSSOP (0.173", 4.40mm Width)
Supplier Device Package	20-LSSOP
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f1056agsp-30

Timers

- 16-bit timer (TAU): 4 channels
- TKB: 1 channel
- 12-bit interval timer: 1 channel
- <R> 8-bit interval timer: 2 channels
- Watchdog timer: 1 channel

A/D converter

- 8/10-bit resolution A/D converter (V_{DD} = 1.6 to 5.5 V)
- Analog input: 10 to 11 channels
- Internal reference voltage (1.45 V) and temperature sensor

D/A converter

- 8/10-bit resolution D/A converter (V_{DD} = 1.6 to 5.5 V)
- <R> Analog input: 2 channels (channel 1: output to the ANO1 pin, channel 0: output to the comparator)
- Output voltage: 0 V to V_{DD}
- Real-time output function

Comparator

- 2 channels
- Operating modes: Comparator high-speed mode, comparator low-speed mode, window mode

PGA

- 1 channels

I/O ports

- I/O port: 17 to 21 (N-ch open drain I/O [V_{DD} withstand voltage[Note 1]/EV_{DD} withstand voltage[Note 2]]: 10 to 14)
- Can be set to N-ch open drain, TTL input buffer, and on-chip pull-up resistor
- Different potential interface: Can connect to a 1.8/2.5/3.0 V device
- On-chip key interrupt function
- On-chip clock output/buzzer output controller

Others

- On-chip BCD (binary-coded decimal) correction circuit
- On-chip data operation circuit

Note 1. 16, 20, 24-pin products

Note 2. 25-pin products

Remark The functions mounted depend on the product. See **1.6 Outline of Functions**.

○ ROM, RAM capacities

Flash ROM	Data flash	RAM	RL78/G11				
			10 pins	16 pins	20 pins	24 pins	25 pins
16 KB	2 KB	1.5 KB	R5F1051A	R5F1054A	R5F1056A	R5F1057A	R5F1058A

Remark The flash library uses RAM in self-programming and rewriting of the data flash memory.
The target products and start address of the RAM areas used by the flash library are shown below.

R5F105xA (x = 1, 4, 6, 7, 8): Start address FF900H

For the RAM areas used by the flash library, see **Self RAM list of Flash Self-Programming Library for RL78 Family (R20UT2944)**.

(2/2)

Item		10-pin R5F1051A	16-pin R5F1054A	20-pin R5F1056A	24-pin R5F1057A	25-pin R5F1058A
Clock output/buzzer output		1		2		
<R>		• 2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (Main system clock: f_{MAIN} = 20 MHz operation) • 117 Hz, 234 Hz, 469 Hz, 938 Hz, 1.875 kHz, 3.75 kHz, 7.5 kHz, 15 kHz (subsystem clock: f_{IL} = 15 kHz operation)				
10-bit resolution A/D converter	External	3 channels	8 channels	10 channels	11 channels	
	Internal	1 channel				
8-bit D/A converter		1 channel	2 channels			
Comparator (Window Comparator)		1 channel	2 channels			
PGA		1 channel				
Data Operation Circuit (DOC)		Comparison, addition, and subtraction of 16-bit data				
<R> Serial interface		[10-pin products] • CSI: 1 channel/UART: 1 channel [16-pin products] • CSI: 2 channels/UART: 2 channels/simplified I^2C: 1 channel [20-pin products] • CSI: 3 channel/UART: 2 channel/simplified I^2C: 3 channel [24-pin, 25-pin products] • CSI: 4 channels/UART: 2 channel/simplified I^2C: 4 channels				
	I^2C bus	None	1 channel	2 channels		
Data transfer controller (DTC)		13 sources	22 sources	23 sources	24 sources	
Event link controller (ELC)		Event input: 11 Event trigger output: 3	Event input: 16 Event trigger output: 4	Event input: 17 Event trigger output: 4	Event input: 18 Event trigger output: 4	
Vectored interrupt sources	Internal	20	24	25		
	External	3	9	10	13	
Key interrupt		None	3	5	8	
Reset		• Reset by $\overline{\text{RESET}}$ pin • Internal reset by watchdog timer • Internal reset by power-on-reset • Internal reset by voltage detector • Internal reset by illegal instruction execution • Internal reset by RAM parity error • Internal reset by illegal-memory access				
Power-on-reset circuit		• Power-on-reset: 1.51 ± 0.04V (T_A = -40 to +85°C) 1.51 ± 0.06V (T_A = +85 to +105°C) • Power-down-reset: 1.50 ± 0.04 V (T_A = -40 to +85°C) 1.51 ± 0.06V (T_A = +85 to +105°C)				
Voltage detector	Power on	1.67 V to 4.06 V (14 stages)				
	Power down	1.63 V to 3.98 V (14 stages)				
On-chip debug function		Provided (Disable to tracing)				
Power supply voltage		V_{DD} = 1.6 to 5.5 V				
Operating ambient temperature		T_A = -40 to +85°C (Consumer applications) T_A = -40 to +105°C (Industrial applications)				

2. ELECTRICAL SPECIFICATIONS (T_A = -40 to +85°C)

This chapter describes the following electrical specifications.

Target products A: Consumer applications (T_A = −40 to +85°C)

R5F105xxAxx

G: When the products “G: Industrial applications (T_A = −40 to +105°C)" is used in the range of T_A = -40 to +85°C

R5F105xxGxx

Caution 1. The RL78 microcontrollers have an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.

Caution 2. The pins mounted depend on the product. Refer to 2.1 Port Functions to 2.2.1 Functions for each product in the RL78/G11 User's Manual.

Caution 3. The EV_{DD} pin is not present on products with 24 or less pins. Accordingly, replace EV_{DD} with V_{DD} and the voltage condition $1.6 \leq EV_{DD} \leq V_{DD} \leq 5.5$ V with $1.6 \leq V_{DD} \leq 5.5$ V.

(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) **(5/5)**

Items	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Input leakage current, high	I_{LIH1}	P00, P01, P30 to P33, P40, and P51 to P56	$V_I = EV_{DD}$				1	μA
	I_{LIH2}	P20 to P23, P125, P137, $\overline{RESET}$	$V_I = V_{DD}$				1	μA
	I_{LIH3}	P121, P122, X1, X2, EXCLK	$V_I = V_{DD}$	In input port or external clock input			1	μA
				In resonator connection			10	μA
Input leakage current, low	I_{LIL1}	P00, P01, P30 to P33, P40, and P51 to P56	$V_I = V_{SS}$				-1	μA
	I_{LIL2}	P20 to P23, P125, P137, $\overline{RESET}$	$V_I = V_{SS}$				-1	μA
	I_{LIL3}	P121, P122, X1, X2, EXCLK	$V_I = V_{SS}$	In input port or external clock input			-1	μA
				In resonator connection			-10	μA
On-chip pull-up resistance	R_U	P00, P01, P30 to P33, P40, P51 to P56, P125	$V_I = V_{SS}$, In input port		10	20	100	kΩ

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) **(2/4)**

Parameter	Symbol	Conditions						MIN.	TYP.	MAX.	Unit
Supply current Note 1	I_{DD1}	Operating mode	Normal operation	Subsystem clock operation	f_{IL} = 15 kHz, T_A = -40°C Note 5	Normal operation			1.8	5.9	μA
					f_{IL} = 15 kHz, T_A = +25°C Note 5	Normal operation			1.9	5.9	
					f_{IL} = 15 kHz, T_A = +85°C Note 5	Normal operation			2.3	8.7	

Note 1. Total current flowing into V_{DD} and EV_{DD}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}. The MAX values include the peripheral operating current. However, these values do not include the current flowing into the A/D converter, comparator, Programmable gain amplifier, LVD circuit, I/O ports, and on-chip pull-up/pull-down resistors, and the current flowing during data flash rewrite.

Note 2. When the high-speed on-chip oscillator clock, middle-speed on-chip oscillator clock and low-speed on-chip oscillator clock are stopped.

Note 3. When the high-speed system clock, middle-speed on-chip oscillator clock and low-speed on-chip oscillator clock are stopped.

Note 4. When the high-speed system clock is stopped.

Note 5. When the high-speed system clock, high-speed on-chip oscillator clock and middle-speed on-chip oscillator clock are stopped.

Note 6. When the high-speed system clock, high-speed on-chip oscillator clock and low-speed on-chip oscillator clock are stopped.

Remark 1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

Remark 2. f_{IH}: High-speed on-chip oscillator clock frequency (24 MHz max.)

Remark 3. f_{IM}: Middle-speed on-chip oscillator clock frequency (4 MHz max.)

Remark 4. f_{IL}: Low-speed on-chip oscillator clock frequency

Remark 5. f_{SUB}: Subsystem clock frequency (Low-speed on-chip oscillator clock frequency)

Remark 6. Except subsystem clock operation, temperature condition of the TYP. value is T_A = 25°C

When P20 is used as TxD1 pin

(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LP (Low-power main) mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Transfer rate		4.0 V ≤ V_{DD} ≤ 5.5 V		f_{MCK}/6 Notes 1, 2, 3		f_{MCK}/6 Notes 1, 2		f_{MCK}/6 Notes 1, 2		f_{MCK}/6 Notes 1, 2	bps
		Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} Notes 1, 3		1.5		1.3		0.1		0.6	Mbps
		2.7 V ≤ V_{DD} ≤ 5.5 V		f_{MCK}/6 Notes 1, 2, 3		f_{MCK}/6 Notes 1, 2		f_{MCK}/6 Notes 1, 2		f_{MCK}/6 Notes 1, 2	bps
		Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} Notes 1, 3		1.2		1.2		0.1		0.6	Mbps
		2.4 V ≤ V_{DD} ≤ 5.5 V		f_{MCK}/6 Notes 1, 2, 3		f_{MCK}/6 Notes 1, 2		f_{MCK}/6 Notes 1, 2		f_{MCK}/6 Notes 1, 2	bps
		Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} Notes 1, 3		1.0		1.0		0.1		0.6	Mbps
		1.8 V ≤ V_{DD} ≤ 5.5 V		Using prohibited		f_{MCK}/6 Notes 1, 2		f_{MCK}/6 Notes 1, 2		f_{MCK}/6 Notes 1, 2	bps
		Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} Notes 1, 3				0.6		0.1		0.6	Mbps
		1.7 V ≤ V_{DD} ≤ 5.5 V				Using prohibited		Using prohibited		f_{MCK}/6 Notes 1, 2	bps
		Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} Notes 1, 3								0.5	Mbps
		1.6 V ≤ V_{DD} ≤ 5.5 V								f_{MCK}/6 Notes 1, 2	bps
		Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} Notes 1, 3								0.5	Mbps

Note 1. f_{MCK} is a frequency selected by setting the CKS bit in the SPS and SMR registers.

Note 2. The transfer rate of 4800 bps is only supported in the SNOOZE mode.
Note that the SNOOZE mode is not supported when fHOCO is 48 MHz.

Note 3. f_{CLK} in each operating mode is as follows.:
HS (high-speed main) mode: 24 MHz (2.7 V ≤ V_{DD} ≤ 5.5 V)
16 MHz (2.4 V ≤ V_{DD} ≤ 5.5 V)
LS (low-speed main) mode: 8 MHz (1.8 V ≤ V_{DD} ≤ 5.5 V)
LP (low-power main) mode: 1 MHz (1.8 V ≤ V_{DD} ≤ 5.5 V)
LV (low-voltage main) mode: 4 MHz (1.6 V ≤ V_{DD} ≤ 5.5 V)

Caution Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

When P20 is used as SO10 pin

(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LP (Low-power main) mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t_{KCY1}	$t_{KCY1} \geq 4/f_{CLK}$	4.0 V ≤ V_{DD} ≤ 5.5 V	600		600		4000		1000		ns
			2.7 V ≤ V_{DD} ≤ 5.5 V	850		850						
			2.4 V ≤ V_{DD} ≤ 5.5 V	1000		1000						
			1.8 V ≤ V_{DD} ≤ 5.5 V	—		1500				1500		
			1.7 V ≤ V_{DD} ≤ 5.5 V	—		—		—		2000		
			1.6 V ≤ V_{DD} ≤ 5.5 V	—		—		—				
SCKp high-/low-level width	t_{KH1}, t_{KL1}	4.0 V ≤ V_{DD} ≤ 5.5 V		t_{KCY1}/2 - 12		t_{KCY1}/2 - 50		t_{KCY1}/2 - 50		t_{KCY1}/2 - 50		ns
		2.7 V ≤ V_{DD} ≤ 5.5 V		t_{KCY1}/2 - 18								
		2.4 V ≤ V_{DD} ≤ 5.5 V		t_{KCY1}/2 - 38								
		1.8 V ≤ V_{DD} ≤ 5.5 V		—								
		1.7 V ≤ V_{DD} ≤ 5.5 V		—		—		—		t_{KCY1}/2 - 100		
		1.6 V ≤ V_{DD} ≤ 5.5 V		—		—		—				
SIp setup time (to SCKp↑) Note 1	t_{SIK1}	4.0 V ≤ V_{DD} ≤ 5.5 V		44		110		110		110		ns
		2.7 V ≤ V_{DD} ≤ 5.5 V										
		2.4 V ≤ V_{DD} ≤ 5.5 V		75								
		1.8 V ≤ V_{DD} ≤ 5.5 V		—								
		1.7 V ≤ V_{DD} ≤ 5.5 V		—		—		—		220		
		1.6 V ≤ V_{DD} ≤ 5.5 V		—		—		—				
SIp hold time (from SCKp↑) Note 2	t_{KSI1}	2.4 V ≤ V_{DD} ≤ 5.5 V		19		19		19		19		ns
		1.8 V ≤ V_{DD} ≤ 5.5 V		—								
		1.6 V ≤ V_{DD} ≤ 5.5 V		—		—		—				
Delay time from SCKp↓ to SOp output Note 3	t_{KSO1}	C = 30 pF Note 4	2.4 V ≤ V_{DD} ≤ 5.5 V		150		250		250		300	ns
			1.8 V ≤ V_{DD} ≤ 5.5 V		—							
			1.6 V ≤ V_{DD} ≤ 5.5 V		—		—		—			

Note 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 4. C is the load capacitance of the SCKp and SOp output lines.

Caution Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remark 1. p: CSI number (p = 00, 01, 10 and 11), m: Unit number (m = 0), n: Channel number (n = 0 to 3), g: PIM and POM numbers (g = 0, 4 and 12)

Remark 2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,
n: Channel number (mn = 00 to 03))

When P20 is used as SO10 pin

(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LP (Low-power main) mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time Note 5	t_{KCY2}	4.0 V ≤ V_{DD} ≤ 5.5 V	f_{MCK} > 20 MHz	14/f_{MCK}		—		—		—		ns
			f_{MCK} ≤ 20 MHz	12/f_{MCK}		12/f_{MCK}		12/f_{MCK}		12/f_{MCK}		
		2.7 V ≤ V_{DD} ≤ 5.5 V	f_{MCK} > 16 MHz	14/f_{MCK} and 850		—		—		—		
			f_{MCK} ≤ 16 MHz	12/f_{MCK} and 850		12/f_{MCK}		12/f_{MCK}		12/f_{MCK}		
		2.4 V ≤ V_{DD} ≤ 5.5 V		12/f_{MCK} and 1000		12/f_{MCK}		12/f_{MCK}		12/f_{MCK}		
		1.8 V ≤ V_{DD} ≤ 5.5 V		—		12/f_{MCK}		12/f_{MCK}		12/f_{MCK}		
		1.7 V ≤ V_{DD} ≤ 5.5V		—		—		—		12/f_{MCK}		
		1.6 V ≤ V_{DD} ≤ 5.5 V		—		—		—				
SCKp high-/low-level width	t_{KH2}, t_{KL2}	4.0 V ≤ V_{DD} ≤ 5.5 V		t_{KCY2}/2 - 7		t_{KCY2}/2 - 7		t_{KCY2}/2 - 7		t_{KCY2}/2 - 7		ns
		2.7 V ≤ V_{DD} ≤ 5.5 V		t_{KCY2}/2 - 8		t_{KCY2}/2 - 8		t_{KCY2}/2 - 8		t_{KCY2}/2 - 8		
		1.8 V ≤ V_{DD} ≤ 5.5 V		—		t_{KCY2}/2 - 18		t_{KCY2}/2 - 18		t_{KCY2}/2 - 18		
		1.7 V ≤ V_{DD} ≤ 5.5 V		—		—		—		t_{KCY2}/2 - 66		
		1.6 V ≤ V_{DD} ≤ 5.5 V		—		—		—				
SIp setup time (to SCKp↑) Note 1	t_{SIK2}	2.7 V ≤ V_{DD} ≤ 5.5 V		1/f_{MCK} + 20		1/f_{MCK} + 30		1/f_{MCK} + 30		1/f_{MCK} + 30		ns
		1.8 V ≤ V_{DD} ≤ 5.5 V		1/f_{MCK} + 30								
		1.7 V ≤ V_{DD} ≤ 5.5 V		—		—		—		1/f_{MCK} + 40		
		1.6 V ≤ V_{DD} ≤ 5.5 V		—		—		—				
SIp hold time (from SCKp↑) Note 2	t_{KSI2}	2.5 V ≤ V_{DD} ≤ 5.5 V		1/f_{MCK} + 31		1/f_{MCK} + 31		1/f_{MCK} + 31		1/f_{MCK} + 31		ns
		1.8 V ≤ V_{DD} ≤ 5.5 V		—		1/f_{MCK} + 31		1/f_{MCK} + 31		1/f_{MCK} + 31		
		1.7 V ≤ V_{DD} ≤ 5.5 V		—		—		—		1/f_{MCK} + 250		
		1.6 V ≤ V_{DD} ≤ 5.5 V		—		—		—				
Delay time from SCKp↓ to SOp output Note 3	t_{KSO2}	C = 30 pF Note 4	2.7 V ≤ V_{DD} ≤ 5.5 V		2/f_{MCK} + 160		2/f_{MCK} + 260		2/f_{MCK} + 260		2/f_{MCK} + 260	ns
			2.4 V ≤ V_{DD} ≤ 5.5 V		2/f_{MCK} + 190							
			1.8 V ≤ V_{DD} ≤ 5.5 V		—							
			1.7 V ≤ V_{DD} ≤ 5.5 V		—		—		—		2/f_{MCK} + 320	
			1.6 V ≤ V_{DD} ≤ 5.5 V		—		—		—			

Note 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes “to SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

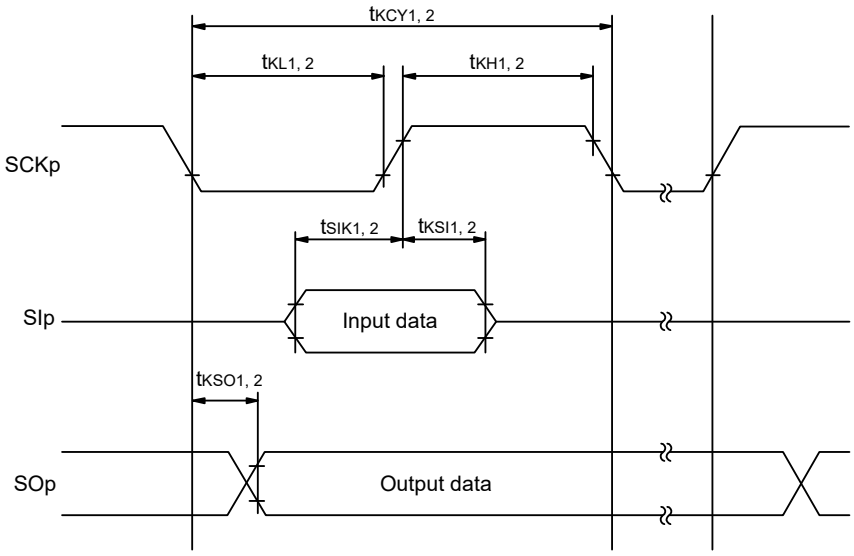
Note 4. C is the load capacitance of the SOp output lines.

Note 5. The maximum transfer rate when using the SNOOZE mode is 1 Mbps.

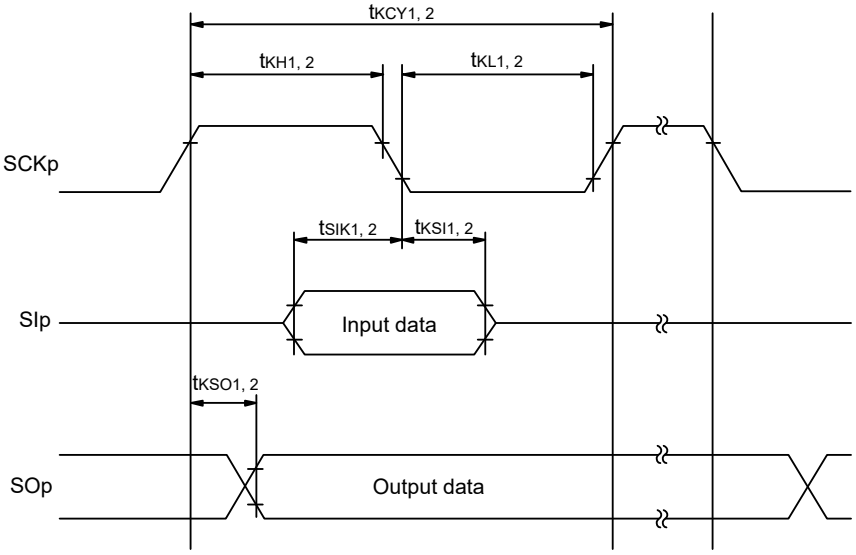
Caution Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remark 1. p: CSI number (p = 00, 01, 10 and 11), m: Unit number (m = 0), n: Channel number (n = 0 to 3), g: PIM and POM numbers (g = 0, 4 and 12)

CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Remark 1. p: CSI number (p = 00, 01, 10 and 11)
Remark 2. m: Unit number, n: Channel number (mn = 00 to 03)

(5) During communication at same potential (simplified I²C mode)

(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LP (Low-power main) mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLr clock frequency	f_{SCL}	2.7 V ≤ EV_{DD} ≤ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ		1000 Note 1		400 Note 1		250 Note 1		400 Note 1	kHz
		1.8 V ≤ EV_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ		400 Note 1							
		1.8 V ≤ EV_{DD} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ		300 Note 1		300 Note 1		250 Note 1		300 Note 1	
		1.7 V ≤ EV_{DD} < 1.8 V, C_b = 100 pF, R_b = 5 kΩ		250 Note 1		250 Note 1		250 Note 1		250 Note 1	
		1.6 V ≤ EV_{DD} < 1.8 V, C_b = 100 pF, R_b = 5 kΩ		—							
Hold time when SCLr = "L"	t_{LOW}	2.7 V ≤ EV_{DD} ≤ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ	475		1150		1150		1150		ns
		1.8 V ≤ EV_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	1150								
		1.8 V ≤ EV_{DD} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ	1550		1550		1550		1550		
		1.7 V ≤ EV_{DD} < 1.8 V, C_b = 100 pF, R_b = 5 kΩ	1850		1850		1850		1850		
		1.6 V ≤ EV_{DD} < 1.8 V, C_b = 100 pF, R_b = 5 kΩ	—								
Hold time when SCLr = "H"	t_{HIGH}	2.7 V ≤ EV_{DD} ≤ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ	475		1150		1150		1150		ns
		1.8 V ≤ EV_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	1150								
		1.8 V ≤ EV_{DD} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ	1550		1550		1550		1550		
		1.7 V ≤ EV_{DD} < 1.8 V, C_b = 100 pF, R_b = 5 kΩ	1850		1850		1850		1850		
		1.6 V ≤ EV_{DD} < 1.8 V, C_b = 100 pF, R_b = 5 kΩ	—								
Data setup time (reception)	$t_{SU:DAT}$	2.7 V ≤ EV_{DD} ≤ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ	1/f_{MCK} + 85 Note 2		1/f_{MCK} + 145 Note 2		1/f_{MCK} + 145 Note 2		1/f_{MCK} + 145 Note 2		ns
		1.8 V ≤ EV_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	1/f_{MCK} + 145 Note 2								
		1.8 V ≤ EV_{DD} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ	1/f_{MCK} + 230 Note 2		1/f_{MCK} + 230 Note 2		1/f_{MCK} + 230 Note 2		1/f_{MCK} + 230 Note 2		
		1.7 V ≤ EV_{DD} < 1.8 V, C_b = 100 pF, R_b = 5 kΩ	1/f_{MCK} + 290 Note 2		1/f_{MCK} + 290 Note 2		1/f_{MCK} + 290 Note 2		1/f_{MCK} + 290 Note 2		
		1.6 V ≤ EV_{DD} < 1.8 V, C_b = 100 pF, R_b = 5 kΩ	—		—		—				
Data hold time (transmission)	$t_{HD:DAT}$	2.7 V ≤ EV_{DD} ≤ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ	0	305	0	305	0	305	0	305	ns
		1.8 V ≤ EV_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ		355		355		355		355	
		1.8 V ≤ EV_{DD} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ		405		405		405		405	
		1.7 V ≤ EV_{DD} < 1.8 V, C_b = 100 pF, R_b = 5 kΩ									
		1.6 V ≤ EV_{DD} < 1.8 V, C_b = 100 pF, R_b = 5 kΩ	—	—							

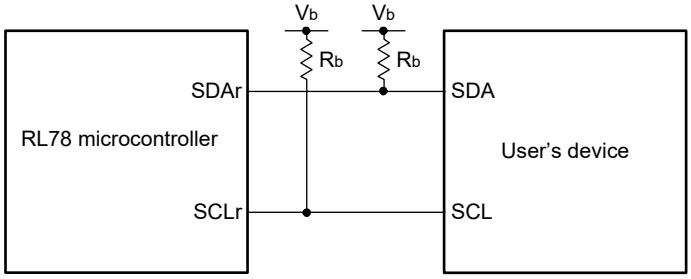
Note 1. The value must be equal to or less than f_{MCK}/4.

Note 2. Use it with $EV_{DD} \geq V_b$.

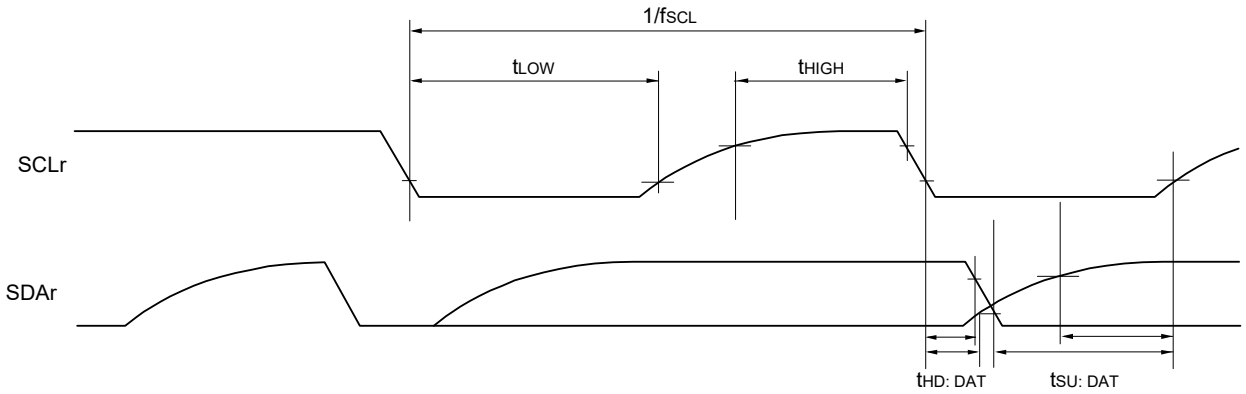
Note 3. Set the f_{MCK} value to keep the hold time of SCLr = "L" and SCLr = "H".

Caution Select the TTL input buffer and the N-ch open drain output (EV_{DD} tolerance) mode for the SDAr pin and the N-ch open drain output (EV_{DD} tolerance) mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

Simplified I²C mode connection diagram (during communication at different potential)



Simplified I²C mode serial transfer timing (during communication at different potential)

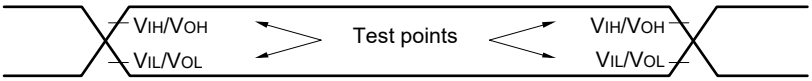


Remark 1. R_b[Ω]: Communication line (SDAr, SCLr) pull-up resistance, C_b[F]: Communication line (SDAr, SCLr) load capacitance, V_b[V]: Communication line voltage

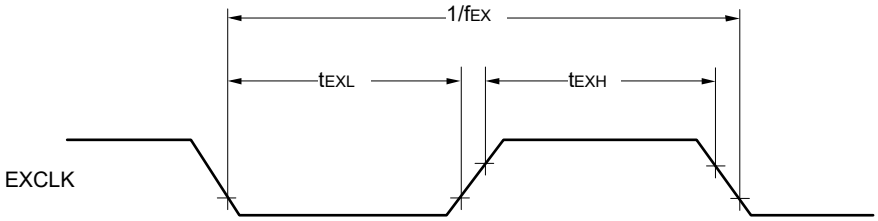
Remark 2. r: IIC number (r = 00, 01, 10 and 11), g: PIM, POM number (g = 0, 3 and 5)

Remark 3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0), n: Channel number (n = 0 to 3), mn = 00 to 03)

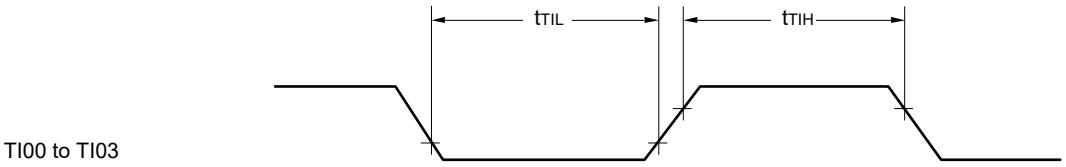
AC Timing Test Points

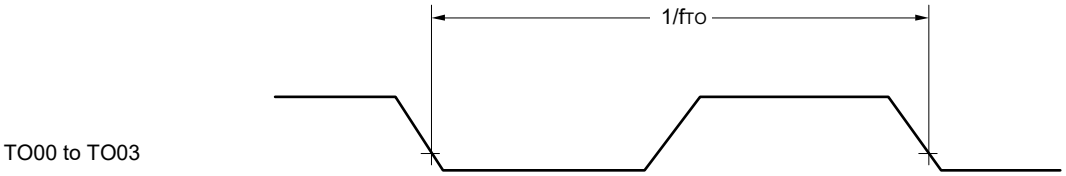


External System Clock Timing

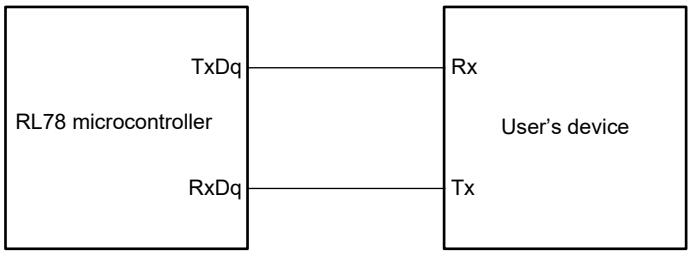


TI/TO Timing

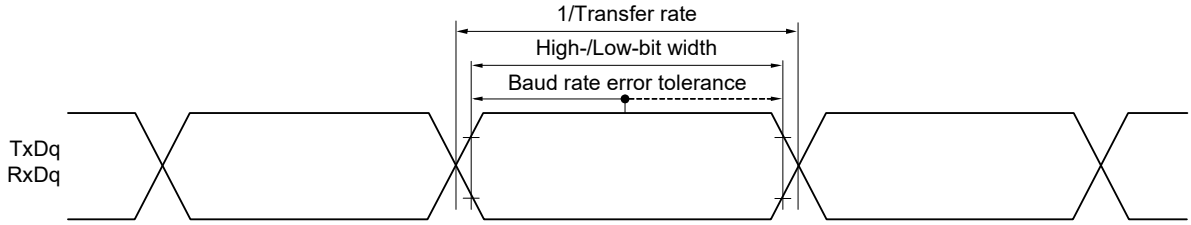




UART mode connection diagram (during communication at same potential)



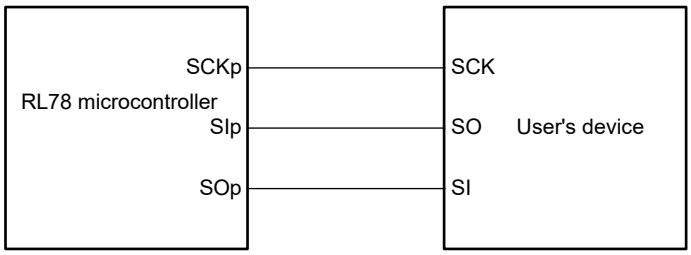
UART mode bit width (during communication at same potential) (reference)



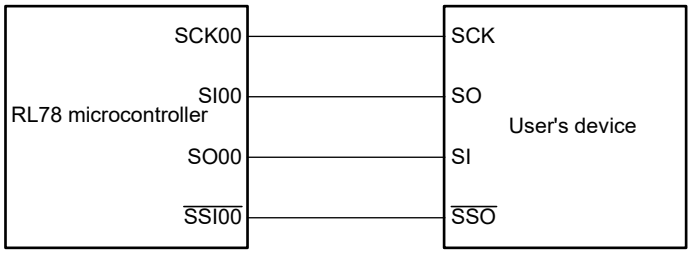
Remark 1. q: UART number (q = 0 and 1), g: PIM and POM number (g = 0, 2, 3 and 5)

Remark 2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03)

CSI mode connection diagram (during communication at same potential)

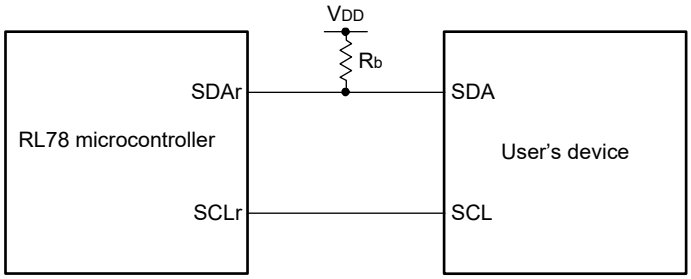


CSI mode connection diagram (during communication at same potential)
(Slave Transmission of slave select input function (CSI00))

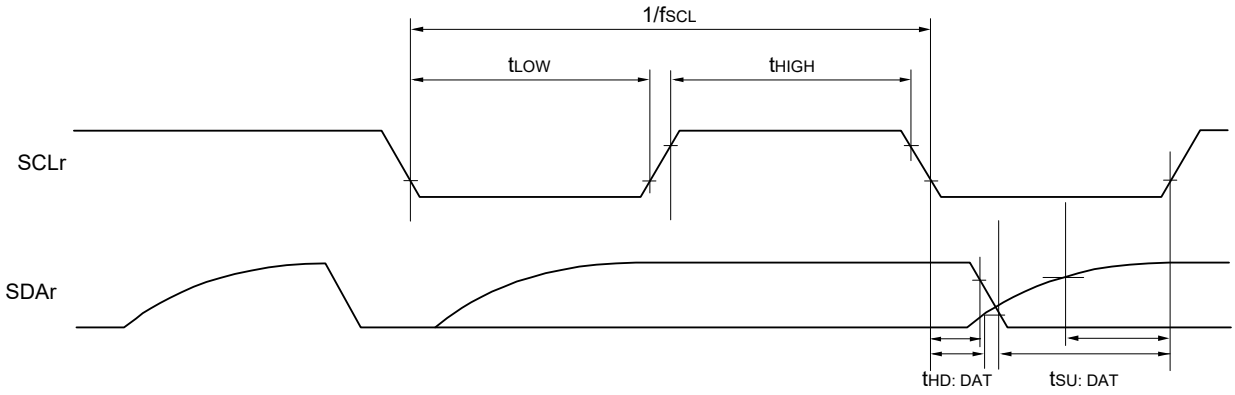


Remark p: CSI number (p = 00, 01, 10 and 11)

Simplified I²C mode connection diagram (during communication at same potential)



Simplified I²C mode serial transfer timing (during communication at same potential)

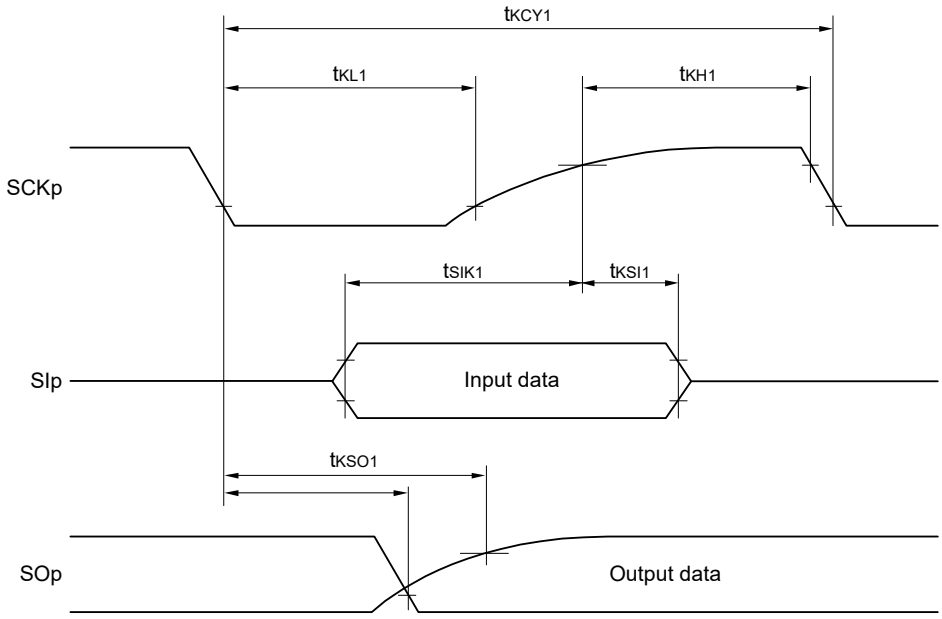


Remark 1. R_b[Ω]: Communication line (SDAr) pull-up resistance, C_b[F]: Communication line (SDAr, SCLr) load capacitance

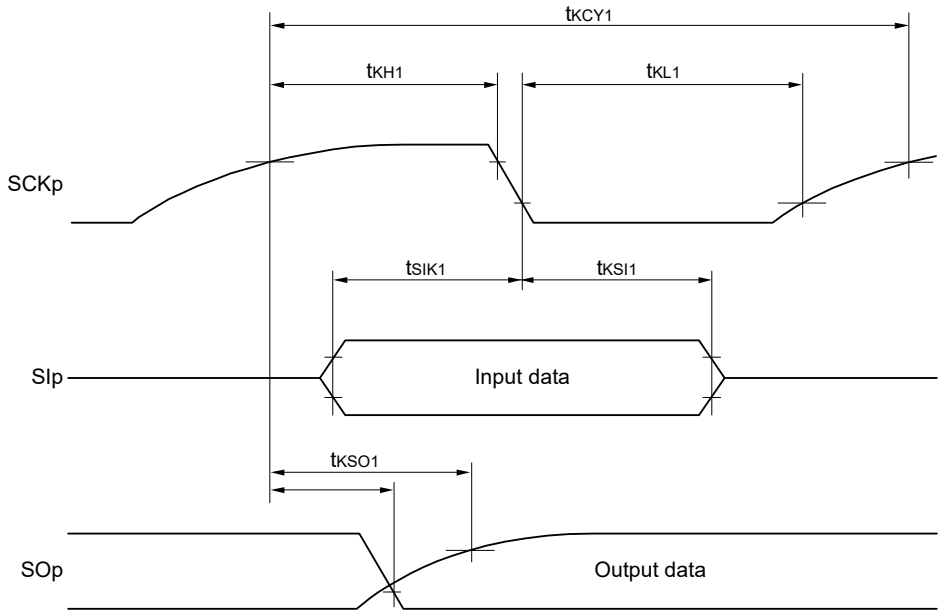
Remark 2. r: IIC number (r = 00, 01, 10 and 11), g: PIM number (g = 0, 3 and 5), h: POM number (h = 0, 3 and 5)

Remark 3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0), n: Channel number (n = 0 to 3), mn = 00 to 03)

CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Remark p: CSI number (p = 00, 01, 10 and 11), m: Unit number (m = 0), n: Channel number (n = 0 to 3), g: PIM and POM numbers (g = 0, 2, 3 to 5 and 12)

(7) Communication at different potential (1.8 V, 2.5 V, 3.0 V) (CSI mode) (slave mode, SCKp... external clock input)

(T_A = -40 to +105°C, 2.4 V ≤ EV_{DD} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		Unit
				MIN.	MAX.	
SCKp cycle time Note 1	t_{KCY2}	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V	20 MHz < f_{MCK} ≤ 24 MHz	24/f_{MCK}		ns
			8 MHz < f_{MCK} ≤ 20 MHz	20/f_{MCK}		ns
			4 MHz < f_{MCK} ≤ 8 MHz	16/f_{MCK}		ns
			f_{MCK} ≤ 4 MHz	12/f_{MCK}		ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V	20 MHz < f_{MCK} ≤ 24 MHz	32/f_{MCK}		ns
			16 MHz < f_{MCK} ≤ 20 MHz	28/f_{MCK}		ns
			8 MHz < f_{MCK} ≤ 16 MHz	24/f_{MCK}		ns
			4 MHz < f_{MCK} ≤ 8 MHz	16/f_{MCK}		ns
			f_{MCK} ≤ 4 MHz	12/f_{MCK}		ns
		2.4 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2	20 MHz < f_{MCK} ≤ 24 MHz	72/f_{MCK}		ns
			16 MHz < f_{MCK} ≤ 20 MHz	64/f_{MCK}		ns
			8 MHz < f_{MCK} ≤ 16 MHz	52/f_{MCK}		ns
			4 MHz < f_{MCK} ≤ 8 MHz	32/f_{MCK}		ns
			f_{MCK} ≤ 4 MHz	20/f_{MCK}		ns
SCKp high-/low-level width	t_{KH2}, t_{KL2}	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V		t_{KCY2}/2 - 24		ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V		t_{KCY2}/2 - 36		ns
		2.4 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2		t_{KCY2}/2 - 100		ns
SIp setup time (to SCKp↑) Note 3	t_{SIK2}	2.7 V ≤ EV_{DD} ≤ 5.5 V, 2.3 V ≤ V_b ≤ 4.0 V		1/f_{MCK} + 40		ns
		2.4 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2		1/f_{MCK} + 60		ns
SIp hold time (from SCKp↑) Note 4	t_{KSI2}			1/f_{MCK} + 62		ns
Delay time from SCKp↓ to SOp output Note 5	t_{KSO2}	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V C_b = 30 pF, R_b = 1.4 kΩ			2/f_{MCK} + 240	ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V C_b = 30 pF, R_b = 2.7 kΩ			2/f_{MCK} + 428	ns
		2.4 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2 C_b = 30 pF, R_b = 5.5 kΩ			2/f_{MCK} + 1146	ns

(**Notes**, **Caution** and **Remarks** are listed on the next page.)

3.6.7 LVD circuit characteristics

(1) LVD Detection Voltage of Reset Mode and Interrupt Mode

(T_A = -40 to +105°C, $V_{PDR} \leq EV_{DD} = V_{DD} \leq$.5.5 V, V_{SS} = 0 V)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	Supply voltage level	V_{LVD0}	Power supply rise time	3.90	4.06	4.22	V
			Power supply fall time	3.83	3.98	4.13	V
		V_{LVD1}	Power supply rise time	3.60	3.75	3.90	V
			Power supply fall time	3.53	3.67	3.81	V
		V_{LVD2}	Power supply rise time	3.01	3.13	3.25	V
			Power supply fall time	2.94	3.06	3.18	V
		V_{LVD3}	Power supply rise time	2.90	3.02	3.14	V
			Power supply fall time	2.85	2.96	3.07	V
		V_{LVD4}	Power supply rise time	2.81	2.92	3.03	V
			Power supply fall time	2.75	2.86	2.97	V
		V_{LVD5}	Power supply rise time	2.71	2.81	2.92	V
			Power supply fall time	2.64	2.75	2.86	V
		V_{LVD6}	Power supply rise time	2.61	2.71	2.81	V
			Power supply fall time	2.55	2.65	2.75	V
		V_{LVD7}	Power supply rise time	2.51	2.61	2.71	V
			Power supply fall time	2.45	2.55	2.65	V
Minimum pulse width		t_{LW}		300			μs
Detection delay time						300	μs

(2) LVD Detection Voltage of Interrupt & Reset Mode

(T_A = -40 to +105°C, $V_{PDR} \leq EV_{DD} \leq V_{DD} \leq$ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Interrupt and reset mode	V_{LVDD0}	V_{POC0}, V_{POC1}, V_{POC2} = 0, 1, 1, falling reset voltage		2.64	2.75	2.86	V
	V_{LVDD1}	LVIS0, LVIS1 = 1, 0	Rising release reset voltage	2.81	2.92	3.03	V
			Falling interrupt voltage	2.75	2.86	2.97	V
	V_{LVDD2}	LVIS0, LVIS1 = 0, 1	Rising release reset voltage	2.90	3.02	3.14	V
			Falling interrupt voltage	2.85	2.96	3.07	V
	V_{LVDD3}	LVIS0, LVIS1 = 0, 0	Rising release reset voltage	3.90	4.06	4.22	V
			Falling interrupt voltage	3.83	3.98	4.13	V

3.6.8 Power supply voltage rising slope characteristics

(T_A = -40 to +105°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Power supply voltage rising slope	S_{VDD}				54	V/ms

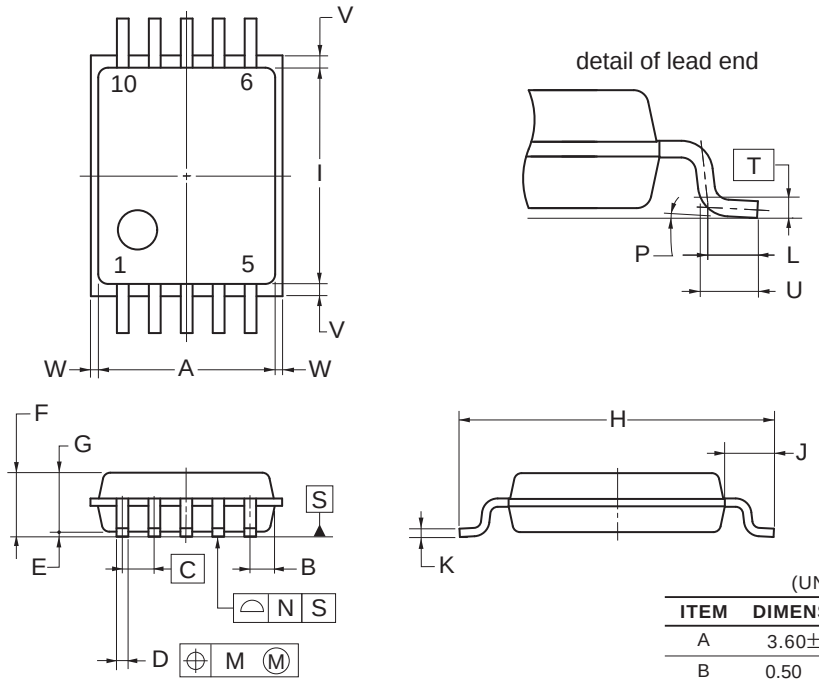
Caution Make sure to keep the internal reset state by the LVD circuit or an external reset until V_{DD} reaches the operating voltage range shown in 3.4 AC Characteristics.

4. PACKAGE DRAWINGS

4.1 10-pin products

R5F1051AGSP, R5F1051AASP

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LSSOP10-4.4x3.6-0.65	PLSP0010JA-A	P10MA-65-CAC-2	0.05



(UNIT:mm)

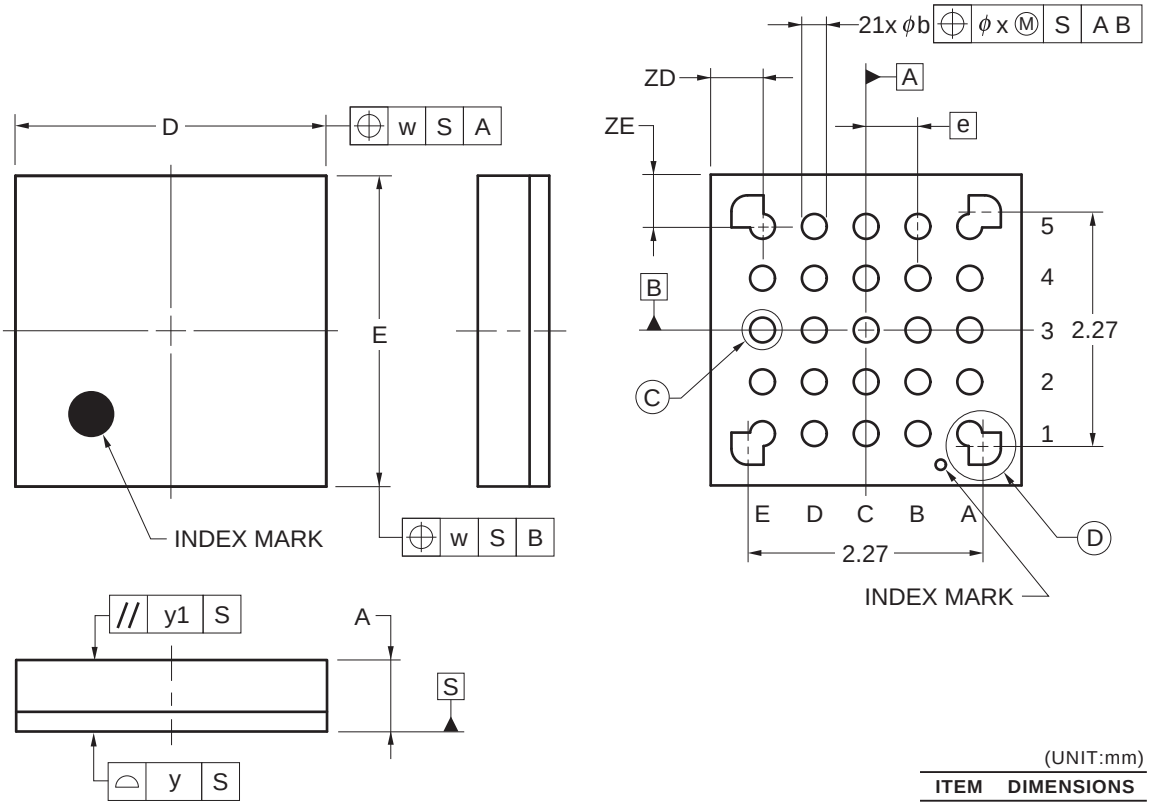
ITEM	DIMENSIONS
A	3.60±0.10
B	0.50
C	0.65 (T.P.)
D	0.24±0.08
E	0.10±0.05
F	1.45 MAX.
G	1.20±0.10
H	6.40±0.20
I	4.40±0.10
J	1.00±0.20
K	$0.17^{+0.08}_{-0.07}$
L	0.50
M	0.13
N	0.10
P	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
T	0.25 (T.P.)
U	0.60±0.15
V	0.25 MAX.
W	0.15 MAX.

NOTE
Each lead centerline is located within 0.13 mm of its true position (T.P.) at maximum material condition.

4.5 25-pin products

R5F1058AGLA, R5F1058AALA

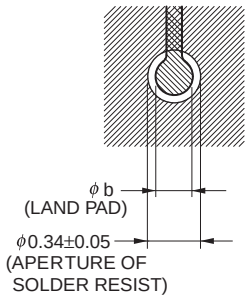
JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-WFLGA25-3x3-0.50	PWLG0025KA-A	P25FC-50-2N2-2	0.01



(UNIT:mm)

ITEM	DIMENSIONS
D	3.00±0.10
E	3.00±0.10
w	0.20
e	0.50
A	0.69±0.07
b	0.24±0.05
x	0.05
y	0.08
y1	0.20
ZD	0.50
ZE	0.50

DETAIL OF Ⓒ PART



DETAIL OF Ⓓ PART