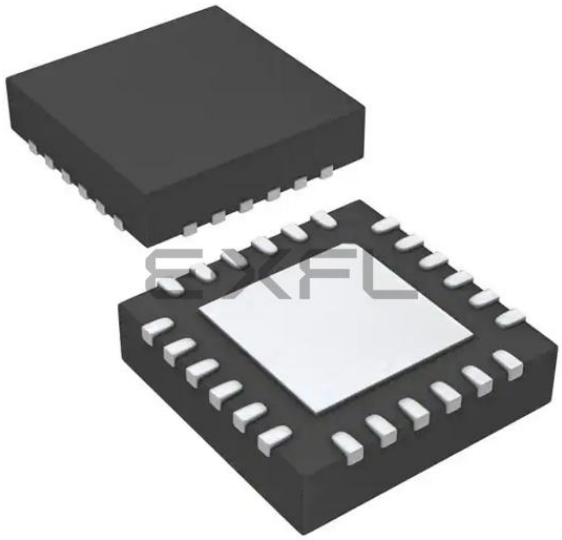

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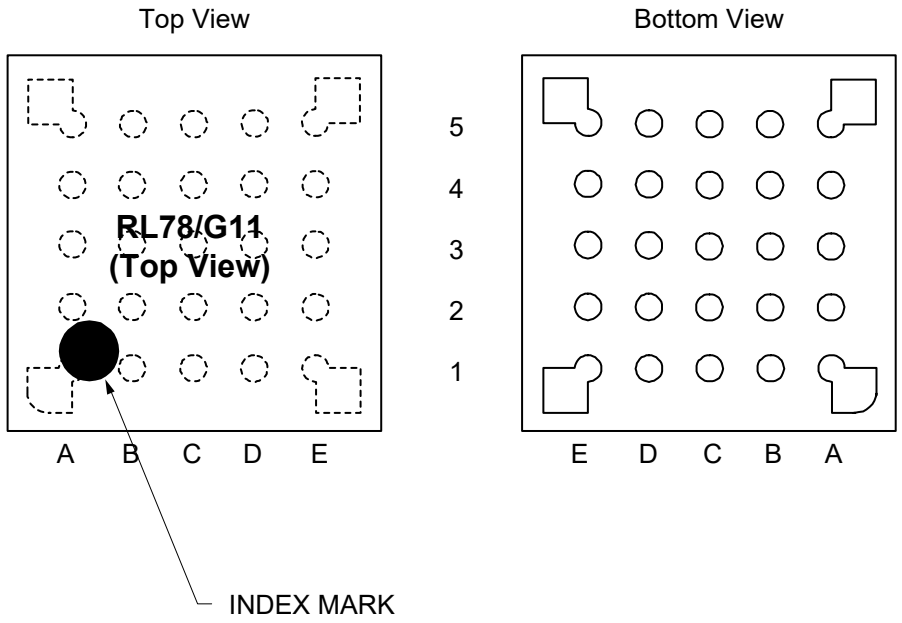
Details	
Product Status	Obsolete
Core Processor	RL78
Core Size	16-Bit
Speed	24MHz
Connectivity	CSI, I²C, UART/USART
Peripherals	LVD, POR, WDT
Number of I/O	21
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	1.5K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 11x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	24-WFQFN Exposed Pad
Supplier Device Package	24-HWQFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f1057aana-u0

1.3.5 25-pin products

• 25-pin plastic WFLGA (3 × 3 mm, 0.5 mm pitch)



	A	B	C	D	E	
5	P40/TOOL0/TO03/(PCLBUZ0)/SCK10/SCL10/VCOUT0/VCOUT1/INTFO/(SCLA1)	P125/$\overline{\text{RESET}}$/INTP9	P01/ANI16/INTP5/SO10/TxD1	P20/ANI0/AVREFP/IVREF1/(SO10/TxD1)	P21/ANI1/AVREFM/IVREF0	5
4	P122/X2/EXCLK/(SI10/RxD1)/(TI02)/INTP1	P137/INTP0/$\overline{\text{SSI00}}$/(TI03)	P00/ANI17/PCLBUZ1/TI03/(VCOUT1)/SI10/RxD1/SDA10/(SDAA1)	P22/ANI2/PGAI/IVCMP0	P23/ANI3/ANO1/PGAGND	4
3	P121/X1/(TI01)/INTP2/(SI01)	V_{DD}	EV_{DD}	P33/ANI18/IVCMP1/(INTP11)/(SCLA1)	P32/ANI19/SO11/(INTP10)/(VCOUT1)/(SDAA1)	3
2	REGC	V_{SS}	P30/ANI21/KR1/TI00/TO01/INTP3/SCK11/SCL11/(TxD0)/PCLBUZ0/TKBO1/(SDAA0)	P31/ANI20/KR0/TI01/TO00/INTP4/TKBO0/(RxD0)/SI11/SDA11/(SCLA0)	P56/ANI22/KR2/SCK00/SCL00/(SO11)/INTP10/(TO03)/(INTFO)/SCLA1	2
1	P51/KR7/INTP8/(TI02)/(TO02)/SCK01/SCL01/(TxD0)	P52/KR6/INTP7/SI01/SDA01/(RxD0)/(SDAA0)	P53/KR5/INTP6/SO01/SDAA0	P54/KR4/SO00/TxD0/TOOLTXD/(TI03)/(TO03)/SCLA0	P55/KR3/SI00/RxD0/SDA00/TOOLRXD/TI02/TO02/INTP11/(VCOUT0)/SDAA1	1
	A	B	C	D	E	

Caution Connect the REGC pin to Vss pin via a capacitor (0.47 to 1 μF).

Remark 1. For pin identification, see **1.4 Pin Identification**.

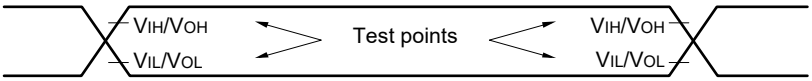
Remark 2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0 to 3 (PIOR0 to PIOR3).

(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = 0 V) **(2/2)**

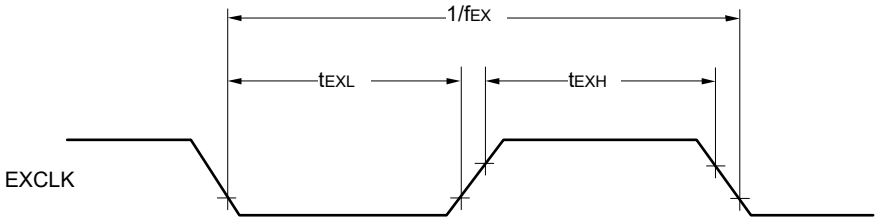
	Items	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
<R>	TO00 to TO03, TKBO0, and TKBO1 output frequency Note	f_{TO}	TO00 to TO03, TKBO0, and TKBO1 (in the case of output from port pins other than P20)	HS (high-speed main) mode	4.0 V ≤ EV_{DD} ≤ 5.5 V			12	MHz
					2.7 V ≤ EV_{DD} < 4.0 V			8	
					1.8 V ≤ EV_{DD} < 2.7 V			4	
					1.6 V ≤ EV_{DD} < 1.8 V			2	
				LS (low-speed main) mode	1.8 V ≤ EV_{DD} ≤ 5.5 V			4	
					1.6 V ≤ EV_{DD} < 1.8 V			2	
				LP (low-power main) mode	1.8 V ≤ EV_{DD} ≤ 5.5 V			0.5	
				LV (low-voltage main) mode	1.6 V ≤ EV_{DD} ≤ 5.5 V			2	
			TKBO1 (in the case of output from P20)	HS (high-speed main) mode	4.0 V ≤ V_{DD} ≤ 5.5 V			1.5	MHz
					2.7 V ≤ V_{DD} < 4.0 V			1.2	
					2.4 V ≤ V_{DD} < 2.7 V			1	
				LS (low-speed main) mode	4.0 V ≤ V_{DD} ≤ 5.5 V			1.5	
					2.7 V ≤ V_{DD} < 4.0 V			1.2	
					2.4 V ≤ V_{DD} < 2.7 V			1	
					1.8 V ≤ V_{DD} < 2.4 V			0.75	
				LP (low-power main) mode	1.8 V ≤ V_{DD} ≤ 5.5 V			0.5	
				LV (low-voltage main) mode	4.0 V ≤ V_{DD} ≤ 5.5 V			1.5	
					2.7 V ≤ V_{DD} < 4.0 V			1.2	
					2.4 V ≤ V_{DD} < 2.7 V			1	
					1.8 V ≤ V_{DD} < 2.4 V			0.75	
					1.6 V ≤ V_{DD} < 1.8 V			0.5	
	PCLBUZ0, PCLBUZ1 output frequency	f_{PCL}	HS (high-speed main) mode		4.0 V ≤ EV_{DD} ≤ 5.5 V			16	MHz
					2.7 V ≤ EV_{DD} < 4.0 V			8	
					1.8 V ≤ EV_{DD} < 2.7 V			4	
					1.6 V ≤ EV_{DD} < 1.8 V			2	
			LS (low-speed main) mode		1.8 V ≤ EV_{DD} ≤ 5.5 V			4	
					1.6 V ≤ EV_{DD} < 1.8 V			2	
			LP (low-power main) mode		1.6 V ≤ EV_{DD} ≤ 5.5 V			1	
			LV (low-voltage main) mode		1.8 V ≤ EV_{DD} ≤ 5.5 V			4	
					1.6 V ≤ EV_{DD} < 1.8 V			2	
<R>	Interrupt input high-/low-level width	t_{INTH}, t_{INTL}	INTP0 to INTP2, INTP9		1.6 V ≤ V_{DD} ≤ 5.5 V	1			µs
			INTP3 to INTP8, INTP10, INTP11		1.6 V ≤ EV_{DD} ≤ 5.5 V	1			
	Key interrupt input low-level width	t_{KR}	KR0 to KR7		1.8 V ≤ EV_{DD} ≤ 5.5 V	250			ns
					1.6 V ≤ EV_{DD} < 1.8 V	1			µs
	$\overline{RESET}$ low-level width	t_{RSL}				10			µs

Note When duty is 50%.

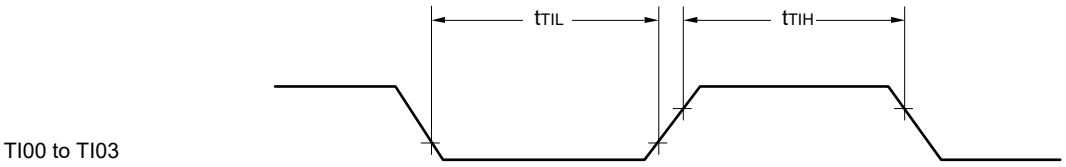
AC Timing Test Points

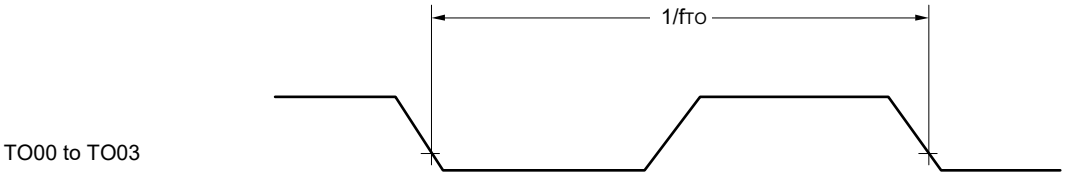


External System Clock Timing



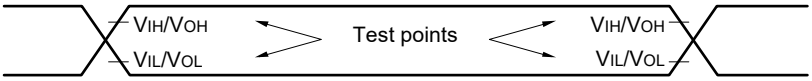
TI/TO Timing



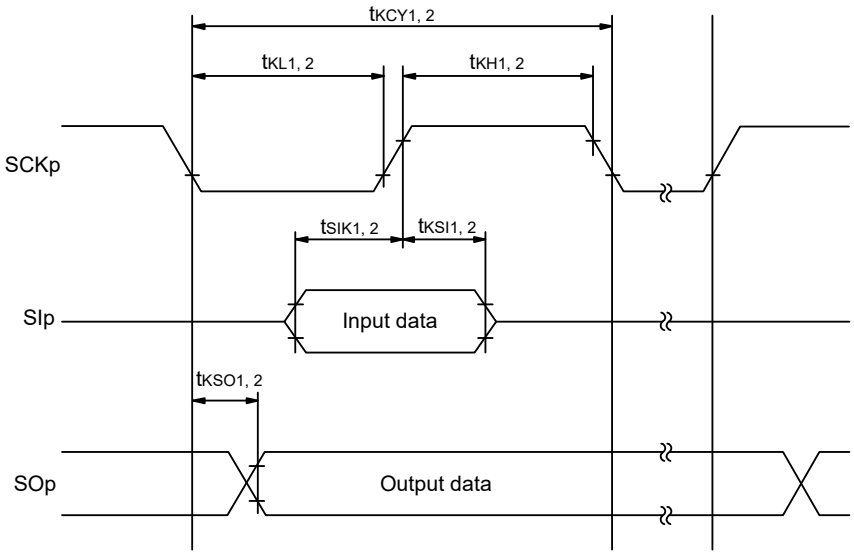


2.5 Peripheral Functions Characteristics

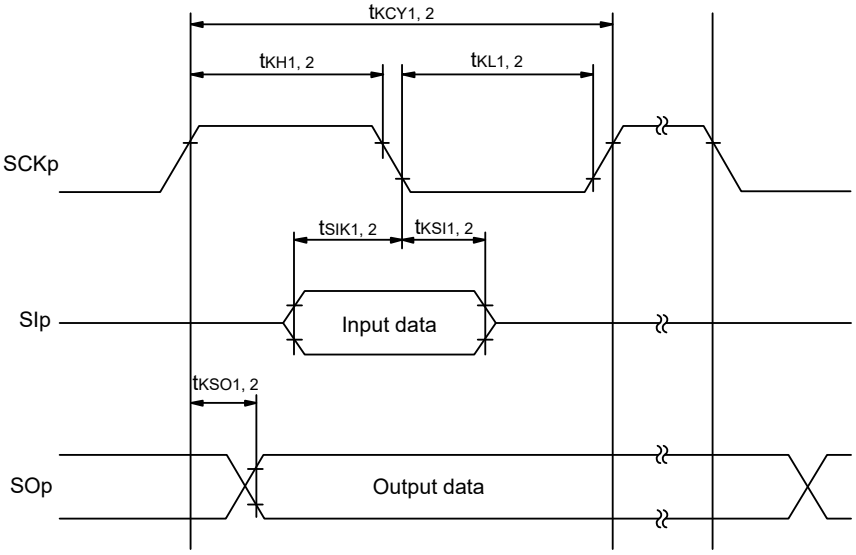
AC Timing Test Points



CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Remark 1. p: CSI number (p = 00, 01, 10 and 11)
Remark 2. m: Unit number, n: Channel number (mn = 00 to 03)

2.5.2 Serial interface IICA

(1) I^2C standard mode

(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) mode		LS (low-speed main) mode		LP (Low-power main) mode		LV (low-voltage main) mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	f_{SCL}	Standard mode: f_{CLK} ≥ 1 MHz	2.7 V ≤ EV_{DD} ≤ 5.5 V	0	100	0	100	0	100	0	100	kHz
			1.8 V ≤ EV_{DD} ≤ 5.5 V	0	100	0	100	0	100	0	100	kHz
			1.7 V ≤ EV_{DD} ≤ 5.5 V	0	100	0	100	0	100	0	100	kHz
			1.6 V ≤ EV_{DD} ≤ 5.5 V	—		0	100	0	100	0	100	kHz
Setup time of restart condition	$t_{SU: STA}$	2.7 V ≤ EV_{DD} ≤ 5.5 V		4.7		4.7		4.7		4.7		µs
		1.8 V ≤ EV_{DD} ≤ 5.5 V		4.7		4.7		4.7		4.7		µs
		1.7 V ≤ EV_{DD} ≤ 5.5 V		4.7		4.7		4.7		4.7		µs
		1.6 V ≤ EV_{DD} ≤ 5.5 V		—		4.7		4.7		4.7		µs
Hold time Note 1	$t_{HD: STA}$	2.7 V ≤ EV_{DD} ≤ 5.5 V		4.0		4.0		4.0		4.0		µs
		1.8 V ≤ EV_{DD} ≤ 5.5 V		4.0		4.0		4.0		4.0		µs
		1.7 V ≤ EV_{DD} ≤ 5.5 V		4.0		4.0		4.0		4.0		µs
		1.6 V ≤ EV_{DD} ≤ 5.5 V		—		4.0		4.0		4.0		µs
Hold time when SCLA0 = "L"	t_{LOW}	2.7 V ≤ EV_{DD} ≤ 5.5 V		4.7		4.7		4.7		4.7		µs
		1.8 V ≤ EV_{DD} ≤ 5.5 V		4.7		4.7		4.7		4.7		µs
		1.7 V ≤ EV_{DD} ≤ 5.5 V		4.7		4.7		4.7		4.7		µs
		1.6 V ≤ EV_{DD} ≤ 5.5 V		—		4.7		4.7		4.7		µs
Hold time when SCLA0 = "H"	t_{HIGH}	2.7 V ≤ EV_{DD} ≤ 5.5 V		4.0		4.0		4.0		4.0		µs
		1.8 V ≤ EV_{DD} ≤ 5.5 V		4.0		4.0		4.0		4.0		µs
		1.7 V ≤ EV_{DD} ≤ 5.5 V		4.0		4.0		4.0		4.0		µs
		1.6 V ≤ EV_{DD} ≤ 5.5 V		—		4.0		4.0		4.0		µs
Data setup time (reception)	$t_{SU: DAT}$	2.7 V ≤ EV_{DD} ≤ 5.5 V		250		250		250		250		ns
		1.8 V ≤ EV_{DD} ≤ 5.5 V		250		250		250		250		ns
		1.7 V ≤ EV_{DD} ≤ 5.5 V		250		250		250		250		ns
		1.6 V ≤ EV_{DD} ≤ 5.5 V		—		250		250		250		ns
Data hold time (transmission) Note 2	$t_{HD: DAT}$	2.7 V ≤ EV_{DD} ≤ 5.5 V		0	3.45	0	3.45	0	3.45	0	3.45	µs
		1.8 V ≤ EV_{DD} ≤ 5.5 V		0	3.45	0	3.45	0	3.45	0	3.45	µs
		1.7 V ≤ EV_{DD} ≤ 5.5 V		0	3.45	0	3.45	0	3.45	0	3.45	µs
		1.6 V ≤ EV_{DD} ≤ 5.5 V		—		0	3.45	0	3.45	0	3.45	µs
Setup time of stop condition	$t_{SU: STO}$	2.7 V ≤ EV_{DD} ≤ 5.5 V		4.0		4.0		4.0		4.0		µs
		1.8 V ≤ EV_{DD} ≤ 5.5 V		4.0		4.0		4.0		4.0		µs
		1.7 V ≤ EV_{DD} ≤ 5.5 V		4.0		4.0		4.0		4.0		µs
		1.6 V ≤ EV_{DD} ≤ 5.5 V		—		4.0		4.0		4.0		µs
Bus-free time	t_{BUF}	2.7 V ≤ EV_{DD} ≤ 5.5 V		4.7		4.7		4.7		4.7		µs
		1.8 V ≤ EV_{DD} ≤ 5.5 V		4.7		4.7		4.7		4.7		µs
		1.7 V ≤ EV_{DD} ≤ 5.5 V		4.7		4.7		4.7		4.7		µs
		1.6 V ≤ EV_{DD} ≤ 5.5 V		—		4.7		4.7		4.7		µs

Note 1. The first clock pulse is generated after this period when the start/restart condition is detected.

Note 2. The maximum value (MAX.) of $t_{HD: DAT}$ is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

Caution The values in the above table are applied even when bit 2 (PIOR02) in the peripheral I/O redirection register 0 (PIOR0) is 1. At this time, the pin characteristics (I_{OH1}, I_{OL1}, V_{OH1}, V_{OL1}) must satisfy the values in the redirect destination.

(3) I^2C fast mode plus

(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) mode		LS (low-speed main) mode		LP (Low-power main) mode		LV (low-voltage main) mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	f_{SCL}	Fast mode plus: f_{CLK} ≥ 10 MHz	2.7 V ≤ EV_{DD} ≤ 5.5 V	0	1000	—		—		—		kHz
Setup time of restart condition	$t_{SU: STA}$	2.7 V ≤ EV_{DD} ≤ 5.5 V		0.26		—		—		—		μs
Hold time Note 1	$t_{HD: STA}$	2.7 V ≤ EV_{DD} ≤ 5.5 V		0.26		—		—		—		μs
Hold time when SCLA0 = "L"	t_{LOW}	2.7 V ≤ EV_{DD} ≤ 5.5 V		0.5		—		—		—		μs
Hold time when SCLA0 = "H"	t_{HIGH}	2.7 V ≤ EV_{DD} ≤ 5.5 V		0.26		—		—		—		μs
Data setup time (reception)	$t_{SU: DAT}$	2.7 V ≤ EV_{DD} ≤ 5.5 V		50		—		—		—		ns
Data hold time (transmission) Note 2	$t_{HD: DAT}$	2.7 V ≤ EV_{DD} ≤ 5.5 V		0	0.45	—		—		—		μs
Setup time of stop condition	$t_{SU: STO}$	2.7 V ≤ EV_{DD} ≤ 5.5 V		0.26		—		—		—		μs
Bus-free time	t_{BUF}	2.7 V ≤ EV_{DD} ≤ 5.5 V		0.5		—		—		—		μs

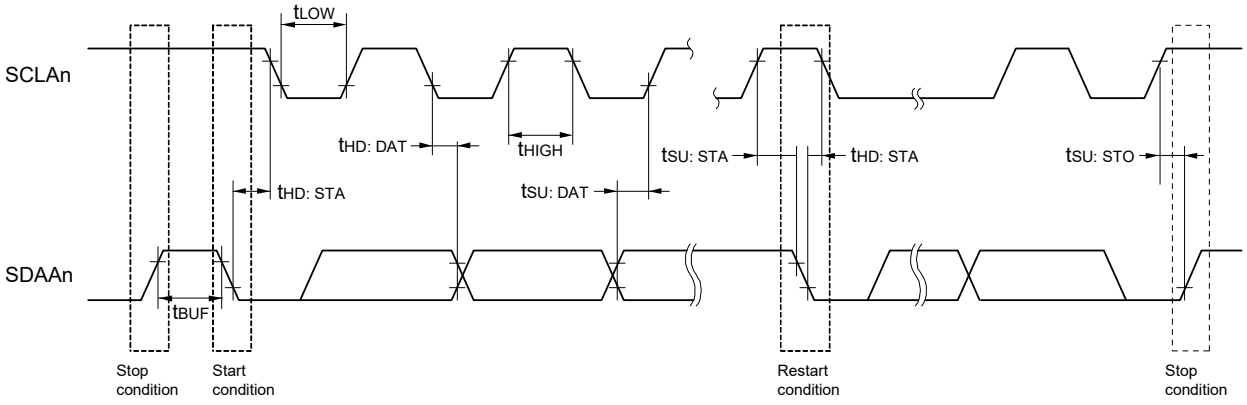
Note 1. The first clock pulse is generated after this period when the start/restart condition is detected.

Note 2. The maximum value (MAX.) of $t_{HD: DAT}$ is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

Caution The values in the above table are applied even when bit 2 (PIOR02) in the peripheral I/O redirection register 0 (PIOR0) is 1. At this time, the pin characteristics (I_{OH1}, I_{OL1}, V_{OH1}, V_{OL1}) must satisfy the values in the redirect destination.

Remark The maximum value of C_b (communication line capacitance) and the value of R_b (communication line pull-up resistor) at that time in each mode are as follows.
Fast mode plus: C_b = 120 pF, R_b = 1.1 kΩ

IICA serial transfer timing



Remark n = 0, 1

2.6 Analog Characteristics

2.6.1 A/D converter characteristics

Classification of A/D converter characteristics

Input channel \ Reference Voltage	Reference voltage (+) = AV_{REFP} Reference voltage (-) = AV_{REFM}	Reference voltage (+) = V_{DD} Reference voltage (-) = V_{SS}	Reference voltage (+) = V_{BGR} Reference voltage (-)= AV_{REFM}
ANI0 to ANI3	Refer to **2.6.1 (1)**.	Refer to **2.6.1 (3)**.	Refer to **2.6.1 (4)**.
ANI16 to ANI22	Refer to **2.6.1 (2)**.		
Internal reference voltage Temperature sensor output voltage	Refer to **2.6.1 (1)**.		—

(1) When reference voltage (+) = AV_{REFP}/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (-) = AV_{REFM}/ANI1 (ADREFM = 1), target pin: ANI2 and ANI3, internal reference voltage, and temperature sensor output voltage

(T_A = -40 to +85°C, 1.6 V ≤ AV_{REFP} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V, Reference voltage (+) = AV_{REFP}, Reference voltage (-) = AV_{REFM} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error Note 1	AINL	10-bit resolution AV_{REFP} = V_{DD} Note 3	1.8 V ≤ AV_{REFP} ≤ 5.5 V		1.2	±3.5	LSB
			1.6 V ≤ AV_{REFP} ≤ 5.5 V Note 4		1.2	±7.0	LSB
Conversion time	tCONV	10-bit resolution Target pin: ANI2 and ANI3	3.6 V ≤ V_{DD} ≤ 5.5 V	2.125		39	μs
			2.7 V ≤ V_{DD} ≤ 5.5 V	3.1875		39	μs
			1.8 V ≤ V_{DD} ≤ 5.5 V	17		39	μs
			1.6 V ≤ V_{DD} ≤ 5.5 V	57		95	μs
		10-bit resolution Target pin: Internal reference voltage, and temperature sensor output voltage	3.6 V ≤ V_{DD} ≤ 5.5 V	2.375		39	μs
			2.7 V ≤ V_{DD} ≤ 5.5 V	3.5625		39	μs
			1.8 V ≤ V_{DD} ≤ 5.5 V	17		39	μs
Zero-scale error Notes 1, 2	EZS	10-bit resolution AV_{REFP} = V_{DD} Note 3	1.8 V ≤ AV_{REFP} ≤ 5.5 V			±0.25	%FSR
			1.6 V ≤ AV_{REFP} ≤ 5.5 V Note 4			±0.50	%FSR
Full-scale error Notes 1, 2	EFS	10-bit resolution AV_{REFP} = V_{DD} Note 3	1.8 V ≤ AV_{REFP} ≤ 5.5 V			±0.25	%FSR
			1.6 V ≤ AV_{REFP} ≤ 5.5 V Note 4			±0.50	%FSR
Integral linearity error Note 1	ILE	10-bit resolution AV_{REFP} = V_{DD} Note 3	1.8 V ≤ AV_{REFP} ≤ 5.5 V			±2.5	LSB
			1.6 V ≤ AV_{REFP} ≤ 5.5 V Note 4			±5.0	LSB
Differential linearity error Note 1	DLE	10-bit resolution AV_{REFP} = V_{DD} Note 3	1.8 V ≤ AV_{REFP} ≤ 5.5 V			±1.5	LSB
			1.6 V ≤ AV_{REFP} ≤ 5.5 V Note 4			±2.0	LSB
Analog input voltage	VAIN	ANI2 and ANI3		0		AV_{REFP}	V
		Internal reference voltage (1.8 V ≤ V_{DD} ≤ 5.5 V)		V_{BGR} Note 5			V
		Temperature sensor output voltage (1.8 V ≤ V_{DD} ≤ 5.5 V)		V_{TMPS25} Note 5			V

Note 1. Excludes quantization error (±1/2 LSB).

Note 2. This value is indicated as a ratio (%FSR) to the full-scale value.

Note 3. When AV_{REFP} < V_{DD}, the MAX. values are as follows.

Overall error: Add ±1.0 LSB to the MAX. value when AV_{REFP} = V_{DD}.

Zero-scale error/Full-scale error: Add ±0.05%FSR to the MAX. value when AV_{REFP} = V_{DD}.

Integral linearity error/ Differential linearity error: Add ±0.5 LSB to the MAX. value when AV_{REFP} = V_{DD}.

Note 4. Values when the conversion time is set to 57 μs (min.) and 95 μs (max.).

Note 5. Refer to **2.6.2 Temperature sensor characteristics/internal reference voltage characteristic**.

2.6.7 LVD circuit characteristics

(1) LVD Detection Voltage of Reset Mode and Interrupt Mode

(T_A = -40 to +85°C, $V_{PDR} \leq EV_{DD} \leq V_{DD} \leq$ 5.5 V, V_{SS} = 0 V)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	Supply voltage level	V_{LVD0}	Power supply rise time	3.98	4.06	4.14	V
			Power supply fall time	3.90	3.98	4.06	V
		V_{LVD1}	Power supply rise time	3.68	3.75	3.82	V
			Power supply fall time	3.60	3.67	3.74	V
		V_{LVD2}	Power supply rise time	3.07	3.13	3.19	V
			Power supply fall time	3.00	3.06	3.12	V
		V_{LVD3}	Power supply rise time	2.96	3.02	3.08	V
			Power supply fall time	2.90	2.96	3.02	V
		V_{LVD4}	Power supply rise time	2.86	2.92	2.97	V
			Power supply fall time	2.80	2.86	2.91	V
		V_{LVD5}	Power supply rise time	2.76	2.81	2.87	V
			Power supply fall time	2.70	2.75	2.81	V
		V_{LVD6}	Power supply rise time	2.66	2.71	2.76	V
			Power supply fall time	2.60	2.65	2.70	V
		V_{LVD7}	Power supply rise time	2.56	2.61	2.66	V
			Power supply fall time	2.50	2.55	2.60	V
		V_{LVD8}	Power supply rise time	2.45	2.50	2.55	V
			Power supply fall time	2.40	2.45	2.50	V
		V_{LVD9}	Power supply rise time	2.05	2.09	2.13	V
			Power supply fall time	2.00	2.04	2.08	V
		V_{LVD10}	Power supply rise time	1.94	1.98	2.02	V
			Power supply fall time	1.90	1.94	1.98	V
		V_{LVD11}	Power supply rise time	1.84	1.88	1.91	V
			Power supply fall time	1.80	1.84	1.87	V
		V_{LVD12}	Power supply rise time	1.74	1.77	1.81	V
			Power supply fall time	1.70	1.73	1.77	V
		V_{LVD13}	Power supply rise time	1.64	1.67	1.70	V
			Power supply fall time	1.60	1.63	1.66	V
Minimum pulse width		t_{LW}		300			µs
Detection delay time						300	µs

3.1 Absolute Maximum Ratings

(1/2)

Parameter	Symbols	Conditions	Ratings	Unit
Supply voltage	V_{DD}, EV_{DD}	$V_{DD} \leq EV_{DD}$	-0.5 to + 6.5	V
	AV_{REFP}		0.3 to V_{DD} + 0.3 Note 2	V
	AV_{REFM}		-0.3 to V_{DD} + 0.3 Note 2 and $AV_{REFM} \leq AV_{REFP}$	V
REGC pin input voltage	V_{IREGC}	REGC	-0.3 to + 2.8 and -0.3 to V_{DD} + 0.3 Note 1	V
Input voltage	V_{I1}	P00, P01, P30 to P33, P40, and P51 to P56	-0.3 to EV_{DD} + 0.3 and -0.3 to V_{DD} + 0.3 Note 2	V
	V_{I2}	P20 to P23, P121, P122, P125, P137, EXCLK, $\overline{\text{RESET}}$	-0.3 to V_{DD} + 0.3 Note 2	V
Output voltage	V_{O1}	P00, P01, P30 to P33, P40, and P51 to P56	-0.3 to EV_{DD} + 0.3 and -0.3 to V_{DD} + 0.3 Note 2	V
	V_{O2}	P20 to P23	-0.3 to V_{DD} + 0.3 Note 2	V
Analog input voltage	V_{AI1}	ANI16 to ANI22	-0.3 to EV_{DD} + 0.3 and -0.3 to AV_{REF}(+) + 0.3 Notes 2, 3	V
	V_{AI2}	ANI0 to ANI3	-0.3 to V_{DD} + 0.3 and -0.3 to AV_{REF}(+) + 0.3 Notes 2, 3	V

Note 1. Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μF). This value regulates the absolute maximum rating of the REGC pin. Do not use this pin with voltage applied to it.

Note 2. Must be 6.5 V or lower.

Note 3. Do not exceed AV_{REF} (+) + 0.3 V in case of A/D conversion target pin.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark 1. Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

Remark 2. AV_{REF} (+): + side reference voltage of the A/D converter.

Remark 3. V_{SS}: Reference voltage

3.3 DC Characteristics

3.3.1 Pin characteristics

(T_A = -40 to +105°C, 2.4 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = 0 V) **(1/5)**

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
<R> Output current, high Note 1	I_{OH1}	Per pin for P00, P01, P30 to P33, P40, and P51 to P56				-3.0 Note 2	mA
		Total of P00, P01, and P40 (When duty ≤ 70% Note 3)	4.0 V ≤ EV_{DD} ≤ 5.5 V			-12.5	mA
			2.7 V ≤ EV_{DD} < 4.0 V			-10.0	mA
			2.4 V ≤ EV_{DD} < 2.7 V			-5.0	mA
		Total of P30 to P33, and P51 to P56 (When duty ≤ 70% Note 3)	4.0 V ≤ EV_{DD} ≤ 5.5 V			-30.0	mA
			2.7 V ≤ EV_{DD} < 4.0 V			-19.0	mA
			2.4 V ≤ EV_{DD} < 2.7 V			-10.0	mA
		Total of all pins (When duty ≤ 70% Note 3)				-42.5	mA
	I_{OH2}	Per pin for P20 to P23				-0.1 Note 2	mA
		Total of all pins (When duty ≤ 70% Note 3)	2.4 V ≤ V_{DD} ≤ 5.5 V			-0.4	mA

Note 1. Value of current at which the device operation is guaranteed even if the current flows from the V_{DD} pin to an output pin.

Note 2. Do not exceed the total current value.

Note 3. Specification under conditions where the duty factor ≤ 70%.
The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = (I_{OH} × 0.7)/(n × 0.01)
  <Example> Where n = 80% and I_{OH} = -10.0 mA
  Total output current of pins = (-10.0 × 0.7)/(80 × 0.01) ≈ -8.7 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor.
A current higher than the absolute maximum rating must not flow into one pin.

Caution **P00, P01, P20, P30 to P33, P40 and P51 to P56 do not output high level in N-ch open-drain mode.**

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T_A = -40 to +105°C, 2.4 V ≤ EV_{DD} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) **(2/5)**

<R>

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, low Note 1	I_{OL1}	Per pin for P00, P01, P30 to P33, P40, and P51 to P56				8.5 Note 2	mA
		Total of P00, P01, and P40 (When duty ≤ 70% Note 3)	4.0 V ≤ EV_{DD} ≤ 5.5 V			-36.0	mA
			2.7 V ≤ EV_{DD} < 4.0 V			15.0	mA
			2.4 V ≤ EV_{DD} < 2.7 V			9.0	mA
		Total of P30 to P33, and P51 to P56 (When duty ≤ 70% Note 3)	4.0 V ≤ EV_{DD} ≤ 5.5 V			40.0	mA
			2.7 V ≤ EV_{DD} < 4.0 V			35.0	mA
			2.4 V ≤ EV_{DD} < 2.7 V			20.0	mA
		Total of all pins (When duty ≤ 70% Note 3)				76.0	mA
	I_{OL2}	Per pin for P20 to P23				0.4 Note 2	mA
		Total of all pins (When duty ≤ 70% Note 3)	2.4 V ≤ V_{DD} ≤ 5.5 V			1.6	mA

Note 1. Value of current at which the device operation is guaranteed even if the current flows from an output pin to the V_{SS} pin.

Note 2. Do not exceed the total current value.

Note 3. Specification under conditions where the duty factor ≤ 70%.
The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = (I_{OL} × 0.7)/(n × 0.01)

<Example> Where n = 80% and I_{OL} = 10.0 mA
Total output current of pins = (10.0 × 0.7)/(80 × 0.01) ≈ 8.7 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor.
A current higher than the absolute maximum rating must not flow into one pin.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T_A = -40 to +105°C, 2.4 V ≤ EV_{DD} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) **(5/5)**

Items	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Input leakage current, high	I_{LIH1}	P00, P01, P30 to P33, P40, and P51 to P56	$V_I = EV_{DD}$				1	μA
	I_{LIH2}	P20 to P23, P125, P137, $\overline{RESET}$	$V_I = V_{DD}$				1	μA
	I_{LIH3}	P121, P122, X1, X2, EXCLK	$V_I = V_{DD}$	In input port or external clock input			1	μA
				In resonator connection			10	μA
Input leakage current, low	I_{LIL1}	P00, P01, P30 to P33, P40, and P51 to P56	$V_I = V_{SS}$				-1	μA
	I_{LIL2}	P20 to P23, P125, P137, $\overline{RESET}$	$V_I = V_{SS}$				-1	μA
	I_{LIL3}	P121, P122, X1, X2, EXCLK	$V_I = V_{SS}$	In input port or external clock input			-1	μA
				In resonator connection			-10	μA
On-chip pull-up resistance	R_U	P00, P01, P30 to P33, P40, P51 to P56, P125	$V_I = V_{SS}$, In input port		10	20	100	kΩ

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

When P20 is used as SO10 pin

(T_A = -40 to +105°C, 2.4 V ≤ EV_{DD} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		Unit
				MIN.	MAX.	
SCKp cycle time Note 4	t_{KCY2}	4.0 V ≤ V_{DD} ≤ 5.5 V	f_{MCK} > 20 MHz	20/f_{MCK}		ns
			f_{MCK} ≤ 20 MHz	18/f_{MCK}		ns
		2.7 V ≤ V_{DD} < 4.0 V	f_{MCK} > 16 MHz	20/fMCK and 1000		ns
			f_{MCK} ≤ 16 MHz	18/f_{MCK}		ns
		2.4 V ≤ V_{DD} < 2.7 V		18/f_{MCK} and 1200		ns
SCKp high-/low-level width	t_{KH2}, t_{KL2}	4.0 V ≤ V_{DD} ≤ 5.5 V		t_{KCY2}/2 - 14		ns
	t_{KH2}, t_{KL2}	2.7 V ≤ V_{DD} < 4.0 V		t_{KCY2}/2 - 16		ns
		2.4 V ≤ V_{DD} < 2.7 V		t_{KCY2}/2 - 36		ns
SIp setup time (to SCKp↑) Note 1	t_{SIK2}	2.7 V ≤ V_{DD} ≤ 5.5 V		1/f_{MCK} + 40		ns
		2.4 V ≤ V_{DD} < 2.7 V		1/f_{MCK} + 60		ns
SIp hold time (from SCKp↑) Note 1	t_{KSI2}			1/f_{MCK} + 62		ns
Delay time from SCKp↓ to SOp output Note 2	t_{KSO2}	C = 30 pF Note 3	2.7 V ≤ V_{DD} ≤ 5.5 V		2/f_{MCK} + 190	ns
			2.4 V ≤ V_{DD} < 2.7 V		2/f_{MCK} + 250	ns

Note 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 3. C is the load capacitance of the SOp output lines.

Note 4. The maximum transfer rate when using the SNOOZE mode is 1 Mbps.

Caution Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remark 1. p: CSI number (p = 00, 01, 10 and 11), m: Unit number (m = 0), n: Channel number (n = 0 to 3), g: PIM and POM numbers (g = 0, 2, 3 to 5 and 12)

Remark 2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03))

(5) Communication at different potential (1.8 V, 2.5 V, 3.0 V) (UART mode) (dedicated baud rate generator output)

(T_A = -40 to +105°C, 2.4 V ≤ EV_{DD} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) **(1/2)**

Parameter	Symbol	Conditions		HS (high-speed main) Mode		Unit
				MIN.	MAX.	
Transfer rate		Reception	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.3 V ≤ V_b ≤ 4.0 V		f_{MCK}/12 Note 1	bps
			Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} Note 3		2.0	Mbps
			2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V		f_{MCK}/12 Note 1	bps
			Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} Note 3		2.0	Mbps
			2.4 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V		f_{MCK}/12 Notes 1, 2	bps
			Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} Note 3		1.3	Mbps

Note 1. Transfer rate in the SNOOZE mode is 4,800 bps only.

Note 2. Use it with EV_{DD} ≥ Vb.

Note 3. The maximum operating frequencies of the CPU/peripheral hardware clock (f_{CLK}) are:
HS (high-speed main) mode: 24 MHz (2.7 V ≤ V_{DD} ≤ 5.5 V)
16 MHz (2.4 V ≤ V_{DD} ≤ 5.5 V)

Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (EV_{DD} tolerance) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

Remark 1. V_b[V]: Communication line voltage

Remark 2. q: UART number (q = 0 and 1), g: PIM and POM numbers (g = 0, 2, 3, 5, 12)

Remark 3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03))

3.6 Analog Characteristics

3.6.1 A/D converter characteristics

Classification of A/D converter characteristics

Input channel \ Reference Voltage	Reference voltage (+) = AV_{REFP} Reference voltage (-) = AV_{REFM}	Reference voltage (+) = V_{DD} Reference voltage (-) = V_{SS}	Reference voltage (+) = V_{BGR} Reference voltage (-)= AV_{REFM}
ANI0 to ANI3	Refer to **3.6.1 (1)**.	Refer to **3.6.1 (3)**.	Refer to **3.6.1 (4)**.
ANI16 to ANI22	Refer to **3.6.1 (2)**.		
Internal reference voltage Temperature sensor output voltage	Refer to **3.6.1 (1)**.		—

(1) When reference voltage (+) = AV_{REFP}/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (-) = AV_{REFM}/ANI1 (ADREFM = 1), target pin: ANI2 and ANI3, internal reference voltage, and temperature sensor output voltage

(T_A = -40 to +105°C, 2.4 V ≤ AV_{REFP} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V, Reference voltage (+) = AV_{REFP}, Reference voltage (-) = AV_{REFM} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error Note 1	AINL	10-bit resolution AV_{REFP} = V_{DD} Note 3	2.4 V ≤ AV_{REFP} ≤ 5.5 V		1.2	±3.5	LSB
Conversion time	t_{CONV}	10-bit resolution Target pin: ANI2 and ANI3	3.6 V ≤ V_{DD} ≤ 5.5 V	2.125		39	µs
			2.7 V ≤ V_{DD} ≤ 5.5 V	3.1875		39	µs
			2.4 V ≤ V_{DD} ≤ 5.5 V	17		39	µs
		10-bit resolution Target pin: Internal reference voltage, and temperature sensor output voltage	3.6 V ≤ V_{DD} ≤ 5.5 V	2.375		39	µs
			2.7 V ≤ V_{DD} ≤ 5.5 V	3.5625		39	µs
			1.8 V ≤ V_{DD} ≤ 5.5 V	17		39	µs
Zero-scale error Notes 1, 2	E_{ZS}	10-bit resolution AV_{REFP} = V_{DD} Note 3	2.4 V ≤ AV_{REFP} ≤ 5.5 V			±0.25	%FSR
Full-scale error Notes 1, 2	E_{FS}	10-bit resolution AV_{REFP} = V_{DD} Note 3	2.4 V ≤ AV_{REFP} ≤ 5.5 V			±0.25	%FSR
Integral linearity error Note 1	ILE	10-bit resolution AV_{REFP} = V_{DD} Note 3	2.4 V ≤ AV_{REFP} ≤ 5.5 V			±2.5	LSB
Differential linearity error Note 1	DLE	10-bit resolution AV_{REFP} = V_{DD} Note 3	2.4 V ≤ AV_{REFP} ≤ 5.5 V			±1.5	LSB
Analog input voltage	V_{AIN}	ANI2 and ANI3		0		AV_{REFP}	V
		Internal reference voltage (2.4 V ≤ V_{DD} ≤ 5.5 V)		V_{BGR} Note 4			V
		Temperature sensor output voltage (2.4 V ≤ V_{DD} ≤ 5.5 V)		V_{TMPS25} Note 4			V

Note 1. Excludes quantization error (±1/2 LSB).

Note 2. This value is indicated as a ratio (%FSR) to the full-scale value.

Note 3. When AV_{REFP} < V_{DD}, the MAX. values are as follows.

Overall error: Add ±1.0 LSB to the MAX. value when AV_{REFP} = V_{DD}.

Zero-scale error/Full-scale error: Add ±0.05%FSR to the MAX. value when AV_{REFP} = V_{DD}.

Integral linearity error/ Differential linearity error: Add ±0.5 LSB to the MAX. value when AV_{REFP} = V_{DD}.

Note 4. Refer to **3.6.2 Temperature sensor characteristics/internal reference voltage characteristic**.

(4) When reference voltage (+) = Internal reference voltage (ADREFP1 = 1, ADREFP0 = 0), reference voltage (-) = AV_{REFM}/ANI1 (ADREFM = 1), target pin: ANI0 to ANI3, ANI16 to ANI22

(T_A = -40 to +105°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, 1.6 V ≤ EV_{DD} ≤ V_{DD} = 0 V,
Reference voltage (+) = V_{BGR} Note 3, Reference voltage (-) = AV_{REFM} = 0 V Note 4)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	RES			8		bit
Conversion time	t_{CONV}		17		39	μs
Zero-scale error Notes 1, 2	E_{ZS}				±0.60	% FSR
Integral linearity error Note 1	ILE				±2.0	LSB
Differential linearity error Note 1	DLE	8-bit resolution			±1.0	LSB
Analog input voltage	V_{AIN}		0		V_{BGR} Note 3	V

Note 1. Excludes quantization error (±1/2 LSB).

Note 2. This value is indicated as a ratio (% FSR) to the full-scale value.

Note 3. Refer to **3.6.2 Temperature sensor characteristics/internal reference voltage characteristic**.

Note 4. When reference voltage (-) = V_{SS}, the MAX. values are as follows.

Zero-scale error: Add ±0.35%FSR to the MAX. value when reference voltage (-) = AV_{REFM}.

Integral linearity error: Add ±0.5 LSB to the MAX. value when reference voltage (-) = AV_{REFM}.

Differential linearity error: Add ±0.2 LSB to the MAX. value when reference voltage (-) = AV_{REFM}.

3.6.5 PGA

(T_A = -40 to +105°C, 2.7 V ≤ EV_{DD} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input offset voltage	V_{IOPGA}					±10	mV
Input voltage range	V_{IPGA}			0		0.9 × V_{DD}/Gain	V
Output voltage range	V_{IOHPGA}			0.93 × V_{DD}			V
	V_{IOLPGA}					0.07 × V_{DD}	V
Gain error		x4, x8				±1	%
		x16				±1.5	%
		x32				±2	%
Slew rate	SR_{RPGA}	Rising When V_{IN} = 0.1V_{DD}/gain to 0.9V_{DD}/gain. 10 to 90% of output voltage amplitude	4.0 V ≤ V_{DD} ≤ 5.5 V (Other than x32)	3.5			V/µs
			4.0 V ≤ V_{DD} ≤ 5.5 V (x32)	3.0			
			2.7 V ≤ V_{DD} ≤ 4.0V	0.5			
	SR_{FPGA}	Falling When V_{IN}= 0.1V_{DD}/gain to 0.9V_{DD}/gain. 90 to 10% of output voltage amplitude	4.0 V ≤ V_{DD} ≤ 5.5 V (Other than x32)	3.5			
			4.0 V ≤ V_{DD} ≤ 5.5 V (x32)	3.0			
			2.7 V ≤ V_{DD} ≤ 4.0V	0.5			
Reference voltage stabilization wait time[Note]	t_{PGA}	x4, x8				5	µs
		x16, x32				10	µs

Note Time required until a state is entered where the DC and AC specifications of the PGA are satisfied after the PGA operation has been enabled (PGAEN = 1).

3.6.7 LVD circuit characteristics

(1) LVD Detection Voltage of Reset Mode and Interrupt Mode

(T_A = -40 to +105°C, $V_{PDR} \leq EV_{DD} = V_{DD} \leq$.5.5 V, V_{SS} = 0 V)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	Supply voltage level	V_{LVD0}	Power supply rise time	3.90	4.06	4.22	V
			Power supply fall time	3.83	3.98	4.13	V
		V_{LVD1}	Power supply rise time	3.60	3.75	3.90	V
			Power supply fall time	3.53	3.67	3.81	V
		V_{LVD2}	Power supply rise time	3.01	3.13	3.25	V
			Power supply fall time	2.94	3.06	3.18	V
		V_{LVD3}	Power supply rise time	2.90	3.02	3.14	V
			Power supply fall time	2.85	2.96	3.07	V
		V_{LVD4}	Power supply rise time	2.81	2.92	3.03	V
			Power supply fall time	2.75	2.86	2.97	V
		V_{LVD5}	Power supply rise time	2.71	2.81	2.92	V
			Power supply fall time	2.64	2.75	2.86	V
		V_{LVD6}	Power supply rise time	2.61	2.71	2.81	V
			Power supply fall time	2.55	2.65	2.75	V
		V_{LVD7}	Power supply rise time	2.51	2.61	2.71	V
			Power supply fall time	2.45	2.55	2.65	V
Minimum pulse width		t_{LW}		300			μs
Detection delay time						300	μs

(2) LVD Detection Voltage of Interrupt & Reset Mode

(T_A = -40 to +105°C, $V_{PDR} \leq EV_{DD} \leq V_{DD} \leq$ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Interrupt and reset mode	V_{LVDD0}	V_{POC0}, V_{POC1}, V_{POC2} = 0, 1, 1, falling reset voltage		2.64	2.75	2.86	V
	V_{LVDD1}	LVIS0, LVIS1 = 1, 0	Rising release reset voltage	2.81	2.92	3.03	V
			Falling interrupt voltage	2.75	2.86	2.97	V
	V_{LVDD2}	LVIS0, LVIS1 = 0, 1	Rising release reset voltage	2.90	3.02	3.14	V
			Falling interrupt voltage	2.85	2.96	3.07	V
	V_{LVDD3}	LVIS0, LVIS1 = 0, 0	Rising release reset voltage	3.90	4.06	4.22	V
			Falling interrupt voltage	3.83	3.98	4.13	V

3.6.8 Power supply voltage rising slope characteristics

(T_A = -40 to +105°C, V_{SS} = 0 V)

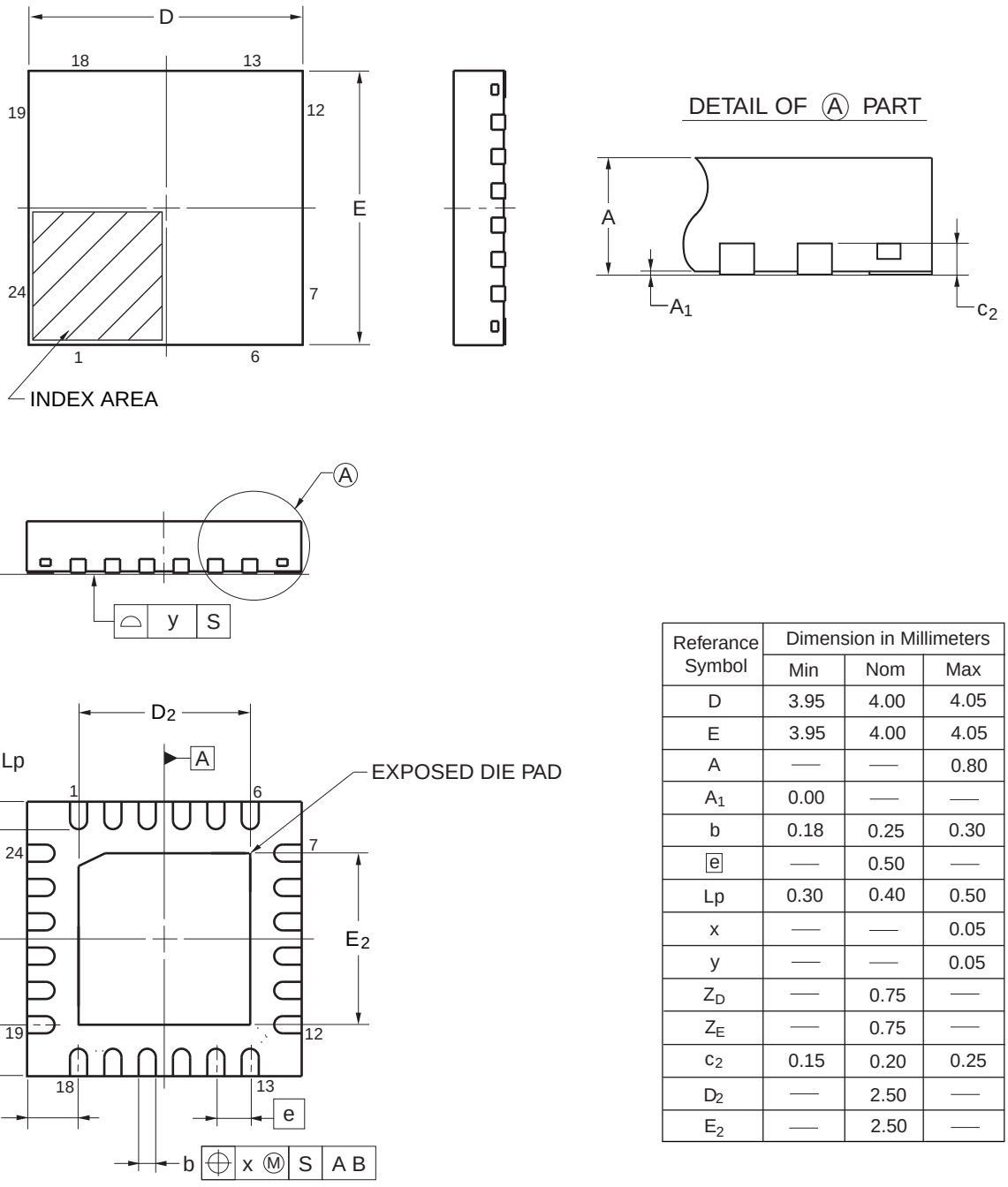
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Power supply voltage rising slope	S_{VDD}				54	V/ms

Caution Make sure to keep the internal reset state by the LVD circuit or an external reset until V_{DD} reaches the operating voltage range shown in 3.4 AC Characteristics.

4.4 24-pin products

R5F1057AGNA, R5F1057AANA

JEITA Package code	RENESAS code	Previous code	MASS(TYP.)[g]
P-HWQFN24-4x4-0.50	PWQN0024KE-A	P24K8-50-CAB-3	0.04



Referance Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	3.95	4.00	4.05
E	3.95	4.00	4.05
A	—	—	0.80
A_1	0.00	—	—
b	0.18	0.25	0.30
e	—	0.50	—
Lp	0.30	0.40	0.50
x	—	—	0.05
y	—	—	0.05
Z_D	—	0.75	—
Z_E	—	0.75	—
c_2	0.15	0.20	0.25
D_2	—	2.50	—
E_2	—	2.50	—