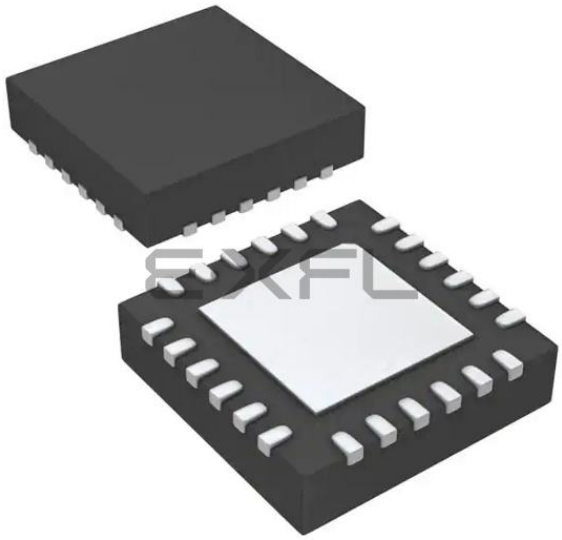
Renesas Electronics America Inc - R5F1057AANA#W0 Datasheet



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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	RL78
Core Size	16-Bit
Speed	24MHz
Connectivity	CSI, I²C, UART/USART
Peripherals	LVD, POR, WDT
Number of I/O	21
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	1.5K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 11x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	24-WFQFN Exposed Pad
Supplier Device Package	24-HWQFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f1057aana-w0

1.6 Outline of Functions

This outline describes the functions at the time when Peripheral I/O redirection register 0 to 3 (PIOR0 to PIOR3) are set to 00H.

(1/2)

Item		10-pin	16-pin	20-pin	24-pin	25-pin
		R5F1051A	R5F1054A	R5F1056A	R5F1057A	R5F1058A
Code flash memory (KB)		16 Kbytes				
Data flash memory (KB)		2 Kbytes				
RAM		1.5 Kbytes				
Address space		1 Mbytes				
Main system clock	High-speed system clock (f_{MX})	X1 (crystal/ceramic) oscillation[Note], external main system clock input (EXCLK) 1 to 20 MHz: V_{DD} = 2.7 to 5.5 V, 1 to 16 MHz: V_{DD} = 2.4 to 2.7 V, 1 to 8 MHz: V_{DD} = 1.8 to 2.4 V, 1 to 4 MHz: V_{DD} = 1.6 to 1.8 V				
	High-speed on-chip oscillator clock (f_{IH}) Max: 24 MHz	HS (High-speed main) mode: 1 to 24 MHz (V_{DD} = 2.7 to 5.5 V), HS (High-speed main) mode: 1 to 16 MHz (V_{DD} = 2.4 to 5.5 V), LS (Low-speed main) mode: 1 to 8 MHz (V_{DD} = 1.8 to 5.5 V), LV (Low-voltage main) mode: 1 to 4 MHz (V_{DD} = 1.6 to 5.5 V), LP (Low-power main) mode: 1 MHz (V_{DD} = 1.8 to 5.5 V)				
	Middle-speed on-chip oscillator clock (f_{IM}) Max: 4 MHz					
<R> Subsystem clock	Low-speed on-chip oscillator clock (f_{IL})	15 kHz (typ.): V_{DD} = 1.6 to 5.5 V				
General-purpose register		8 bits × 32 registers (8 bits × 8 registers × 4 banks)				
Minimum instruction execution time		0.04167 μs (High-speed on-chip oscillator clock: f_{IH} = 24 MHz operation)				
		0.05 μs (High-speed system clock: f_{MX} = 20 MHz operation)				
Instruction set		• Data transfer (8/16 bits) • Adder and subtractor/logical operation (8/16 bits) • Multiplication (8 bits × 8 bits, 16 bits × 16 bits), Division (16 bits ÷ 16 bits, 32 bits ÷ 32 bits) • Multiplication and Accumulation (16 bits × 16 bits + 32 bits) • Rotate, barrel shift, and bit manipulation (Set, reset, test, and Boolean operation), etc.				
I/O port	Total	7	13	17	21	
	CMOS I/O	4	9	13	17	
	CMOS input	3	4			
Timer	16-bit timer	4 channels				
	Watchdog timer	1 channel				
	Timer KB	1 channel				
	12-bit interval timer	1 channel				
	8/16-bit interval timer	2 channels (8 bit)/1 channel (16 bit)				
	Timer output	3	5	6		

Note 16, 20, 24, 25-pin products

Caution The flash library uses RAM in self-programming and rewriting of the data flash memory.
The target products and start address of the RAM areas used by the flash library are shown below.

R5F105xA (x = 1, 4, 6, 7, 8): Start address FF900H

For the RAM areas used by the flash library, see Self RAM list of Flash Self-Programming Library for RL78 Family (R20UT2944).

2.2 Oscillator Characteristics

2.2.1 X1 characteristics

(T_A = -40 to +85°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Resonator	Resonator	Conditions	MIN.	TYP.	MAX.	Unit
X1 clock oscillation frequency (f_X) Note	Ceramic resonator/ crystal resonator	2.7 V ≤ V_{DD} ≤ 5.5 V	1.0		20.0	MHz
		2.4 V ≤ V_{DD} < 2.7 V	1.0		16.0	
		1.8 V ≤ V_{DD} < 2.4 V	1.0		8.0	
		1.6 V ≤ V_{DD} < 1.8 V	1.0		4.0	

Note Indicates only permissible oscillator frequency ranges. Refer to **2.4 AC Characteristics** for instruction execution time. Request evaluation by the manufacturer of the oscillator circuit mounted on a board to check the oscillator characteristics.

Caution **Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.**

Remark When using the X1 oscillator, refer to **6.4 System Clock Oscillator** in the RL78/G11 User's Manual.

2.2.2 On-chip oscillator characteristics

(T_A = -40 to +85°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Oscillators	Parameters	Conditions		MIN.	TYP.	MAX.	Unit
High-speed on-chip oscillator clock frequency Notes 1, 2	f_{IH}	2.7 V ≤ V_{DD} ≤ 5.5 V		1		24	MHz
		2.4 V ≤ V_{DD} ≤ 5.5 V		1		16	
		1.8 V ≤ V_{DD} ≤ 5.5 V		1		8	
		1.6 V ≤ V_{DD} ≤ 5.5 V		1		4	
High-speed on-chip oscillator clock frequency accuracy		T_A = -20 to +85°C	1.8 V ≤ V_{DD} ≤ 5.5 V	-1		1	%
			1.6 V ≤ V_{DD} < 1.8 V	-5		5	
		T_A = -40 to -20°C	1.8 V ≤ V_{DD} ≤ 5.5 V	-1.5		1.5	%
			1.6 V ≤ V_{DD} < 1.8 V	-5.5		5.5	
Middle-speed on-chip oscillator oscillation frequency Note 2	f_{IM}			1		4	MHz
Middle-speed on-chip oscillator oscillation frequency accuracy				-12		+12	%
<R> Temperature drift of Middle-speed on-chip oscillator oscillation frequency accuracy	D_{IMT}				0.008		%/°C
<R> Voltage drift of Middle-speed on-chip oscillator oscillation frequency accuracy	D_{IMV}	T_A = 25°C	2.1 V ≤ V_{DD} ≤ 5.5 V		0.02		%/V
			2.0 V ≤ V_{DD} < 2.1 V		-12		
			1.6 V ≤ V_{DD} < 2.0 V		10		
Low-speed on-chip oscillator clock frequency Note 2	f_{IL}				15		kHz
Low-speed on-chip oscillator clock frequency accuracy				-15		+15	%

Note 1. High-speed on-chip oscillator frequency is selected with bits 0 to 3 of the option byte (000C2H) and bits 0 to 2 of the HOCODIV register.

Note 2. This only indicates the oscillator characteristics. Refer to **2.4 AC Characteristics** for instruction execution time.

2.4 AC Characteristics

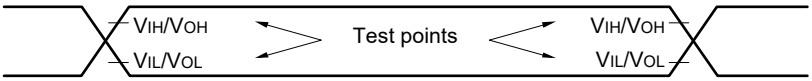
(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) **(1/2)**

Items	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Instruction cycle (minimum instruction execution time)	T_{CY}	Main system clock (f_{MAIN}) operation	HS (high-speed main) mode	2.7 V ≤ V_{DD} ≤ 5.5 V	0.04167		1	μs
				2.4 V ≤ V_{DD} < 2.7 V	0.0625		1	μs
			LS (low-speed main) mode	1.8 V ≤ V_{DD} ≤ 5.5 V PMMC. MCSEL = 0	0.125		1	μs
				1.8 V ≤ V_{DD} ≤ 5.5 V PMMC. MCSEL = 1	0.25		1	
			LP (low-power main) mode	1.8 V ≤ V_{DD} ≤ 5.5 V	1			μs
			LV (low-voltage main) mode	1.6 V ≤ V_{DD} ≤ 5.5 V	0.25		1	μs
		Subsystem clock (f_{SUB}) operation	f_{IL}	1.8 V ≤ V_{DD} ≤ 5.5 V		66.7		μs
		In the self-programming mode	HS (high-speed main) mode	2.7 V ≤ V_{DD} ≤ 5.5 V	0.04167		1	μs
				2.4 V ≤ V_{DD} < 2.7 V	0.0625		1	μs
			LS (low-speed main) mode	1.8 V ≤ V_{DD} ≤ 5.5 V	0.125		1	μs
			LV (low-voltage main) mode	1.8 V ≤ V_{DD} ≤ 5.5 V	0.25		1	μs
External system clock frequency	f_{EX}	2.7 V ≤ V_{DD} ≤ 5.5 V			1		20	MHz
		2.4 V ≤ V_{DD} < 2.7 V			1		16	MHz
		1.8 V ≤ V_{DD} < 2.4 V			1		8	MHz
		1.6 V ≤ V_{DD} < 1.8 V			1		4	MHz
External system clock input high-/low-level width	t_{EXH}, t_{EXL}	2.7 V ≤ V_{DD} ≤ 5.5 V			24			ns
		2.4 V ≤ V_{DD} < 2.7 V			30			ns
		1.8 V ≤ V_{DD} < 2.4 V			60			ns
		1.6 V ≤ V_{DD} < 1.8 V			120			ns
TI00 to TI03 input high-/low-level width	t_{TIH}, t_{TIL} Note				1/f_{MCK} + 10			ns

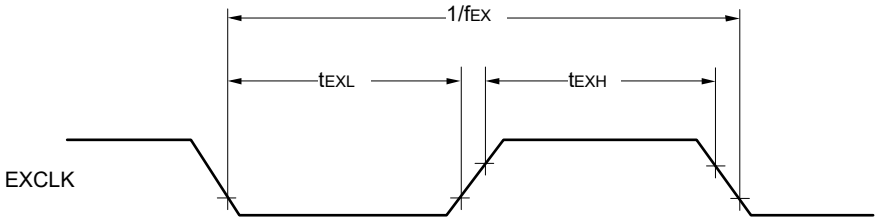
Note Following conditions must be satisfied on low level interface of EV_{DD} < V_{DD}.
1.8 V ≤ EV_{DD} ≤ 2.7 V: MIN. 125 ns
1.6 V ≤ EV_{DD} < 1.8 V: MIN. 250 ns

Remark f_{MCK}: Timer array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of timer mode register mn (TMRmn). m: Unit number (m = 0), n: Channel number (n = 0 to 3))

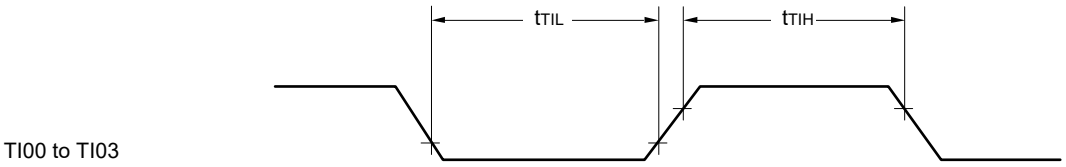
AC Timing Test Points

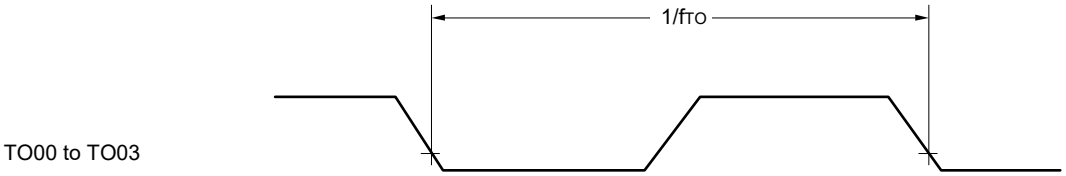


External System Clock Timing



TI/TO Timing





2.5.1 Serial array unit

(1) During communication at same potential (UART mode)

When P01, P30, P31 and P54 are used as TxDq pins

(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LP (Low-power main) mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Transfer rate Note 1, 2		2.7 V ≤ EV_{DD} ≤ 5.5V		f_{MCK}/6		f_{MCK}/6		f_{MCK}/6		f_{MCK}/6	bps
		Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} Note 3		4.0		1.3		0.1		0.6	Mbps
		1.8 V ≤ EV_{DD} ≤ 5.5 V		f_{MCK}/6		f_{MCK}/6		f_{MCK}/6		f_{MCK}/6	bps
		Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} Note 3		4.0		1.3		0.1		0.6	Mbps
		1.7 V ≤ EV_{DD} ≤ 5.5 V		f_{MCK}/6		f_{MCK}/6		f_{MCK}/6		f_{MCK}/6	bps
		Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} Note 3		4.0		1.3		0.1		0.6	Mbps
		1.6 V ≤ EV_{DD} ≤ 5.5 V	—			f_{MCK}/6		f_{MCK}/6		f_{MCK}/6	bps
		Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} Note 3	—			1.3		0.1		0.6	Mbps

Note 1. Transfer rate in the SNOOZE mode is 4800 bps only.

Note 2. Following conditions must be satisfied on low level interface of EV_{DD} < V_{DD}.
2.4 V ≤ EV_{DD} ≤ 2.7 V: MAX.2.6 Mbps
1.8 V ≤ EV_{DD} ≤ 2.4 V: MAX.1.3 Mbps
1.6 V ≤ EV_{DD} ≤ 1.8 V: MAX.0.6 Mbps

Note 3. The maximum operating frequencies of the CPU/peripheral hardware clock (f_{CLK}) are:
HS (high-speed main) mode: 24 MHz (2.7 V ≤ EV_{DD} ≤ 5.5 V)
16 MHz (2.4 V ≤ EV_{DD} ≤ 5.5 V)
LS (low-speed main) mode: 8 MHz (1.8 V ≤ EV_{DD} ≤ 5.5 V)
LP (low-power main) mode: 1 MHz (1.8 V ≤ EV_{DD} ≤ 5.5 V)
LV (low-voltage main) mode: 4 MHz (1.6 V ≤ EV_{DD} ≤ 5.5 V)

Caution Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

When P20 is used as SO10 pin

(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LP (Low-power main) mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t_{KCY1}	$t_{KCY1} \geq 4/f_{CLK}$	4.0 V ≤ V_{DD} ≤ 5.5 V	600		600		4000		1000		ns
			2.7 V ≤ V_{DD} ≤ 5.5 V	850		850						
			2.4 V ≤ V_{DD} ≤ 5.5 V	1000		1000						
			1.8 V ≤ V_{DD} ≤ 5.5 V	—		1500				1500		
			1.7 V ≤ V_{DD} ≤ 5.5 V	—		—		—		2000		
			1.6 V ≤ V_{DD} ≤ 5.5 V	—		—		—				
SCKp high-/low-level width	t_{KH1}, t_{KL1}	4.0 V ≤ V_{DD} ≤ 5.5 V		t_{KCY1}/2 - 12		t_{KCY1}/2 - 50		t_{KCY1}/2 - 50		t_{KCY1}/2 - 50		ns
		2.7 V ≤ V_{DD} ≤ 5.5 V		t_{KCY1}/2 - 18								
		2.4 V ≤ V_{DD} ≤ 5.5 V		t_{KCY1}/2 - 38								
		1.8 V ≤ V_{DD} ≤ 5.5 V		—								
		1.7 V ≤ V_{DD} ≤ 5.5 V		—		—		—		t_{KCY1}/2 - 100		
		1.6 V ≤ V_{DD} ≤ 5.5 V		—		—		—				
SIp setup time (to SCKp↑) Note 1	t_{SIK1}	4.0 V ≤ V_{DD} ≤ 5.5 V		44		110		110		110		ns
		2.7 V ≤ V_{DD} ≤ 5.5 V										
		2.4 V ≤ V_{DD} ≤ 5.5 V		75								
		1.8 V ≤ V_{DD} ≤ 5.5 V		—								
		1.7 V ≤ V_{DD} ≤ 5.5 V		—		—		—		220		
		1.6 V ≤ V_{DD} ≤ 5.5 V		—		—		—				
SIp hold time (from SCKp↑) Note 2	t_{KSI1}	2.4 V ≤ V_{DD} ≤ 5.5 V		19		19		19		19		ns
		1.8 V ≤ V_{DD} ≤ 5.5 V		—								
		1.6 V ≤ V_{DD} ≤ 5.5 V		—		—		—				
Delay time from SCKp↓ to SOp output Note 3	t_{KSO1}	C = 30 pF Note 4	2.4 V ≤ V_{DD} ≤ 5.5 V		150		250		250		300	ns
			1.8 V ≤ V_{DD} ≤ 5.5 V		—							
			1.6 V ≤ V_{DD} ≤ 5.5 V		—		—		—			

Note 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

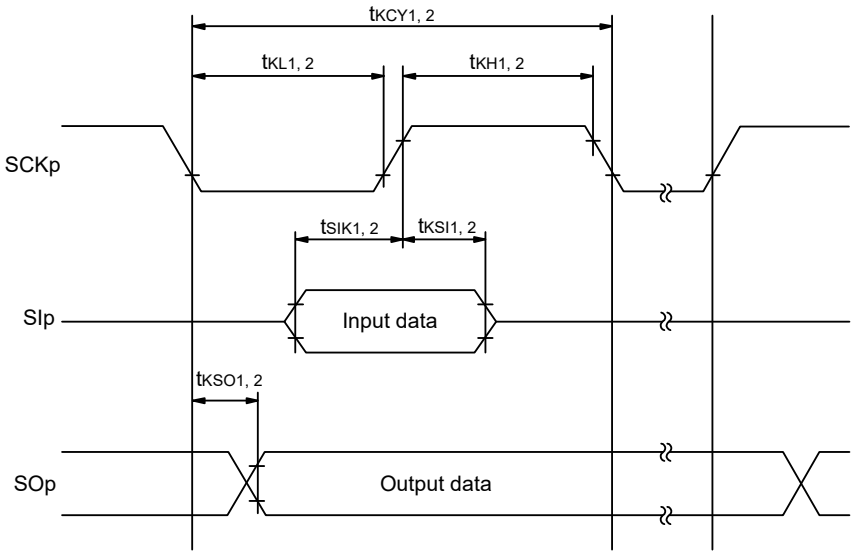
Note 4. C is the load capacitance of the SCKp and SOp output lines.

Caution Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

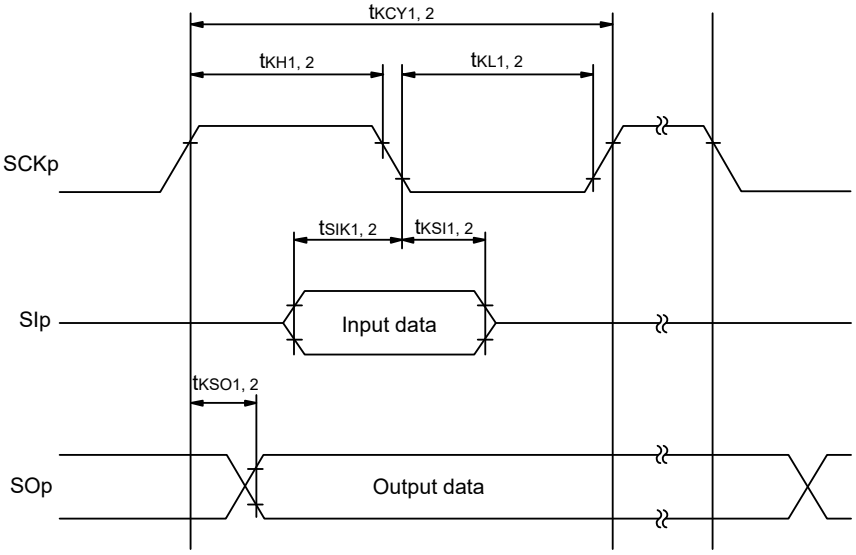
Remark 1. p: CSI number (p = 00, 01, 10 and 11), m: Unit number (m = 0), n: Channel number (n = 0 to 3), g: PIM and POM numbers (g = 0, 4 and 12)

Remark 2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,
n: Channel number (mn = 00 to 03))

CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Remark 1. p: CSI number (p = 00, 01, 10 and 11)
Remark 2. m: Unit number, n: Channel number (mn = 00 to 03)

(T_A = -40 to +85°C, 1.8 V ≤ EV_{DD} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) **(2/2)**

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LP (Low-power main) mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Transfer rate		Transmission	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V		Note 1		Note 1		Note 1		Note 1	bps
			Theoretical value of the maximum transfer rate C_b = 50 pF, R_b = 1.4 kΩ, V_b = 2.7 V		2.8 Note 2		2.8 Note 2		2.8 Note 2		2.8 Note 2	Mbps
			2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V		Note 3		Note 3		Note 3		Note 3	bps
			Theoretical value of the maximum transfer rate C_b = 50 pF, R_b = 2.7 kΩ, V_b = 2.3 V		1.2 Note 4		1.2 Note 4		1.2 Note 4		1.2 Note 4	Mbps
			1.8 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V		Notes 5, 6		Notes 5, 6		Notes 5, 6		Notes 5, 6	bps
			Theoretical value of the maximum transfer rate C_b = 50 pF, R_b = 5.5 kΩ, V_b = 1.6 V		0.43 Note 7		0.43 Note 7		0.43 Note 7		0.43 Note 7	Mbps

Note 1. The smaller maximum transfer rate derived by using f_{MCK}/6 or the following expression is the valid maximum transfer rate.
Expression for calculating the transfer rate when 4.0 V ≤ EV_{DD} ≤ 5.5 V and 2.7 V ≤ V_b ≤ 4.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides

Note 2. This value as an example is calculated when the conditions described in the “Conditions” column are met.
Refer to Note 1 above to calculate the maximum transfer rate under conditions of the customer.

Note 3. The smaller maximum transfer rate derived by using f_{MCK}/6 or the following expression is the valid maximum transfer rate.
Expression for calculating the transfer rate when 2.7 V ≤ EV_{DD} ≤ 4.0 V and 2.3 V ≤ V_b ≤ 2.7 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\} \times 3} \text{ [bps]}$$

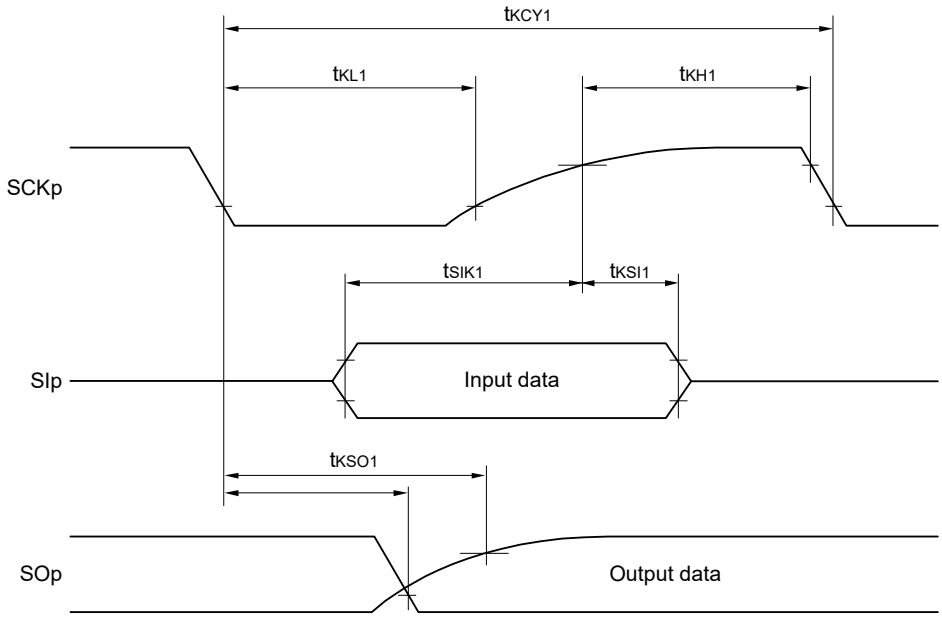
$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides

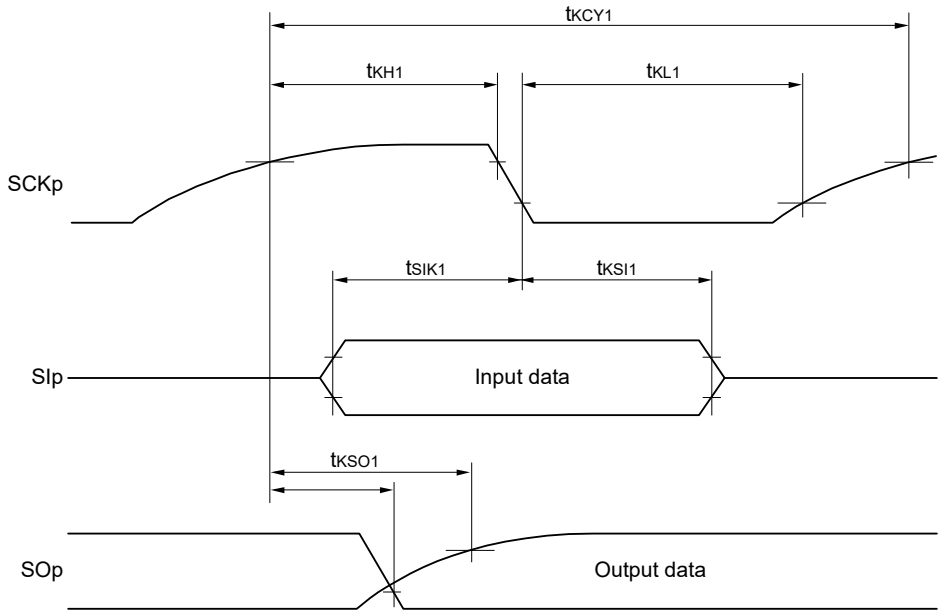
Note 4. This value as an example is calculated when the conditions described in the “Conditions” column are met.
Refer to Note 3 above to calculate the maximum transfer rate under conditions of the customer.

Note 5. Use it with EV_{DD} ≥ V_b.

CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Remark p: CSI number (p = 00, 01, 10 and 11), m: Unit number (m = 0), n: Channel number (n = 0 to 3), g: PIM and POM numbers (g = 0, 2, 3 to 5 and 12)

(9) Communication at different potential (1.8 V, 2.5 V, 3.0 V) (CSI mode) (slave mode, SCKp... external clock input)

(T_A = -40 to 85°C, 1.8 V ≤ EV_{DD} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LP (Low-power main) mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time Note 1	t_{KCY2}	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V	20 MHz < f_{MCK} ≤ 24 MHz	12/f_{MCK}		—		—		—		ns
			8 MHz < f_{MCK} ≤ 20 MHz	10/f_{MCK}		—		—		—		ns
			4 MHz < f_{MCK} ≤ 8 MHz	8/f_{MCK}		16/f_{MCK}		—		—		ns
			f_{MCK} ≤ 4 MHz	6/f_{MCK}		10/f_{MCK}		10/f_{MCK}		10/f_{MCK}		ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V	20 MHz < f_{MCK} ≤ 24 MHz	16/f_{MCK}		—		—		—		ns
			16 MHz < f_{MCK} ≤ 20 MHz	14/f_{MCK}		—		—		—		ns
			8 MHz < f_{MCK} ≤ 16 MHz	12/f_{MCK}		—		—		—		ns
			4 MHz < f_{MCK} ≤ 8 MHz	8/f_{MCK}		16/f_{MCK}		—		—		ns
			f_{MCK} ≤ 4 MHz	6/f_{MCK}		10/f_{MCK}		10/f_{MCK}		10/f_{MCK}		ns
		1.8 V ≤ EV_{DD} < 2.7 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2	20 MHz < f_{MCK} ≤ 24 MHz	36/f_{MCK}		—		—		—		ns
			16 MHz < f_{MCK} ≤ 20 MHz	32/f_{MCK}		—		—		—		ns
			8 MHz < f_{MCK} ≤ 16 MHz	26/f_{MCK}		—		—		—		ns
			4 MHz < f_{MCK} ≤ 8 MHz	16/f_{MCK}		16/f_{MCK}		—		—		ns
			f_{MCK} ≤ 4 MHz	10/f_{MCK}		10/f_{MCK}		10/f_{MCK}		10/f_{MCK}		ns
SCKp high-/low-level width	t_{KH2}, t_{KL2}	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V		t_{KCY2}/2 - 12		t_{KCY2}/2 - 50		t_{KCY2}/2 - 50		t_{KCY2}/2 - 50		ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V		t_{KCY2}/2 - 18		t_{KCY2}/2 - 50		t_{KCY2}/2 - 50		t_{KCY2}/2 - 50		ns
		1.8 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2		t_{KCY2}/2 - 50		t_{KCY2}/2 - 50		t_{KCY2}/2 - 50		t_{KCY2}/2 - 50		ns
SIp setup time (to SCKp↑) Note 3	t_{SIK2}	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V		1/f_{MCK} + 20		1/f_{MCK} + 30		1/f_{MCK} + 30		1/f_{MCK} + 30		ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V		1/f_{MCK} + 20		1/f_{MCK} + 30		1/f_{MCK} + 30		1/f_{MCK} + 30		ns
		1.8 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2		1/f_{MCK} + 30		1/f_{MCK} + 30		1/f_{MCK} + 30		1/f_{MCK} + 30		ns
SIp hold time (from SCKp↑) Note 3	t_{KSI2}			1/f_{MCK} + 31		1/f_{MCK} + 31		1/f_{MCK} + 31		1/f_{MCK} + 31		ns
Delay time from SCKp↓ to SOp output Note 4	t_{KSO2}	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ			2/f_{MCK} + 120		2/f_{MCK} + 573		2/f_{MCK} + 573		2/f_{MCK} + 573	ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ			2/f_{MCK} + 214		2/f_{MCK} + 573		2/f_{MCK} + 573		2/f_{MCK} + 573	ns
		1.8 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2, C_b = 30 pF, R_b = 5.5 kΩ			2/f_{MCK} + 573		2/f_{MCK} + 573		2/f_{MCK} + 573		2/f_{MCK} + 573	ns

(**Notes, Caution** and **Remarks** are listed on the next page.)

2.6 Analog Characteristics

2.6.1 A/D converter characteristics

Classification of A/D converter characteristics

Input channel \ Reference Voltage	Reference voltage (+) = AV_{REFP} Reference voltage (-) = AV_{REFM}	Reference voltage (+) = V_{DD} Reference voltage (-) = V_{SS}	Reference voltage (+) = V_{BGR} Reference voltage (-)= AV_{REFM}
ANI0 to ANI3	Refer to **2.6.1 (1)**.	Refer to **2.6.1 (3)**.	Refer to **2.6.1 (4)**.
ANI16 to ANI22	Refer to **2.6.1 (2)**.		
Internal reference voltage Temperature sensor output voltage	Refer to **2.6.1 (1)**.		—

(1) When reference voltage (+) = AV_{REFP}/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (-) = AV_{REFM}/ANI1 (ADREFM = 1), target pin: ANI2 and ANI3, internal reference voltage, and temperature sensor output voltage

(T_A = -40 to +85°C, 1.6 V ≤ AV_{REFP} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V, Reference voltage (+) = AV_{REFP}, Reference voltage (-) = AV_{REFM} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error Note 1	AINL	10-bit resolution AV_{REFP} = V_{DD} Note 3	1.8 V ≤ AV_{REFP} ≤ 5.5 V		1.2	±3.5	LSB
			1.6 V ≤ AV_{REFP} ≤ 5.5 V Note 4		1.2	±7.0	LSB
Conversion time	tCONV	10-bit resolution Target pin: ANI2 and ANI3	3.6 V ≤ V_{DD} ≤ 5.5 V	2.125		39	μs
			2.7 V ≤ V_{DD} ≤ 5.5 V	3.1875		39	μs
			1.8 V ≤ V_{DD} ≤ 5.5 V	17		39	μs
			1.6 V ≤ V_{DD} ≤ 5.5 V	57		95	μs
		10-bit resolution Target pin: Internal reference voltage, and temperature sensor output voltage	3.6 V ≤ V_{DD} ≤ 5.5 V	2.375		39	μs
			2.7 V ≤ V_{DD} ≤ 5.5 V	3.5625		39	μs
			1.8 V ≤ V_{DD} ≤ 5.5 V	17		39	μs
Zero-scale error Notes 1, 2	EZS	10-bit resolution AV_{REFP} = V_{DD} Note 3	1.8 V ≤ AV_{REFP} ≤ 5.5 V			±0.25	%FSR
			1.6 V ≤ AV_{REFP} ≤ 5.5 V Note 4			±0.50	%FSR
Full-scale error Notes 1, 2	EFS	10-bit resolution AV_{REFP} = V_{DD} Note 3	1.8 V ≤ AV_{REFP} ≤ 5.5 V			±0.25	%FSR
			1.6 V ≤ AV_{REFP} ≤ 5.5 V Note 4			±0.50	%FSR
Integral linearity error Note 1	ILE	10-bit resolution AV_{REFP} = V_{DD} Note 3	1.8 V ≤ AV_{REFP} ≤ 5.5 V			±2.5	LSB
			1.6 V ≤ AV_{REFP} ≤ 5.5 V Note 4			±5.0	LSB
Differential linearity error Note 1	DLE	10-bit resolution AV_{REFP} = V_{DD} Note 3	1.8 V ≤ AV_{REFP} ≤ 5.5 V			±1.5	LSB
			1.6 V ≤ AV_{REFP} ≤ 5.5 V Note 4			±2.0	LSB
Analog input voltage	VAIN	ANI2 and ANI3		0		AV_{REFP}	V
		Internal reference voltage (1.8 V ≤ V_{DD} ≤ 5.5 V)		V_{BGR} Note 5			V
		Temperature sensor output voltage (1.8 V ≤ V_{DD} ≤ 5.5 V)		V_{TMPS25} Note 5			V

Note 1. Excludes quantization error (±1/2 LSB).

Note 2. This value is indicated as a ratio (%FSR) to the full-scale value.

Note 3. When AV_{REFP} < V_{DD}, the MAX. values are as follows.

Overall error: Add ±1.0 LSB to the MAX. value when AV_{REFP} = V_{DD}.

Zero-scale error/Full-scale error: Add ±0.05%FSR to the MAX. value when AV_{REFP} = V_{DD}.

Integral linearity error/ Differential linearity error: Add ±0.5 LSB to the MAX. value when AV_{REFP} = V_{DD}.

Note 4. Values when the conversion time is set to 57 μs (min.) and 95 μs (max.).

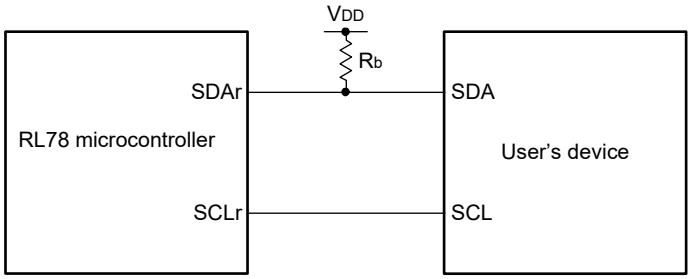
Note 5. Refer to **2.6.2 Temperature sensor characteristics/internal reference voltage characteristic**.

(T_A = -40 to +105°C, 2.4 V ≤ EV_{DD} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) **(5/5)**

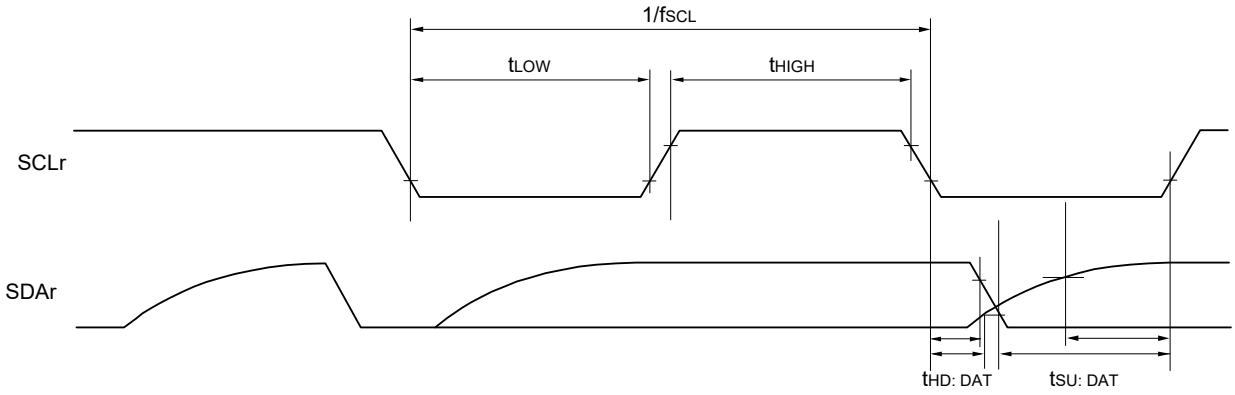
Items	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Input leakage current, high	I_{LIH1}	P00, P01, P30 to P33, P40, and P51 to P56	$V_I = EV_{DD}$				1	μA
	I_{LIH2}	P20 to P23, P125, P137, $\overline{RESET}$	$V_I = V_{DD}$				1	μA
	I_{LIH3}	P121, P122, X1, X2, EXCLK	$V_I = V_{DD}$	In input port or external clock input			1	μA
				In resonator connection			10	μA
Input leakage current, low	I_{LIL1}	P00, P01, P30 to P33, P40, and P51 to P56	$V_I = V_{SS}$				-1	μA
	I_{LIL2}	P20 to P23, P125, P137, $\overline{RESET}$	$V_I = V_{SS}$				-1	μA
	I_{LIL3}	P121, P122, X1, X2, EXCLK	$V_I = V_{SS}$	In input port or external clock input			-1	μA
				In resonator connection			-10	μA
On-chip pull-up resistance	R_U	P00, P01, P30 to P33, P40, P51 to P56, P125	$V_I = V_{SS}$, In input port		10	20	100	kΩ

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

Simplified I²C mode connection diagram (during communication at same potential)



Simplified I²C mode serial transfer timing (during communication at same potential)

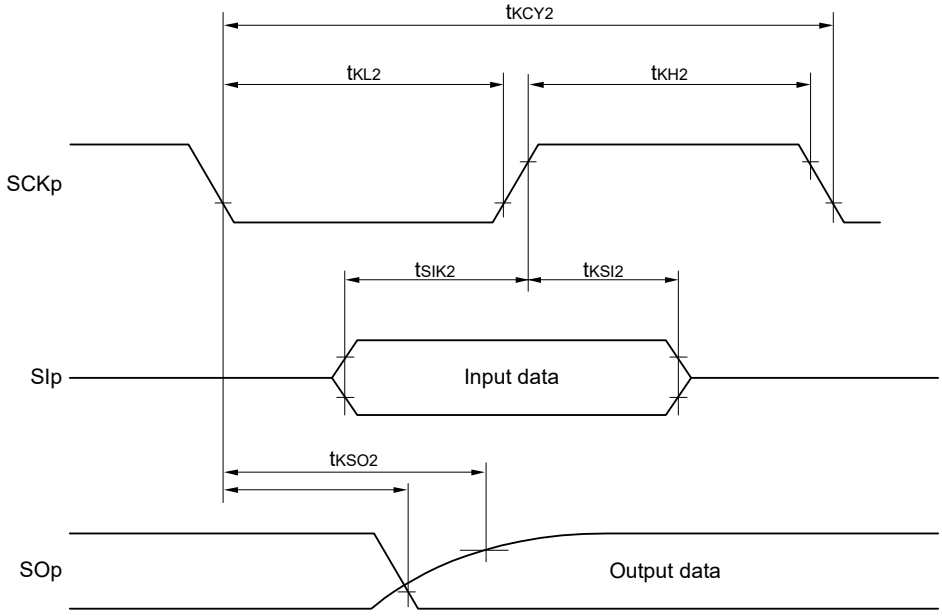


Remark 1. R_b[Ω]: Communication line (SDAr) pull-up resistance, C_b[F]: Communication line (SDAr, SCLr) load capacitance

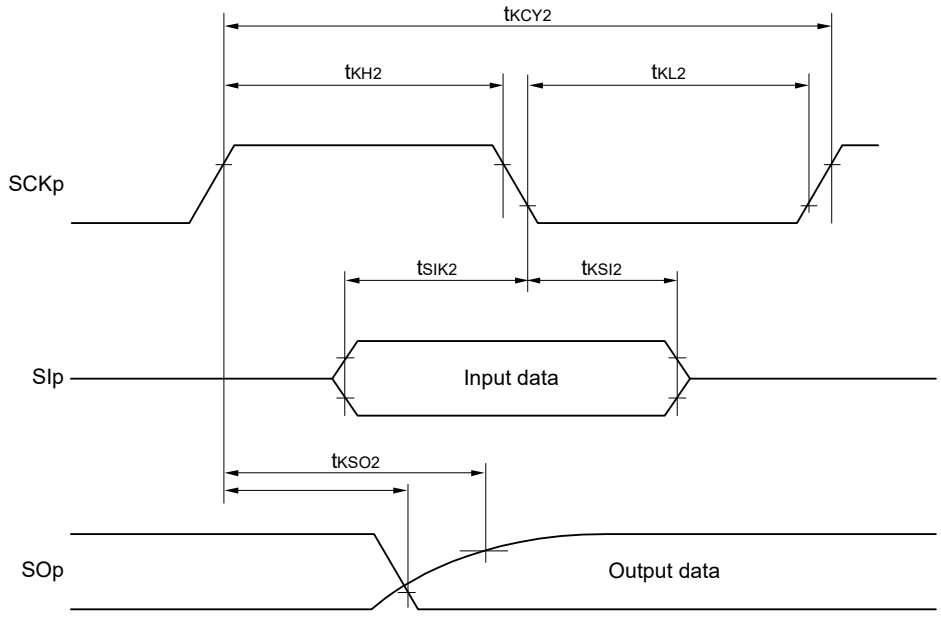
Remark 2. r: IIC number (r = 00, 01, 10 and 11), g: PIM number (g = 0, 3 and 5), h: POM number (h = 0, 3 and 5)

Remark 3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0), n: Channel number (n = 0 to 3), mn = 00 to 03)

CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Remark p: CSI number (p = 00, 01, 10 and 11), m: Unit number (m = 0), n: Channel number (n = 0 to 3), g: PIM and POM numbers (g = 0, 2, 3 to 5 and 12)

3.5.2 Serial interface IICA

(T_A = -40 to +105°C, 2.4 V ≤ EV_{DD} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) mode				Unit
			Standard mode		Fast mode		
			MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	f_{SCL}	Fast mode: f_{CLK} ≥ 3.5 MHz	—	—	0	400	kHz
		Standard mode: f_{CLK} ≥ 1 MHz	0	100	—	—	kHz
Setup time of restart condition	$t_{SU: STA}$		4.7		0.6		µs
Hold time Note 1	$t_{HD: STA}$		4.0		0.6		µs
Hold time when SCLA0 = "L"	t_{LOW}		4.7		1.3		µs
Hold time when SCLA0 = "H"	t_{HIGH}		4.0		0.6		µs
Data setup time (reception)	$t_{SU: DAT}$		250		100		ns
Data hold time (transmission) Note 2	$t_{HD: DAT}$		0	3.45	0	0.9	µs
Setup time of stop condition	$t_{SU: STO}$		4.0		0.6		µs
Bus-free time	t_{BUF}		4.7		1.3		µs

Note 1. The first clock pulse is generated after this period when the start/restart condition is detected.

Note 2. The maximum value (MAX.) of $t_{HD: DAT}$ is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

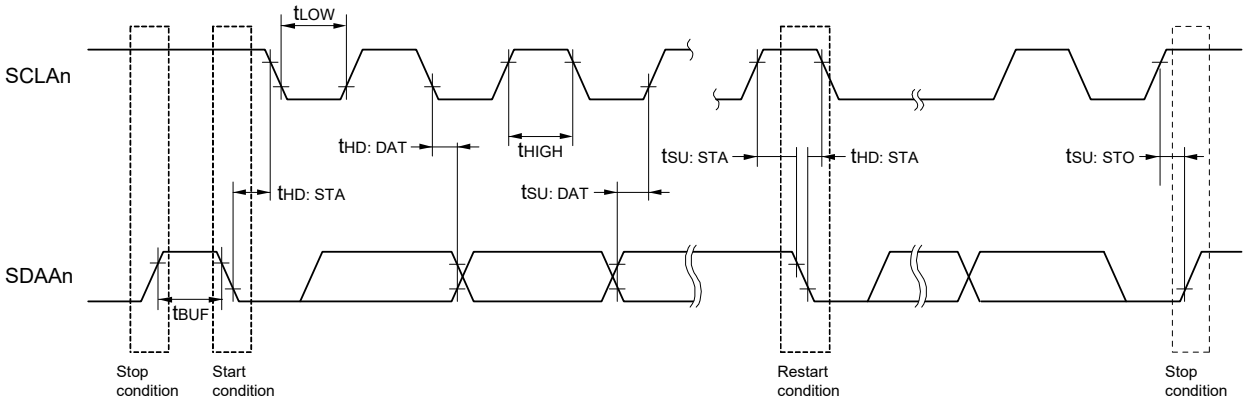
Caution The values in the above table are applied even when bit 2 (PIOR02) in the peripheral I/O redirection register 0 (PIOR0) is 1. At this time, the pin characteristics (I_{OH1}, I_{OL1}, V_{OH1}, V_{OL1}) must satisfy the values in the redirect destination.

Remark The maximum value of C_b (communication line capacitance) and the value of R_b (communication line pull-up resistor) at that time in each mode are as follows.

Standard mode: C_b = 400 pF, R_b = 2.7 kΩ

Fast mode: C_b = 320 pF, R_b = 1.1 kΩ

IICA serial transfer timing



Remark n = 0, 1

(2) When reference voltage (+) = AV_{REFP}/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (-) = AV_{REFM}/ANI1 (ADREFM = 1), target pin: ANI16 to ANI22

(T_A = -40 to +105°C, 2.4 V ≤ EV_{DD} ≤ V_{DD} ≤ 5.5 V, 2.4 V ≤ AV_{REFP} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V,
Reference voltage (+) = AV_{REFP}, Reference voltage (-) = AV_{REFM} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error Note 1	AINL	10-bit resolution EV_{DD} ≤ AV_{REFP} = V_{DD} Notes 3, 4	2.4 V ≤ AV_{REFP} ≤ 5.5 V		1.2	±5.0	LSB
Conversion time	t_{CONV}	10-bit resolution Target ANI pin: ANI16 to ANI22	3.6 V ≤ V_{DD} ≤ 5.5 V	2.125		39	μs
			2.7 V ≤ V_{DD} ≤ 5.5 V	3.1875		39	μs
			2.4 V ≤ V_{DD} ≤ 5.5 V	17		39	μs
Zero-scale error Notes 1, 2	E_{ZS}	10-bit resolution EV_{DD} ≤ AV_{REFP} = V_{DD} Notes 3, 4	2.4 V ≤ AV_{REFP} ≤ 5.5 V			±0.35	%FSR
Full-scale error Notes 1, 2	E_{FS}	10-bit resolution EV_{DD} ≤ AV_{REFP} = V_{DD} Notes 3, 4	2.4 V ≤ AV_{REFP} ≤ 5.5 V			±0.35	%FSR
Integral linearity error Note 1	ILE	10-bit resolution EV_{DD} ≤ AV_{REFP} = V_{DD} Notes 3, 4	2.4 V ≤ AV_{REFP} ≤ 5.5 V			±3.5	LSB
Differential linearity error Note 1	DLE	10-bit resolution EV_{DD} ≤ AV_{REFP} = V_{DD} Notes 3, 4	2.4 V ≤ AV_{REFP} ≤ 5.5 V			±2.0	LSB
Analog input voltage	V_{AIN}	ANI16 to ANI22		0		AV_{REFP} and EV_{DD}	V

Note 1. Excludes quantization error (±1/2 LSB).

Note 2. This value is indicated as a ratio (%FSR) to the full-scale value.

Note 3. When EV_{DD} ≤ AV_{REFP} ≤ V_{DD}, the MAX. values are as follows.

Overall error: Add ±1.0 LSB to the MAX. value when AV_{REFP} = V_{DD}.
Zero-scale error/Full-scale error: Add ±0.05%FSR to the MAX. value when AV_{REFP} = V_{DD}.
Integral linearity error/ Differential linearity error: Add ±0.5 LSB to the MAX. value when AV_{REFP} = V_{DD}.

Note 4. When AV_{REFP} < EV_{DD} ≤ V_{DD}, the MAX. values are as follows.

Overall error: Add ±4.0 LSB to the MAX. value when AV_{REFP} = V_{DD}.
Zero-scale error/Full-scale error: Add ±0.20%FSR to the MAX. value when AV_{REFP} = V_{DD}.
Integral linearity error/ Differential linearity error: Add ±2.0 LSB to the MAX. value when AV_{REFP} = V_{DD}.

3.6.7 LVD circuit characteristics

(1) LVD Detection Voltage of Reset Mode and Interrupt Mode

(T_A = -40 to +105°C, $V_{PDR} \leq EV_{DD} = V_{DD} \leq$.5.5 V, V_{SS} = 0 V)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	Supply voltage level	V_{LVD0}	Power supply rise time	3.90	4.06	4.22	V
			Power supply fall time	3.83	3.98	4.13	V
		V_{LVD1}	Power supply rise time	3.60	3.75	3.90	V
			Power supply fall time	3.53	3.67	3.81	V
		V_{LVD2}	Power supply rise time	3.01	3.13	3.25	V
			Power supply fall time	2.94	3.06	3.18	V
		V_{LVD3}	Power supply rise time	2.90	3.02	3.14	V
			Power supply fall time	2.85	2.96	3.07	V
		V_{LVD4}	Power supply rise time	2.81	2.92	3.03	V
			Power supply fall time	2.75	2.86	2.97	V
		V_{LVD5}	Power supply rise time	2.71	2.81	2.92	V
			Power supply fall time	2.64	2.75	2.86	V
		V_{LVD6}	Power supply rise time	2.61	2.71	2.81	V
			Power supply fall time	2.55	2.65	2.75	V
		V_{LVD7}	Power supply rise time	2.51	2.61	2.71	V
			Power supply fall time	2.45	2.55	2.65	V
Minimum pulse width		t_{LW}		300			μs
Detection delay time						300	μs

(2) LVD Detection Voltage of Interrupt & Reset Mode

(T_A = -40 to +105°C, $V_{PDR} \leq EV_{DD} \leq V_{DD} \leq$ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Interrupt and reset mode	V_{LVDD0}	V_{POC0}, V_{POC1}, V_{POC2} = 0, 1, 1, falling reset voltage		2.64	2.75	2.86	V
	V_{LVDD1}	LVIS0, LVIS1 = 1, 0	Rising release reset voltage	2.81	2.92	3.03	V
			Falling interrupt voltage	2.75	2.86	2.97	V
	V_{LVDD2}	LVIS0, LVIS1 = 0, 1	Rising release reset voltage	2.90	3.02	3.14	V
			Falling interrupt voltage	2.85	2.96	3.07	V
	V_{LVDD3}	LVIS0, LVIS1 = 0, 0	Rising release reset voltage	3.90	4.06	4.22	V
			Falling interrupt voltage	3.83	3.98	4.13	V

3.6.8 Power supply voltage rising slope characteristics

(T_A = -40 to +105°C, V_{SS} = 0 V)

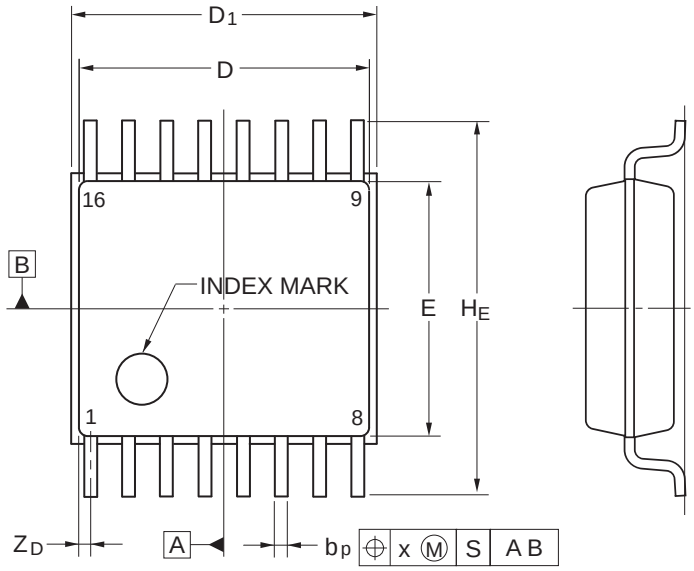
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Power supply voltage rising slope	S_{VDD}				54	V/ms

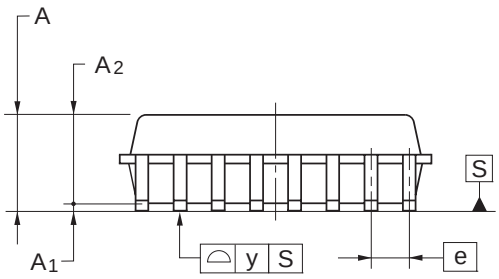
Caution Make sure to keep the internal reset state by the LVD circuit or an external reset until V_{DD} reaches the operating voltage range shown in 3.4 AC Characteristics.

4.2 16-pin products

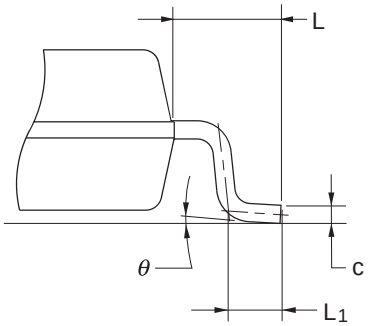
R5F1054AGSP, R5F1054AASP

JEITA Package code	RENESAS code	Previous code	MASS(TYP.)[g]
P-SSOP16-4.4x5-0.65	PRSP0016JC-B	P16MA-65-FAB	0.08



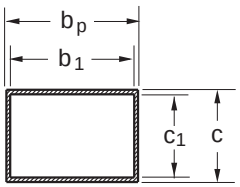


detail of lead end



Referance Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	4.85	5.00	5.15
D_1	5.05	5.20	5.35
E	4.20	4.40	4.60
A_2	—	1.50	—
A_1	0.075	0.125	0.175
A	—	—	1.725
b_p	0.17	0.24	0.32
b_1	—	0.22	—
c	0.14	0.17	0.20
c_1	—	0.15	—
θ	0°	—	8°
H_E	6.20	6.40	6.60
e	—	0.65	—
x	—	—	0.13
y	—	—	0.10
Z_D	—	0.225	—
L	0.35	0.50	0.65
L_1	—	1.00	—

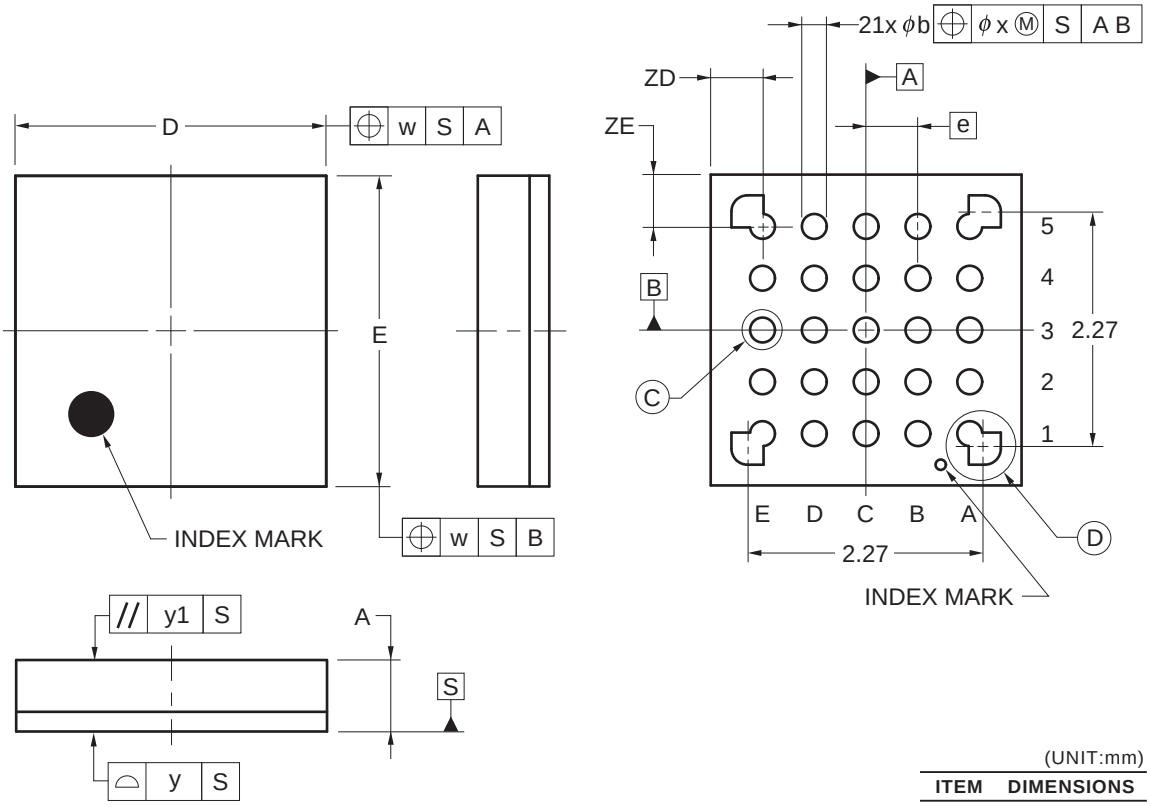
Terminal cross section



4.5 25-pin products

R5F1058AGLA, R5F1058AALA

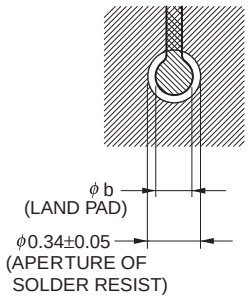
JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-WFLGA25-3x3-0.50	PWLG0025KA-A	P25FC-50-2N2-2	0.01



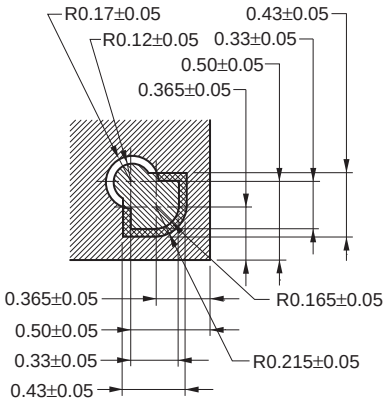
(UNIT:mm)

ITEM	DIMENSIONS
D	3.00±0.10
E	3.00±0.10
w	0.20
e	0.50
A	0.69±0.07
b	0.24±0.05
x	0.05
y	0.08
y1	0.20
ZD	0.50
ZE	0.50

DETAIL OF Ⓒ PART



DETAIL OF Ⓓ PART



Rev.	Date	Description	
		Page	Summary
2.00	Feb 15, 2018	p.13, 14	Modification of table in 1.6 Outline of Functions
		p.18	Modification of 2.2.2 On-chip oscillator characteristics
		p.19, 21	Modification of 2.3.1 Pin characteristics
		p.24	Modification of 2.3.2 Supply current characteristics
		p.32	Modification of 2.4 AC Characteristics
		p.79	Modification of figure in 2.10 Timing of Entry to Flash Memory Programming Modes
		p.84	Modification of 3.2.1 X1 characteristics
		p.84	Modification of 3.2.2 On-chip oscillator characteristics
		p.85, 86, 87	Modification of 3.3.1 Pin characteristics
		p.95	Modification of 3.4 AC Characteristics
		p.99	Modification of note in 3.5.1 Serial array unit (1)
		p.134	Modification of figure in 3.10 Timing of Entry to Flash Memory Programming Modes