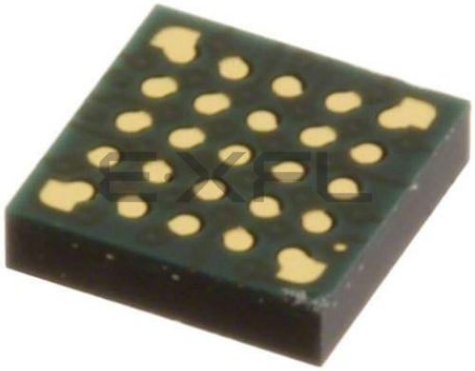

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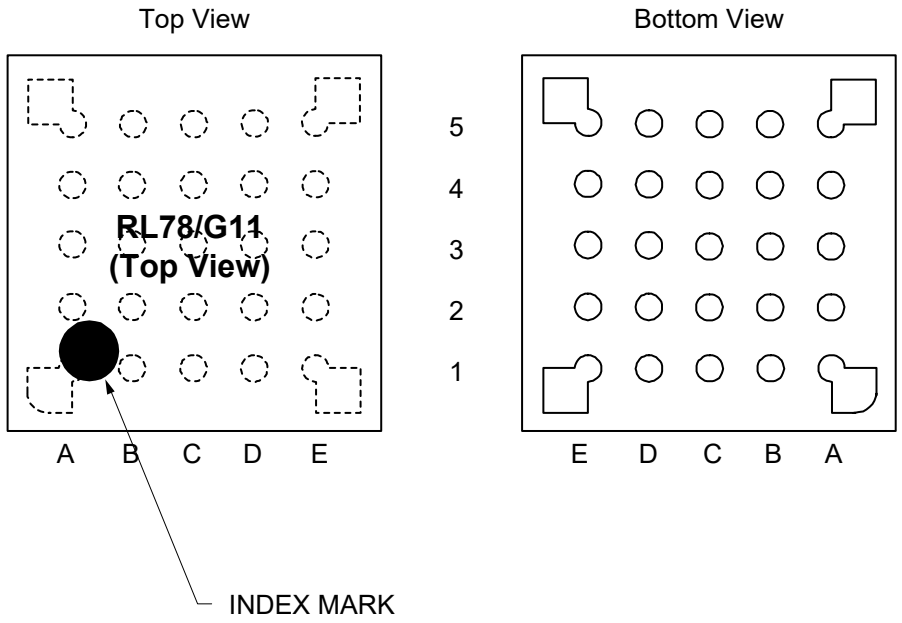
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	RL78
Core Size	16-Bit
Speed	24MHz
Connectivity	CSI, I²C, UART/USART
Peripherals	LVD, POR, WDT
Number of I/O	21
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	1.5K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 11x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	25-WFLGA
Supplier Device Package	25-LGA (3x3)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f1058agla-u0

1.3.5 25-pin products

• 25-pin plastic WFLGA (3 × 3 mm, 0.5 mm pitch)



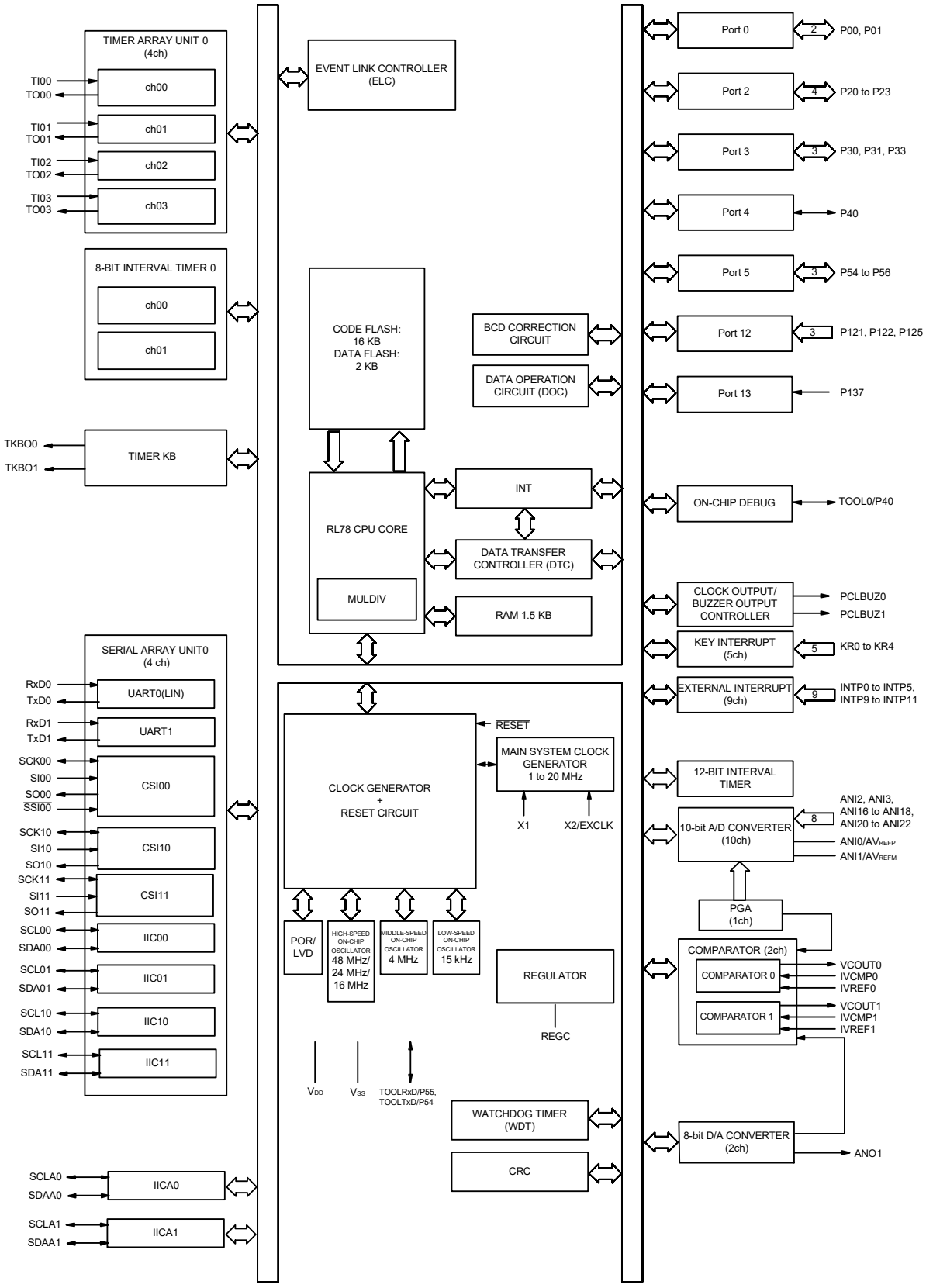
	A	B	C	D	E	
5	P40/TOOL0/TO03/(PCLBUZ0)/SCK10/SCL10/VCOUT0/VCOUT1/INTFO/(SCLA1)	P125/$\overline{\text{RESET}}$/INTP9	P01/ANI16/INTP5/SO10/TxD1	P20/ANI0/AVREFP/IVREF1/(SO10/TxD1)	P21/ANI1/AVREFM/IVREF0	5
4	P122/X2/EXCLK/(SI10/RxD1)/(TI02)/INTP1	P137/INTP0/$\overline{\text{SSI00}}$/(TI03)	P00/ANI17/PCLBUZ1/TI03/(VCOUT1)/SI10/RxD1/SDA10/(SDAA1)	P22/ANI2/PGAI/IVCMP0	P23/ANI3/ANO1/PGAGND	4
3	P121/X1/(TI01)/INTP2/(SI01)	V_{DD}	EV_{DD}	P33/ANI18/IVCMP1/(INTP11)/(SCLA1)	P32/ANI19/SO11/(INTP10)/(VCOUT1)/(SDAA1)	3
2	REGC	V_{SS}	P30/ANI21/KR1/TI00/TO01/INTP3/SCK11/SCL11/(TxD0)/PCLBUZ0/TKBO1/(SDAA0)	P31/ANI20/KR0/TI01/TO00/INTP4/TKBO0/(RxD0)/SI11/SDA11/(SCLA0)	P56/ANI22/KR2/SCK00/SCL00/(SO11)/INTP10/(TO03)/(INTFO)/SCLA1	2
1	P51/KR7/INTP8/(TI02)/(TO02)/SCK01/SCL01/(TxD0)	P52/KR6/INTP7/SI01/SDA01/(RxD0)/(SDAA0)	P53/KR5/INTP6/SO01/SDAA0	P54/KR4/SO00/TxD0/TOOLTXD/(TI03)/(TO03)/SCLA0	P55/KR3/SI00/RxD0/SDA00/TOOLRXD/TI02/TO02/INTP11/(VCOUT0)/SDAA1	1
	A	B	C	D	E	

Caution Connect the REGC pin to Vss pin via a capacitor (0.47 to 1 μF).

Remark 1. For pin identification, see **1.4 Pin Identification**.

Remark 2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0 to 3 (PIOR0 to PIOR3).

<R> 1.5.3 20-pin products



2.2 Oscillator Characteristics

2.2.1 X1 characteristics

(T_A = -40 to +85°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Resonator	Resonator	Conditions	MIN.	TYP.	MAX.	Unit
X1 clock oscillation frequency (f_X) Note	Ceramic resonator/ crystal resonator	2.7 V ≤ V_{DD} ≤ 5.5 V	1.0		20.0	MHz
		2.4 V ≤ V_{DD} < 2.7 V	1.0		16.0	
		1.8 V ≤ V_{DD} < 2.4 V	1.0		8.0	
		1.6 V ≤ V_{DD} < 1.8 V	1.0		4.0	

Note Indicates only permissible oscillator frequency ranges. Refer to **2.4 AC Characteristics** for instruction execution time. Request evaluation by the manufacturer of the oscillator circuit mounted on a board to check the oscillator characteristics.

Caution **Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.**

Remark When using the X1 oscillator, refer to **6.4 System Clock Oscillator** in the RL78/G11 User's Manual.

2.2.2 On-chip oscillator characteristics

(T_A = -40 to +85°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Oscillators	Parameters	Conditions		MIN.	TYP.	MAX.	Unit
High-speed on-chip oscillator clock frequency Notes 1, 2	f_{IH}	2.7 V ≤ V_{DD} ≤ 5.5 V		1		24	MHz
		2.4 V ≤ V_{DD} ≤ 5.5 V		1		16	
		1.8 V ≤ V_{DD} ≤ 5.5 V		1		8	
		1.6 V ≤ V_{DD} ≤ 5.5 V		1		4	
High-speed on-chip oscillator clock frequency accuracy		T_A = -20 to +85°C	1.8 V ≤ V_{DD} ≤ 5.5 V	-1		1	%
			1.6 V ≤ V_{DD} < 1.8 V	-5		5	
		T_A = -40 to -20°C	1.8 V ≤ V_{DD} ≤ 5.5 V	-1.5		1.5	%
			1.6 V ≤ V_{DD} < 1.8 V	-5.5		5.5	
Middle-speed on-chip oscillator oscillation frequency Note 2	f_{IM}			1		4	MHz
Middle-speed on-chip oscillator oscillation frequency accuracy				-12		+12	%
<R> Temperature drift of Middle-speed on-chip oscillator oscillation frequency accuracy	D_{IMT}				0.008		%/°C
<R> Voltage drift of Middle-speed on-chip oscillator oscillation frequency accuracy	D_{IMV}	T_A = 25°C	2.1 V ≤ V_{DD} ≤ 5.5 V		0.02		%/V
			2.0 V ≤ V_{DD} < 2.1 V		-12		
			1.6 V ≤ V_{DD} < 2.0 V		10		
Low-speed on-chip oscillator clock frequency Note 2	f_{IL}				15		kHz
Low-speed on-chip oscillator clock frequency accuracy				-15		+15	%

Note 1. High-speed on-chip oscillator frequency is selected with bits 0 to 3 of the option byte (000C2H) and bits 0 to 2 of the HOCODIV register.

Note 2. This only indicates the oscillator characteristics. Refer to **2.4 AC Characteristics** for instruction execution time.

When P20 is used as TxD1 pin

(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LP (Low-power main) mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Transfer rate		4.0 V ≤ V_{DD} ≤ 5.5 V		f_{MCK}/6 Notes 1, 2, 3		f_{MCK}/6 Notes 1, 2		f_{MCK}/6 Notes 1, 2		f_{MCK}/6 Notes 1, 2	bps
		Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} Notes 1, 3		1.5		1.3		0.1		0.6	Mbps
		2.7 V ≤ V_{DD} ≤ 5.5 V		f_{MCK}/6 Notes 1, 2, 3		f_{MCK}/6 Notes 1, 2		f_{MCK}/6 Notes 1, 2		f_{MCK}/6 Notes 1, 2	bps
		Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} Notes 1, 3		1.2		1.2		0.1		0.6	Mbps
		2.4 V ≤ V_{DD} ≤ 5.5 V		f_{MCK}/6 Notes 1, 2, 3		f_{MCK}/6 Notes 1, 2		f_{MCK}/6 Notes 1, 2		f_{MCK}/6 Notes 1, 2	bps
		Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} Notes 1, 3		1.0		1.0		0.1		0.6	Mbps
		1.8 V ≤ V_{DD} ≤ 5.5 V		Using prohibited		f_{MCK}/6 Notes 1, 2		f_{MCK}/6 Notes 1, 2		f_{MCK}/6 Notes 1, 2	bps
		Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} Notes 1, 3				0.6		0.1		0.6	Mbps
		1.7 V ≤ V_{DD} ≤ 5.5 V				Using prohibited		Using prohibited		f_{MCK}/6 Notes 1, 2	bps
		Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} Notes 1, 3								0.5	Mbps
		1.6 V ≤ V_{DD} ≤ 5.5 V								f_{MCK}/6 Notes 1, 2	bps
		Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} Notes 1, 3								0.5	Mbps

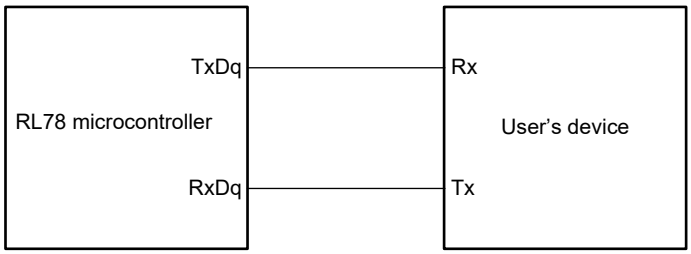
Note 1. f_{MCK} is a frequency selected by setting the CKS bit in the SPS and SMR registers.

Note 2. The transfer rate of 4800 bps is only supported in the SNOOZE mode.
Note that the SNOOZE mode is not supported when fHOCO is 48 MHz.

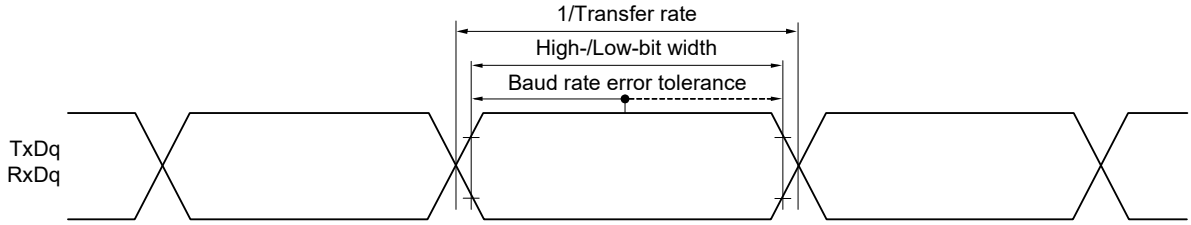
Note 3. f_{CLK} in each operating mode is as follows.:
HS (high-speed main) mode: 24 MHz (2.7 V ≤ V_{DD} ≤ 5.5 V)
16 MHz (2.4 V ≤ V_{DD} ≤ 5.5 V)
LS (low-speed main) mode: 8 MHz (1.8 V ≤ V_{DD} ≤ 5.5 V)
LP (low-power main) mode: 1 MHz (1.8 V ≤ V_{DD} ≤ 5.5 V)
LV (low-voltage main) mode: 4 MHz (1.6 V ≤ V_{DD} ≤ 5.5 V)

Caution Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

UART mode connection diagram (during communication at same potential)



UART mode bit width (during communication at same potential) (reference)

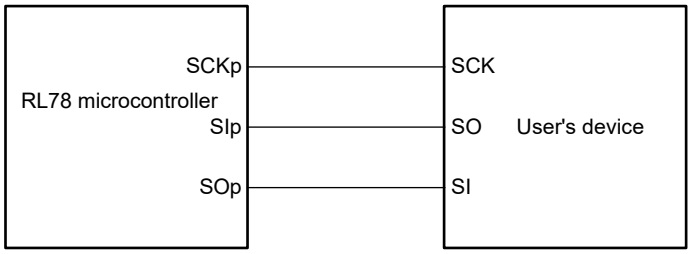


Remark 1. q: UART number (q = 0 and 1), g: PIM and POM number (g = 0, 2, 3 and 5)

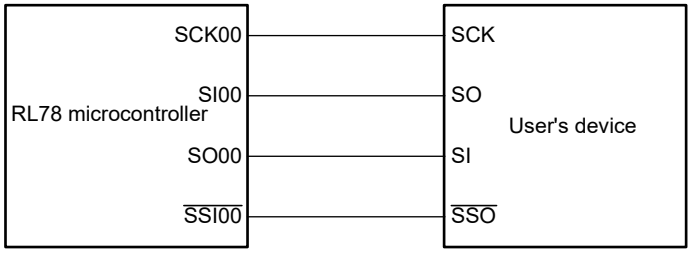
Remark 2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03))

Remark 2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03))

CSI mode connection diagram (during communication at same potential)

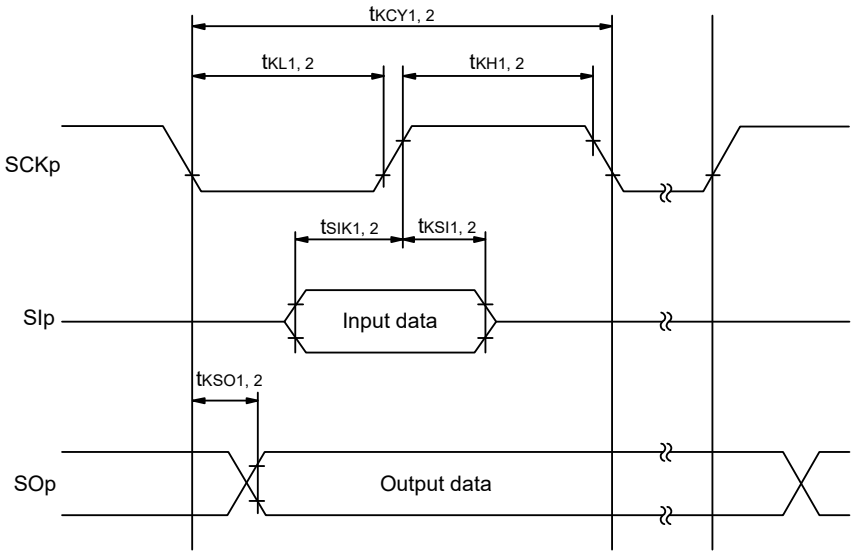


CSI mode connection diagram (during communication at same potential)
(Slave Transmission of slave select input function (CSI00))

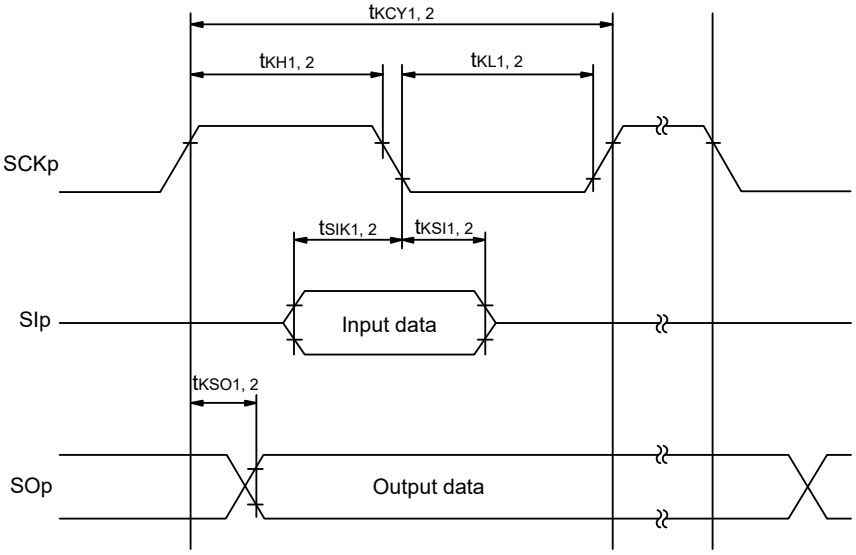


Remark p: CSI number (p = 00, 01, 10 and 11)

CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Remark 1. p: CSI number (p = 00, 01, 10 and 11)
Remark 2. m: Unit number, n: Channel number (mn = 00 to 03)

(5) During communication at same potential (simplified I²C mode)

(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LP (Low-power main) mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLr clock frequency	f_{SCL}	2.7 V ≤ EV_{DD} ≤ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ		1000 Note 1		400 Note 1		250 Note 1		400 Note 1	kHz
		1.8 V ≤ EV_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ		400 Note 1							
		1.8 V ≤ EV_{DD} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ		300 Note 1		300 Note 1		250 Note 1		300 Note 1	
		1.7 V ≤ EV_{DD} < 1.8 V, C_b = 100 pF, R_b = 5 kΩ		250 Note 1		250 Note 1		250 Note 1		250 Note 1	
		1.6 V ≤ EV_{DD} < 1.8 V, C_b = 100 pF, R_b = 5 kΩ		—							
Hold time when SCLr = "L"	t_{LOW}	2.7 V ≤ EV_{DD} ≤ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ	475		1150		1150		1150		ns
		1.8 V ≤ EV_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	1150								
		1.8 V ≤ EV_{DD} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ	1550		1550		1550		1550		
		1.7 V ≤ EV_{DD} < 1.8 V, C_b = 100 pF, R_b = 5 kΩ	1850		1850		1850		1850		
		1.6 V ≤ EV_{DD} < 1.8 V, C_b = 100 pF, R_b = 5 kΩ	—								
Hold time when SCLr = "H"	t_{HIGH}	2.7 V ≤ EV_{DD} ≤ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ	475		1150		1150		1150		ns
		1.8 V ≤ EV_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	1150								
		1.8 V ≤ EV_{DD} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ	1550		1550		1550		1550		
		1.7 V ≤ EV_{DD} < 1.8 V, C_b = 100 pF, R_b = 5 kΩ	1850		1850		1850		1850		
		1.6 V ≤ EV_{DD} < 1.8 V, C_b = 100 pF, R_b = 5 kΩ	—								
Data setup time (reception)	$t_{SU:DAT}$	2.7 V ≤ EV_{DD} ≤ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ	1/f_{MCK} + 85 Note 2		1/f_{MCK} + 145 Note 2		1/f_{MCK} + 145 Note 2		1/f_{MCK} + 145 Note 2		ns
		1.8 V ≤ EV_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	1/f_{MCK} + 145 Note 2								
		1.8 V ≤ EV_{DD} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ	1/f_{MCK} + 230 Note 2		1/f_{MCK} + 230 Note 2		1/f_{MCK} + 230 Note 2		1/f_{MCK} + 230 Note 2		
		1.7 V ≤ EV_{DD} < 1.8 V, C_b = 100 pF, R_b = 5 kΩ	1/f_{MCK} + 290 Note 2		1/f_{MCK} + 290 Note 2		1/f_{MCK} + 290 Note 2		1/f_{MCK} + 290 Note 2		
		1.6 V ≤ EV_{DD} < 1.8 V, C_b = 100 pF, R_b = 5 kΩ	—		—		—				
Data hold time (transmission)	$t_{HD:DAT}$	2.7 V ≤ EV_{DD} ≤ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ	0	305	0	305	0	305	0	305	ns
		1.8 V ≤ EV_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ		355		355		355		355	
		1.8 V ≤ EV_{DD} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ		405		405		405		405	
		1.7 V ≤ EV_{DD} < 1.8 V, C_b = 100 pF, R_b = 5 kΩ									
		1.6 V ≤ EV_{DD} < 1.8 V, C_b = 100 pF, R_b = 5 kΩ	—	—							

Note 6. The smaller maximum transfer rate derived by using f_{MCK}/6 or the following expression is the valid maximum transfer rate.
Expression for calculating the transfer rate when 1.8 V ≤ EV_{DD} < 3.3 V and 1.6 V ≤ V_b ≤ 2.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides

Note 7. This value as an example is calculated when the conditions described in the “Conditions” column are met.
Refer to Note 6 above to calculate the maximum transfer rate under conditions of the customer.

Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (EV_{DD} tolerance) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

(2) I^2C fast mode

(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) mode		LS (low-speed main) mode		LP (Low-power main) mode		LV (low-voltage main) mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	f_{SCL}	Fast mode: f_{CLK} ≥ 3.5 MHz	2.7 V ≤ EV_{DD} ≤ 5.5 V	0	400	0	400	0	400	0	400	kHz
			1.8 V ≤ EV_{DD} ≤ 5.5 V	0	400	0	400	0	400	0	400	kHz
Setup time of restart condition	$t_{SU: STA}$	2.7 V ≤ EV_{DD} ≤ 5.5 V		0.6		0.6		0.6		0.6		µs
		1.8 V ≤ EV_{DD} ≤ 5.5 V		0.6		0.6		0.6		0.6		µs
Hold time Note 1	$t_{HD: STA}$	2.7 V ≤ EV_{DD} ≤ 5.5 V		0.6		0.6		0.6		0.6		µs
		1.8 V ≤ EV_{DD} ≤ 5.5 V		0.6		0.6		0.6		0.6		µs
Hold time when SCLA0 = "L"	t_{LOW}	2.7 V ≤ EV_{DD} ≤ 5.5 V		1.3		1.3		1.3		1.3		µs
		1.8 V ≤ EV_{DD} ≤ 5.5 V		1.3		1.3		1.3		1.3		µs
Hold time when SCLA0 = "H"	t_{HIGH}	2.7 V ≤ EV_{DD} ≤ 5.5 V		0.6		0.6		0.6		0.6		µs
		1.8 V ≤ EV_{DD} ≤ 5.5 V		0.6		0.6		0.6		0.6		µs
Data setup time (reception)	$t_{SU: DAT}$	2.7 V ≤ EV_{DD} ≤ 5.5 V		100		100		100		100		ns
		1.8 V ≤ EV_{DD} ≤ 5.5 V		100		100		100		100		ns
Data hold time (transmission) Note 2	$t_{HD: DAT}$	2.7 V ≤ EV_{DD} ≤ 5.5 V		0	0.9	0	0.9	0	0.9	0	0.9	µs
		1.8 V ≤ EV_{DD} ≤ 5.5 V		0	0.9	0	0.9	0	0.9	0	0.9	µs
Setup time of stop condition	$t_{SU: STO}$	2.7 V ≤ EV_{DD} ≤ 5.5 V		0.6		0.6		0.6		0.6		µs
		1.8 V ≤ EV_{DD} ≤ 5.5 V		0.6		0.6		0.6		0.6		µs
Bus-free time	t_{BUF}	2.7 V ≤ EV_{DD} ≤ 5.5 V		1.3		1.3		1.3		1.3		µs
		1.8 V ≤ EV_{DD} ≤ 5.5 V		1.3		1.3		1.3		1.3		µs

Note 1. The first clock pulse is generated after this period when the start/restart condition is detected.

Note 2. The maximum value (MAX.) of $t_{HD: DAT}$ is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

Caution The values in the above table are applied even when bit 2 (PIOR02) in the peripheral I/O redirection register 0 (PIOR0) is 1. At this time, the pin characteristics (I_{OH1}, I_{OL1}, V_{OH1}, V_{OL1}) must satisfy the values in the redirect destination.

Remark The maximum value of C_b (communication line capacitance) and the value of R_b (communication line pull-up resistor) at that time in each mode are as follows.

Fast mode: C_b = 320 pF, R_b = 1.1 kΩ

(4) When reference voltage (+) = Internal reference voltage (ADREFP1 = 1, ADREFP0 = 0), reference voltage (-) = AV_{REFM}/ANI1 (ADREFM = 1), target pin: ANI0, ANI2 and ANI3, ANI16 to ANI22

(T_A = -40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, 1.6 V ≤ EV_{DD} ≤ V_{DD}, V_{SS} = 0 V, Reference voltage (+) = V_{BGR} Note 3, Reference voltage (-) = AV_{REFM} = 0 V Note 4, HS (high-speed main) mode)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	RES		8			bit
Conversion time	t_{CONV}		17		39	μs
Zero-scale error Notes 1, 2	E_{ZS}				±0.60	% FSR
Integral linearity error Note 1	ILE				±2.0	LSB
Differential linearity error Note 1	DLE				±1.0	LSB
Analog input voltage	V_{AIN}		0		V_{BGR} Note 3	V

Note 1. Excludes quantization error (±1/2 LSB).

Note 2. This value is indicated as a ratio (% FSR) to the full-scale value.

Note 3. Refer to **2.6.2 Temperature sensor characteristics/internal reference voltage characteristic**.

Note 4. When reference voltage (-) = V_{SS}, the MAX. values are as follows.

Zero-scale error: Add ±0.35%FSR to the MAX. value when reference voltage (-) = AV_{REFM}.

Integral linearity error: Add ±0.5 LSB to the MAX. value when reference voltage (-) = AV_{REFM}.

Differential linearity error: Add ±0.2 LSB to the MAX. value when reference voltage (-) = AV_{REFM}.

3.1 Absolute Maximum Ratings

(1/2)

Parameter	Symbols	Conditions	Ratings	Unit
Supply voltage	V_{DD}, EV_{DD}	$V_{DD} \leq EV_{DD}$	-0.5 to + 6.5	V
	AV_{REFP}		0.3 to V_{DD} + 0.3 Note 2	V
	AV_{REFM}		-0.3 to V_{DD} + 0.3 Note 2 and $AV_{REFM} \leq AV_{REFP}$	V
REGC pin input voltage	V_{IREGC}	REGC	-0.3 to + 2.8 and -0.3 to V_{DD} + 0.3 Note 1	V
Input voltage	V_{I1}	P00, P01, P30 to P33, P40, and P51 to P56	-0.3 to EV_{DD} + 0.3 and -0.3 to V_{DD} + 0.3 Note 2	V
	V_{I2}	P20 to P23, P121, P122, P125, P137, EXCLK, $\overline{\text{RESET}}$	-0.3 to V_{DD} + 0.3 Note 2	V
Output voltage	V_{O1}	P00, P01, P30 to P33, P40, and P51 to P56	-0.3 to EV_{DD} + 0.3 and -0.3 to V_{DD} + 0.3 Note 2	V
	V_{O2}	P20 to P23	-0.3 to V_{DD} + 0.3 Note 2	V
Analog input voltage	V_{AI1}	ANI16 to ANI22	-0.3 to EV_{DD} + 0.3 and -0.3 to AV_{REF}(+) + 0.3 Notes 2, 3	V
	V_{AI2}	ANI0 to ANI3	-0.3 to V_{DD} + 0.3 and -0.3 to AV_{REF}(+) + 0.3 Notes 2, 3	V

Note 1. Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μF). This value regulates the absolute maximum rating of the REGC pin. Do not use this pin with voltage applied to it.

Note 2. Must be 6.5 V or lower.

Note 3. Do not exceed AV_{REF} (+) + 0.3 V in case of A/D conversion target pin.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark 1. Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

Remark 2. AV_{REF} (+): + side reference voltage of the A/D converter.

Remark 3. V_{SS}: Reference voltage

(T_A = -40 to +105°C, 2.4 V ≤ EV_{DD} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) **(2/5)**

<R>

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, low Note 1	I_{OL1}	Per pin for P00, P01, P30 to P33, P40, and P51 to P56				8.5 Note 2	mA
		Total of P00, P01, and P40 (When duty ≤ 70% Note 3)	4.0 V ≤ EV_{DD} ≤ 5.5 V			-36.0	mA
			2.7 V ≤ EV_{DD} < 4.0 V			15.0	mA
			2.4 V ≤ EV_{DD} < 2.7 V			9.0	mA
		Total of P30 to P33, and P51 to P56 (When duty ≤ 70% Note 3)	4.0 V ≤ EV_{DD} ≤ 5.5 V			40.0	mA
			2.7 V ≤ EV_{DD} < 4.0 V			35.0	mA
			2.4 V ≤ EV_{DD} < 2.7 V			20.0	mA
		Total of all pins (When duty ≤ 70% Note 3)				76.0	mA
	I_{OL2}	Per pin for P20 to P23				0.4 Note 2	mA
		Total of all pins (When duty ≤ 70% Note 3)	2.4 V ≤ V_{DD} ≤ 5.5 V			1.6	mA

Note 1. Value of current at which the device operation is guaranteed even if the current flows from an output pin to the V_{SS} pin.

Note 2. Do not exceed the total current value.

Note 3. Specification under conditions where the duty factor ≤ 70%.
The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = (I_{OL} × 0.7)/(n × 0.01)

<Example> Where n = 80% and I_{OL} = 10.0 mA
Total output current of pins = (10.0 × 0.7)/(80 × 0.01) ≈ 8.7 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor.
A current higher than the absolute maximum rating must not flow into one pin.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T_A = -40 to +105°C, 2.4 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = 0 V) **(4/5)**

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output voltage, high	V_{OH1}	P00, P01, P30 to P33, P40, and P51 to P56	4.0 V ≤ EV_{DD} ≤ 5.5 V, I_{OH} = -3.0 mA	EV_{DD} - 0.7			V
			2.7 V ≤ EV_{DD} ≤ 5.5 V, I_{OH} = -2.0 mA	EV_{DD} - 0.6			V
			2.4 V ≤ EV_{DD} ≤ 5.5 V I_{OH} = -1.5 mA	EV_{DD} - 0.5			V
	V_{OH2}	P20 to P23	2.4 V ≤ V_{DD} ≤ 5.5 V, I_{OH} = -100 μA	V_{DD} - 0.5			V
Output voltage, low	V_{OL1}	P00, P01, P30 to P33, P40, and P51 to P56	4.0 V ≤ EV_{DD} ≤ 5.5 V, I_{OL} = 8.5 mA			0.7	V
			2.7 V ≤ EV_{DD} ≤ 5.5 V, I_{OL} = 3.0 mA			0.6	V
			2.7 V ≤ EV_{DD} ≤ 5.5 V, I_{OL} = 1.5 mA			0.4	V
			2.4 V ≤ EV_{DD} ≤ 5.5 V, I_{OL} = 0.6 mA			0.4	V
	V_{OL2}	P20 to P23	2.4 V ≤ V_{DD} ≤ 5.5 V, I_{OL} = 400 μA			0.4	V

Caution P00, P01, P20, P30 to P33, P40 and P51 to P56 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

3.5.1 Serial array unit

(1) during communication at same potential (UART mode)

When P01, P30, P31 and P54 are used as TxDq pin

(T_A = -40 to +105°C, 2.4 V ≤ EV_{DD} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
Transfer rate		Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} = 24 MHz		$f_{MCK}/12$ Notes 1, 2	bps
				2.0	Mbps

Note 1. Transfer rate in the SNOOZE mode is 4800 bps only.

Note 2. The maximum operating frequencies of the CPU/peripheral hardware clock (f_{CLK}) are:
HS (high-speed main) mode:
2.4 V ≤ EV_{DD} ≤ 2.7 V: MAX. 1.3 Mbps

Caution Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

When P20 is used as TxD1 pin

(T_A = -40 to +105°C, 2.4 V ≤ EV_{DD} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
Transfer rate		4.0 V ≤ V_{DD} ≤ 5.5 V		$f_{MCK}/16$ Note	bps
		Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} = 24 MHz		1.5	Mbps
		2.7 V ≤ V_{DD} ≤ 5.5 V		$f_{MCK}/20$ Note	bps
		Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} = 24 MHz		1.2	Mbps
		2.4 V ≤ V_{DD} ≤ 5.5 V		$f_{MCK}/16$ Note	bps
		Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} = 16 MHz		1.0	Mbps

<R> **Note** Transfer rate in the SNOOZE mode is 4800 bps only. When f_{HOCO} = 48 MHz, SNOOZE mode is not supported.

(3) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input)

When P01, P32, P53, P54 and P56 are used as SOmn pins

(T_A = -40 to +105°C, 2.4 V ≤ EV_{DD} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) (1/2)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		Unit
				MIN.	MAX.	
SCKp cycle time Note 4	t_{KCY2}	4.0 V ≤ EV_{DD} ≤ 5.5 V	f_{MCK} > 20 MHz	16/f_{MCK}		ns
			f_{MCK} ≤ 20 MHz	12/f_{MCK}		ns
		2.7 V ≤ EV_{DD} < 4.0 V	f_{MCK} > 16 MHz	16/f_{MCK}		ns
			f_{MCK} ≤ 16 MHz	12/f_{MCK}		ns
		2.4 V ≤ EV_{DD} < 2.7 V		12/f_{MCK} and 1000		ns
SCKp high-/low-level width	t_{KH2}, t_{KL2}	4.0 V ≤ EV_{DD} ≤ 5.5 V		t_{KCY2}/2 - 14		ns
	t_{KH2}, t_{KL2}	2.7 V ≤ EV_{DD} < 4.0 V		t_{KCY2}/2 - 16		ns
		2.4 V ≤ EV_{DD} < 2.7 V		t_{KCY2}/2 - 36		ns
SIp setup time (to SCKp↑) Note 1	t_{SIK2}	2.7 V ≤ EV_{DD} ≤ 5.5 V		1/f_{MCK} + 40		ns
		2.4 V ≤ EV_{DD} < 2.7 V		1/f_{MCK} + 60		ns
SIp hold time (from SCKp↑) Note 1	t_{KSI2}			1/f_{MCK} + 62		ns
Delay time from SCKp↓ to SOp output Note 2	t_{KSO2}	C = 30 pF Note 3	2.7 V ≤ EV_{DD} ≤ 5.5 V		2/f_{MCK} + 66	ns
			2.4 V ≤ EV_{DD} < 2.7 V		2/f_{MCK} + 113	ns

Note 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 3. C is the load capacitance of the SOp output lines.

Note 4. The maximum transfer rate when using the SNOOZE mode is 1 Mbps.

Caution Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remark 1. p: CSI number (p = 00, 01, 10 and 11), m: Unit number (m = 0), n: Channel number (n = 0 to 3), g: PIM and POM numbers (g = 0, 2, 3 to 5 and 12)

Remark 2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03))

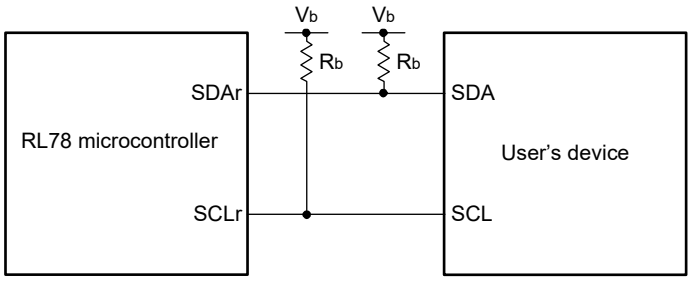
Note 1. The value must be equal to or less than f_{MCK}/4.

Note 2. Use it with $EV_{DD} \geq V_b$.

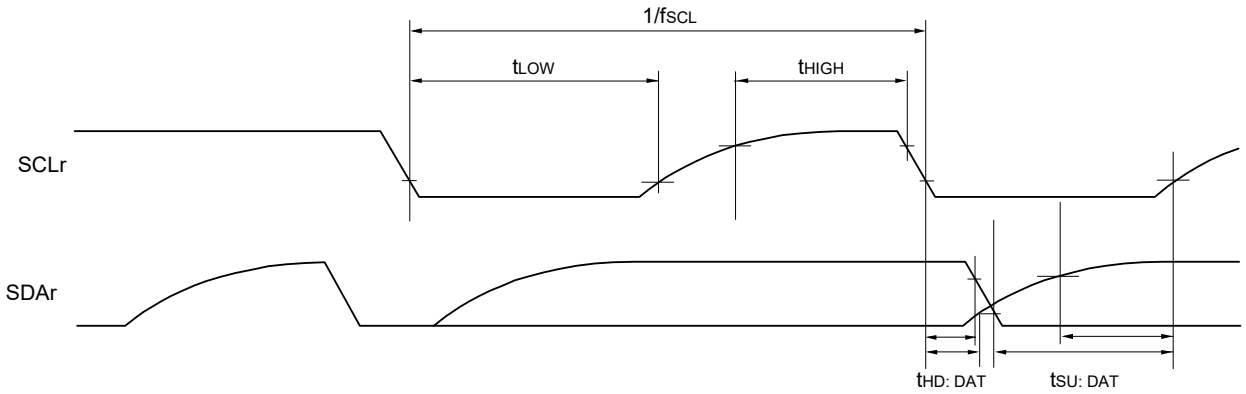
Note 3. Set the f_{MCK} value to keep the hold time of SCLr = "L" and SCLr = "H".

Caution Select the TTL input buffer and the N-ch open drain output (EV_{DD} tolerance) mode for the SDAr pin and the N-ch open drain output (EV_{DD} tolerance) mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

Simplified I²C mode connection diagram (during communication at different potential)



Simplified I²C mode serial transfer timing (during communication at different potential)



Remark 1. R_b[Ω]: Communication line (SDAr, SCLr) pull-up resistance, C_b[F]: Communication line (SDAr, SCLr) load capacitance, V_b[V]: Communication line voltage

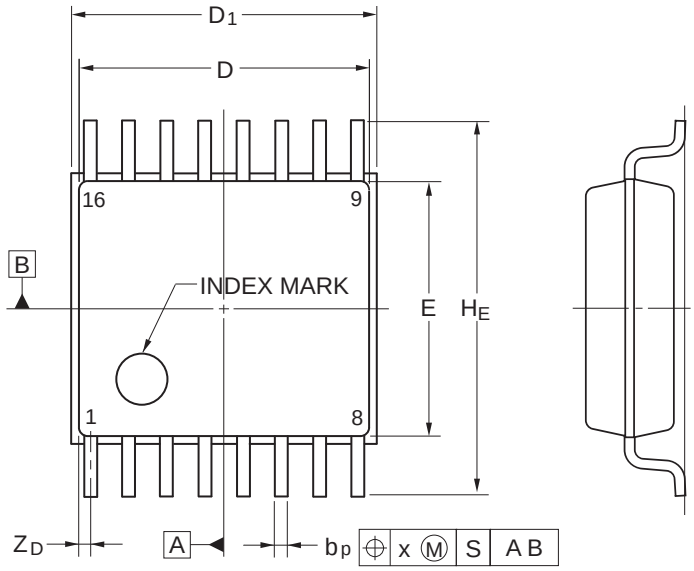
Remark 2. r: IIC number (r = 00, 01, 10 and 11), g: PIM, POM number (g = 0, 3 and 5)

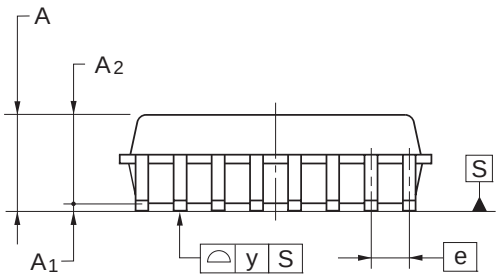
Remark 3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0), n: Channel number (n = 0 to 3), mn = 00 to 03)

4.2 16-pin products

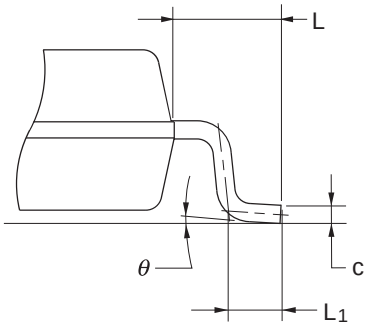
R5F1054AGSP, R5F1054AASP

JEITA Package code	RENESAS code	Previous code	MASS(TYP.)[g]
P-SSOP16-4.4x5-0.65	PRSP0016JC-B	P16MA-65-FAB	0.08



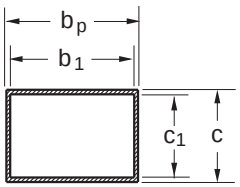


detail of lead end



Referance Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	4.85	5.00	5.15
D_1	5.05	5.20	5.35
E	4.20	4.40	4.60
A_2	—	1.50	—
A_1	0.075	0.125	0.175
A	—	—	1.725
b_p	0.17	0.24	0.32
b_1	—	0.22	—
c	0.14	0.17	0.20
c_1	—	0.15	—
θ	0°	—	8°
H_E	6.20	6.40	6.60
e	—	0.65	—
x	—	—	0.13
y	—	—	0.10
Z_D	—	0.225	—
L	0.35	0.50	0.65
L_1	—	1.00	—

Terminal cross section



REVISION HISTORY	RL78/G11 Datasheet

Rev.	Date	Description	
		Page	Summary
0.50	Mar 31 2016	—	First Edition issued
1.00	Sep 28 2016	p.7	Modification of Pin Configuration in 1.3.3 25-pin products
		p.9	Addition of 1.5.1 20-pin products
		p.10	Addition of product name and Modification of Block Diagram in 1.5.2 24-pin, 25-pin products
		p.12	Addition of I^2C bus in 1.6 Outline of Functions
		p.15	Modification of Conditions of I_{OH1}, I_{OL1} in 2.1 Absolute Maximum Ratings
		p.16	Modification of High-speed on-chip oscillator clock frequency accuracy and addition of D_{IMT}, D_{IMV} in 2.2.2 On-chip oscillator characteristics
		p.17	Modification of Caution in 2.3.1 Pin characteristics
		p.19	Modification of Input voltage, high and Input voltage, low in 2.3.1 Pin characteristics
		p.19, 20	Modification of Caution in 2.3.1 Pin characteristics
		p.22, 23, 24, 26, 27	Modification of specifications in 2.3.2 Supply current characteristics
		p.29, 30	Modification of specification in 2.4 AC Characteristics
		p.35	Modification of specifications in 2.5.1 Serial array unit (1)
		p.39	Modification of specifications in 2.5.1 Serial array unit (3)
		p.40, 42	Modification of specification in 2.5.1 Serial array unit (4)
		p.62	Addition of LP (Low-power main) mode in 2.5.2 Serial interface IICA (1)
		p.64	Addition of LP (Low-power main) mode in 2.5.2 Serial interface IICA (2)
		p.65	Addition of LP (Low-power main) mode in 2.5.2 Serial interface IICA (3)
		p.70	Modification of Conditions in 2.6.2 Temperature sensor haracteristics/internal reference voltage characteristic
		p.79	Addition of description in 3 ELECTRICAL SPECIFICATIONS (TA = -40 to +105°C)
		p.82	Modification of High-speed on-chip oscillator clock frequency accuracy and addition of D_{IMT}, D_{IMV} in 3.2.2 On-chip oscillator characteristics
		p.83	Modification of Caution in 3.3.1 Pin characteristics
		p.85	Modification of Input voltage, high and Input voltage, low in 3.3.1 Pin characteristics
		p.85, 86	Modification of Caution in 3.3.1 Pin characteristics
		p.88 to 91	Modification of specifications in 3.3.2 Supply current characteristics
		p.97	Modification of specifications and specification table in 3.5.1 Serial array unit (1)
		p.103	Modification of specifications in 3.5.1 Serial array unit (3)
		p.125	Modification of Conditions in 3.6.1 A/D converter characteristics (4)
		p.126	Modification of Conditions in 3.6.2 Temperature sensor haracteristics/internal reference voltage characteristic
1.10	Dec 28 2016	p.4	Modification of 1.2 Ordering Information
2.00	Feb 15, 2018	Throughout	Addition of specifications of 10-pin and 16-pin products
		p.2	Modification of description in 1.1 Features
		p.6	Modification of figure in 1.3.4 24-pin products
		p.11	Modification of figure in 1.5.3 20-pin products
		p.12	Modification of figure in 1.5.4 24-pin, 25-pin products

Rev.	Date	Description	
		Page	Summary
2.00	Feb 15, 2018	p.13, 14	Modification of table in 1.6 Outline of Functions
		p.18	Modification of 2.2.2 On-chip oscillator characteristics
		p.19, 21	Modification of 2.3.1 Pin characteristics
		p.24	Modification of 2.3.2 Supply current characteristics
		p.32	Modification of 2.4 AC Characteristics
		p.79	Modification of figure in 2.10 Timing of Entry to Flash Memory Programming Modes
		p.84	Modification of 3.2.1 X1 characteristics
		p.84	Modification of 3.2.2 On-chip oscillator characteristics
		p.85, 86, 87	Modification of 3.3.1 Pin characteristics
		p.95	Modification of 3.4 AC Characteristics
		p.99	Modification of note in 3.5.1 Serial array unit (1)
		p.134	Modification of figure in 3.10 Timing of Entry to Flash Memory Programming Modes