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### Applications of "[Embedded - Microcontrollers](#)"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	I <sup>2</sup> C, SPI
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	22
Program Memory Size	3.5KB (2K x 14)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 5.5V
Data Converters	A/D 5x8b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	28-DIP (0.300", 7.62mm)
Supplier Device Package	28-SPDIP
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/pic16c72a-04i-sp">https://www.e-xfl.com/product-detail/microchip-technology/pic16c72a-04i-sp</a>

# PIC16C62B/72A

**TABLE 1-1 PIC16C62B/PIC16C72A PINOUT DESCRIPTION**

Pin Name	DIP Pin#	SOIC Pin#	I/O/P Type	Buffer Type	Description
OSC1/CLKIN	9	9	I	ST/CMOS <sup>(3)</sup>	Oscillator crystal input/external clock source input.
OSC2/CLKOUT	10	10	O	—	Oscillator crystal output. Connects to crystal or resonator in crystal oscillator mode. In RC mode, the OSC2 pin outputs CLKOUT which has 1/4 the frequency of OSC1, and denotes the instruction cycle rate.
MCLR/VPP	1	1	I/P	ST	Master clear (reset) input or programming voltage input. This pin is an active low reset to the device.
RA0/AN0 <sup>(4)</sup>	2	2	I/O	TTL	PORTA is a bi-directional I/O port. RA0 can also be analog input 0 RA1 can also be analog input 1 RA2 can also be analog input 2 RA3 can also be analog input 3 or analog reference voltage RA4 can also be the clock input to the Timer0 module. Output is open drain type. RA5 can also be analog input 4 or the slave select for the synchronous serial port.
RA1/AN1 <sup>(4)</sup>	3	3	I/O	TTL	
RA2/AN2 <sup>(4)</sup>	4	4	I/O	TTL	
RA3/AN3/VREF <sup>(4)</sup>	5	5	I/O	TTL	
RA4/T0CKI	6	6	I/O	ST	
RA5/SS/AN4 <sup>(4)</sup>	7	7	I/O	TTL	
RB0/INT	21	21	I/O	TTL/ST <sup>(1)</sup>	PORTB is a bi-directional I/O port. PORTB can be software programmed for internal weak pull-up on all inputs. RB0 can also be the external interrupt pin.  Interrupt on change pin. Interrupt on change pin. Interrupt on change pin. Serial programming clock. Interrupt on change pin. Serial programming data.
RB1	22	22	I/O	TTL	
RB2	23	23	I/O	TTL	
RB3	24	24	I/O	TTL	
RB4	25	25	I/O	TTL	
RB5	26	26	I/O	TTL	
RB6	27	27	I/O	TTL/ST <sup>(2)</sup>	
RB7	28	28	I/O	TTL/ST <sup>(2)</sup>	
RC0/T1OSO/T1CKI	11	11	I/O	ST	PORTC is a bi-directional I/O port. RC0 can also be the Timer1 oscillator output or Timer1 clock input. RC1 can also be the Timer1 oscillator input. RC2 can also be the Capture1 input/Compare1 output/PWM1 output. RC3 can also be the synchronous serial clock input/output for both SPI and I <sup>2</sup> C modes. RC4 can also be the SPI Data In (SPI mode) or data I/O (I <sup>2</sup> C mode). RC5 can also be the SPI Data Out (SPI mode).
RC1/T1OSI	12	12	I/O	ST	
RC2/CCP1	13	13	I/O	ST	
RC3/SCK/SCL	14	14	I/O	ST	
RC4/SDI/SDA	15	15	I/O	ST	
RC5/SDO	16	16	I/O	ST	
RC6	17	17	I/O	ST	
RC7	18	18	I/O	ST	
Vss	8, 19	8, 19	P	—	Ground reference for logic and I/O pins.
VDD	20	20	P	—	Positive supply for logic and I/O pins.

Legend: I = input      O = output      I/O = input/output      P = power or program  
 — = Not used      TTL = TTL input      ST = Schmitt Trigger input

- Note 1:** This buffer is a Schmitt Trigger input when configured as the external interrupt.  
**Note 2:** This buffer is a Schmitt Trigger input when used in serial programming mode.  
**Note 3:** This buffer is a Schmitt Trigger input when configured in RC oscillator mode and a CMOS input otherwise.  
**Note 4:** The A/D module is not available on the PIC16C62B.

## 2.2.2 SPECIAL FUNCTION REGISTERS

The Special Function Registers are registers used by the CPU and Peripheral Modules for controlling the desired operation of the device. These registers are implemented as static RAM. A list of these registers is given in Table 2-1.

The Special Function Registers can be classified into two sets; core (CPU) and peripheral. Those registers associated with the core functions are described in detail in this section. Those related to the operation of the peripheral features are described in detail in the peripheral feature section.

**TABLE 2-1 SPECIAL FUNCTION REGISTER SUMMARY**

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other resets (4)		
<b>Bank 0</b>													
00h	INDF <sup>(1)</sup>	Addressing this location uses contents of FSR to address data memory (not a physical register)								0000 0000	0000 0000		
01h	TMR0	Timer0 module's register								xxxx xxxx	uuuu uuuu		
02h	PCL <sup>(1)</sup>	Program Counter's (PC) Least Significant Byte								0000 0000	0000 0000		
03h	STATUS <sup>(1)</sup>	IRP <sup>(5)</sup>	RP1 <sup>(5)</sup>	RP0	T $\bar{O}$	PD	Z	DC	C	0001 1xxx	000q quuu		
04h	FSR <sup>(1)</sup>	Indirect data memory address pointer								xxxx xxxx	uuuu uuuu		
05h	PORTA <sup>(6,7)</sup>	—	—	PORTA Data Latch when written: PORTA pins when read								--0x 0000	--0u 0000
06h	PORTB <sup>(6,7)</sup>	PORTB Data Latch when written: PORTB pins when read								xxxx xxxx	uuuu uuuu		
07h	PORTC <sup>(6,7)</sup>	PORTC Data Latch when written: PORTC pins when read								xxxx xxxx	uuuu uuuu		
08h-09h	—	Unimplemented								—	—		
0Ah	PCLATH <sup>(1,2)</sup>	—	—	—	Write Buffer for the upper 5 bits of the Program Counter						---0 0000	---0 0000	
0Bh	INTCON <sup>(1)</sup>	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000u		
0Ch	PIR1	—	ADIF <sup>(3)</sup>	—	—	SSPIF	CCP1IF	TMR2IF	TMR1IF	-0-- 0000	-0-- 0000		
0Dh	—	Unimplemented								—	—		
0Eh	TMR1L	Holding register for the Least Significant Byte of the 16-bit TMR1 register								xxxx xxxx	uuuu uuuu		
0Fh	TMR1H	Holding register for the Most Significant Byte of the 16-bit TMR1 register								xxxx xxxx	uuuu uuuu		
10h	T1CON	—	—	T1CKPS1	T1CKPS0	T1OSCEN	T1SYN $\bar{C}$	TMR1CS	TMR1ON	--00 0000	--uu uuuu		
11h	TMR2	Timer2 module's register								0000 0000	0000 0000		
12h	T2CON	—	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0	-000 0000	-000 0000		
13h	SSPBUF	Synchronous Serial Port Receive Buffer/Transmit Register								xxxx xxxx	uuuu uuuu		
14h	SSPCON	WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0	0000 0000	0000 0000		
15h	CCPR1L	Capture/Compare/PWM Register1 (LSB)								xxxx xxxx	uuuu uuuu		
16h	CCPR1H	Capture/Compare/PWM Register1 (MSB)								xxxx xxxx	uuuu uuuu		
17h	CCP1CON	—	—	CCP1X	CCP1Y	CCP1M3	CCP1M2	CCP1M1	CCP1M0	--00 0000	--00 0000		
18h-1Dh	—	Unimplemented								—	—		
1Eh	ADRES <sup>(3)</sup>	A/D Result Register								xxxx xxxx	uuuu uuuu		
1Fh	ADCON0 <sup>(3)</sup>	ADCS1	ADCS0	CHS2	CHS1	CHS0	GO/DONE	—	ADON	0000 00-0	0000 00-0		

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, read as '0', Shaded locations are unimplemented, read as '0'.

- Note 1:** These registers can be addressed from either bank.  
**Note 2:** The upper byte of the program counter is not directly accessible. PCLATH is a holding register for PC<12:8> whose contents are transferred to the upper byte of the program counter.  
**Note 3:** A/D not implemented on the PIC16C62B, maintain as '0'.  
**Note 4:** Other (non power-up) resets include: external reset through  $\overline{MCLR}$  and the Watchdog Timer Reset.  
**Note 5:** The IRP and RP1 bits are reserved. Always maintain these bits clear.  
**Note 6:** On any device reset, these pins are configured as inputs.  
**Note 7:** This is the value that will be in the port output latch.

# PIC16C62B/72A

**TABLE 3-3 PORTB FUNCTIONS**

Name	Bit#	Buffer	Function
RB0/INT	bit0	TTL/ST <sup>(1)</sup>	Input/output pin or external interrupt input. Internal software programmable weak pull-up.
RB1	bit1	TTL	Input/output pin. Internal software programmable weak pull-up.
RB2	bit2	TTL	Input/output pin. Internal software programmable weak pull-up.
RB3	bit3	TTL	Input/output pin. Internal software programmable weak pull-up.
RB4	bit4	TTL	Input/output pin (with interrupt on change). Internal software programmable weak pull-up.
RB5	bit5	TTL	Input/output pin (with interrupt on change). Internal software programmable weak pull-up.
RB6	bit6	TTL/ST <sup>(2)</sup>	Input/output pin (with interrupt on change). Internal software programmable weak pull-up. Serial programming clock.
RB7	bit7	TTL/ST <sup>(2)</sup>	Input/output pin (with interrupt on change). Internal software programmable weak pull-up. Serial programming data.

Legend: TTL = TTL input, ST = Schmitt Trigger input

**Note 1:** This buffer is a Schmitt Trigger input when configured as the external interrupt.

**2:** This buffer is a Schmitt Trigger input when used in serial programming mode.

**TABLE 3-4 SUMMARY OF REGISTERS ASSOCIATED WITH PORTB**

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other resets
06h	PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx xxxx	uuuu uuuu
86h	TRISB	PORTB Data Direction Register								1111 1111	1111 1111
81h	OPTION_REG	RBPU	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111

Legend: x = unknown, u = unchanged. Shaded cells are not used by PORTB.

## 5.2 Timer1 Oscillator

A crystal oscillator circuit is built-in between pins T1OSI (input) and T1OSO (amplifier output). It is enabled by setting control bit T1OSCEN (T1CON<3>). When the Timer1 oscillator is enabled, RC0 and RC1 pins become T1OSO and T1OSI inputs, overriding TRISC<1:0>.

The oscillator is a low power oscillator rated up to 200 kHz. It will continue to run during SLEEP. It is primarily intended for a 32 kHz crystal. Table 5-1 shows the capacitor selection for the Timer1 oscillator.

The Timer1 oscillator is identical to the LP oscillator. The user must provide a software time delay to ensure proper oscillator start-up.

**TABLE 5-1 CAPACITOR SELECTION FOR THE TIMER1 OSCILLATOR**

Osc Type	Freq	C1	C2
LP	32 kHz	33 pF	33 pF
	100 kHz	15 pF	15 pF
	200 kHz	15 pF	15 pF
<b>These values are for design guidance only.</b>			
<b>Crystals Tested:</b>			
32.768 kHz	Epson C-001R32.768K-A	± 20 PPM	
100 kHz	Epson C-2100.00 KC-P	± 20 PPM	
200 kHz	STD XTAL 200.000 kHz	± 20 PPM	
<p><b>Note 1:</b> Higher capacitance increases the stability of oscillator but also increases the start-up time.</p> <p><b>2:</b> Since each resonator/crystal has its own characteristics, the user should consult the resonator/crystal manufacturer for appropriate values of external components.</p>			

**TABLE 5-2 REGISTERS ASSOCIATED WITH TIMER1 AS A TIMER/COUNTER**

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other resets
0Bh,8Bh	INTCON	GIE	PEIE	TOIE	INTE	RBIE	TOIF	INTF	RBIF	0000 000x	0000 000u
0Ch	PIR1	—	ADIF	—	—	SSPIF	CCP1IF	TMR2IF	TMR1IF	-0-- 0000	-0-- 0000
8Ch	PIE1	—	ADIE	—	—	SSPIE	CCP1IE	TMR2IE	TMR1IE	-0-- 0000	-0-- 0000
0Eh	TMR1L	Holding register for the Least Significant Byte of the 16-bit TMR1 register								xxxx xxxx	uuuu uuuu
0Fh	TMR1H	Holding register for the Most Significant Byte of the 16-bit TMR1 register								xxxx xxxx	uuuu uuuu
10h	T1CON	—	—	T1CKPS1	T1CKPS0	T1OSCEN	T1SYNC	TMR1CS	TMR1ON	--00 0000	--uu uuuu

Legend: x = unknown, u = unchanged, - = unimplemented read as '0'. Shaded cells are not used by the Timer1 module.

## 5.3 Timer1 Interrupt

The TMR1 Register pair (TMR1H:TMR1L) increments from 0000h to FFFFh and rolls over to 0000h. The TMR1 Interrupt, if enabled, is generated on overflow and is latched in interrupt flag bit TMR1IF (PIR1<0>). This interrupt can be enabled by setting TMR1 interrupt enable bit TMR1IE (PIE1<0>).

## 5.4 Resetting Timer1 using a CCP Trigger Output

If the CCP module is configured in compare mode to generate a "special event trigger" (CCP1M3:CCP1M0 = 1011), this signal will reset Timer1 and start an A/D conversion (if the A/D module is enabled).

**Note:** The special event trigger from the CCP1 module will not set interrupt flag bit TMR1IF (PIR1<0>).

Timer1 must be configured for either timer or synchronized counter mode to take advantage of this feature. If Timer1 is running in asynchronous counter mode, this reset operation may not work.

In the event that a write to Timer1 coincides with a special event trigger from CCP1, the write will take precedence.

In this mode of operation, the CCPR1H:CCPR1L registers pair effectively becomes the period register for Timer1.

# PIC16C62B/72A

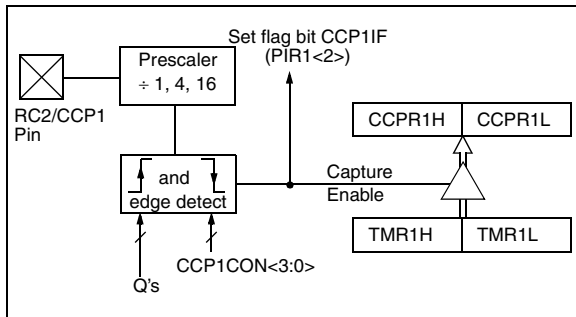
## 7.1 Capture Mode

In Capture mode, CCP1H:CCP1L captures the 16-bit value of the TMR1 register, when an event occurs on pin RC2/CCP1. An event is defined as:

- every falling edge
- every rising edge
- every 4th rising edge
- every 16th rising edge

An event is selected by control bits CCP1M3:CCP1M0 (CCP1CON<3:0>). When a capture is made, the interrupt request flag bit, CCP1IF (PIR1<2>), is set. It must be cleared in software. If another capture occurs before the value in register CCP1 is read, the old captured value will be lost.

**FIGURE 7-1: CAPTURE MODE OPERATION BLOCK DIAGRAM**



### 7.1.1 CCP PIN CONFIGURATION

In Capture mode, the RC2/CCP1 pin should be configured as an input by setting the TRISC<2> bit.

**Note:** If the RC2/CCP1 is configured as an output, a write to the port can cause a capture condition.

### 7.1.2 TIMER1 MODE SELECTION

Timer1 must be running in timer mode or synchronized counter mode for the CCP module to use the capture feature. In asynchronous counter mode, the capture operation may not work consistently.

### 7.1.3 SOFTWARE INTERRUPT

When the Capture mode is changed, a false capture interrupt may be generated. The user should clear CCP1IE (PIE1<2>) before changing the capture mode to avoid false interrupts. Clear the interrupt flag bit, CCP1IF before setting CCP1IE.

### 7.1.4 CCP PRESCALER

There are four prescaler settings, specified by bits CCP1M3:CCP1M0. Whenever the CCP module is turned off, or the CCP module is not in capture mode, the prescaler counter is cleared. This means that any reset will clear the prescaler counter.

Switching from one capture prescaler to another may generate an interrupt. Also, the prescaler counter will not be cleared, therefore the first capture may be from a non-zero prescaler. Example 7-1 shows the recommended method for switching between capture prescalers. This example also clears the prescaler counter and will not generate the “false” interrupt.

**EXAMPLE 7-1: CHANGING BETWEEN CAPTURE PRESCALERS**

```

CLRWF  CCP1CON      ;Turn CCP module off
MOVLW  NEW_CAPT_PS  ;Load the W reg with
                    ; the new prescaler
                    ; mode value and CCP ON
MOVWF  CCP1CON      ;Load CCP1CON with this
                    ; value
    
```

## 7.3.3 SET-UP FOR PWM OPERATION

The following steps should be taken when configuring the CCP module for PWM operation:

1. Set the PWM period by writing to the PR2 register.
2. Set the PWM on-time by writing to the CCPR1L register and CCP1CON<5:4> bits.
3. Make the CCP1 pin an output by clearing the TRISC<2> bit.
4. Set the TMR2 prescale value and enable Timer2 by writing to T2CON.
5. Configure the CCP1 module for PWM operation.

**TABLE 7-4 EXAMPLE PWM FREQUENCIES AND RESOLUTIONS AT 20 MHz**

PWM Frequency	1.22 kHz	4.88 kHz	19.53 kHz	78.12 kHz	156.3 kHz	208.3 kHz
Timer Prescaler (1, 4, 16)	16	4	1	1	1	1
PR2 Value	0xFF	0xFF	0xFF	0x3F	0x1F	0x17
Maximum Resolution (bits)	10	10	10	8	7	5.5

**TABLE 7-5 REGISTERS ASSOCIATED WITH PWM AND TIMER2**

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other resets
0Bh,8Bh	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000u
0Ch	PIR1	—	ADIF	—	—	SSPIF	CCP1IF	TMR2IF	TMR1IF	-0-- 0000	-0-- 0000
8Ch	PIE1	—	ADIE	—	—	SSPIE	CCP1IE	TMR2IE	TMR1IE	-0-- 0000	-0-- 0000
87h	TRISC	PORTC Data Direction Register								1111 1111	1111 1111
11h	TMR2	Timer2 module's register								0000 0000	0000 0000
92h	PR2	Timer2 module's period register								1111 1111	1111 1111
12h	T2CON	—	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0	-000 0000	-000 0000
15h	CCPR1L	Capture/Compare/PWM register1 (LSB)								xxxx xxxx	uuuu uuuu
16h	CCPR1H	Capture/Compare/PWM register1 (MSB)								xxxx xxxx	uuuu uuuu
17h	CCP1CON	—	—	CCP1X	CCP1Y	CCP1M3	CCP1M2	CCP1M1	CCP1M0	--00 0000	--00 0000

Legend: x = unknown, u = unchanged, - = unimplemented read as '0'. Shaded cells are not used by PWM and Timer2.

# PIC16C62B/72A

**TABLE 8-1 REGISTERS ASSOCIATED WITH SPI OPERATION**

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other resets
0Bh,8Bh	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000u
0Ch	PIR1	—	ADIF	—	—	SSPIF	CCP1IF	TMR2IF	TMR1IF	-0-- 0000	-0-- 0000
8Ch	PIE1	—	ADIE	—	—	SSPIE	CCP1IE	TMR2IE	TMR1IE	-0-- 0000	-0-- 0000
13h	SSPBUF	Synchronous Serial Port Receive Buffer/Transmit Register								xxxx xxxx	uuuu uuuu
14h	SSPCON	WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0	0000 0000	0000 0000
94h	SSPSTAT	SMP	CKE	D/ $\bar{A}$	P	S	R/ $\bar{W}$	UA	BF	0000 0000	0000 0000
85h	TRISA	—	—	PORTA Data Direction Register						--11 1111	--11 1111
87h	TRISC	PORTC Data Direction Register								1111 1111	1111 1111

Legend: x = unknown, u = unchanged, - = unimplemented read as '0'. Shaded cells are not used by the SSP in SPI mode.



# PIC16C62B/72A

## 10.2 Oscillator Configurations

### 10.2.1 OSCILLATOR TYPES

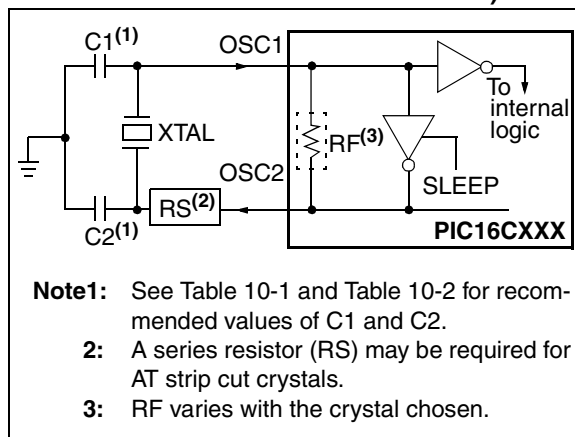
The PIC16CXXX can be operated in four different oscillator modes. The user can program two configuration bits (FOSC1 and FOSC0) to select one of these four modes:

- LP Low Power Crystal
- XT Crystal/Resonator
- HS High Speed Crystal/Resonator
- RC Resistor/Capacitor

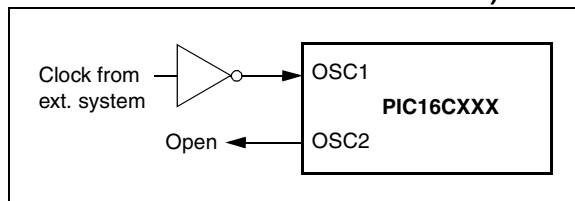
### 10.2.2 CRYSTAL OSCILLATOR/CERAMIC RESONATORS

In XT, LP or HS modes, a crystal or ceramic resonator is connected to the OSC1/CLKIN and OSC2/CLKOUT pins to establish oscillation (Figure 10-2). The PIC16CXXX oscillator design requires the use of a parallel cut crystal. Use of a series cut crystal may give a frequency out of the crystal manufacturers specifications. When in XT, LP or HS modes, the device can use an external clock source to drive the OSC1/CLKIN pin (Figure 10-3).

**FIGURE 10-2: CRYSTAL/CERAMIC RESONATOR OPERATION (HS, XT OR LP OSC CONFIGURATION)**



**FIGURE 10-3: EXTERNAL CLOCK INPUT OPERATION (HS, XT OR LP OSC CONFIGURATION)**



**TABLE 10-1 CERAMIC RESONATORS**

Ranges Tested:			
Mode	Freq	OSC1	OSC2
XT	455 kHz	68 - 100 pF	68 - 100 pF
	2.0 MHz	15 - 68 pF	15 - 68 pF
	4.0 MHz	15 - 68 pF	15 - 68 pF
HS	8.0 MHz	10 - 68 pF	10 - 68 pF
	16.0 MHz	10 - 22 pF	10 - 22 pF
<b>These values are for design guidance only. See notes at bottom of page.</b>			
Resonators Used:			
455 kHz	Panasonic EFO-A455K04B	± 0.3%	
2.0 MHz	Murata Erie CSA2.00MG	± 0.5%	
4.0 MHz	Murata Erie CSA4.00MG	± 0.5%	
8.0 MHz	Murata Erie CSA8.00MT	± 0.5%	
16.0 MHz	Murata Erie CSA16.00MX	± 0.5%	
Resonators did not have built-in capacitors.			

**TABLE 10-2 CAPACITOR SELECTION FOR CRYSTAL OSCILLATOR**

Osc Type	Crystal Freq	Cap. Range C1	Cap. Range C2
LP	32 kHz	33 pF	33 pF
	200 kHz	15 pF	15 pF
XT	200 kHz	47-68 pF	47-68 pF
	1 MHz	15 pF	15 pF
	4 MHz	15 pF	15 pF
HS	4 MHz	15 pF	15 pF
	8 MHz	15-33 pF	15-33 pF
	20 MHz	15-33 pF	15-33 pF
<b>These values are for design guidance only. See notes at bottom of page.</b>			
Crystals Used			
32 kHz	Epson C-001R32.768K-A	± 20 PPM	
200 kHz	STD XTL 200.000KHz	± 20 PPM	
1 MHz	ECS ECS-10-13-1	± 50 PPM	
4 MHz	ECS ECS-40-20-1	± 50 PPM	
8 MHz	EPSON CA-301 8.000M-C	± 30 PPM	
20 MHz	EPSON CA-301 20.000M-C	± 30 PPM	

- Note 1:** Higher capacitance increases the stability of the oscillator, but also increases the start-up time.  
**2:** Since each resonator/crystal has its own characteristics, the user should consult the resonator/crystal manufacturer for appropriate values of external components.  
**3:** Rs may be required in HS mode, as well as XT mode, to avoid overdriving crystals with low drive level specification.  
**4:** Oscillator performance should be verified when migrating between devices (including PIC16C62A to PIC16C62B and PIC16C72 to PIC16C72A)

# PIC16C62B/72A

## 10.8 Time-out Sequence

When a POR reset occurs, the PWRT delay starts (if enabled). When PWRT ends, the OST counts 1024 oscillator cycles (LP, XT, HS modes only). When OST completes, the device comes out of reset. The total time-out will vary based on oscillator configuration and the status of the PWRT. For example, in RC mode with the PWRT disabled, there will be no time-out at all.

If  $\overline{\text{MCLR}}$  is kept low long enough, the time-outs will expire. Bringing  $\overline{\text{MCLR}}$  high will begin execution immediately. This is useful for testing purposes or to synchronize more than one PIC16CXXX device operating in parallel.

### Status Register

IRP	RP1	RP0	$\overline{\text{TO}}$	$\overline{\text{PD}}$	Z	DC	C
-----	-----	-----	------------------------	------------------------	---	----	---

### PCON Register

						$\overline{\text{POR}}$	$\overline{\text{BOR}}$
--	--	--	--	--	--	-------------------------	-------------------------

TABLE 10-3 TIME-OUT IN VARIOUS SITUATIONS

Oscillator Configuration	Power-up		Brown-out	Wake-up from SLEEP
	$\overline{\text{PWRTE}} = 0$	$\overline{\text{PWRTE}} = 1$		
XT, HS, LP	72 ms + 1024Tosc	1024Tosc	72 ms + 1024Tosc	1024Tosc
RC	72 ms	—	72 ms	—

TABLE 10-4 STATUS BITS AND THEIR SIGNIFICANCE

$\overline{\text{POR}}$	$\overline{\text{BOR}}$	$\overline{\text{TO}}$	$\overline{\text{PD}}$	
0	x	1	1	Power-on Reset
0	x	0	x	Illegal, $\overline{\text{TO}}$ is set on $\overline{\text{POR}}$
0	x	x	0	Illegal, $\overline{\text{PD}}$ is set on $\overline{\text{POR}}$
1	0	1	1	Brown-out Reset
1	1	0	1	WDT Reset
1	1	0	0	WDT Wake-up
1	1	u	u	$\overline{\text{MCLR}}$ Reset during normal operation
1	1	1	0	$\overline{\text{MCLR}}$ Reset during SLEEP or interrupt wake-up from SLEEP

TABLE 10-5 RESET CONDITION FOR SPECIAL REGISTERS

Condition	Program Counter	STATUS Register	PCON Register
Power-on Reset	000h	0001 1xxx	---- --0x
$\overline{\text{MCLR}}$ Reset during normal operation	000h	000u uuuu	---- --uu
$\overline{\text{MCLR}}$ Reset during SLEEP	000h	0001 0uuu	---- --uu
WDT Reset	000h	0000 1uuu	---- --uu
WDT Wake-up	PC + 1	uuu0 0uuu	---- --uu
Brown-out Reset	000h	0001 1uuu	---- --u0
Interrupt wake-up from SLEEP	PC + 1 <sup>(1)</sup>	uuu1 0uuu	---- --uu

Legend: u = unchanged, x = unknown, - = unimplemented bit read as '0'.

Note 1: When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).

Table 10-5 shows the reset conditions for the STATUS, PCON and PC registers, while Table 10-6 shows the reset conditions for all the registers.

## 10.9 Power Control/Status Register (PCON)

The  $\overline{\text{BOR}}$  bit is unknown on Power-on Reset. If the Brown-out Reset circuit is used, the  $\overline{\text{BOR}}$  bit must be set by the user and checked on subsequent resets to see if it was cleared, indicating a Brown-out has occurred.

$\overline{\text{POR}}$  (Power-on Reset Status bit) is cleared on a Power-on Reset and unaffected otherwise. The user

**COMF**                    **Complement f**

---

Syntax:                    [ *label* ] COMF f,d

Operands:                 $0 \leq f \leq 127$   
 $d \in [0,1]$

Operation:                 $(\bar{f}) \rightarrow (\text{destination})$

Status Affected:        Z

Description:              The contents of register 'f' are complemented. If 'd' is 0, the result is stored in W. If 'd' is 1, the result is stored back in register 'f'.

**GOTO**                    **Unconditional Branch**

---

Syntax:                    [ *label* ] GOTO k

Operands:                 $0 \leq k \leq 2047$

Operation:                 $k \rightarrow PC<10:0>$   
 $PCLATH<4:3> \rightarrow PC<12:11>$

Status Affected:        None

Description:              GOTO is an unconditional branch. The eleven bit immediate value is loaded into PC bits <10:0>. The upper bits of PC are loaded from PCLATH<4:3>. GOTO is a two cycle instruction.

**DECf**                    **Decrement f**

---

Syntax:                    [ *label* ] DECf f,d

Operands:                 $0 \leq f \leq 127$   
 $d \in [0,1]$

Operation:                 $(f) - 1 \rightarrow (\text{destination})$

Status Affected:        Z

Description:              Decrement register 'f'. If 'd' is 0, the result is stored in the W register. If 'd' is 1, the result is stored back in register 'f'.

**INCF**                    **Increment f**

---

Syntax:                    [ *label* ] INCF f,d

Operands:                 $0 \leq f \leq 127$   
 $d \in [0,1]$

Operation:                 $(f) + 1 \rightarrow (\text{destination})$

Status Affected:        Z

Description:              The contents of register 'f' are incremented. If 'd' is 0, the result is placed in the W register. If 'd' is 1, the result is placed back in register 'f'.

**DECFSZ**                **Decrement f, Skip if 0**

---

Syntax:                    [ *label* ] DECFSZ f,d

Operands:                 $0 \leq f \leq 127$   
 $d \in [0,1]$

Operation:                 $(f) - 1 \rightarrow (\text{destination});$   
skip if result = 0

Status Affected:        None

Description:              The contents of register 'f' are decremented. If 'd' is 0, the result is placed in the W register. If 'd' is 1, the result is placed back in register 'f'. If the result is 1, the next instruction, is executed. If the result is 0, then a NOP is executed instead making it a 2TCY instruction.

**INCFSZ**                **Increment f, Skip if 0**

---

Syntax:                    [ *label* ] INCFSZ f,d

Operands:                 $0 \leq f \leq 127$   
 $d \in [0,1]$

Operation:                 $(f) + 1 \rightarrow (\text{destination});$   
skip if result = 0

Status Affected:        None

Description:              The contents of register 'f' are incremented. If 'd' is 0, the result is placed in the W register. If 'd' is 1, the result is placed back in register 'f'. If the result is 1, the next instruction is executed. If the result is 0, a NOP is executed instead making it a 2TCY instruction.

# PIC16C62B/72A

---

## **IORLW**      **Inclusive OR Literal with W**

---

Syntax:      [ *label* ] IORLW k  
Operands:     $0 \leq k \leq 255$   
Operation:    (W) .OR. k  $\rightarrow$  (W)  
Status Affected: Z  
Description:    The contents of the W register is OR'ed with the eight bit literal 'k'. The result is placed in the W register.

## **MOVLW**      **Move Literal to W**

---

Syntax:      [ *label* ] MOVLW k  
Operands:     $0 \leq k \leq 255$   
Operation:    k  $\rightarrow$  (W)  
Status Affected: None  
Description:    The eight bit literal 'k' is loaded into W register. The don't cares will assemble as 0's.

## **IORWF**      **Inclusive OR W with f**

---

Syntax:      [ *label* ] IORWF f,d  
Operands:     $0 \leq f \leq 127$   
                 $d \in [0,1]$   
Operation:    (W) .OR. (f)  $\rightarrow$  (destination)  
Status Affected: Z  
Description:    Inclusive OR the W register with register 'f'. If 'd' is 0, the result is placed in the W register. If 'd' is 1, the result is placed back in register 'f'.

## **MOVWF**      **Move W to f**

---

Syntax:      [ *label* ] MOVWF f  
Operands:     $0 \leq f \leq 127$   
Operation:    (W)  $\rightarrow$  (f)  
Status Affected: None  
Description:    Move data from W register to register 'f'.

## **MOVF**      **Move f**

---

Syntax:      [ *label* ] MOVF f,d  
Operands:     $0 \leq f \leq 127$   
                 $d \in [0,1]$   
Operation:    (f)  $\rightarrow$  (destination)  
Status Affected: Z  
Description:    The contents of register f is moved to a destination dependant upon the status of d. If d = 0, destination is W register. If d = 1, the destination is file register f itself. d = 1 is useful to test a file register since status flag Z is affected.

## **NOP**      **No Operation**

---

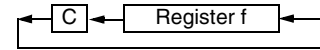
Syntax:      [ *label* ] NOP  
Operands:    None  
Operation:    No operation  
Status Affected: None  
Description:    No operation.

## **RETFIE**      **Return from Interrupt**

Syntax:      [ *label* ] RETFIE  
 Operands:    None  
 Operation:    TOS → PC,  
                   1 → GIE  
 Status Affected: None

## **RLF**            **Rotate Left f through Carry**

Syntax:      [ *label* ] RLF f,d  
 Operands:     $0 \leq f \leq 127$   
                    $d \in [0,1]$   
 Operation:    See description below  
 Status Affected: C  
 Description:    The contents of register 'f' are rotated one bit to the left through the Carry Flag. If 'd' is 0, the result is placed in the W register. If 'd' is 1, the result is stored back in register 'f'.

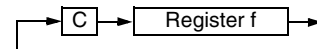


## **RETLW**        **Return with Literal in W**

Syntax:      [ *label* ] RETLW k  
 Operands:     $0 \leq k \leq 255$   
 Operation:     $k \rightarrow (W)$ ;  
                   TOS → PC  
 Status Affected: None  
 Description:    The W register is loaded with the eight bit literal 'k'. The program counter is loaded from the top of the stack (the return address). This is a two cycle instruction.

## **RRF**            **Rotate Right f through Carry**

Syntax:      [ *label* ] RRF f,d  
 Operands:     $0 \leq f \leq 127$   
                    $d \in [0,1]$   
 Operation:    See description below  
 Status Affected: C  
 Description:    The contents of register 'f' are rotated one bit to the right through the Carry Flag. If 'd' is 0, the result is placed in the W register. If 'd' is 1, the result is placed back in register 'f'.



## **RETURN**       **Return from Subroutine**

Syntax:      [ *label* ] RETURN  
 Operands:    None  
 Operation:    TOS → PC  
 Status Affected: None  
 Description:    Return from subroutine. The stack is POPed and the top of the stack (TOS) is loaded into the program counter. This is a two cycle instruction.

## **SLEEP**

Syntax:      [ *label* ] SLEEP  
 Operands:    None  
 Operation:    00h → WDT,  
                   0 → WDT prescaler,  
                   1 →  $\overline{TO}$ ,  
                   0 →  $\overline{PD}$   
 Status Affected:  $\overline{TO}$ ,  $\overline{PD}$   
 Description:    The power-down status bit,  $\overline{PD}$  is cleared. Time-out status bit,  $\overline{TO}$  is set. Watchdog Timer and its prescaler are cleared. The processor is put into SLEEP mode with the oscillator stopped. See Section 10.13 for more details.

# PIC16C62B/72A

## 13.1 DC Characteristics: PIC16C62B/72A-04 (Commercial, Industrial, Extended) PIC16C62B/72A-20 (Commercial, Industrial, Extended)

DC CHARACTERISTICS		Standard Operating Conditions (unless otherwise stated) Operating temperature 0°C ≤ TA ≤ +70°C for commercial -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended					
Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
D001 D001A	VDD	Supply Voltage	4.0 4.5 VBOR*	- - -	5.5 5.5 5.5	V V V	XT, RC and LP osc mode HS osc mode BOR enabled (Note 7)
D002*	VDR	RAM Data Retention Voltage (Note 1)	-	1.5	-	V	
D003	VPOR	VDD Start Voltage to ensure internal Power-on Reset signal	-	VSS	-	V	See section on Power-on Reset for details
D004* D004A*	SVDD	VDD Rise Rate to ensure internal Power-on Reset signal	0.05 TBD	- -	- -	V/ms	PWRT enabled (PWRT $\overline{\text{E}}$ bit clear) PWRT disabled (PWRT $\overline{\text{E}}$ bit set) See section on Power-on Reset for details
D005	VBOR	Brown-out Reset voltage trip point	3.65	-	4.35	V	BODEN bit set
D010  D013	IDD	Supply Current (Note 2, 5)	-  -	2.7  10	5  20	mA  mA	XT, RC osc modes FOSC = 4 MHz, VDD = 5.5V (Note 4)  HS osc mode FOSC = 20 MHz, VDD = 5.5V
D020 D021 D021B	IPD	Power-down Current (Note 3, 5)	- - - -	10.5 1.5 1.5 2.5	42 16 19 19	μA μA μA μA	VDD = 4.0V, WDT enabled, -40°C to +85°C VDD = 4.0V, WDT disabled, 0°C to +70°C VDD = 4.0V, WDT disabled, -40°C to +85°C VDD = 4.0V, WDT disabled, -40°C to +125°C
D022* D022A*	ΔIWDT ΔIBOR	Module Differential Current (Note 6) Watchdog Timer Brown-out Reset	- -	6.0 TBD	20 200	μA μA	WDTE BIT SET, VDD = 4.0V BODEN bit set, VDD = 5.0V

\* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** This is the limit to which VDD can be lowered without losing RAM data.

**2:** The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.

The test conditions for all IDD measurements in active operation mode are:

OSC1 = external square wave, from rail to rail; all I/O pins tristated, pulled to VDD,

MCLR = VDD; WDT enabled/disabled as specified.

**3:** The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.

**4:** For RC osc mode, current through Rext is not included. The current through the resistor can be estimated by the formula  $I_r = V_{DD}/2R_{ext}$  (mA) with Rext in kOhm.

**5:** Timer1 oscillator (when enabled) adds approximately 20 μA to the specification. This value is from characterization and is for design guidance only. This is not tested.

**6:** The Δ current is the additional current consumed when this peripheral is enabled. This current should be added to the base IDD or IPD measurement.

**7:** This is the voltage where the device enters the Brown-out Reset. When BOR is enabled, the device will perform a brown-out reset when VDD falls below VBOR.

# PIC16C62B/72A

## 13.4 AC (Timing) Characteristics

### 13.4.1 TIMING PARAMETER SYMBOLOGY

The timing parameter symbols have been created following one of the following formats:

1. TppS2ppS
2. TppS
3. TCC:ST (I<sup>2</sup>C specifications only)
4. Ts (I<sup>2</sup>C specifications only)

<b>T</b>			
F	Frequency	T	Time

Lowercase letters (pp) and their meanings:

<b>pp</b>			
cc	CCP1	osc	OSC1
ck	CLKOUT	rd	$\overline{RD}$
cs	$\overline{CS}$	rw	$\overline{RD}$ or $\overline{WR}$
di	SDI	sc	SCK
do	SDO	ss	$\overline{SS}$
dt	Data in	t0	T0CKI
io	I/O port	t1	T1CKI
mc	$\overline{MCLR}$	wr	$\overline{WR}$

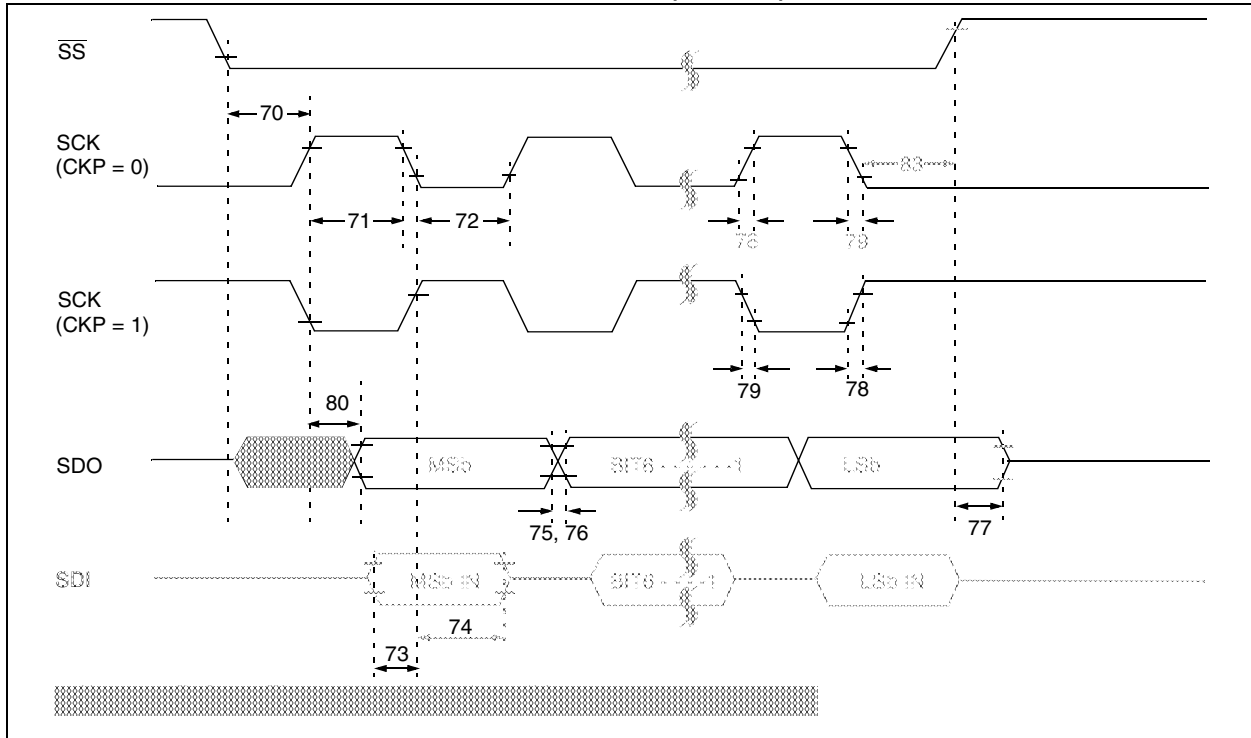
Uppercase letters and their meanings:

<b>S</b>			
F	Fall	P	Period
H	High	R	Rise
I	Invalid (Hi-impedance)	V	Valid
L	Low	Z	Hi-impedance
<b>I<sup>2</sup>C only</b>			
AA	output access	High	High
BUF	Bus free	Low	Low

TCC:ST (I<sup>2</sup>C specifications only)

<b>CC</b>			
HD	Hold	SU	Setup
<b>ST</b>			
DAT	DATA input hold	STO	STOP condition
STA	START condition		

**FIGURE 13-13: EXAMPLE SPI SLAVE MODE TIMING (CKE = 0)**



**TABLE 13-9: EXAMPLE SPI MODE REQUIREMENTS (SLAVE MODE TIMING (CKE = 0))**

Param. No.	Symbol	Characteristic	Min	Typ†	Max	Units	Conditions
70	TssL2sch, TssL2scl	$\overline{SS}\downarrow$ to SCK $\downarrow$ or SCK $\uparrow$ input	T <sub>CY</sub>	—	—	ns	
71	Tsch	SCK input high time (slave mode)	Continuous	1.25T <sub>CY</sub> + 30	—	—	ns
71A			Single Byte	40	—	—	ns
72	TscL	SCK input low time (slave mode)	Continuous	1.25T <sub>CY</sub> + 30	—	—	ns
72A			Single Byte	40	—	—	ns
73	TdiV2sch, TdiV2scl	Setup time of SDI data input to SCK edge	100	—	—	ns	
73A	TB2B	Last clock edge of Byte1 to the 1st clock edge of Byte2	1.5T <sub>CY</sub> + 40	—	—	ns	Note 1
74	Tsch2diL, TscL2diL	Hold time of SDI data input to SCK edge	100	—	—	ns	
75	TdoR	SDO data output rise time	PIC16CXX	—	10	25	ns
			PIC16LCXX	—	20	45	ns
76	TdoF	SDO data output fall time	—	10	25	ns	
77	TssH2doZ	$\overline{SS}\uparrow$ to SDO output hi-impedance	10	—	50	ns	
78	TscR	SCK output rise time (master mode)	PIC16CXX	—	10	25	ns
			PIC16LCXX	—	20	45	ns
79	TscF	SCK output fall time (master mode)	—	10	25	ns	
80	Tsch2doV, TscL2doV	SDO data output valid after SCK edge	PIC16CXX	—	—	50	ns
			PIC16LCXX	—	—	100	ns
83	Tsch2ssH, TscL2ssH	$\overline{SS}\uparrow$ after SCK edge	1.5T <sub>CY</sub> + 40	—	—	ns	

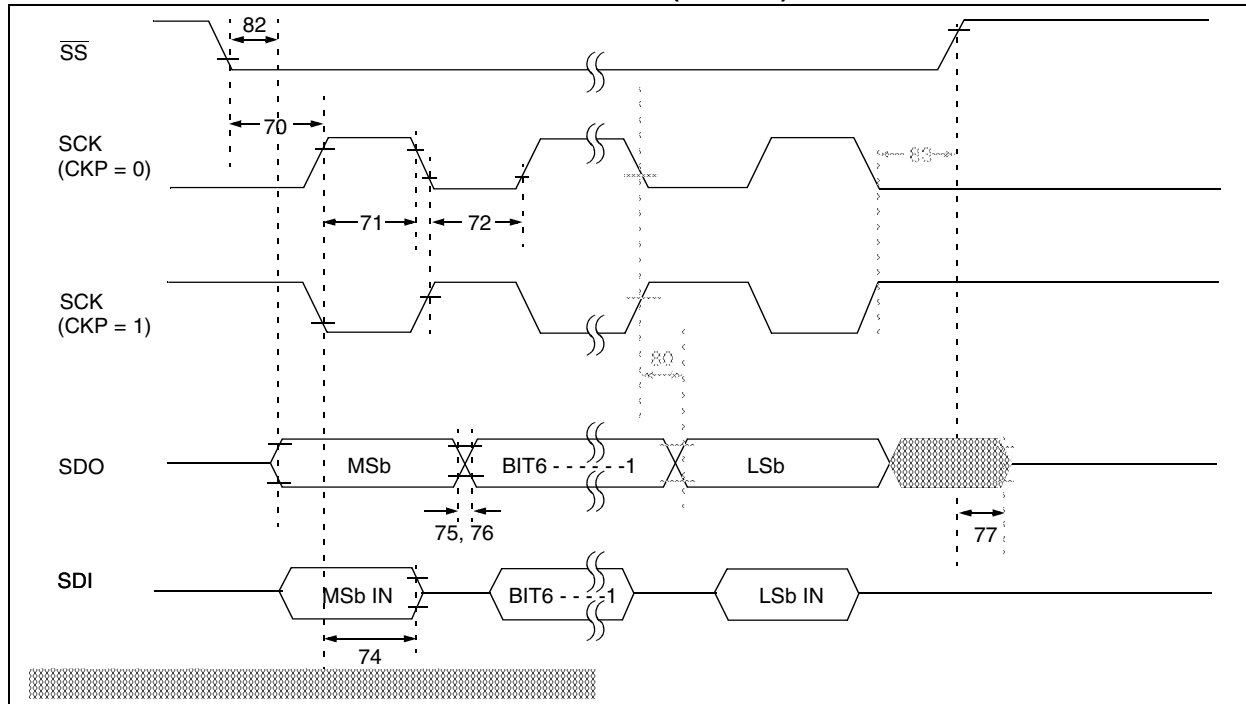
† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** Specification 73A is only required if specifications 71A and 72A are used.



# PIC16C62B/72A

**FIGURE 13-14: EXAMPLE SPI SLAVE MODE TIMING (CKE = 1)**



**TABLE 13-10: EXAMPLE SPI SLAVE MODE REQUIREMENTS (CKE = 1)**

Param. No.	Symbol	Characteristic	Min	Typ†	Max	Units	Conditions
70	TssL2scH, TssL2scL	$\overline{SS} \downarrow$ to SCK $\downarrow$ or SCK $\uparrow$ input	T <sub>CY</sub>	—	—	ns	
71	TscH	SCK input high time (slave mode)	Continuous	1.25T <sub>CY</sub> + 30	—	—	ns
71A			Single Byte	40	—	—	ns
72	TscL	SCK input low time (slave mode)	Continuous	1.25T <sub>CY</sub> + 30	—	—	ns
72A			Single Byte	40	—	—	ns
73A	Tb2B	Last clock edge of Byte1 to the 1st clock edge of Byte2	1.5T <sub>CY</sub> + 40	—	—	ns	Note 1
74	Tsch2diL, TscL2diL	Hold time of SDI data input to SCK edge	100	—	—	ns	
75	TdoR	SDO data output rise time	PIC16CXX	—	10	25	ns
			PIC16LCXX	—	20	45	ns
76	TdoF	SDO data output fall time	—	10	25	ns	
77	TssH2doZ	$\overline{SS} \uparrow$ to SDO output hi-impedance	10	—	50	ns	
78	TscR	SCK output rise time (master mode)	PIC16CXX	—	10	25	ns
			PIC16LCXX	—	20	45	ns
79	TscF	SCK output fall time (master mode)	—	10	25	ns	
80	Tsch2doV, TscL2doV	SDO data output valid after SCK edge	PIC16CXX	—	—	50	ns
			PIC16LCXX	—	—	100	ns
82	TssL2doV	SDO data output valid after $\overline{SS} \downarrow$ edge	PIC16CXX	—	—	50	ns
			PIC16LCXX	—	—	100	ns
83	Tsch2ssH, TscL2ssH	$\overline{SS} \uparrow$ after SCK edge	1.5T <sub>CY</sub> + 40	—	—	ns	

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** Specification 73A is only required if specifications 71A and 72A are used.

**TABLE 13-13: A/D CONVERTER CHARACTERISTICS:  
 PIC16C72A-04 (COMMERCIAL, INDUSTRIAL, EXTENDED)  
 PIC16C72A-20 (COMMERCIAL, INDUSTRIAL, EXTENDED)  
 PIC16LC72A-04 (COMMERCIAL, INDUSTRIAL)**

Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions	
A01	NR	Resolution	—	—	8-bits	bit	VREF = VDD = 5.12V, VSS ≤ VAIN ≤ VREF	
A02	EABS	Total Absolute error	—	—	< ± 1	LSB	VREF = VDD = 5.12V, VSS ≤ VAIN ≤ VREF	
A03	EIL	Integral linearity error	—	—	< ± 1	LSB	VREF = VDD = 5.12V, VSS ≤ VAIN ≤ VREF	
A04	EDL	Differential linearity error	—	—	< ± 1	LSB	VREF = VDD = 5.12V, VSS ≤ VAIN ≤ VREF	
A05	EFS	Full scale error	—	—	< ± 1	LSB	VREF = VDD = 5.12V, VSS ≤ VAIN ≤ VREF	
A06	E0FF	Offset error	—	—	< ± 1	LSB	VREF = VDD = 5.12V, VSS ≤ VAIN ≤ VREF	
A10	—	Monotonicity	—	guaranteed (Note 3)	—	—	VSS ≤ VAIN ≤ VREF	
A20	VREF	Reference voltage	2.5V	—	VDD + 0.3	V		
A25	VAIN	Analog input voltage	VSS - 0.3	—	VREF + 0.3	V		
A30	ZAIN	Recommended impedance of analog voltage source	—	—	10.0	kΩ		
A40	IAD	A/D conversion current (VDD)	PIC16CXX	—	180	—	μA	Average current consumption when A/D is on. (Note 1)
			PIC16LCXX	—	90	—	μA	
A50	IREF	VREF input current (Note 2)	10	—	1000	μA	During VAIN acquisition. Based on differential of VHOLD to VAIN to charge CHOLD, see Section 9.1. During A/D conversion cycle	
			—	—	10	μA		

\* These parameters are characterized but not tested.

† Data in “Typ” column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** When A/D is off, it will not consume any current other than minor leakage current.

The power-down current spec includes any such leakage from the A/D module.

**2:** VREF current is from RA3 pin or VDD pin, whichever is selected as reference input.

**3:** The A/D conversion result never decreases with an increase in the Input Voltage and has no missing codes.

## 15.0 PACKAGING INFORMATION

### 15.1 Package Marking Information

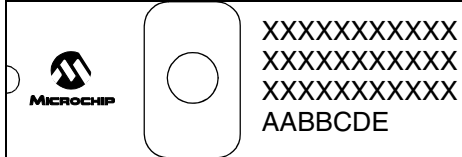
28-Lead PDIP (Skinny DIP)



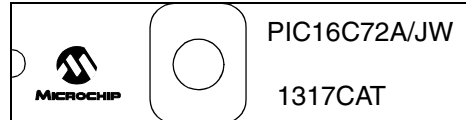
Example



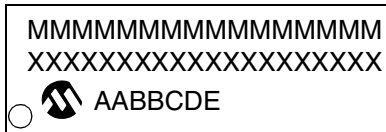
28-Lead CERDIP Windowed



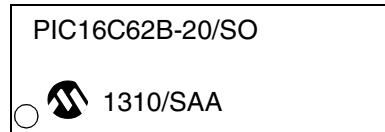
Example



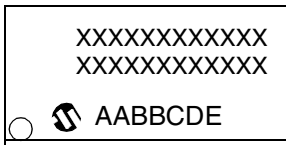
28-Lead SOIC



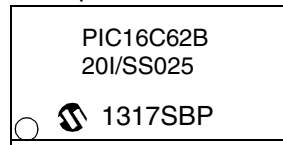
Example



28-Lead SSOP



Example



<b>Legend:</b> MM...M	Microchip part number information
XX...X	Customer specific information*
AA	Year code (last 2 digits of calendar year)
BB	Week code (week of January 1 is week '01')
C	Facility code of the plant at which wafer is manufactured
	O = Outside Vendor
	C = 5" Line
	S = 6" Line
	H = 8" Line
D	Mask revision number
E	Assembly code of the plant or country of origin in which part was assembled

**Note:** In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line thus limiting the number of available characters for customer specific information.

\* Standard OTP marking consists of Microchip part number, year code, week code, facility code, mask rev#, and assembly code. For OTP marking beyond this, certain price adders apply. Please check with your Microchip Sales Office. For QTP devices, any special marking adders are included in QTP price.

## APPENDIX A: REVISION HISTORY

Version	Date	Revision Description
A	7/98	This is a new data sheet. However, the devices described in this data sheet are the upgrades to the devices found in the <i>PIC16C6X Data Sheet</i> , DS30234, and the <i>PIC16C7X Data Sheet</i> , DS30390.

## APPENDIX B: CONVERSION CONSIDERATIONS

Considerations for converting from previous versions of devices to the ones listed in this data sheet are listed in Table B-1.

**TABLE B-1: CONVERSION CONSIDERATIONS**

Difference	PIC16C62A/72	PIC16C62B/72A
Voltage Range	2.5V - 6.0V	2.5V - 5.5V
SSP module	Basic SSP (2 mode SPI)	SSP (4 mode SPI)
CCP module	CCP does not reset TMR1 when in special event trigger mode.	N/A
Timer1 module	Writing to TMR1L register can cause overflow in TMR1H register.	N/A

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