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#### Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	I <sup>2</sup> C, SPI
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	22
Program Memory Size	3.5KB (2K x 14)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 5.5V
Data Converters	A/D 5x8b
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Through Hole
Package / Case	28-DIP (0.300", 7.62mm)
Supplier Device Package	28-SPDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16c72a-20-sp

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NOTES:

#### 2.2 Data Memory Organization

The data memory is partitioned into multiple banks which contain the General Purpose Registers and the Special Function Registers. Bits RP1 and RP0 are the bank select bits.

	RP1 <sup>(1)</sup>	RP0 (STATUS<6:5>)
	= 00 $\rightarrow$	Bank0
	= 01 $\rightarrow$	Bank1
	= 10 $\rightarrow$	Bank2 (not implemented)
_	= 11 $\rightarrow$	Bank3 (not implemented)
ſ	Note 1:	Maintain this bit clear to ensure upward compati-
		bility with future products.

Each bank extends up to 7Fh (128 bytes). The lower locations of each bank are reserved for the Special Function Registers. Above the Special Function Registers are General Purpose Registers, implemented as static RAM. All implemented banks contain Special Function Registers. Some "high use" Special Function Registers from one bank may be mirrored in another bank for code reduction and quicker access.

#### 2.2.1 GENERAL PURPOSE REGISTER FILE

The register file can be accessed either directly, or indirectly through the File Select Register FSR (Section 2.5).

## FIGURE 2-2: REGISTER FILE MAP

File			File
Address			Address
00h	INDF <sup>(1)</sup>	INDF <sup>(1)</sup>	80h
01h	TMR0	OPTION_REG	81h
02h	PCL	PCL	82h
03h	STATUS	STATUS	83h
04h	FSR	FSR	84h
05h	PORTA	TRISA	85h
06h	PORTB	TRISB	86h
07h	PORTC	TRISC	87h
08h	_	_	88h
09h	_	_	89h
0Ah	PCLATH	PCLATH	8Ah
0Bh	INTCON	INTCON	8Bh
0Ch	PIR1	PIE1	8Ch
0Dh	—	—	8Dh
0Eh	TMR1L	PCON	8Eh
0Fh	TMR1H	_	8Fh
10h	T1CON	_	90h
11h	TMR2	_	91h
12h	T2CON	PR2	92h
13h	SSPBUF	SSPADD	93h
14h	SSPCON	SSPSTAT	94h
15h	CCPR1L	_	95h
16h	CCPR1H	_	96h
17h	CCP1CON		97h
18h	_		98h
19h			99h
1Ah			9Ah
1Bh			9Bh
1Ch			9Ch
1Dh			9Dh
1Eh	ADRES <sup>(2)</sup>		9Eh
1Fh ADCONO		ADCON1 <sup>(2)</sup>	9Fh
20h		Gonoral	A0h
		Purpose	
	General	Registers	BFh
	Purpose	_	C0h
	Registers	_	
7Fh		_	FFh
	Bank 0	Bank 1	l
Lin	implemented d	ata memory local	tions
read	as '0'.		
Note 1: No	ot a physical ree	gister.	
2: Th	nese registers a	re not implemen	ted on the
PI	U IOUOZD, IEad	1 as U.	

## 3.2 PORTB and the TRISB Register

PORTB is an 8-bit wide bi-directional port. The corresponding data direction register is TRISB. Setting a TRISB bit (=1) will make the corresponding PORTB pin an input, (i.e., put the corresponding output driver in a hi-impedance mode). Clearing a TRISB bit (=0) will make the corresponding PORTB pin an output, (i.e., put the contents of the output latch on the selected pin).

Each of the PORTB pins has a weak internal pull-up. A single control bit can turn on all the pull-ups. This is performed by clearing bit  $\overline{\text{RBPU}}$  (OPTION\_REG<7>). The weak pull-up is automatically turned off when the port pin is configured as an output. The pull-ups are disabled on a Power-on Reset.

#### FIGURE 3-3: BLOCK DIAGRAM OF RB3:RB0 PINS



Four of PORTB's pins, RB7:RB4, have an interrupt on change feature. Only pins configured as inputs can cause this interrupt to occur (i.e. any RB7:RB4 pin configured as an output is excluded from the interrupt on change comparison). The input pins (of RB7:RB4) are compared with the old value latched on the last read of PORTB. The "mismatch" outputs of RB7:RB4 are OR'ed together to generate the RB Port Change Interrupt with flag bit RBIF (INTCON<0>).

This interrupt can wake the device from SLEEP. The user, in the interrupt service routine, can clear the interrupt in the following manner:

- a) Any read or write of PORTB. This will end the mismatch condition.
- b) Clear flag bit RBIF.

A mismatch condition will continue to set flag bit RBIF. Reading PORTB will end the mismatch condition and allow flag bit RBIF to be cleared.

The interrupt on change feature is recommended for wake-up on key depression operation and operations where PORTB is only used for the interrupt on change feature. Polling of PORTB is not recommended while using the interrupt on change feature.

RB0/INT is an external interupt pin and is configured using the INTEDG bit (OPTION\_REG<6>). RB0/INT is discussed in detail in Section 10.10.1.





## FIGURE 5-1: TIMER1 BLOCK DIAGRAM



## 8.0 SYNCHRONOUS SERIAL PORT (SSP) MODULE

#### 8.1 <u>SSP Module Overview</u>

The Synchronous Serial Port (SSP) module is a serial interface useful for communicating with other peripheral or microcontroller devices. These peripheral devices may be Serial EEPROMs, shift registers, display drivers, A/D converters, etc. The SSP module can operate in one of two modes:

- Serial Peripheral Interface (SPI)
- Inter-Integrated Circuit (I<sup>2</sup>C)

For more information on SSP operation (including an I<sup>2</sup>C Overview), refer to the PIC<sup>®</sup> MCU Mid-Range Reference Manual, (DS33023). Also, refer to Application Note AN578, *"Use of the SSP Module in the I<sup>2</sup>C Multi-Master Environment."* 

## 8.2 SPI Mode

This section contains register definitions and operational characteristics of the SPI module.

Additional information on SPI operation may be found in the PIC<sup>®</sup> MCU Mid-Range Reference Manual, (DS33023).

8.2.1 OPERATION OF SSP MODULE IN SPI MODE

A block diagram of the SSP Module in SPI Mode is shown in Figure 8-1.

The SPI mode allows 8-bits of data to be synchronously transmitted and received simultaneously. To accomplish communication, three pins are used:

- Serial Data Out (SDO)RC5/SDO
- Serial Data In (SDI)RC4/SDI/SDA
- Serial Clock (SCK)RC3/SCK/SCL

Additionally, a fourth pin may be used when in a slave mode of operation:

Slave Select (SS)RA5/SS/AN4

When initializing the SPI, several options need to be specified. This is done by programming the appropriate control bits in the SSPCON register (SSPCON<5:0>) and SSPSTAT<7:6>. These control bits allow the following to be specified:

- Master Operation (SCK is the clock output)
- Slave Mode (SCK is the clock input)
- Clock Polarity (Idle state of SCK)
- Clock Edge (Output data on rising/falling edge of SCK)
- Clock Rate (master operation only)
- Slave Select Mode (Slave mode only)

To enable the serial port, SSP Enable bit, SSPEN (SSPCON<5>) must be set. To reset or reconfigure SPI mode, clear bit SSPEN, re-initialize the SSPCON reg-

ister, and then set bit SSPEN. This configures the SDI, SDO, SCK and  $\overline{SS}$  pins as serial port pins. For the pins to behave as the serial port function, they must have their data direction bits (in the TRISC register) appropriately programmed. That is:

- SDI must have TRISC<4> set
- SDO must have TRISC<5> cleared
- SCK (master operation) must have TRISC<3> cleared
- SCK (Slave mode) must have TRISC<3> set
- SS must have TRISA<5> set (if used)

Note: When the SPI is in Slave Mode with  $\overline{SS}$  pin control enabled, (SSPCON<3:0> = 0100) the SPI module will reset if the  $\overline{SS}$  pin is set to VDD.

**Note:** If the SPI is used in Slave Mode with CKE = '1', then the  $\overline{SS}$  pin control must be enabled.

#### FIGURE 8-1: SSP BLOCK DIAGRAM (SPI MODE)



## 8.3 <u>SSP I<sup>2</sup>C Operation</u>

The SSP module in I<sup>2</sup>C mode fully implements all slave functions, except general call support, and provides interrupts on start and stop bits in hardware to support firmware implementations of the master functions. The SSP module implements the standard mode specifications, as well as 7-bit and 10-bit addressing.

Two pins are used for data transfer. These are the RC3/SCK/SCL pin, which is the clock (SCL), and the RC4/SDI/SDA pin, which is the data (SDA). The user must configure these pins as inputs or outputs through the TRISC<4:3> bits.

The SSP module functions are enabled by setting SSP Enable bit SSPEN (SSPCON<5>).

FIGURE 8-2: SSP BLOCK DIAGRAM (I<sup>2</sup>C MODE)



The SSP module has five registers for  $I^2C$  operation. These are the:

- SSP Control Register (SSPCON)
- SSP Status Register (SSPSTAT)
- Serial Receive/Transmit Buffer (SSPBUF)
- SSP Shift Register (SSPSR) Not accessible
- SSP Address Register (SSPADD)

The SSPCON register allows control of the  $I^2C$  operation. Four mode selection bits (SSPCON<3:0>) allow one of the following  $I^2C$  modes to be selected:

- I<sup>2</sup>C Slave mode (7-bit address)
- I<sup>2</sup>C Slave mode (10-bit address)
- I<sup>2</sup>C Slave mode (7-bit address), with start and stop bit interrupts enabled for firmware master mode support
- I<sup>2</sup>C Slave mode (10-bit address), with start and stop bit interrupts enabled for firmware master mode support
- I<sup>2</sup>C start and stop bit interrupts enabled for firmware master mode support, slave mode idle

Selection of any I<sup>2</sup>C mode, with the SSPEN bit set, forces the SCL and SDA pins to be operated as open drain outputs, provided these pins are programmed to inputs by setting the appropriate TRISC bits.

Additional information on SSP I<sup>2</sup>C operation may be found in the PIC<sup>®</sup> MCU Mid-Range Reference Manual, (DS33023).

#### 8.3.1 SLAVE MODE

In slave mode, the SCL and SDA pins must be configured as inputs (TRISC<4:3> set). The SSP module will override the input state with the output data when required (slave-transmitter).

When an address is matched or the data transfer after an address match is received, the hardware automatically will generate the acknowledge ( $\overline{ACK}$ ) pulse, and load the SSPBUF register with the received value in the SSPSR register.

There are certain conditions that will cause the SSP module not to give this  $\overline{ACK}$  pulse. This happens if either of the following conditions occur:

- a) The buffer full bit BF (SSPSTAT<0>) was set before the transfer was completed.
- b) The overflow bit SSPOV (SSPCON<6>) was set before the transfer was completed.

In this case, the SSPSR register value is not loaded into the SSPBUF, but bit SSPIF (PIR1<3>) is set. Table 8-2 shows what happens when a data transfer byte is received, given the status of bits BF and SSPOV. The shaded cells show the condition where user software did not properly clear the overflow condition. Flag bit BF is cleared by reading the SSPBUF register, while bit SSPOV is cleared through software.

The SCL clock input must have a minimum high and low for proper operation. The high and low times of the  $I^2C$  specification, as well as the requirement of the SSP module, is shown in timing parameter #100, THIGH, and parameter #101, TLOW.

#### 8.3.1.1 ADDRESSING

Once the SSP module has been enabled, it waits for a START condition to occur. Following the START condition, 8 bits are shifted into the SSPSR register. All incoming bits are sampled with the rising edge of the clock (SCL) line. The value of register SSPSR<7:1> is compared to the value of the SSPADD register. The address is compared on the falling edge of the eighth clock (SCL) pulse. If the addresses match and the BF and SSPOV bits are clear, the following events occur:

- a) The SSPSR register value is loaded into the SSPBUF register.
- b) The buffer full bit, BF is set.
- c) An ACK pulse is generated.
- d) SSP interrupt flag bit, SSPIF (PIR1<3>), is set (interrupt is generated if enabled) on the falling edge of the ninth SCL pulse.

In 10-bit address mode, two address bytes need to be received by the slave. The five Most Significant bits (MSbs) of the first address byte specify if this is a 10-bit address. Bit R/W (SSPSTAT<2>) must specify a write so the slave device will receive the second address byte. For a 10-bit address, the first byte would equal

'1111 0 A9 A8 0', where A9 and A8 are the two MSbs of the address. The sequence of events for 10-bit address is as follows, with steps 7-9 for slave-transmitter:

- 1. Receive first (high) byte of Address (bits SSPIF, BF, and bit UA (SSPSTAT<1>) are set).
- Update the SSPADD register with second (low) byte of Address (clears bit UA and releases the SCL line).
- 3. Read the SSPBUF register (clears bit BF) and clear flag bit SSPIF.
- 4. Receive second (low) byte of Address (bits SSPIF, BF, and UA are set).
- 5. Update the SSPADD register with the first (high) byte of Address, if match releases SCL line, this will clear bit UA.
- 6. Read the SSPBUF register (clears bit BF) and clear flag bit SSPIF.
- 7. Receive repeated START condition.
- 8. Receive first (high) byte of Address (bits SSPIF and BF are set).
- 9. Read the SSPBUF register (clears bit BF) and clear flag bit SSPIF.

Status Bi Transfer i	its as Data s Received		Conoroto ACK	Set bit SSPIF
BF	SSPOV	$SSPSR \to SSPBUF$	Pulse	if enabled)
0	0	Yes	Yes	Yes
1	0	No	No	Yes
1	1	No	No	Yes
0	1	Yes	No	Yes

#### TABLE 8-2 DATA TRANSFER RECEIVED BYTE ACTIONS

Note: Shaded cells show the conditions where the user software did not properly clear the overflow condition.

#### 8.3.2 MASTER OPERATION

Master operation is supported in firmware using interrupt generation on the detection of the START and STOP conditions. The STOP (P) and START (S) bits are cleared by a reset or when the SSP module is disabled. The STOP (P) and START (S) bits will toggle based on the START and STOP conditions. Control of the  $I^2C$  bus may be taken when the P bit is set, or the bus is idle and both the S and P bits are clear.

In master operation, the SCL and SDA lines are manipulated in software by clearing the corresponding TRISC<4:3> bit(s). The output level is always low, irrespective of the value(s) in PORTC<4:3>. So when transmitting data, a '1' data bit must have the TRISC<4> bit set (input) and a '0' data bit must have the TRISC<4> bit cleared (output). The same scenario is true for the SCL line with the TRISC<3> bit.

The following events will cause SSP Interrupt Flag bit, SSPIF, to be set (SSP Interrupt if enabled):

- START condition
- STOP condition
- Byte transfer completed

Master operation can be done with either the slave mode idle (SSPM3:SSPM0 = 1011) or with the slave active. When both master operation and slave modes are used, the software needs to differentiate the source(s) of the interrupt.

For more information on master operation, see AN554 - Software Implementation of  $I^2C$  Bus Master.

#### 8.3.3 MULTI-MASTER OPERATION

In multi-master operation, the interrupt generation on the detection of the START and STOP conditions allows the determination of when the bus is free. The STOP (P) and START (S) bits are cleared from a reset or when the SSP module is disabled. The STOP (P) and START (S) bits will toggle based on the START and STOP conditions. Control of the  $I^2C$  bus may be taken when bit P (SSPSTAT<4>) is set, or the bus is idle and both the S and P bits clear. When the bus is busy, enabling the SSP Interrupt will generate the interrupt when the STOP condition occurs.

In multi-master operation, the SDA line must be monitored to see if the signal level is the expected output level. This check only needs to be done when a high level is output. If a high level is expected and a low level is present, the device needs to release the SDA and SCL lines (set TRISC<4:3>). There are two stages where this arbitration can be lost, these are:

- Address Transfer
- Data Transfer

When the slave logic is enabled, the slave continues to receive. If arbitration was lost during the address transfer stage, communication to the device may be in progress. If addressed, an ACK pulse will be generated. If arbitration was lost during the data transfer stage, the device will need to re-transfer the data at a later time.

For more information on master operation, see AN578 - Use of the SSP Module in the of  $l^2C$  Multi-Master Environment.

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other resets
0Bh, 8Bh	INTCON	GIE	PEIE	TOIE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000u
0Ch	PIR1	_	ADIF	_	_	SSPIF	CCP1IF	TMR2IF	TMR1IF	-0 0000	-0 0000
8Ch	PIE1	—	ADIE	_	_	SSPIE	CCP1IE	TMR2IE	TMR1IE	-0 0000	-0 0000
13h	SSPBUF	Synchronou	nchronous Serial Port Receive Buffer/Transmit Register								uuuu uuuu
93h	SSPADD	Synchronou	ynchronous Serial Port (I <sup>2</sup> C mode) Address Register							0000 0000	0000 0000
14h	SSPCON	WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0	0000 0000	0000 0000
94h	SSPSTAT	SMP <sup>(1)</sup>	CKE <sup>(1)</sup>	D/A	Р	S	R/W	UA	BF	0000 0000	0000 0000
87h	TRISC	PORTC Dat	a Directio	on register		•	•			1111 1111	1111 1111

## TABLE 8-3REGISTERS ASSOCIATED WITH I<sup>2</sup>C OPERATION

Legend: x = unknown, u = unchanged, - = unimplemented locations read as '0'. Shaded cells are not used by SSP module in SPI mode.

**Note 1:** Maintain these bits clear in  $I^2C$  mode.

## 10.2 Oscillator Configurations

#### 10.2.1 OSCILLATOR TYPES

The PIC16CXXX can be operated in four different oscillator modes. The user can program two configuration bits (FOSC1 and FOSC0) to select one of these four modes:

- LP Low Power Crystal
- XT Crystal/Resonator
- HS High Speed Crystal/Resonator
- RC Resistor/Capacitor

# 10.2.2 CRYSTAL OSCILLATOR/CERAMIC RESONATORS

In XT, LP or HS modes, a crystal or ceramic resonator is connected to the OSC1/CLKIN and OSC2/CLKOUT pins to establish oscillation (Figure 10-2). The PIC16CXXX oscillator design requires the use of a parallel cut crystal. Use of a series cut crystal may give a frequency out of the crystal manufacturers specifications. When in XT, LP or HS modes, the device can use an external clock source to drive the OSC1/CLKIN pin (Figure 10-3).

#### FIGURE 10-2: CRYSTAL/CERAMIC RESONATOR OPERATION (HS, XT OR LP OSC CONFIGURATION)



3: RF varies with the crystal chosen.

#### FIGURE 10-3: EXTERNAL CLOCK INPUT OPERATION (HS, XT OR LP OSC CONFIGURATION)



## TABLE 10-1 CERAMIC RESONATORS

## Ranges Tested:

nanges ie	sieu.							
Mode	Freq	OSC1	0\$C2					
XT	455 kHz	68 - 100 pF	68 - 100 pF					
	2.0 MHz	15 - 68 pF 🛛 <	15-68 pF					
	4.0 MHz	15 - 68 pF	15 - 68 pF					
HS	8.0 MHz	10 - 68(pF	∕10 - 68 pF					
	16.0 MHz	10,-22,0F	10 - 22 pF					
The note	se values are f	ior design guidar	nce only. See					
Resonators Used:								
455 kHz	Panasonie	Panasonie EFO-A455K04B						
2.0 MHz	Wurata Erie CSA2.00MG ± 0.5%							
4.0 MHz	MHz Murata Erie CSA4.00MG ± 0.5%							
8.0 MATHZ	Murata Erie (	CSA8.00MT	± 0.5%					
16.0 MHz	Murata Erie	CSA16.00MX	$\pm 0.5\%$					
Resona	ators did not ha	ve built-in capacito	ors.					

# TABLE 10-2CAPACITOR SELECTION FOR<br/>CRYSTAL OSCILLATOR

Osc Type	Crystal Freq	Cap. Range C1	Cap. Range C2						
LP	32 kHz	33 pF	33 pF						
	200 kHz	15 pF	15 pF						
XT	200 kHz	47-68 pF	47-68 pF						
	1 MHz	15 pF 🔍	✓ 15 pF						
	4 MHz								
HS	4 MHz	15 pt	💛 15 pF						
	8 MHz	15-33 pE>	15-33 pF						
20 MHz (15-33 pF 15-33 pF									
These values are for design guidance only. See notes at bottom of page.									
Crystals Used									
32 kHz Epson C-001R32.768K-A ± 20 PPM									
200 KHZ	STO XTL 2	00.000KHz	± 20 PPM						
1 MHz S	ECS ECS-	10-13-1	± 50 PPM						
4 MHz	ECS ECS-4	40-20-1	± 50 PPM						
8 MHz	EPSON CA	-301 8.000M-C	± 30 PPM						

**Note 1:** Higher capacitance increases the stability of the oscillator, but also increases the start-up time.

EPSON CA-301 20.000M-C

20 MHz

2: Since each resonator/crystal has its own characteristics, the user should consult the resonator/crystal manufacturer for appropriate values of external components.

± 30 PPM

- 3: Rs may be required in HS mode, as well as XT mode, to avoid overdriving crystals with low drive level specification.
- 4: Oscillator performance should be verified when migrating between devices (including PIC16C62A to PIC16C62B and PIC16C72 to PIC16C72A)



#### FIGURE 10-5: SIMPLIFIED BLOCK DIAGRAM OF ON-CHIP RESET CIRCUIT

## FIGURE 10-10: WAKE-UP FROM SLEEP THROUGH INTERRUPT

; a1   a2   a3   a4 ; a osc1////////////////////////////////////	21   Q2   Q3   Q4		a1 a2 a3 a4	01 02 03 04	01   02   03   04	a1 a2 a3 a4
CLKOUT(4)		Tost(2)				
INT pin			1 1			
INTF flag (INTCON<1>)		<u>`</u>	, , ,	Interrupt Latency (Note 2)		
GIE bit (INTCON<7>)	 	Processor in	<u> </u>     			
INSTRUCTION FLOW	1		1 1	· · ·	 	
PC X PC X	PC+1	PC+2	PC+2	PC + 2	0004h	0005h
Instruction { fetched { Inst(PC) = SLEEP	Inst(PC + 1)		Inst(PC + 2)		Inst(0004h)	Inst(0005h)
Instruction Inst(PC - 1)	SLEEP		Inst(PC + 1)	Dummy cycle	Dummy cycle	Inst(0004h)

**Note 1:** XT, HS or LP oscillator mode assumed.

**2:** TOST = 1024TOSC (drawing not to scale) This delay will not be there for RC osc mode.

3: GIE = '1' assumed. In this case after wake- up, the processor jumps to the interrupt routine. If GIE = '0', execution will continue in-line.

4: CLKOUT is not available in these osc modes, but shown here for timing reference.

#### 10.14 Program Verification/Code Protection

If the code protection bits have not been programmed, the on-chip program memory can be read out for verification purposes.

Note:	Microchip does not recommend code pro-
	tecting windowed devices.

#### 10.15 ID Locations

Four memory locations (2000h - 2003h) are designated as ID locations where the user can store checksum or other code-identification numbers. These locations are not accessible during normal execution, but are readable and writable during program/verify. It is recommended that only the 4 least significant bits of the ID location are used.

For ROM devices, these values are submitted along with the ROM code.

#### 10.16 In-Circuit Serial Programming™

PIC16CXXX microcontrollers can be serially programmed while in the end application circuit. This is simply done with two lines for clock and data, and three more lines for power, ground and the programming voltage. This allows customers to manufacture boards with unprogrammed devices, and then program the microcontroller just before shipping the product. This also allows the most recent firmware or a custom firmware to be programmed.

For complete details of serial programming, please refer to the In-Circuit Serial Programming (ICSP<sup>™</sup>) Guide, DS30277.

	PIC12CXXX	PIC14000	PIC16C5X	PIC16C6X	PIC16CXXX	PIC16F62X	X7OðfOld	XX7OðfOlq	PIC16C8X	PIC16F8XX	PIC16C9XX	X4271219	XX7371319	PIC18CXX2	63CXX 52CXX/ 54CXX/	хххсэн	мсвеххх	WCP2510
MPLAB™ Integrated 0 Development Environment	>	~	~	>	>	>	>	>	>	>	>	>	>	>				
MPLAB™ C17 Compiler												~	>					
WPLAB™ C18 Compiler														>				
0 MPASM/MPLINK	~	~	>	~	~	>	~	~	~	>	>	~	~	~	~	~		
20 MPLAB™-ICE	>	~	>	>	>	**^	>	>	>	>	>	>	>	>				
	>	~	>	>	>		>	>	>		>	>	>					
E ICEPIC™ Low-Cost □ In-Circuit Emulator	~		~	>	>		>	>	`		>							
Debugger Debugger				*>			*>			>								
ଥି PICSTART®Plus b Low-Cost Universal Dev. Kit	~	`	~	>	>	**>	>	>	`	>	>	>	`	`				
ଅଟେ PRO MATE® I ତା Universal Programmer	>	>	>	>	>	**^	>	>	>	>	>	>	~	~	~	~		
SIMICE	~		>															
PICDEM-1			>		>		+√		>			>						
PICDEM-2				+∕			+∕							>				
PICDEM-3											>							
PICDEM-14A		~																
PICDEM-17													~					
e KeeLoo <sup>®</sup> Evaluation Kit																~		
KEELoo Transponder Kit																~		
ö microlD™ Programmer's Kit																	`	
25 kHz microID Developer's Kit																	`	
Developer's Kit																	>	
13.56 MHz Anticollision microlD Developer's Kit																	>	
MCP2510 CAN Developer's Kit																		~
* Contact the Microchip Technology In ** Contact Microchip Technology Inc. 1 <sup>†</sup> Development tool is available on se	nc. web si for availab elect device	te at www ility date. es.	. microchi	o.com for	informatio	woh no n	to use the	e MPLAB	-ICD In-C	circuit Det	ougger (D	V164001	) with PIC	0.16C62, 6	33, 64, 65	5, 72, 73, 7	74, 76, 77	

TABLE 12-1: DEVELOPMENT TOOLS FROM MICROCHIP

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## 14.0 DC AND AC CHARACTERISTICS GRAPHS AND TABLES

The graphs and tables provided in this section are for **design guidance** and are **not tested**.

In some graphs or tables, the data presented are **outside specified operating range** (i.e., outside specified VDD range). This is for **information only** and devices are guaranteed to operate properly only within the specified range.

The data presented in this section is a **statistical summary** of data collected on units from different lots over a period of time and matrix samples. 'Typical' represents the mean of the distribution at  $25^{\circ}$ C. 'Max' or 'min' represents (mean +  $3\sigma$ ) or (mean -  $3\sigma$ ) respectively, where  $\sigma$  is standard deviation, over the whole temperature range.

## Graphs and Tables not available at this time.

Data is not available at this time but you may reference the *PIC16C72 Series Data Sheet* (DS39016,) DC and AC characteristic section, which contains data similar to what is expected.

NOTES:

## 15.3 <u>28-Lead Ceramic Dual In-line with Window (JW) – 300 mil (CERDIP)</u>



	0		Eo				
Dimension	Limits	MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		28			28	
Pitch	р		.100			2.54	
Top to Seating Plane	A	.170	.183	.195	4.32	4.64	4.95
Ceramic Package Height	A2	.155	.160	.165	3.94	4.06	4.19
Standoff	A1	.015	.023	.030	0.38	0.57	0.76
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Ceramic Pkg. Width	E1	.285	.290	.295	7.24	7.37	7.49
Overall Length	D	1.430	1.458	1.485	36.32	37.02	37.72
Tip to Seating Plane	L	.135	.140	.145	3.43	3.56	3.68
Lead Thickness	с	.008	.010	.012	0.20	0.25	0.30
Upper Lead Width	B1	.050	.058	.065	1.27	1.46	1.65
Lower Lead Width	В	.016	.019	.021	0.41	0.47	0.53
Overall Row Spacing	eB	.345	.385	.425	8.76	9.78	10.80
Window Width	W1	.130	.140	.150	3.30	3.56	3.81
Window Length	W2	.290	.300	.310	7.37	7.62	7.87

\*Controlling Parameter JEDEC Equivalent: MO-058 Drawing No. C04-080

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#### 28-Lead Plastic Shrink Small Outline (SS) - 209 mil, 5.30 mm (SSOP) 15.5



	Units		INCHES		N	<b>1ILLIMETERS</b>	S*
Dimension	Limits	MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		28			28	
Pitch	р		.026			0.66	
Overall Height	Α	.068	.073	.078	1.73	1.85	1.98
Molded Package Thickness	A2	.064	.068	.072	1.63	1.73	1.83
Standoff	A1	.002	.006	.010	0.05	0.15	0.25
Overall Width	E	.299	.309	.319	7.59	7.85	8.10
Molded Package Width	E1	.201	.207	.212	5.11	5.25	5.38
Overall Length	D	.396	.402	.407	10.06	10.20	10.34
Foot Length	L	.022	.030	.037	0.56	0.75	0.94
Lead Thickness	С	.004	.007	.010	0.10	0.18	0.25
Foot Angle	¢	0	4	8	0.00	101.60	203.20
Lead Width	В	.010	.013	.015	0.25	0.32	0.38
Mold Draft Angle Top	α	0	5	10	0	5	10
Mold Draft Angle Bottom	β	0	5	10	0	5	10

\*Controlling Parameter

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side. JEDEC Equivalent: MS-150

Drawing No. C04-073

## **APPENDIX A: REVISION HISTORY**

Version	Date	Revision Description
A	7/98	This is a new data sheet. However, the devices described in this data sheet are the upgrades to the devices found in the <i>PIC16C6X Data Sheet</i> , DS30234, and the <i>PIC16C7X Data Sheet</i> , DS30390.

## APPENDIX B: CONVERSION CONSIDERATIONS

Considerations for converting from previous versions of devices to the ones listed in this data sheet are listed in Table B-1.

## TABLE B-1: CONVERSION CONSIDERATIONS

Difference	PIC16C62A/72	PIC16C62B/72A
Voltage Range	2.5V - 6.0V	2.5V - 5.5V
SSP module	Basic SSP (2 mode SPI)	SSP (4 mode SPI)
CCP module	CCP does not reset TMR1 when in special event trigger mode.	N/A
Timer1 module	Writing to TMR1L register can cause over- flow in TMR1H register.	N/A

#### Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
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ISBN: 9781620769270

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