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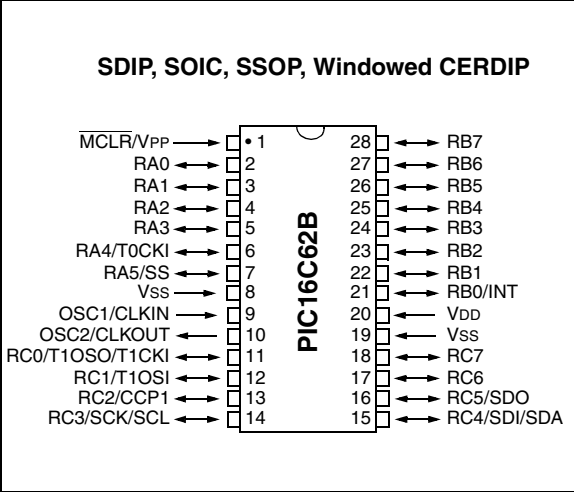
Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	I ² C, SPI
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	22
Program Memory Size	3.5KB (2K x 14)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 5.5V
Data Converters	A/D 5x8b
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16c72a-20-ss

PIC16C62B/72A

Pin Diagrams



Key Features PIC® Mid-Range Reference Manual (DS33023)	PIC16C62B	PIC16C72A
Operating Frequency	DC - 20 MHz	DC - 20 MHz
Resets (and Delays)	POR, BOR (PWRT, OST)	POR, BOR (PWRT, OST)
Program Memory (14-bit words)	2K	2K
Data Memory (bytes)	128	128
Interrupts	7	8
I/O Ports	Ports A,B,C	Ports A,B,C
Timers	3	3
Capture/Compare/PWM modules	1	1
Serial Communications	SSP	SSP
8-bit Analog-to-Digital Module	—	5 input channels

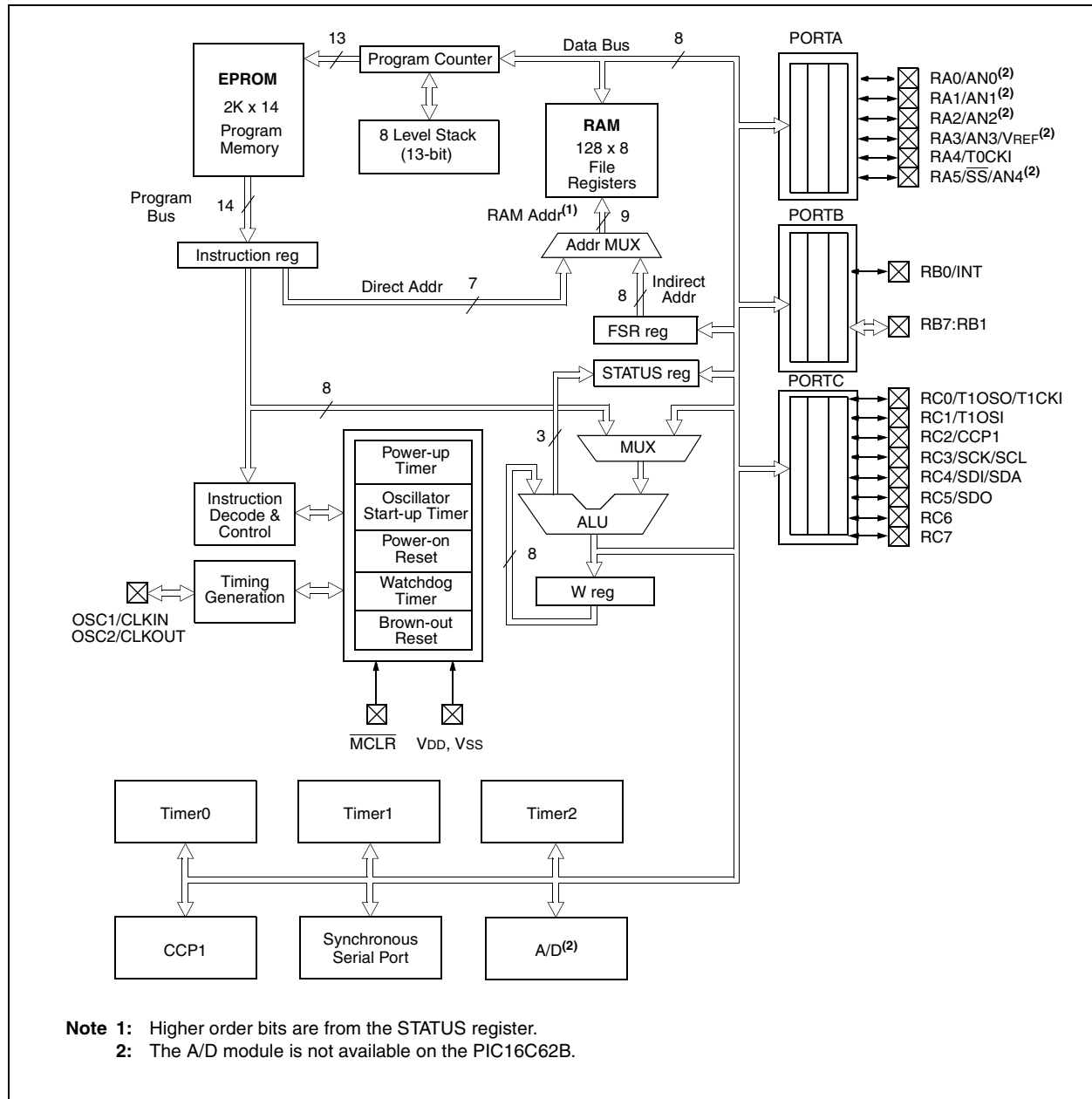
1.0 DEVICE OVERVIEW

This document contains device-specific information. Additional information may be found in the PIC® MCU Mid-Range Reference Manual, (DS33023), which may be obtained from your local Microchip Sales Representative or downloaded from the Microchip website. The Reference Manual should be considered a complementary document to this data sheet, and is highly recommended reading for a better understanding of the device architecture and operation of the peripheral modules.

There are two devices (PIC16C62B, PIC16C72A) covered by this datasheet. The PIC16C62B does not have the A/D module implemented.

Figure 1-1 is the block diagram for both devices. The pinouts are listed in Table 1-1.

FIGURE 1-1: PIC16C62B/PIC16C72A BLOCK DIAGRAM



PIC16C62B/72A

NOTES:

6.1 Timer2 Operation

The Timer2 output is also used by the CCP module to generate the PWM "On-Time", and the PWM period with a match with PR2.

The TMR2 register is readable and writable, and is cleared on any device reset.

The input clock ($F_{osc}/4$) has a prescale option of 1:1, 1:4 or 1:16, selected by control bits T2CKPS1:T2CKPS0 (T2CON<1:0>).

The match output of TMR2 goes through a 4-bit postscaler (which gives a 1:1 to 1:16 scaling) to generate a TMR2 interrupt (latched in flag bit TMR2IF, (PIR1<1>)).

The prescaler and postscaler counters are cleared when any of the following occurs:

- a write to the TMR2 register
- a write to the T2CON register
- any device reset (Power-on Reset, \overline{MCLR} reset, Watchdog Timer reset or Brown-out Reset)

TMR2 is not cleared when T2CON is written.

6.2 Timer2 Interrupt

The Timer2 module has an 8-bit period register PR2. Timer2 increments from 00h until it matches PR2 and then resets to 00h on the next increment cycle. PR2 is a readable and writable register. The PR2 register is initialized to FFh upon reset.

6.3 Output of TMR2

The output of TMR2 (before the postscaler) is fed to the Synchronous Serial Port module, which optionally uses it to generate shift clock.

TABLE 6-1 REGISTERS ASSOCIATED WITH TIMER2 AS A TIMER/COUNTER

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other resets
0Bh,8Bh	INTCON	GIE	PEIE	TOIE	INTE	RBIE	TOIF	INTF	RBIF	0000 000x	0000 000u
0Ch	PIR1	—	ADIF	—	—	SSPIF	CCP1IF	TMR2IF	TMR1IF	-00- 0000	0000 0000
8Ch	PIE1	—	ADIE	—	—	SSPIE	CCP1IE	TMR2IE	TMR1IE	-0-- 0000	0000 0000
11h	TMR2	Timer2 module's register								0000 0000	0000 0000
12h	T2CON	—	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0	-000 0000	-000 0000
92h	PR2	Timer2 Period Register								1111 1111	1111 1111

Legend: x = unknown, u = unchanged, - = unimplemented read as '0'. Shaded cells are not used by the Timer2 module.

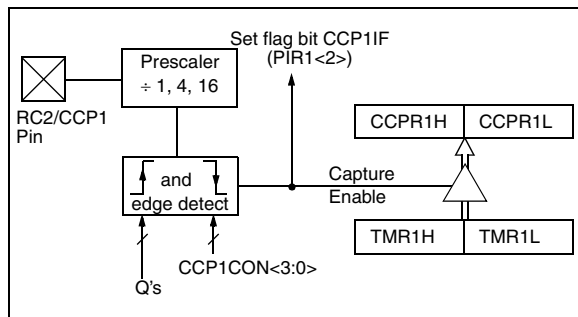
7.1 Capture Mode

In Capture mode, CCP1H:CCP1L captures the 16-bit value of the TMR1 register, when an event occurs on pin RC2/CCP1. An event is defined as:

- every falling edge
- every rising edge
- every 4th rising edge
- every 16th rising edge

An event is selected by control bits CCP1M3:CCP1M0 (CCP1CON<3:0>). When a capture is made, the interrupt request flag bit, CCP1IF (PIR1<2>), is set. It must be cleared in software. If another capture occurs before the value in register CCP1 is read, the old captured value will be lost.

FIGURE 7-1: CAPTURE MODE OPERATION BLOCK DIAGRAM



7.1.1 CCP PIN CONFIGURATION

In Capture mode, the RC2/CCP1 pin should be configured as an input by setting the TRISC<2> bit.

Note: If the RC2/CCP1 is configured as an output, a write to the port can cause a capture condition.

7.1.2 TIMER1 MODE SELECTION

Timer1 must be running in timer mode or synchronized counter mode for the CCP module to use the capture feature. In asynchronous counter mode, the capture operation may not work consistently.

7.1.3 SOFTWARE INTERRUPT

When the Capture mode is changed, a false capture interrupt may be generated. The user should clear CCP1IE (PIE1<2>) before changing the capture mode to avoid false interrupts. Clear the interrupt flag bit, CCP1IF before setting CCP1IE.

7.1.4 CCP PRESCALER

There are four prescaler settings, specified by bits CCP1M3:CCP1M0. Whenever the CCP module is turned off, or the CCP module is not in capture mode, the prescaler counter is cleared. This means that any reset will clear the prescaler counter.

Switching from one capture prescaler to another may generate an interrupt. Also, the prescaler counter will not be cleared, therefore the first capture may be from a non-zero prescaler. Example 7-1 shows the recommended method for switching between capture prescalers. This example also clears the prescaler counter and will not generate the “false” interrupt.

EXAMPLE 7-1: CHANGING BETWEEN CAPTURE PRESCALERS

```
CLRF    CCP1CON    ;Turn CCP module off
MOVLW   NEW_CAPT_PS ;Load the W reg with
                        ; the new prescaler
                        ; mode value and CCP ON
MOVWF   CCP1CON    ;Load CCP1CON with this
                        ; value
```

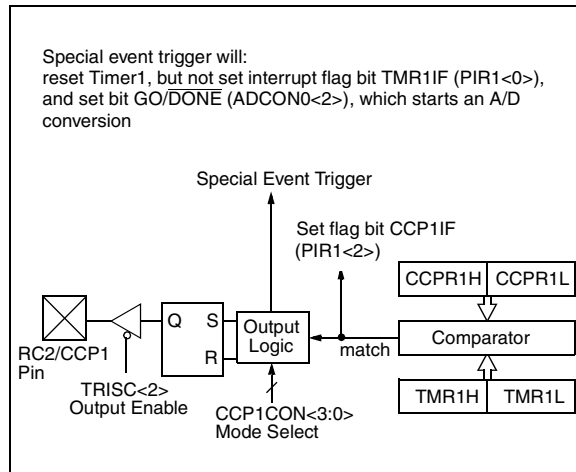
7.2 Compare Mode

In Compare mode, the 16-bit CCPR1 register value is constantly compared against the TMR1 register pair value. When a match occurs, the RC2/CCP1 pin is:

- driven High
- driven Low
- remains Unchanged

The action on the pin is based on the value of control bits CCP1M3:CCP1M0 (CCP1CON<3:0>). The interrupt flag bit, CCP1IF, is set on all compare matches.

FIGURE 7-2: COMPARE MODE OPERATION BLOCK DIAGRAM



7.2.1 CCP PIN CONFIGURATION

The user must configure the RC2/CCP1 pin as an output by clearing the TRISC<2> bit.

Note: Clearing the CCP1CON register will force the RC2/CCP1 compare output latch to the default low level. This is not the data latch.

7.2.2 TIMER1 MODE SELECTION

Timer1 must be running in Timer mode or Synchronized Counter mode if the CCP module is using the compare feature. In Asynchronous Counter mode, the compare operation may not work.

7.2.3 SOFTWARE INTERRUPT MODE

When a generated software interrupt is chosen, the CCP1 pin is not affected. Only a CCP interrupt is generated (if enabled).

7.2.4 SPECIAL EVENT TRIGGER

In this mode, an internal hardware trigger is generated, which may be used to initiate an action.

The special event trigger output of CCP1 resets the TMR1 register pair. This allows the CCPR1 register to effectively be a 16-bit programmable period register for Timer1.

The special trigger output of CCP1 resets the TMR1 register pair and starts an A/D conversion (if the A/D module is enabled).

TABLE 7-3 REGISTERS ASSOCIATED WITH CAPTURE, COMPARE, AND TIMER1

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other resets
0Bh,8Bh	INTCON	GIE	PEIE	TOIE	INTE	RBIE	TOIF	INTF	RBIF	0000 000x	0000 000u
0Ch	PIR1	—	ADIF	—	—	SSPIF	CCP1IF	TMR2IF	TMR1IF	-0-- 0000	-0-- 0000
8Ch	PIE1	—	ADIE	—	—	SSPIE	CCP1IE	TMR2IE	TMR1IE	-0-- 0000	-0-- 0000
87h	TRISC	PORTC Data Direction Register								1111 1111	1111 1111
0Eh	TMR1L	Holding register for the Least Significant Byte of the 16-bit TMR1 register								xxxx xxxx	uuuu uuuu
0Fh	TMR1H	Holding register for the Most Significant Byte of the 16-bit TMR1 register								xxxx xxxx	uuuu uuuu
10h	T1CON	—	—	T1CKPS1	T1CKPS0	T1OSCEN	T1SYN \bar{C}	TMR1CS	TMR1ON	--00 0000	--uu uuuu
15h	CCPR1L	Capture/Compare/PWM register1 (LSB)								xxxx xxxx	uuuu uuuu
16h	CCPR1H	Capture/Compare/PWM register1 (MSB)								xxxx xxxx	uuuu uuuu
17h	CCP1CON	—	—	CCP1X	CCP1Y	CCP1M3	CCP1M2	CCP1M1	CCP1M0	--00 0000	--00 0000

Legend: x = unknown, u = unchanged, - = unimplemented read as '0'. Shaded cells are not used by Capture and Timer1.

7.3 PWM Mode

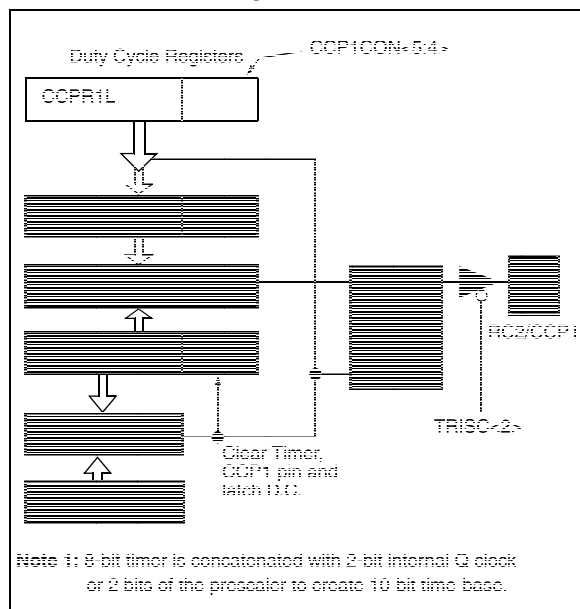
In Pulse Width Modulation (PWM) mode, the CCP1 pin produces up to a 10-bit resolution PWM output. Since the CCP1 pin is multiplexed with the PORTC data latch, the TRISC<2> bit must be cleared to make the CCP1 pin an output.

Note: Clearing the CCP1CON register will force the CCP1 PWM output latch to the default low level. This is not the PORTC I/O data latch.

Figure 7-3 shows a simplified block diagram of the CCP module in PWM mode.

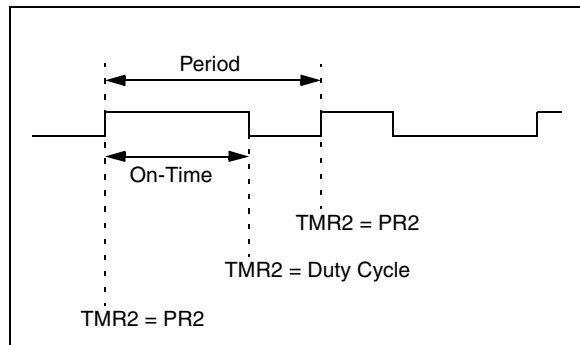
For a step by step procedure on how to set up the CCP module for PWM operation, see Section 7.3.3.

FIGURE 7-3: SIMPLIFIED PWM BLOCK DIAGRAM



A PWM output (Figure 7-4) has a time base (period) and a time that the output stays high (on-time). The frequency of the PWM is the inverse of the period (1/period).

FIGURE 7-4: PWM OUTPUT



7.3.1 PWM PERIOD

The PWM period is specified by writing to the PR2 register. The PWM period can be calculated using the following formula:

$$\text{PWM period} = [(PR2) + 1] \cdot 4 \cdot T_{osc} \cdot (\text{TMR2 prescale value})$$

PWM frequency is defined as $1 / [\text{PWM period}]$.

When TMR2 is equal to PR2, the following three events occur on the next increment cycle:

- TMR2 is cleared
- The CCP1 pin is set (exception: if PWM duty cycle = 0%, the CCP1 pin will not be set)
- The PWM duty cycle is latched from CCPR1L into CCPR1H

Note: The Timer2 postscaler (see Section 6.0) is not used in the determination of the PWM frequency. The postscaler could be used to have a servo update rate at a different frequency than the PWM output.

7.3.2 PWM ON-TIME

The PWM on-time is specified by writing to the CCPR1L register and to the CCP1CON<5:4> bits. Up to 10-bit resolution is available. CCPR1L contains eight MSBs and CCP1CON<5:4> contains two LSbs. This 10-bit value is represented by CCPR1L:CCP1CON<5:4>. The following equation is used to calculate the PWM duty cycle in time:

$$\text{PWM on-time} = (\text{CCPR1L:CCP1CON<5:4>}) \cdot T_{osc} \cdot (\text{TMR2 prescale value})$$

CCPR1L and CCP1CON<5:4> can be written to at any time, but the on-time value is not latched into CCPR1H until after a match between PR2 and TMR2 occurs (i.e., the period is complete). In PWM mode, CCPR1H is a read-only register.

The CCPR1H register and a 2-bit internal latch are used to double buffer the PWM on-time. This double buffering is essential for glitchless PWM operation.

When the CCPR1H and 2-bit latch match TMR2 concatenated with an internal 2-bit Q clock or 2 bits of the TMR2 prescaler, the CCP1 pin is cleared.

Maximum PWM resolution (bits) for a given PWM frequency:

$$\text{Resolution} = \frac{\log \left(\frac{F_{osc}}{F_{pwm}} \right)}{\log(2)} \text{ bits}$$

Note: If the PWM on-time value is larger than the PWM period, the CCP1 pin will not be cleared.

For an example PWM period and on-time calculation, see the PIC® MCU Mid-Range Reference Manual, (DS33023).

8.3.2 MASTER OPERATION

Master operation is supported in firmware using interrupt generation on the detection of the START and STOP conditions. The STOP (P) and START (S) bits are cleared by a reset or when the SSP module is disabled. The STOP (P) and START (S) bits will toggle based on the START and STOP conditions. Control of the I²C bus may be taken when the P bit is set, or the bus is idle and both the S and P bits are clear.

In master operation, the SCL and SDA lines are manipulated in software by clearing the corresponding TRISC<4:3> bit(s). The output level is always low, irrespective of the value(s) in PORTC<4:3>. So when transmitting data, a '1' data bit must have the TRISC<4> bit set (input) and a '0' data bit must have the TRISC<4> bit cleared (output). The same scenario is true for the SCL line with the TRISC<3> bit.

The following events will cause SSP Interrupt Flag bit, SSPIF, to be set (SSP Interrupt if enabled):

- START condition
- STOP condition
- Byte transfer completed

Master operation can be done with either the slave mode idle (SSPM3:SSPM0 = 1011) or with the slave active. When both master operation and slave modes are used, the software needs to differentiate the source(s) of the interrupt.

For more information on master operation, see AN554 - *Software Implementation of I²C Bus Master*.

8.3.3 MULTI-MASTER OPERATION

In multi-master operation, the interrupt generation on the detection of the START and STOP conditions allows the determination of when the bus is free. The STOP (P) and START (S) bits are cleared from a reset or when the SSP module is disabled. The STOP (P) and START (S) bits will toggle based on the START and STOP conditions. Control of the I²C bus may be taken when bit P (SSPSTAT<4>) is set, or the bus is idle and both the S and P bits clear. When the bus is busy, enabling the SSP Interrupt will generate the interrupt when the STOP condition occurs.

In multi-master operation, the SDA line must be monitored to see if the signal level is the expected output level. This check only needs to be done when a high level is output. If a high level is expected and a low level is present, the device needs to release the SDA and SCL lines (set TRISC<4:3>). There are two stages where this arbitration can be lost, these are:

- Address Transfer
- Data Transfer

When the slave logic is enabled, the slave continues to receive. If arbitration was lost during the address transfer stage, communication to the device may be in progress. If addressed, an ACK pulse will be generated. If arbitration was lost during the data transfer stage, the device will need to re-transfer the data at a later time.

For more information on master operation, see AN578 - *Use of the SSP Module in the of I²C Multi-Master Environment*.

TABLE 8-3 REGISTERS ASSOCIATED WITH I²C OPERATION

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other resets
0Bh, 8Bh	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000u
0Ch	PIR1	—	ADIF	—	—	SSPIF	CCP1IF	TMR2IF	TMR1IF	-0-- 0000	-0-- 0000
8Ch	PIE1	—	ADIE	—	—	SSPIE	CCP1IE	TMR2IE	TMR1IE	-0-- 0000	-0-- 0000
13h	SSPBUF	Synchronous Serial Port Receive Buffer/Transmit Register								xxxx xxxx	uuuu uuuu
93h	SSPADD	Synchronous Serial Port (I ² C mode) Address Register								0000 0000	0000 0000
14h	SSPCON	WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0	0000 0000	0000 0000
94h	SSPSTAT	SMP ⁽¹⁾	CKE ⁽¹⁾	D/ \bar{A}	P	S	R/ \bar{W}	UA	BF	0000 0000	0000 0000
87h	TRISC	PORTC Data Direction register								1111 1111	1111 1111

Legend: x = unknown, u = unchanged, - = unimplemented locations read as '0'.
Shaded cells are not used by SSP module in SPI mode.

Note 1: Maintain these bits clear in I²C mode.

PIC16C62B/72A

REGISTER 9-2:ADCON1 REGISTER (ADDRESS 9Fh)

U-0

U-0

U-0

U-0

U-0

R/W-0

R/W-0

R/W-0

—	—	—	—	—	PCFG2	PCFG1	PCFG0
---	---	---	---	---	-------	-------	-------

bit7

bit0

R = Readable bit
W = Writable bit
U = Unimplemented bit,
read as '0'
- n = Value at POR
reset

bit 7-3: **Unimplemented:** Read as '0'

bit 2-0: **PCFG2:PCFG0:** A/D Port Configuration Control bits

PCFG2:PCFG0	RA0	RA1	RA2	RA5	RA3	VREF
000	A	A	A	A	A	VDD
001	A	A	A	A	VREF	RA3
010	A	A	A	A	A	VDD
011	A	A	A	A	VREF	RA3
100	A	A	D	D	A	VDD
101	A	A	D	D	VREF	RA3
11x	D	D	D	D	D	VDD

A = Analog input

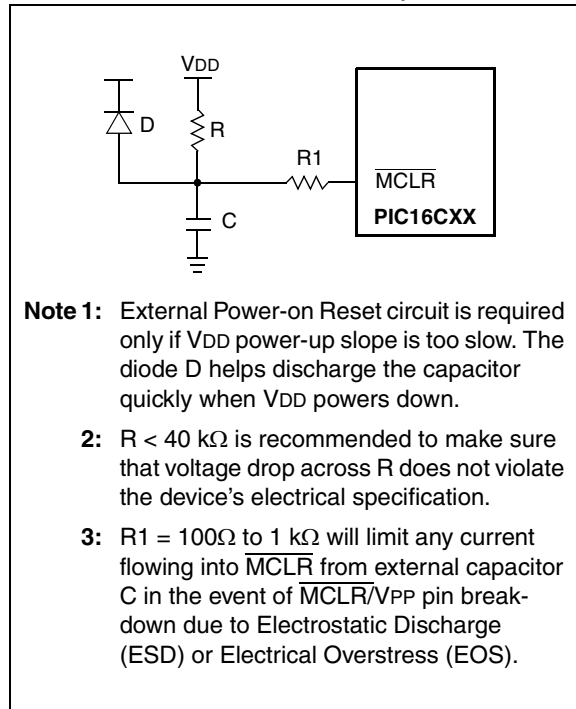
D = Digital I/O

10.4 Power-On Reset (POR)

A Power-on Reset pulse is generated on-chip when VDD rise is detected (in the range of 1.5V - 2.1V). To take advantage of the POR, just tie the $\overline{\text{MCLR}}$ pin directly (or through a resistor) to VDD. This will eliminate external RC components usually needed to create a Power-on Reset. A maximum rise time for VDD is specified (SVDD, parameter D004). For a slow rise time, see Figure 10-6.

When the device starts normal operation (exits the reset condition), device operating parameters (voltage, frequency, temperature,...) must be met to ensure operation. If these conditions are not met, the device must be held in reset until the operating conditions are met. Brown-out Reset may be used to meet the start-up conditions.

FIGURE 10-6: EXTERNAL POWER-ON RESET CIRCUIT (FOR SLOW VDD POWER-UP)



10.5 Power-up Timer (PWRT)

The Power-up Timer provides a fixed nominal time-out (TPWRT, parameter #33) from the POR. The Power-up Timer operates on an internal RC oscillator. The chip is kept in reset as long as the PWRT is active. The PWRT's time delay allows VDD to rise to an acceptable level. A configuration bit is provided to enable/disable the PWRT.

The power-up time delay will vary from chip-to-chip due to VDD, temperature and process variation. See DC parameters for details.

10.6 Oscillator Start-up Timer (OST)

The Oscillator Start-up Timer (OST) provides a delay of 1024 oscillator cycles (from OSC1 input) after the PWRT delay is over (TOST, parameter #32). This ensures that the crystal oscillator or resonator has started and stabilized.

The OST time-out is invoked only for XT, LP and HS modes and only on Power-on Reset or wake-up from SLEEP.

Note: The OST delay may not occur when the device wakes from SLEEP.

10.7 Brown-Out Reset (BOR)

The configuration bit, BODEN, can enable or disable the Brown-Out Reset circuit. If VPP falls below Vbor (parameter #35, about 100 μ S), the brown-out situation will reset the device. If VDD falls below VBOR for less than TBOR, a reset may not occur.

Once the brown-out occurs, the device will remain in brown-out reset until VDD rises above VBOR. The power-up timer then keeps the device in reset for TPWRT (parameter #33, about 72mS). If VDD should fall below VBOR during TPWRT, the brown-out reset process will restart when VDD rises above VBOR with the power-up timer reset. The power-up timer is always enabled when the brown-out reset circuit is enabled, regardless of the state of the $\overline{\text{PWRT}}$ configuration bit.

10.12 Watchdog Timer (WDT)

The Watchdog Timer is a free running on-chip RC oscillator which does not require any external components. This RC oscillator is separate from the RC oscillator of the OSC1/CLKIN pin. The WDT will run, even if the clock on the OSC1/CLKIN and OSC2/CLKOUT pins of the device has been stopped, for example, by execution of a `SLEEP` instruction.

During normal operation, a WDT time-out generates a device RESET (Watchdog Timer Reset). If the device is in SLEEP mode, a WDT time-out causes the device to wake-up and continue with normal operation (Watchdog Timer Wake-up). The \overline{TO} bit in the STATUS register will be cleared upon a Watchdog Timer time-out.

The WDT can be permanently disabled by clearing configuration bit WDTE (Section 10.1).

The WDT time-out period (T_{WDT} , parameter #31) is multiplied by the prescaler ratio, when the prescaler is assigned to the WDT. The prescaler assignment (assigned to either the WDT or Timer0) and prescaler ratio are set in the OPTION_REG register.

Note: The `CLRWDT` and `SLEEP` instructions clear the WDT and the postscaler, if assigned to the WDT, and prevent it from timing out and generating a device RESET condition.

Note: When a `CLRWDT` instruction is executed and the prescaler is assigned to the WDT, the prescaler count will be cleared, but the prescaler assignment is not changed.

FIGURE 10-8: WATCHDOG TIMER BLOCK DIAGRAM

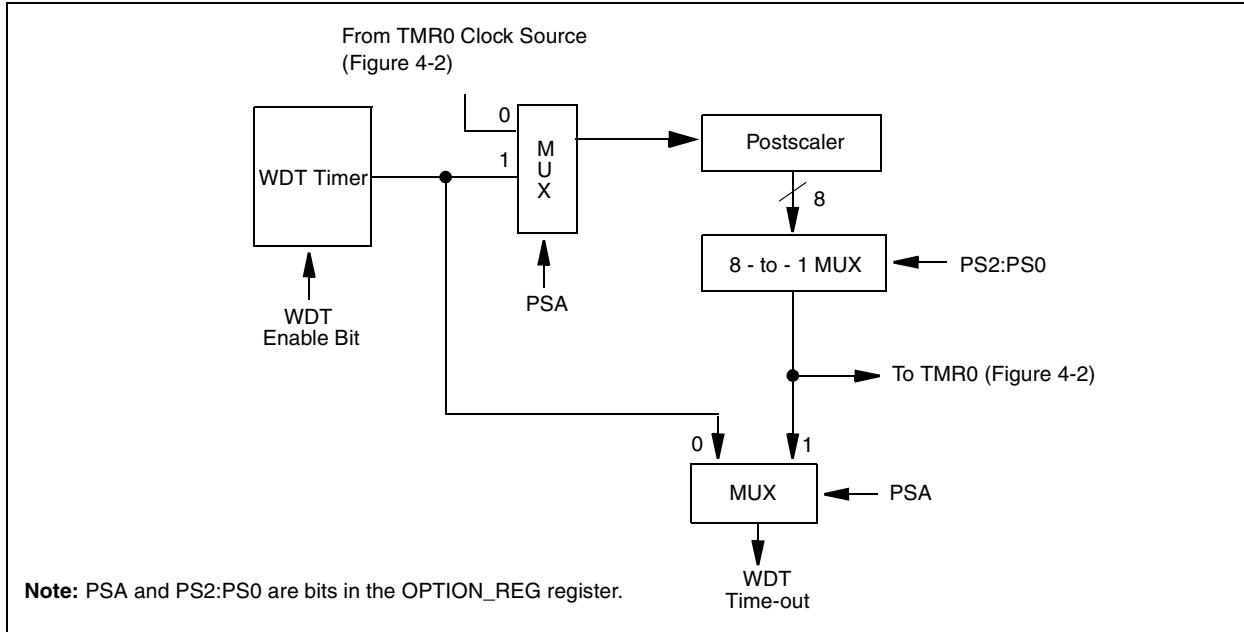


FIGURE 10-9: SUMMARY OF WATCHDOG TIMER REGISTERS

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
2007h	Config. bits		BODEN	CP1	CP0	\overline{PWRTE}	WDTE	FOSC1	FOSC0
81h	OPTION_REG	\overline{RBPU}	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0

Legend: Shaded cells are not used by the Watchdog Timer.

12.0 DEVELOPMENT SUPPORT

The PIC® microcontrollers are supported with a full range of hardware and software development tools:

- Integrated Development Environment
 - MPLAB™ IDE Software
- Assemblers/Compilers/Linkers
 - MPASM Assembler
 - MPLAB-C17 and MPLAB-C18 C Compilers
 - MPLINK/MPLIB Linker/Librarian
- Simulators
 - MPLAB-SIM Software Simulator
- Emulators
 - MPLAB-ICE Real-Time In-Circuit Emulator
 - PICMASTER®/PICMASTER-CE In-Circuit Emulator
 - ICEPIC™
- In-Circuit Debugger
 - MPLAB-ICD for PIC16F877
- Device Programmers
 - PRO MATE® II Universal Programmer
 - PICSTART® Plus Entry-Level Prototype Programmer
- Low-Cost Demonstration Boards
 - SIMICE
 - PICDEM-1
 - PICDEM-2
 - PICDEM-3
 - PICDEM-17
 - SEEVAL®
 - KEELOQ®

12.1 MPLAB Integrated Development Environment Software

- The MPLAB IDE software brings an ease of software development previously unseen in the 8-bit microcontroller market. MPLAB is a Windows®-based application which contains:
- Multiple functionality
 - editor
 - simulator
 - programmer (sold separately)
 - emulator (sold separately)
- A full featured editor
- A project manager
- Customizable tool bar and key mapping
- A status bar
- On-line help

MPLAB allows you to:

- Edit your source files (either assembly or 'C')
- One touch assemble (or compile) and download to PIC MCU tools (automatically updates all project information)
- Debug using:
 - source files
 - absolute listing file
 - object code

The ability to use MPLAB with Microchip's simulator, MPLAB-SIM, allows a consistent platform and the ability to easily switch from the cost-effective simulator to the full featured emulator with minimal retraining.

12.2 MPASM Assembler

MPASM is a full featured universal macro assembler for all PIC MCUs. It can produce absolute code directly in the form of HEX files for device programmers, or it can generate relocatable objects for MPLINK.

MPASM has a command line interface and a Windows shell and can be used as a standalone application on a Windows 3.x or greater system. MPASM generates relocatable object files, Intel standard HEX files, MAP files to detail memory usage and symbol reference, an absolute LST file which contains source lines and generated machine code, and a COD file for MPLAB debugging.

MPASM features include:

- MPASM and MPLINK are integrated into MPLAB projects.
- MPASM allows user defined macros to be created for streamlined assembly.
- MPASM allows conditional assembly for multi purpose source files.
- MPASM directives allow complete control over the assembly process.

12.3 MPLAB-C17 and MPLAB-C18 C Compilers

The MPLAB-C17 and MPLAB-C18 Code Development Systems are complete ANSI 'C' compilers and integrated development environments for Microchip's PIC17CXXX and PIC18CXXX family of microcontrollers, respectively. These compilers provide powerful integration capabilities and ease of use not found with other compilers.

For easier source level debugging, the compilers provide symbol information that is compatible with the MPLAB IDE memory display.

12.4 MPLINK/MPLIB Linker/Librarian

MPLINK is a relocatable linker for MPASM and MPLAB-C17 and MPLAB-C18. It can link relocatable objects from assembly or C source files along with pre-compiled libraries using directives from a linker script.

and test the sample code. In addition, PICDEM-17 supports down-loading of programs to and executing out of external FLASH memory on board. The PICDEM-17 is also usable with the MPLAB-ICE or PICMASTER emulator, and all of the sample programs can be run and modified using either emulator. Additionally, a generous prototype area is available for user hardware.

12.17 SEEVAL Evaluation and Programming System

The SEEVAL SEEPROM Designer's Kit supports all Microchip 2-wire and 3-wire Serial EEPROMs. The kit includes everything necessary to read, write, erase or program special features of any Microchip SEEPROM product including Smart Serials™ and secure serials. The Total Endurance™ Disk is included to aid in trade-off analysis and reliability calculations. The total kit can significantly reduce time-to-market and result in an optimized system.

12.18 KEELOQ Evaluation and Programming Tools

KEELOQ evaluation and programming tools support Microchips HCS Secure Data Products. The HCS evaluation kit includes an LCD display to show changing codes, a decoder to decode transmissions, and a programming interface to program test transmitters.

TABLE 12-1: DEVELOPMENT TOOLS FROM MICROCHIP

	PIC12CXXX	PIC14000	PIC16C5X	PIC16C6X	PIC16CXXX	PIC16F62X	PIC16C7X	PIC16C7XX	PIC16C8X	PIC16F8XX	PIC16C9XX	PIC17C4X	PIC17C7XX	PIC18CXX2	24CXX/ 25CXX/ 93CXX	HC5XX	MCRFXXX	MCP2510
Software Tools	MPLAB™ Integrated Development Environment	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		✓
	MPLAB™ C17 Compiler																	
Software Tools	MPLAB™ C18 Compiler																	
	MPASM/MPLINK	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		
Emulators	MPLAB™-ICE	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		
	PICMASTER/PICMASTER-CE	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		
Emulators	ICEPIC™ Low-Cost In-Circuit Emulator	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		
Debugger	MPLAB-ICD In-Circuit Debugger				✓*		✓*			✓								
Programmers	PICSTART® Plus Low-Cost Universal Dev. Kit	✓	✓	✓	✓	✓**	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		
	PRO MATE® II Universal Programmer	✓	✓	✓	✓	✓**	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		
Demo Boards and Eval Kits	SIMICE	✓	✓	✓			✓†											
	PICDEM-1		✓	✓					✓			✓						
	PICDEM-2				✓†		✓†							✓				
	PICDEM-3										✓							
	PICDEM-14A		✓															
	PICDEM-17											✓						
	KEELOQ® Evaluation Kit															✓		
	KEELOQ Transponder Kit															✓		
	microID™ Programmer's Kit																✓	
	125 kHz microID Developer's Kit																✓	
Demo Boards and Eval Kits	125 kHz Anticollision microID Developer's Kit																✓	
	13.56 MHz Anticollision microID Developer's Kit																✓	
	MCP2510 CAN Developer's Kit																✓	✓

* Contact the Microchip Technology Inc. web site at www.microchip.com for information on how to use the MPLAB-ICD In-Circuit Debugger (DV164001) with PIC16C62, 63, 64, 65, 72, 73, 74, 76, 77

** Contact Microchip Technology Inc. for availability date.

† Development tool is available on select devices.

Standard Operating Conditions (unless otherwise stated) Operating temperature 0°C ≤ TA ≤ +70°C for commercial -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended Operating voltage VDD range as described in DC spec Section 13.1 and Section 13.2							
Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
D083		OSC2/CLKOUT (RC osc mode)	- - -	- - -	0.6 0.6 0.6	V V V	IOL = 7.0 mA, VDD = 4.5V, -40°C to +125°C IOL = 1.6 mA, VDD = 4.5V, -40°C to +85°C IOL = 1.2 mA, VDD = 4.5V, -40°C to +125°C
D090	VOH	Output High Voltage I/O ports (Note 3)	VDD-0.7	-	-	V	IOH = -3.0 mA, VDD = 4.5V, -40°C to +85°C
			VDD-0.7	-	-	V	IOH = -2.5 mA, VDD = 4.5V, -40°C to +125°C
D092		OSC2/CLKOUT (RC osc mode)	VDD-0.7	-	-	V	IOH = -1.3 mA, VDD = 4.5V, -40°C to +85°C
			VDD-0.7	-	-	V	IOH = -1.0 mA, VDD = 4.5V, -40°C to +125°C
D150*	VOD	Open-Drain High Voltage	-	-	8.5	V	RA4 pin
		Capacitive Loading Specs on Output Pins					
D100	Cosc2	OSC2 pin	-	-	15	pF	In XT, HS and LP modes when external clock is used to drive OSC1.
D101	Cio	All I/O pins and OSC2 (in RC mode)	-	-	50	pF	
D102	Cb	SCL, SDA in I²C mode	-	-	400	pF	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In RC oscillator mode, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the device be driven with external clock in RC mode.

2: The leakage current on the \overline{MCLR}/V_{PP} pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as current sourced by the pin.

FIGURE 13-7: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER TIMING

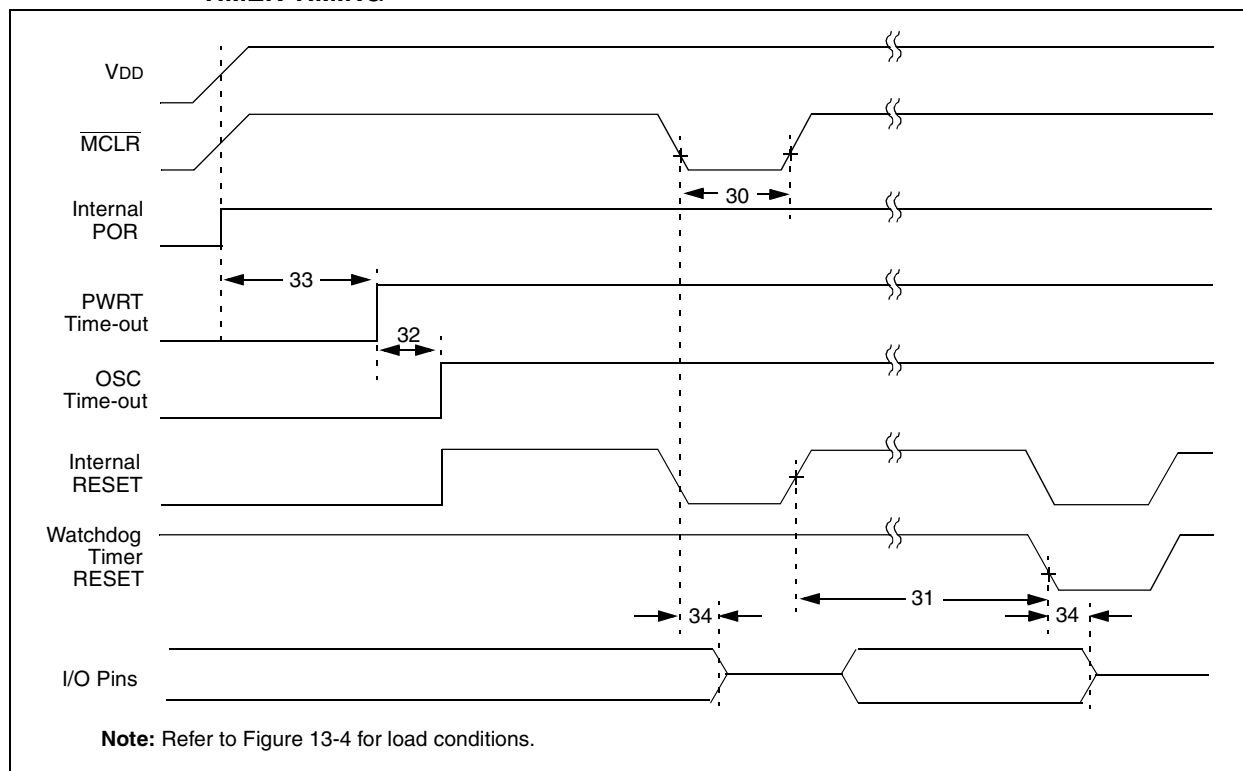


FIGURE 13-8: BROWN-OUT RESET TIMING

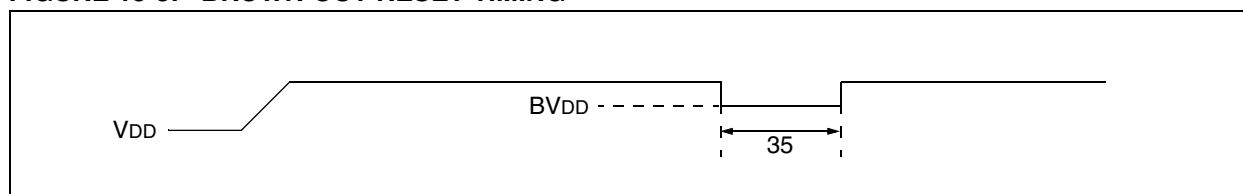


TABLE 13-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, POWER-UP TIMER AND BROWN-OUT RESET REQUIREMENTS

Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
30	T _{mcL}	MCLR Pulse Width (low)	2	—	—	μs	V _{DD} = 5V, -40°C to +125°C
31*	T _{wdt}	Watchdog Timer Time-out Period (No Prescaler)	7	18	33	ms	V _{DD} = 5V, -40°C to +125°C
32	T _{ost}	Oscillator Start-up Timer Period	—	1024 T _{osc}	—	—	T _{osc} = OSC1 period
33*	T _{pwrt}	Power-up Timer Period	28	72	132	ms	V _{DD} = 5V, -40°C to +125°C
34	T _{ioz}	I/O Hi-impedance from MCLR Low or WDT reset	—	—	2.1	μs	
35	T _{bor}	Brown-out Reset Pulse Width	100	—	—	μs	V _{DD} ≤ BV _{DD} (D005)

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 13-9: TIMER0 AND TIMER1 EXTERNAL CLOCK TIMINGS

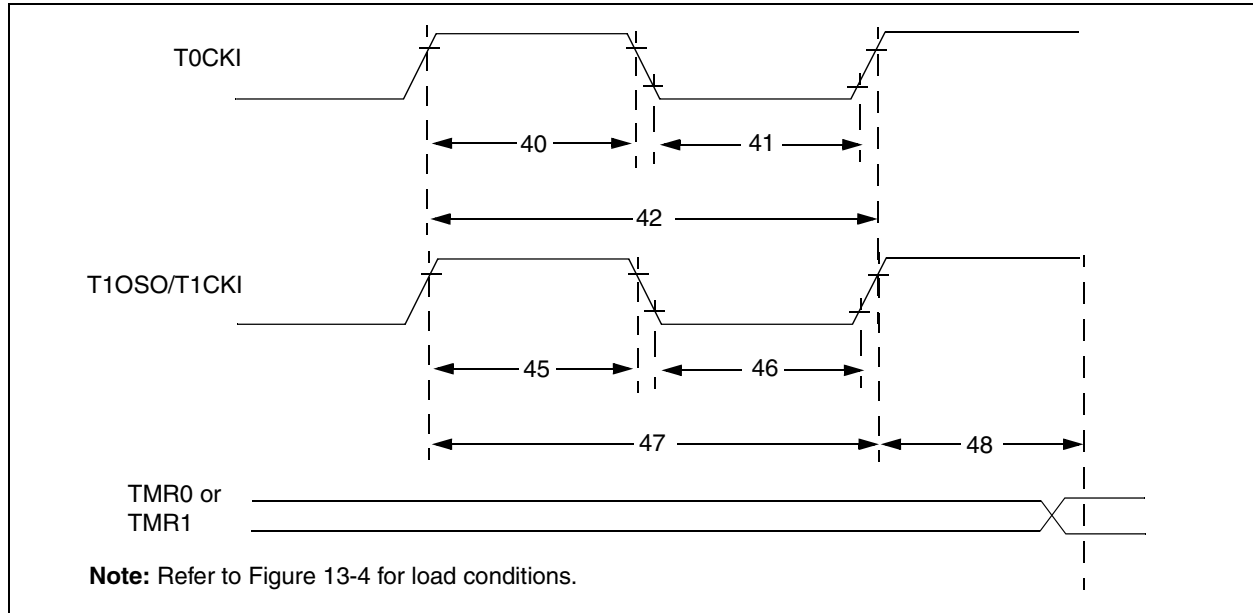


TABLE 13-5: TIMER0 AND TIMER1 EXTERNAL CLOCK REQUIREMENTS

Param No.	Sym	Characteristic		Min	Typ†	Max	Units	Conditions	
40*	Tt0H	T0CKI High Pulse Width		No Prescaler 0.5TCY + 20 With Prescaler 10	— —	— —	ns ns	Must also meet parameter 42	
41*	Tt0L	T0CKI Low Pulse Width		No Prescaler 0.5TCY + 20 With Prescaler 10	— —	— —	ns ns	Must also meet parameter 42	
42*	Tt0P	T0CKI Period		No Prescaler TCY + 40 With Prescaler Greater of: 20 or $\frac{TCY + 40}{N}$	— —	— —	ns ns	N = prescale value (2, 4,..., 256)	
45*	Tt1H	T1CKI High Time	Synchronous, Prescaler = 1	0.5TCY + 20	—	—	ns	Must also meet parameter 47	
	Synchronous, Prescaler = 2,4,8		PIC16CXX	15	—	—	ns		
			PIC16LCXX	25	—	—	ns		
	Asynchronous		PIC16CXX	30	—	—	ns		
			PIC16LCXX	50	—	—	ns		
46*	Tt1L	T1CKI Low Time	Synchronous, Prescaler = 1	0.5TCY + 20	—	—	ns	Must also meet parameter 47	
	Synchronous, Prescaler = 2,4,8		PIC16CXX	15	—	—	ns		
			PIC16LCXX	25	—	—	ns		
	Asynchronous		PIC16CXX	30	—	—	ns		
			PIC16LCXX	50	—	—	ns		
47*	Tt1P	T1CKI input period	Synchronous	PIC16CXX	GREATER OF: 30 OR $\frac{TCY + 40}{N}$	—	—	ns	N = prescale value (1, 2, 4, 8)
				PIC16LCXX	GREATER OF: 50 OR $\frac{TCY + 40}{N}$				N = prescale value (1, 2, 4, 8)
			Asynchronous	PIC16CXX	60	—	—	ns	
				PIC16LCXX	100	—	—	ns	
	Ft1		Timer1 oscillator input frequency range (oscillator enabled by setting bit T1OSCEN)		DC	—	200	kHz	
48	TCKEZtmr1	Delay from external clock edge to timer increment		2Tosc	—	7Tosc	—		

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

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CLRF	70	RB0/INT Flag (INTF Bit)	13
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