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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	I <sup>2</sup> C, SPI
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	22
Program Memory Size	3.5KB (2K x 14)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 5.5V
Data Converters	A/D 5x8b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	28-DIP (0.300", 7.62mm)
Supplier Device Package	28-SPDIP
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/pic16c72a-20i-sp">https://www.e-xfl.com/product-detail/microchip-technology/pic16c72a-20i-sp</a>

## 2.2.2.1 STATUS REGISTER

The STATUS register, shown in Register 2-1, contains the arithmetic status of the ALU, the RESET status and the bank select bits for data memory.

The STATUS register can be the destination for any instruction, as with any other register. If the STATUS register is the destination for an instruction that affects the Z, DC or C bits, the write to these three bits is disabled. These bits are set or cleared according to the device logic. The  $\overline{\text{TO}}$  and  $\overline{\text{PD}}$  bits are not writable. The result of an instruction with the STATUS register as destination may be different than intended.

For example, `CLRF STATUS` will clear the upper-three bits and set the Z bit. This leaves the STATUS register as `000u u1uu` (where u = unchanged).

It is recommended, therefore, that only `BCF`, `BSF`, `SWAPF` and `MOVWF` instructions are used to alter the STATUS register, because these instructions do not affect the Z, C or DC bits from the STATUS register. For other instructions, not affecting any status bits, see the "Instruction Set Summary."

**Note 1:** The IRP and RP1 bits are reserved. Maintain these bits clear to ensure upward compatibility with future products.

**Note 2:** The C and DC bits operate as a borrow and digit borrow bit, respectively, in subtraction. See the `SUBLW` and `SUBWF` instructions.

### REGISTER 2-1: STATUS REGISTER (ADDRESS 03h, 83h)

R/W-0	R/W-0	R/W-0	R-1	R-1	R/W-x	R/W-x	R/W-x
IRP	RP1	RP0	$\overline{\text{TO}}$	$\overline{\text{PD}}$	Z	DC	C
bit7							bit0

R = Readable bit  
W = Writable bit  
U = Unimplemented bit, read as '0'  
- n = Value at POR reset

- bit 7: **IRP:** Register Bank Select bit (used for indirect addressing) (reserved, maintain clear)
- bit 6-5: **RP1:RP0:** Register Bank Select bits (used for direct addressing)
  - 01 = Bank 1 (80h - FFh)
  - 00 = Bank 0 (00h - 7Fh)
  - Each bank is 128 bytes
  - Note:** RP1 is reserved, maintain clear
- bit 4:  **$\overline{\text{TO}}$ :** Time-out bit
  - 1 = After power-up, `CLRWDI` instruction, or `SLEEP` instruction
  - 0 = A WDT time-out occurred
- bit 3:  **$\overline{\text{PD}}$ :** Power-down bit
  - 1 = After power-up or by the `CLRWDI` instruction
  - 0 = By execution of the `SLEEP` instruction
- bit 2: **Z:** Zero bit
  - 1 = The result of an arithmetic or logic operation is zero
  - 0 = The result of an arithmetic or logic operation is not zero
- bit 1: **DC:** Digit carry/borrow bit (`ADDWF`, `ADDLW`, `SUBLW`, `SUBWF` instructions) (for borrow, the polarity is reversed)
  - 1 = A carry-out from the 4th low order bit of the result occurred
  - 0 = No carry-out from the 4th low order bit of the result
- bit 0: **C:** Carry/borrow bit (`ADDWF`, `ADDLW`, `SUBLW`, `SUBWF` instructions) (for borrow, the polarity is reversed)
  - 1 = A carry-out from the most significant bit of the result occurred
  - 0 = No carry-out from the most significant bit of the result occurred

**Note:** For borrow, the polarity is reversed. A subtraction is executed by adding the two's complement of the second operand. For rotate (`RRF`, `RLF`) instructions, this bit is loaded with either the high or low order bit of the source register.

## 5.0 TIMER1 MODULE

The Timer1 module timer/counter has the following features:

- 16-bit timer/counter
- Readable and writable
- Internal or external clock select
- Interrupt on overflow from FFFFh to 0000h
- Reset from CCP module trigger

Timer1 has a control register, shown in Register 5-1. Timer1 can be enabled/disabled by setting/clearing control bit TMR1ON (T1CON<0>).

Figure 5-1 is a simplified block diagram of the Timer1 module.

Additional information on timer modules is available in the PIC® MCU Mid-Range Reference Manual, (DS33023).

## 5.1 Timer1 Operation

Timer1 can operate in one of these modes:

- As a timer
- As a synchronous counter
- As an asynchronous counter

The operating mode is determined by the clock select bit, TMR1CS (T1CON<1>).

In timer mode, Timer1 increments every instruction cycle. In counter mode, it increments on every rising edge of the external clock input.

When the Timer1 oscillator is enabled (T1OSCEN is set), the RC1/T1OSI and RC0/T1OSO/T1CKI pins become inputs. That is, the TRISC<1:0> value is ignored.

Timer1 also has an internal “reset input”. This reset can be generated by the CCP module as a special event trigger (Section 7.0).

### REGISTER 5-1: T1CON: TIMER1 CONTROL REGISTER (ADDRESS 10h)

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	T1CKPS1	T1CKPS0	T1OSCEN	T1SYN̄C	TMR1CS	TMR1ON
bit7							bit0

R = Readable bit  
W = Writable bit  
U = Unimplemented bit, read as '0'  
- n = Value at POR reset

bit 7-6: **Unimplemented:** Read as '0'

bit 5-4: **T1CKPS1:T1CKPS0:** Timer1 Input Clock Prescale Select bits  
11 = 1:8 Prescale value  
10 = 1:4 Prescale value  
01 = 1:2 Prescale value  
00 = 1:1 Prescale value

bit 3: **T1OSCEN:** Timer1 Oscillator Enable Control bit  
1 = Oscillator is enabled (TRISC<1:0> ignored)  
0 = Oscillator is shut off  
(The oscillator is turned off to reduce power drain)

bit 2: **T1SYN̄C:** Timer1 External Clock Input Synchronization Control bit  
TMR1CS = 1  
1 = Do not synchronize external clock input  
0 = Synchronize external clock input  
TMR1CS = 0  
This bit is ignored. Timer1 uses the internal clock when TMR1CS = 0.

bit 1: **TMR1CS:** Timer1 Clock Source Select bit  
1 = External clock from pin RC0/T1OSO/T1CKI (on the rising edge)  
0 = Internal clock (Fosc/4)

bit 0: **TMR1ON:** Timer1 On bit  
1 = Enables Timer1  
0 = Stops Timer1

## 6.1 Timer2 Operation

The Timer2 output is also used by the CCP module to generate the PWM "On-Time", and the PWM period with a match with PR2.

The TMR2 register is readable and writable, and is cleared on any device reset.

The input clock ( $F_{osc}/4$ ) has a prescale option of 1:1, 1:4 or 1:16, selected by control bits T2CKPS1:T2CKPS0 (T2CON<1:0>).

The match output of TMR2 goes through a 4-bit postscaler (which gives a 1:1 to 1:16 scaling) to generate a TMR2 interrupt (latched in flag bit TMR2IF, (PIR1<1>)).

The prescaler and postscaler counters are cleared when any of the following occurs:

- a write to the TMR2 register
- a write to the T2CON register
- any device reset (Power-on Reset,  $\overline{MCLR}$  reset, Watchdog Timer reset or Brown-out Reset)

TMR2 is not cleared when T2CON is written.

## 6.2 Timer2 Interrupt

The Timer2 module has an 8-bit period register PR2. Timer2 increments from 00h until it matches PR2 and then resets to 00h on the next increment cycle. PR2 is a readable and writable register. The PR2 register is initialized to FFh upon reset.

## 6.3 Output of TMR2

The output of TMR2 (before the postscaler) is fed to the Synchronous Serial Port module, which optionally uses it to generate shift clock.

**TABLE 6-1 REGISTERS ASSOCIATED WITH TIMER2 AS A TIMER/COUNTER**

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other resets
0Bh,8Bh	INTCON	GIE	PEIE	TOIE	INTE	RBIE	TOIF	INTF	RBIF	0000 000x	0000 000u
0Ch	PIR1	—	ADIF	—	—	SSPIF	CCP1IF	TMR2IF	TMR1IF	-00- 0000	0000 0000
8Ch	PIE1	—	ADIE	—	—	SSPIE	CCP1IE	TMR2IE	TMR1IE	-0-- 0000	0000 0000
11h	TMR2	Timer2 module's register								0000 0000	0000 0000
12h	T2CON	—	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0	-000 0000	-000 0000
92h	PR2	Timer2 Period Register								1111 1111	1111 1111

Legend: x = unknown, u = unchanged, - = unimplemented read as '0'. Shaded cells are not used by the Timer2 module.

## 7.3.3 SET-UP FOR PWM OPERATION

The following steps should be taken when configuring the CCP module for PWM operation:

1. Set the PWM period by writing to the PR2 register.
2. Set the PWM on-time by writing to the CCPR1L register and CCP1CON<5:4> bits.
3. Make the CCP1 pin an output by clearing the TRISC<2> bit.
4. Set the TMR2 prescale value and enable Timer2 by writing to T2CON.
5. Configure the CCP1 module for PWM operation.

**TABLE 7-4 EXAMPLE PWM FREQUENCIES AND RESOLUTIONS AT 20 MHz**

PWM Frequency	1.22 kHz	4.88 kHz	19.53 kHz	78.12 kHz	156.3 kHz	208.3 kHz
Timer Prescaler (1, 4, 16)	16	4	1	1	1	1
PR2 Value	0xFF	0xFF	0xFF	0x3F	0x1F	0x17
Maximum Resolution (bits)	10	10	10	8	7	5.5

**TABLE 7-5 REGISTERS ASSOCIATED WITH PWM AND TIMER2**

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other resets
0Bh,8Bh	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000u
0Ch	PIR1	—	ADIF	—	—	SSPIF	CCP1IF	TMR2IF	TMR1IF	-0-- 0000	-0-- 0000
8Ch	PIE1	—	ADIE	—	—	SSPIE	CCP1IE	TMR2IE	TMR1IE	-0-- 0000	-0-- 0000
87h	TRISC	PORTC Data Direction Register								1111 1111	1111 1111
11h	TMR2	Timer2 module's register								0000 0000	0000 0000
92h	PR2	Timer2 module's period register								1111 1111	1111 1111
12h	T2CON	—	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0	-000 0000	-000 0000
15h	CCPR1L	Capture/Compare/PWM register1 (LSB)								xxxx xxxx	uuuu uuuu
16h	CCPR1H	Capture/Compare/PWM register1 (MSB)								xxxx xxxx	uuuu uuuu
17h	CCP1CON	—	—	CCP1X	CCP1Y	CCP1M3	CCP1M2	CCP1M1	CCP1M0	--00 0000	--00 0000

Legend: x = unknown, u = unchanged, - = unimplemented read as '0'. Shaded cells are not used by PWM and Timer2.

NOTES:

## 8.0 SYNCHRONOUS SERIAL PORT (SSP) MODULE

### 8.1 SSP Module Overview

The Synchronous Serial Port (SSP) module is a serial interface useful for communicating with other peripheral or microcontroller devices. These peripheral devices may be Serial EEPROMs, shift registers, display drivers, A/D converters, etc. The SSP module can operate in one of two modes:

- Serial Peripheral Interface (SPI)
- Inter-Integrated Circuit (I<sup>2</sup>C)

For more information on SSP operation (including an I<sup>2</sup>C Overview), refer to the PIC<sup>®</sup> MCU Mid-Range Reference Manual, (DS33023). Also, refer to Application Note AN578, "Use of the SSP Module in the I<sup>2</sup>C Multi-Master Environment."

### 8.2 SPI Mode

This section contains register definitions and operational characteristics of the SPI module.

Additional information on SPI operation may be found in the PIC<sup>®</sup> MCU Mid-Range Reference Manual, (DS33023).

#### 8.2.1 OPERATION OF SSP MODULE IN SPI MODE

A block diagram of the SSP Module in SPI Mode is shown in Figure 8-1.

The SPI mode allows 8-bits of data to be synchronously transmitted and received simultaneously. To accomplish communication, three pins are used:

- Serial Data Out (SDO) RC5/SDO
- Serial Data In (SDI) RC4/SDI/SDA
- Serial Clock (SCK) RC3/SCK/SCL

Additionally, a fourth pin may be used when in a slave mode of operation:

- Slave Select ( $\overline{SS}$ ) RA5/ $\overline{SS}$ /AN4

When initializing the SPI, several options need to be specified. This is done by programming the appropriate control bits in the SSPCON register (SSPCON<5:0>) and SSPSTAT<7:6>. These control bits allow the following to be specified:

- Master Operation (SCK is the clock output)
- Slave Mode (SCK is the clock input)
- Clock Polarity (Idle state of SCK)
- Clock Edge (Output data on rising/falling edge of SCK)
- Clock Rate (master operation only)
- Slave Select Mode (Slave mode only)

To enable the serial port, SSP Enable bit, SSPEN (SSPCON<5>) must be set. To reset or reconfigure SPI mode, clear bit SSPEN, re-initialize the SSPCON reg-

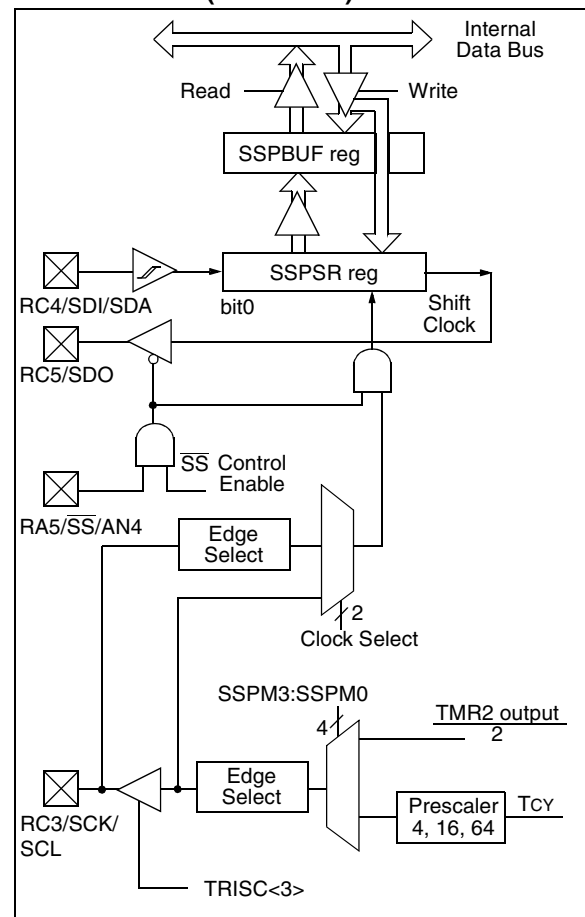
ister, and then set bit SSPEN. This configures the SDI, SDO, SCK and  $\overline{SS}$  pins as serial port pins. For the pins to behave as the serial port function, they must have their data direction bits (in the TRISC register) appropriately programmed. That is:

- SDI must have TRISC<4> set
- SDO must have TRISC<5> cleared
- SCK (master operation) must have TRISC<3> cleared
- SCK (Slave mode) must have TRISC<3> set
- $\overline{SS}$  must have TRISA<5> set (if used)

**Note:** When the SPI is in Slave Mode with  $\overline{SS}$  pin control enabled, (SSPCON<3:0> = 0100) the SPI module will reset if the  $\overline{SS}$  pin is set to V<sub>DD</sub>.

**Note:** If the SPI is used in Slave Mode with CKE = '1', then the  $\overline{SS}$  pin control must be enabled.

**FIGURE 8-1: SSP BLOCK DIAGRAM (SPI MODE)**



## 8.3.1.3 TRANSMISSION

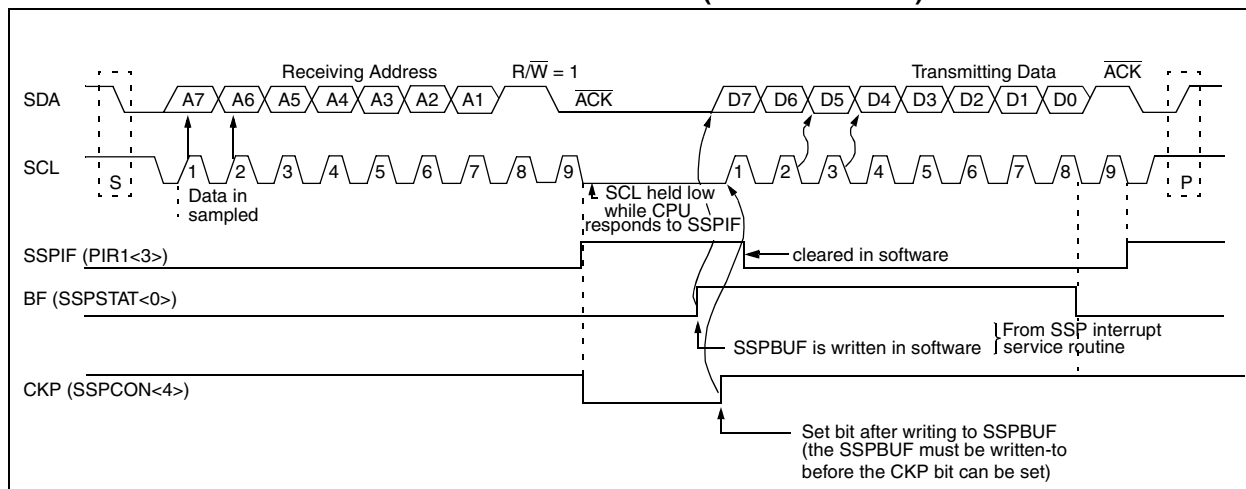
When the  $\overline{R/\overline{W}}$  bit of the incoming address byte is set and an address match occurs, the  $\overline{R/\overline{W}}$  bit of the SSPSTAT register is set. The received address is loaded into the SSPBUF register. The  $\overline{ACK}$  pulse will be sent on the ninth bit and the CKP will be cleared by hardware, holding SCL low. Slave devices cause the master to wait by holding the SCL line low. The transmit data is loaded into the SSPBUF register, which in turn loads the SSPSR register. When bit CKP (SSP-CON<4>) is set, pin RC3/SCK/SCL releases SCL. When the SCL line goes high, the master may resume operating the SCL line and receiving data. The master must monitor the SCL pin prior to asserting another clock pulse. The slave devices may be holding off the master by stretching the clock. The eight data bits are

shifted out on the falling edge of the SCL input. This ensures that the SDA signal is valid during the SCL high time (Figure 8-4).

An SSP interrupt is generated for each data transfer byte. Flag bit SSPIF must be cleared in software, and the SSPSTAT register used to determine the status of the byte. Flag bit SSPIF is set on the falling edge of the ninth clock pulse.

As a slave-transmitter, the  $\overline{ACK}$  pulse from the master-receiver is latched on the rising edge of the ninth SCL input pulse. If the SDA line was high (not  $\overline{ACK}$ ), then the data transfer is complete. When the  $\overline{ACK}$  is latched by the slave, the slave logic is reset (resets SSPSTAT register) and the slave then monitors for another occurrence of the START bit. If the SDA line was low ( $\overline{ACK}$ ), the transmit data must be loaded into the SSPBUF register, which also loads the SSPSR register. Then pin RC3/SCK/SCL should be enabled by setting bit CKP.

**FIGURE 8-4: I<sup>2</sup>C WAVEFORMS FOR TRANSMISSION (7-BIT ADDRESS)**





## 8.3.2 MASTER OPERATION

Master operation is supported in firmware using interrupt generation on the detection of the START and STOP conditions. The STOP (P) and START (S) bits are cleared by a reset or when the SSP module is disabled. The STOP (P) and START (S) bits will toggle based on the START and STOP conditions. Control of the I<sup>2</sup>C bus may be taken when the P bit is set, or the bus is idle and both the S and P bits are clear.

In master operation, the SCL and SDA lines are manipulated in software by clearing the corresponding TRISC<4:3> bit(s). The output level is always low, irrespective of the value(s) in PORTC<4:3>. So when transmitting data, a '1' data bit must have the TRISC<4> bit set (input) and a '0' data bit must have the TRISC<4> bit cleared (output). The same scenario is true for the SCL line with the TRISC<3> bit.

The following events will cause SSP Interrupt Flag bit, SSPIF, to be set (SSP Interrupt if enabled):

- START condition
- STOP condition
- Byte transfer completed

Master operation can be done with either the slave mode idle (SSPM3:SSPM0 = 1011) or with the slave active. When both master operation and slave modes are used, the software needs to differentiate the source(s) of the interrupt.

For more information on master operation, see AN554 - *Software Implementation of I<sup>2</sup>C Bus Master*.

## 8.3.3 MULTI-MASTER OPERATION

In multi-master operation, the interrupt generation on the detection of the START and STOP conditions allows the determination of when the bus is free. The STOP (P) and START (S) bits are cleared from a reset or when the SSP module is disabled. The STOP (P) and START (S) bits will toggle based on the START and STOP conditions. Control of the I<sup>2</sup>C bus may be taken when bit P (SSPSTAT<4>) is set, or the bus is idle and both the S and P bits clear. When the bus is busy, enabling the SSP Interrupt will generate the interrupt when the STOP condition occurs.

In multi-master operation, the SDA line must be monitored to see if the signal level is the expected output level. This check only needs to be done when a high level is output. If a high level is expected and a low level is present, the device needs to release the SDA and SCL lines (set TRISC<4:3>). There are two stages where this arbitration can be lost, these are:

- Address Transfer
- Data Transfer

When the slave logic is enabled, the slave continues to receive. If arbitration was lost during the address transfer stage, communication to the device may be in progress. If addressed, an ACK pulse will be generated. If arbitration was lost during the data transfer stage, the device will need to re-transfer the data at a later time.

For more information on master operation, see AN578 - *Use of the SSP Module in the of I<sup>2</sup>C Multi-Master Environment*.

**TABLE 8-3 REGISTERS ASSOCIATED WITH I<sup>2</sup>C OPERATION**

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other resets
0Bh, 8Bh	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000u
0Ch	PIR1	—	ADIF	—	—	SSPIF	CCP1IF	TMR2IF	TMR1IF	-0-- 0000	-0-- 0000
8Ch	PIE1	—	ADIE	—	—	SSPIE	CCP1IE	TMR2IE	TMR1IE	-0-- 0000	-0-- 0000
13h	SSPBUF	Synchronous Serial Port Receive Buffer/Transmit Register								xxxx xxxx	uuuu uuuu
93h	SSPADD	Synchronous Serial Port (I <sup>2</sup> C mode) Address Register								0000 0000	0000 0000
14h	SSPCON	WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0	0000 0000	0000 0000
94h	SSPSTAT	SMP <sup>(1)</sup>	CKE <sup>(1)</sup>	D/ $\bar{A}$	P	S	R/ $\bar{W}$	UA	BF	0000 0000	0000 0000
87h	TRISC	PORTC Data Direction register								1111 1111	1111 1111

Legend: x = unknown, u = unchanged, - = unimplemented locations read as '0'.  
Shaded cells are not used by SSP module in SPI mode.

**Note 1:** Maintain these bits clear in I<sup>2</sup>C mode.

## REGISTER 8-1: SSPSTAT: SYNC SERIAL PORT STATUS REGISTER (ADDRESS 94h)

R/W-0	R/W-0	R-0	R-0	R-0	R-0	R-0	R-0
SMP	CKE	D/A	P	S	R/W	UA	BF

bit7

bit0

R = Readable bit  
W = Writable bit  
U = Unimplemented bit, read as '0'  
- n = Value at POR reset

bit 7: **SMP**: SPI data input sample phase

SPI Master Operation

1 = Input data sampled at end of data output time

0 = Input data sampled at middle of data output time

SPI Slave Mode

SMP must be cleared when SPI is used in slave mode

I<sup>2</sup>C Mode

This bit must be maintained clear

bit 6: **CKE**: SPI Clock Edge Select

SPI Mode

CKP = 0

1 = Data transmitted on rising edge of SCK

0 = Data transmitted on falling edge of SCK

CKP = 1

1 = Data transmitted on falling edge of SCK

0 = Data transmitted on rising edge of SCK

I<sup>2</sup>C Mode

This bit must be maintained clear

bit 5: **D/A**: Data/Address bit (I<sup>2</sup>C mode only)

1 = Indicates that the last byte received or transmitted was data

0 = Indicates that the last byte received or transmitted was address

bit 4: **P**: Stop bit (I<sup>2</sup>C mode only. This bit is cleared when the SSP module is disabled, or when the Start bit is detected last, SSPEN is cleared)

1 = Indicates that a stop bit has been detected last (this bit is '0' on RESET)

0 = Stop bit was not detected last

bit 3: **S**: Start bit (I<sup>2</sup>C mode only. This bit is cleared when the SSP module is disabled, or when the Stop bit is detected last, SSPEN is cleared)

1 = Indicates that a start bit has been detected last (this bit is '0' on RESET)

0 = Start bit was not detected last

bit 2: **R/W**: Read/Write bit information (I<sup>2</sup>C mode only)

This bit holds the R/W bit information following the last address match. This bit is only valid from the address match to the next start bit, stop bit, or ACK bit.

1 = Read

0 = Write

bit 1: **UA**: Update Address (10-bit I<sup>2</sup>C mode only)

1 = Indicates that the user needs to update the address in the SSPADD register

0 = Address does not need to be updated

bit 0: **BF**: Buffer Full Status bit

Receive (SPI and I<sup>2</sup>C modes)

1 = Receive complete, SSPBUF is full

0 = Receive not complete, SSPBUF is empty

Transmit (I<sup>2</sup>C mode only)

1 = Transmit in progress, SSPBUF is full

0 = Transmit complete, SSPBUF is empty

## 9.0 ANALOG-TO-DIGITAL CONVERTER (A/D) MODULE

**Note:** This section applies to the PIC16C72A only.

The analog-to-digital (A/D) converter module has five input channels.

The A/D allows conversion of an analog input signal to a corresponding 8-bit digital number (refer to Application Note AN546 for use of A/D Converter). The output of the sample and hold is the input into the converter, which generates the result via successive approximation. The analog reference voltage is software selectable to either the device's positive supply voltage (VDD) or the voltage level on the RA3/AN3/VREF pin.

The A/D converter has the feature of being able to operate while the device is in SLEEP mode. To operate in sleep, the A/D conversion clock must be derived from the A/D's internal RC oscillator.

Additional information on the A/D module is available in the PIC® MCU Mid-Range Reference Manual, (DS33023).

The A/D module has three registers. These registers are:

- A/D Result Register (ADRES)
- A/D Control Register 0 (ADCON0)
- A/D Control Register 1 (ADCON1)

A device reset forces all registers to their reset state. This forces the A/D module to be turned off, and any conversion is aborted.

The ADCON0 register, shown in Figure 9-1, controls the operation of the A/D module. The ADCON1 register, shown in Figure 9-2, configures the functions of the port pins. The port pins can be configured as analog inputs (RA3 can also be a voltage reference) or as digital I/O.

### REGISTER 9-1: ADCON0 REGISTER (ADDRESS 1Fh)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0
ADCS1	ADCS0	CHS2	CHS1	CHS0	GO/DONE	—	ADON
bit7							bit0

R = Readable bit  
W = Writable bit  
U = Unimplemented bit, read as '0'  
- n = Value at POR reset

bit 7-6: **ADCS1:ADCS0:** A/D Conversion Clock Select bits  
00 = Fosc/2  
01 = Fosc/8  
10 = Fosc/32  
11 = FRC (clock derived from an internal RC oscillator)

bit 5-3: **CHS2:CHS0:** Analog Channel Select bits  
000 = channel 0, (RA0/AN0)  
001 = channel 1, (RA1/AN1)  
010 = channel 2, (RA2/AN2)  
011 = channel 3, (RA3/AN3)  
100 = channel 4, (RA5/AN4)

bit 2: **GO/DONE:** A/D Conversion Status bit  
If ADON = 1  
1 = A/D conversion in progress (setting this bit starts the A/D conversion)  
0 = A/D conversion not in progress (This bit is automatically cleared by hardware when the A/D conversion is complete)

bit 1: **Unimplemented:** Read as '0'

bit 0: **ADON:** A/D On bit  
1 = A/D converter module is operating  
0 = A/D converter module is shutoff and consumes no operating current

# PIC16C62B/72A

## REGISTER 9-2:ADCON1 REGISTER (ADDRESS 9Fh)

U-0

U-0

U-0

U-0

U-0

R/W-0

R/W-0

R/W-0

—	—	—	—	—	PCFG2	PCFG1	PCFG0
---	---	---	---	---	-------	-------	-------

bit7

bit0

R = Readable bit  
W = Writable bit  
U = Unimplemented bit,  
read as '0'  
- n = Value at POR  
reset

bit 7-3: **Unimplemented:** Read as '0'

bit 2-0: **PCFG2:PCFG0:** A/D Port Configuration Control bits

PCFG2:PCFG0	RA0	RA1	RA2	RA5	RA3	VREF
000	A	A	A	A	A	VDD
001	A	A	A	A	VREF	RA3
010	A	A	A	A	A	VDD
011	A	A	A	A	VREF	RA3
100	A	A	D	D	A	VDD
101	A	A	D	D	VREF	RA3
11x	D	D	D	D	D	VDD

A = Analog input

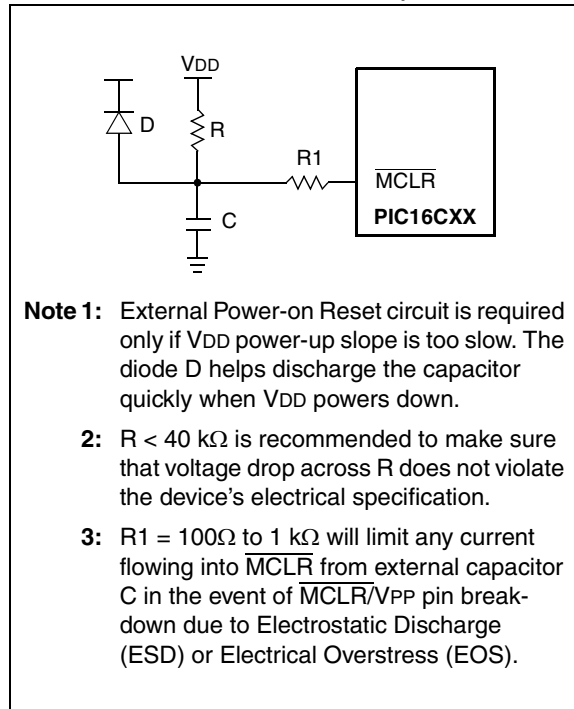
D = Digital I/O

## 10.4 Power-On Reset (POR)

A Power-on Reset pulse is generated on-chip when VDD rise is detected (in the range of 1.5V - 2.1V). To take advantage of the POR, just tie the  $\overline{\text{MCLR}}$  pin directly (or through a resistor) to VDD. This will eliminate external RC components usually needed to create a Power-on Reset. A maximum rise time for VDD is specified (SVDD, parameter D004). For a slow rise time, see Figure 10-6.

When the device starts normal operation (exits the reset condition), device operating parameters (voltage, frequency, temperature,...) must be met to ensure operation. If these conditions are not met, the device must be held in reset until the operating conditions are met. Brown-out Reset may be used to meet the start-up conditions.

**FIGURE 10-6: EXTERNAL POWER-ON RESET CIRCUIT (FOR SLOW VDD POWER-UP)**



## 10.5 Power-up Timer (PWRT)

The Power-up Timer provides a fixed nominal time-out (TPWRT, parameter #33) from the POR. The Power-up Timer operates on an internal RC oscillator. The chip is kept in reset as long as the PWRT is active. The PWRT's time delay allows VDD to rise to an acceptable level. A configuration bit is provided to enable/disable the PWRT.

The power-up time delay will vary from chip-to-chip due to VDD, temperature and process variation. See DC parameters for details.

## 10.6 Oscillator Start-up Timer (OST)

The Oscillator Start-up Timer (OST) provides a delay of 1024 oscillator cycles (from OSC1 input) after the PWRT delay is over (TOST, parameter #32). This ensures that the crystal oscillator or resonator has started and stabilized.

The OST time-out is invoked only for XT, LP and HS modes and only on Power-on Reset or wake-up from SLEEP.

**Note:** The OST delay may not occur when the device wakes from SLEEP.

## 10.7 Brown-Out Reset (BOR)

The configuration bit, BODEN, can enable or disable the Brown-Out Reset circuit. If VPP falls below Vbor (parameter #35, about 100 $\mu$ S), the brown-out situation will reset the device. If VDD falls below VBOR for less than TBOR, a reset may not occur.

Once the brown-out occurs, the device will remain in brown-out reset until VDD rises above VBOR. The power-up timer then keeps the device in reset for TPWRT (parameter #33, about 72mS). If VDD should fall below VBOR during TPWRT, the brown-out reset process will restart when VDD rises above VBOR with the power-up timer reset. The power-up timer is always enabled when the brown-out reset circuit is enabled, regardless of the state of the  $\overline{\text{PWRT}}$  configuration bit.

**TABLE 10-6 INITIALIZATION CONDITIONS FOR ALL REGISTERS**

Register	Applicable Devices		Power-on Reset, Brown-out Reset	MCLR Resets WDT Reset	Wake-up via WDT or Interrupt
W	62B	72A	xxxx xxxx	uuuu uuuu	uuuu uuuu
INDF	62B	72A	N/A	N/A	N/A
TMR0	62B	72A	xxxx xxxx	uuuu uuuu	uuuu uuuu
PCL	62B	72A	0000h	0000h	PC + 1 <sup>(2)</sup>
STATUS	62B	72A	0001 1xxx	000q quuu <sup>(3)</sup>	uuuq quuu <sup>(3)</sup>
FSR	62B	72A	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORTA <sup>(4)</sup>	62B	72A	--0x 0000	--0u 0000	--uu uuuu
PORTB <sup>(5)</sup>	62B	72A	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORTC <sup>(5)</sup>	62B	72A	xxxx xxxx	uuuu uuuu	uuuu uuuu
PCLATH	62B	72A	---0 0000	---0 0000	---u uuuu
INTCON	62B	72A	0000 000x	0000 000u	uuuu uuuu <sup>(1)</sup>
PIR1	62B	72A	---- 0000	---- 0000	---- uuuu <sup>(1)</sup>
	62B	72A	-0-- 0000	-0-- 0000	-u-- uuuu <sup>(1)</sup>
TMR1L	62B	72A	xxxx xxxx	uuuu uuuu	uuuu uuuu
TMR1H	62B	72A	xxxx xxxx	uuuu uuuu	uuuu uuuu
T1CON	62B	72A	--00 0000	--uu uuuu	--uu uuuu
TMR2	62B	72A	0000 0000	0000 0000	uuuu uuuu
T2CON	62B	72A	-000 0000	-000 0000	-uuu uuuu
SSPBUF	62B	72A	xxxx xxxx	uuuu uuuu	uuuu uuuu
SSPCON	62B	72A	0000 0000	0000 0000	uuuu uuuu
CCPR1L	62B	72A	xxxx xxxx	uuuu uuuu	uuuu uuuu
CCPR1H	62B	72A	xxxx xxxx	uuuu uuuu	uuuu uuuu
CCP1CON	62B	72A	--00 0000	--00 0000	--uu uuuu
ADRES	62B	72A	xxxx xxxx	uuuu uuuu	uuuu uuuu
ADCON0	62B	72A	0000 00-0	0000 00-0	uuuu uu-u
OPTION_REG	62B	72A	1111 1111	1111 1111	uuuu uuuu
TRISA	62B	72A	--11 1111	--11 1111	--uu uuuu
TRISB	62B	72A	1111 1111	1111 1111	uuuu uuuu
TRISC	62B	72A	1111 1111	1111 1111	uuuu uuuu
PIE1	62B	72A	---- 0000	---- 0000	---- uuuu
	62B	72A	-0-- 0000	-0-- 0000	-u-- uuuu
PCON	62B	72A	---- --0q	---- --uq	---- --uq
PR2	62B	72A	1111 1111	1111 1111	1111 1111
SSPADDD	62B	72A	0000 0000	0000 0000	uuuu uuuu
SSPSTAT	62B	72A	0000 0000	0000 0000	uuuu uuuu
ADCON1	62B	72A	---- -000	---- -000	---- -uuu

Legend: u = unchanged, x = unknown, - = unimplemented bit, read as '0', q = value depends on condition

**Note 1:** One or more bits in INTCON and/or PIR1 will be affected (to cause wake-up).

**2:** When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).

**3:** See Table 10-5 for reset value for specific condition.

**4:** On any device reset, these pins are configured as inputs.

**5:** This is the value that will be in the port output latch.

<b>BTFSS</b>	<b>Bit Test f, Skip if Set</b>
Syntax:	<code>[label] BTFSS f,b</code>
Operands:	$0 \leq f \leq 127$ $0 \leq b < 7$
Operation:	skip if $(f \ll b) = 1$
Status Affected:	None
Description:	If bit 'b' in register 'f' is '0', then the next instruction is executed. If bit 'b' is '1', then the next instruction is discarded and a NOP is executed instead, making this a 2TCY instruction.

<b>CLRF</b>	<b>Clear f</b>
Syntax:	<code>[label] CLRF f</code>
Operands:	$0 \leq f \leq 127$
Operation:	$00h \rightarrow (f)$ $1 \rightarrow Z$
Status Affected:	Z
Description:	The contents of register 'f' are cleared and the Z bit is set.

<b>BTFSC</b>	<b>Bit Test, Skip if Clear</b>
Syntax:	<code>[label] BTFSC f,b</code>
Operands:	$0 \leq f \leq 127$ $0 \leq b \leq 7$
Operation:	skip if $(f \ll b) = 0$
Status Affected:	None
Description:	If bit 'b' in register 'f' is '1', then the next instruction is executed. If bit 'b' in register 'f' is '0', then the next instruction is discarded, and a NOP is executed instead, making this a 2TCY instruction.

<b>CLRW</b>	<b>Clear W</b>
Syntax:	<code>[label] CLRW</code>
Operands:	None
Operation:	$00h \rightarrow (W)$ $1 \rightarrow Z$
Status Affected:	Z
Description:	W register is cleared. Zero bit (Z) is set.

<b>CALL</b>	<b>Call Subroutine</b>
Syntax:	<code>[label] CALL k</code>
Operands:	$0 \leq k \leq 2047$
Operation:	$(PC) + 1 \rightarrow TOS$ , $k \rightarrow PC \langle 10:0 \rangle$ , $(PCLATH \langle 4:3 \rangle) \rightarrow PC \langle 12:11 \rangle$
Status Affected:	None
Description:	Call Subroutine. First, return address $(PC+1)$ is pushed onto the stack. The eleven bit immediate address is loaded into PC bits $\langle 10:0 \rangle$ . The upper bits of the PC are loaded from PCLATH. CALL is a two cycle instruction.

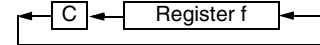
<b>CLRWDT</b>	<b>Clear Watchdog Timer</b>
Syntax:	<code>[label] CLRWDT</code>
Operands:	None
Operation:	$00h \rightarrow WDT$ $0 \rightarrow WDT \text{ prescaler}$ , $1 \rightarrow \overline{TO}$ $1 \rightarrow \overline{PD}$
Status Affected:	$\overline{TO}$ , $\overline{PD}$
Description:	CLRWDT instruction resets the Watchdog Timer. It also resets the prescaler of the WDT. Status bits $\overline{TO}$ and $\overline{PD}$ are set.

## RETFIE Return from Interrupt

Syntax: [ *label* ] RETFIE  
 Operands: None  
 Operation: TOS → PC,  
 1 → GIE  
 Status Affected: None

## RLF Rotate Left f through Carry

Syntax: [ *label* ] RLF f,d  
 Operands:  $0 \leq f \leq 127$   
 $d \in [0,1]$   
 Operation: See description below  
 Status Affected: C  
 Description: The contents of register 'f' are rotated one bit to the left through the Carry Flag. If 'd' is 0, the result is placed in the W register. If 'd' is 1, the result is stored back in register 'f'.

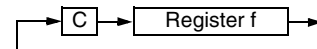


## RETLW Return with Literal in W

Syntax: [ *label* ] RETLW k  
 Operands:  $0 \leq k \leq 255$   
 Operation: k → (W);  
 TOS → PC  
 Status Affected: None  
 Description: The W register is loaded with the eight bit literal 'k'. The program counter is loaded from the top of the stack (the return address). This is a two cycle instruction.

## RRF Rotate Right f through Carry

Syntax: [ *label* ] RRF f,d  
 Operands:  $0 \leq f \leq 127$   
 $d \in [0,1]$   
 Operation: See description below  
 Status Affected: C  
 Description: The contents of register 'f' are rotated one bit to the right through the Carry Flag. If 'd' is 0, the result is placed in the W register. If 'd' is 1, the result is placed back in register 'f'.



## RETURN Return from Subroutine

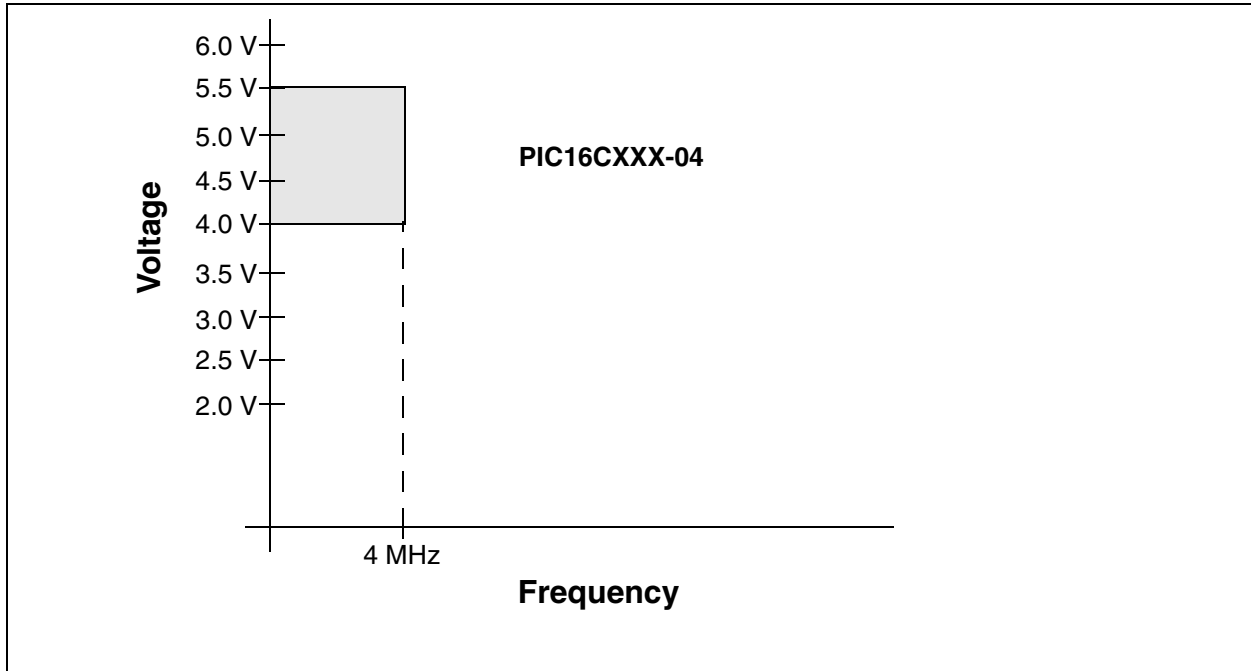
Syntax: [ *label* ] RETURN  
 Operands: None  
 Operation: TOS → PC  
 Status Affected: None  
 Description: Return from subroutine. The stack is POPed and the top of the stack (TOS) is loaded into the program counter. This is a two cycle instruction.

## SLEEP

Syntax: [ *label* ] SLEEP  
 Operands: None  
 Operation: 00h → WDT,  
 0 → WDT prescaler,  
 1 →  $\overline{TO}$ ,  
 0 →  $\overline{PD}$   
 Status Affected:  $\overline{TO}$ ,  $\overline{PD}$   
 Description: The power-down status bit,  $\overline{PD}$  is cleared. Time-out status bit,  $\overline{TO}$  is set. Watchdog Timer and its prescaler are cleared. The processor is put into SLEEP mode with the oscillator stopped. See Section 10.13 for more details.



**FIGURE 13-3: PIC16C62B/72A-04 VOLTAGE-FREQUENCY GRAPH**



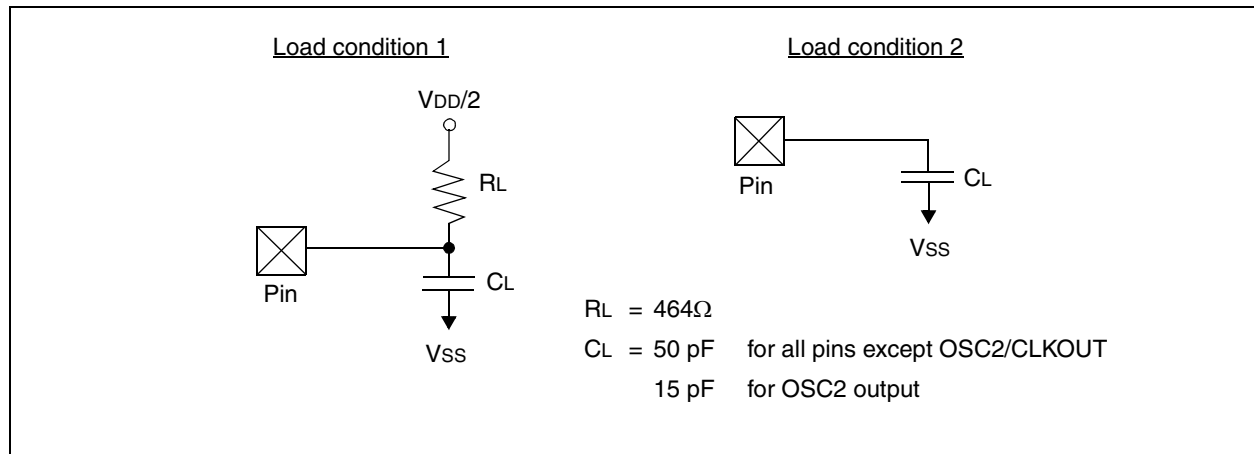
## 13.4.2 TIMING CONDITIONS

The temperature and voltages specified in Table 13-1 apply to all timing specifications unless otherwise noted. Figure 13-4 specifies the load conditions for the timing specifications.

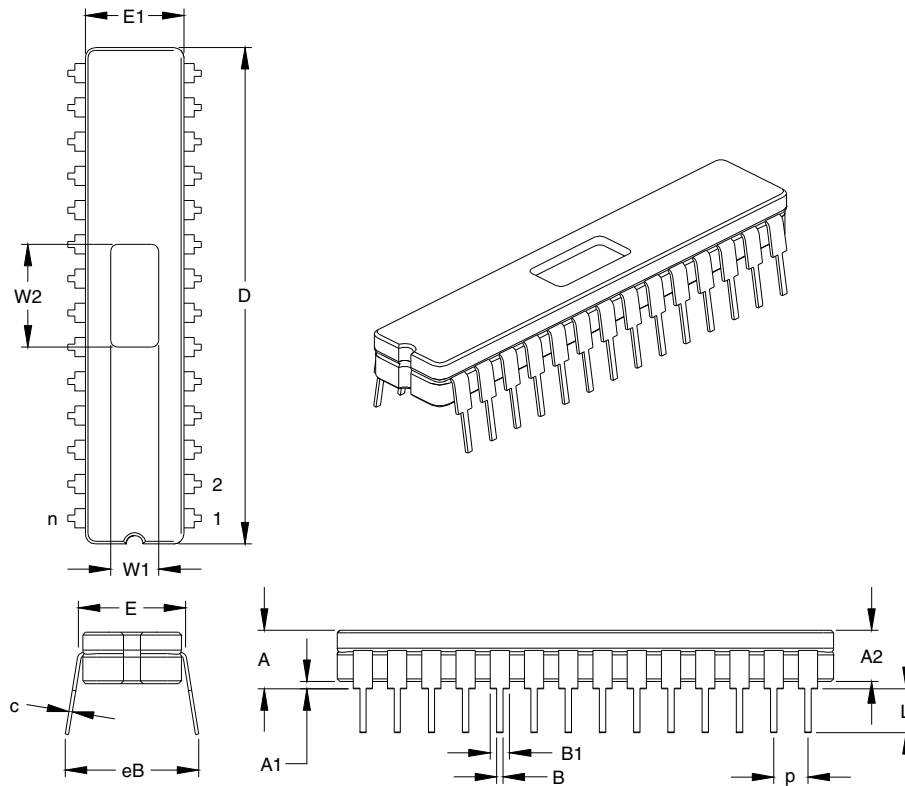
**TABLE 13-1: TEMPERATURE AND VOLTAGE SPECIFICATIONS - AC**

AC CHARACTERISTICS	Standard Operating Conditions (unless otherwise stated)
Operating temperature	$0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ for commercial $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for extended
Operating voltage $V_{DD}$	range as described in DC spec Section 13.1 and Section 13.2.
	LC parts operate for commercial/industrial temp's only.

**FIGURE 13-4: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS**



## 15.3 28-Lead Ceramic Dual In-line with Window (JW) – 300 mil (CERDIP)



Dimension	Units	INCHES*			MILLIMETERS		
		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		28			28	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.170	.183	.195	4.32	4.64	4.95
Ceramic Package Height	A2	.155	.160	.165	3.94	4.06	4.19
Standoff	A1	.015	.023	.030	0.38	0.57	0.76
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Ceramic Pkg. Width	E1	.285	.290	.295	7.24	7.37	7.49
Overall Length	D	1.430	1.458	1.485	36.32	37.02	37.72
Tip to Seating Plane	L	.135	.140	.145	3.43	3.56	3.68
Lead Thickness	c	.008	.010	.012	0.20	0.25	0.30
Upper Lead Width	B1	.050	.058	.065	1.27	1.46	1.65
Lower Lead Width	B	.016	.019	.021	0.41	0.47	0.53
Overall Row Spacing	eB	.345	.385	.425	8.76	9.78	10.80
Window Width	W1	.130	.140	.150	3.30	3.56	3.81
Window Length	W2	.290	.300	.310	7.37	7.62	7.87

\*Controlling Parameter  
JEDEC Equivalent: MO-058  
Drawing No. C04-080

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