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Details

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Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	I ² C, SPI
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	22
Program Memory Size	3.5KB (2K x 14)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	- ·
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lc62bt-04-so

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NOTES:

2.2.2 SPECIAL FUNCTION REGISTERS

The Special Function Registers are registers used by the CPU and Peripheral Modules for controlling the desired operation of the device. These registers are implemented as static RAM. A list of these registers is given in Table 2-1. The Special Function Registers can be classified into two sets; core (CPU) and peripheral. Those registers associated with the core functions are described in detail in this section. Those related to the operation of the peripheral features are described in detail in the peripheral feature section.

TABLE 2-1	SPECIAL FUN	CTION REGISTER	SUMMARY

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other resets (4)			
Bank 0														
00h	INDF ⁽¹⁾	Addressing	this locatio	cal register)	0000 0000	0000 0000								
01h	TMR0	Timer0 mo	Fimer0 module's register											
02h	PCL ⁽¹⁾	Program C	0000 0000	0000 0000										
03h	STATUS ⁽¹⁾	IRP ⁽⁵⁾	0001 1xxx	000q quuu										
04h	FSR ⁽¹⁾	Indirect dat	a memory a	ddress poir	nter					xxxx xxxx	uuuu uuuu			
05h	PORTA ^(6,7)	—	—	PORTA Da	ta Latch whe	en written: P	ORTA pins w	hen read		0x 0000	0u 0000			
06h	PORTB ^(6,7)	PORTB Da	ita Latch wh	en written: F	PORTB pins	when read				xxxx xxxx	uuuu uuuu			
07h	PORTC ^(6,7)	PORTC Da	ata Latch wh	en written: I	PORTC pins	when read				xxxx xxxx	uuuu uuuu			
08h-09h	—	Unimpleme	ented							—	_			
0Ah	PCLATH ^(1,2)	—	—	_	Write Buffe	r for the uppe	er 5 bits of th	e Program (Counter	0 0000	0 0000			
0Bh	INTCON ⁽¹⁾	GIE	PEIE	TOIE	INTE	RBIE	TOIF	INTF	RBIF	0000 000x	0000 000u			
0Ch	PIR1	—	ADIF ⁽³⁾	—	—	SSPIF	CCP1IF	TMR2IF	TMR1IF	-0 0000	-0 0000			
0Dh	_	Unimpleme	ented							_	—			
0Eh	TMR1L	Holding reg	gister for the	Least Signi	ificant Byte o	of the 16-bit T	MR1 registe	r		xxxx xxxx	uuuu uuuu			
0Fh	TMR1H	Holding reg	gister for the	Most Signif	icant Byte o	f the 16-bit T	MR1 register	r		xxxx xxxx	uuuu uuuu			
10h	T1CON	—	—	T1CKPS1	T1CKPS0	T1OSCEN	T1SYNC	TMR1CS	TMR1ON	00 0000	uu uuuu			
11h	TMR2	Timer2 mo	dule's regist	er						0000 0000	0000 0000			
12h	T2CON	—	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0	-000 0000	-000 0000			
13h	SSPBUF	Synchrono	us Serial Po	rt Receive E	Buffer/Transr	nit Register				xxxx xxxx	uuuu uuuu			
14h	SSPCON	WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0	0000 0000	0000 0000			
15h	CCPR1L	Capture/Co	ompare/PWI	V Register1	(LSB)					xxxx xxxx	uuuu uuuu			
16h	CCPR1H	Capture/Compare/PWM Register1 (MSB)									uuuu uuuu			
17h	CCP1CON	—	—	CCP1X	CCP1Y	CCP1M3	CCP1M2	CCP1M1	CCP1M0	00 0000	00 0000			
18h-1Dh	—	Unimplemented									—			
1Eh	ADRES ⁽³⁾	A/D Result	Register							xxxx xxxx	uuuu uuuu			
1Fh	ADCON0 ⁽³⁾	ADCS1	ADCS0	CHS2	CHS1	CHS0	GO/DONE	—	ADON	0000 00-0	0000 00-0			

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, read as '0',

Shaded locations are unimplemented, read as '0'. **Note 1:** These registers can be addressed from either bank.

2: The upper byte of the program counter is not directly accessible. PCLATH is a holding register for PC<12:8> whose contents are transferred to the upper byte of the program counter.

- 3: A/D not implemented on the PIC16C62B, maintain as '0'.
- 4: Other (non power-up) resets include: external reset through MCLR and the Watchdog Timer Reset.
- 5: The IRP and RP1 bits are reserved. Always maintain these bits clear.
- 6: On any device reset, these pins are configured as inputs.
- 7: This is the value that will be in the port output latch.

2.2.2.2 OPTION_REG REGISTER

Г

The OPTION_REG register is a readable and writable register, which contains various control bits to configure the TMR0 prescaler/WDT postscaler (single assignable register known as the prescaler), the External INT Interrupt, TMR0 and the weak pull-ups on PORTB.

Note: To achieve a 1:1 prescaler assignment for the TMR0 register, assign the prescaler to the Watchdog Timer.

REGISTER 2-2: OPTION_REG REGISTER (ADDRESS 81h)

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1							
RBPU	INTEDG	TOCS	T0SE	PSA	PS2	PS1	PS0	R = Readable bit						
bit7	1 1						bit0	W = Writable bit						
								- n = Value at POR reset						
bit 7:	RBPU: PORTB Pull-up Enable bit													
	1 = PORTB pull-ups are disabled													
	0 = PORTB pull-ups are enabled for all PORTB inputs													
bit 6 [.]	INTEDG: Interrupt Edge Select bit													
Dit 0.	IN I EDG: Interrupt Edge Select bit 1 = Interrupt on rising edge of BB0/INT pin													
	1 = Interrupt on rising edge of RB0/INT pin 0 = Interrupt on falling edge of RB0/INT pin													
bit E.	TOCE		Source S	alaat hit	r									
DIL 5.	1 – Transit	ion on R		nin										
	1 - Internet	linetruct	ion cycle /	pin Nock (CLk										
					001)									
bit 4:	TOSE: IMI	R0 Sourc	e Edge Se	elect bit										
	1 = Increm	ient on hi	gh-to-low	transition	on RA4/100	JKI pin								
	0 = Increm	ient on lo	w-to-nign	transition	on RA4/100	JKI pin								
bit 3:	PSA: Pres	caler Ass	signment b	oit										
	1 = Presca	aler is ass	signed to t	he WDT										
	0 = Presca	aler is ass	signed to t	he Timer0	module									
bit 2-0:	PS2:PS0 :	Prescale	r Rate Sel	ect bits										
	Bit Value	TMR0 R	ate WD	r Rate										
	000	1.2	1:	1										
	001	1:4	1:	2										
	010	1:8	1:	4										
	011	1:16	3 1:	8										
	100	1:32		10 32										
	110	1:64	+ 1: 08 1:	64										
	111	1:25	56 1:	128										

2.2.2.3 INTCON REGISTER

The INTCON Register is a readable and writable register, which contains various interrupt enable and flag bits for the TMR0 register overflow, RB Port change and External RB0/INT pin interrupts. Note: Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the global enable bit, GIE (INTCON<7>). User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

REGISTER 2-3: INTCON REGISTER (ADDRESS 0Bh, 8Bh)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-x							
GIE	PEIE	TOIE	INTE	RBIE	T0IF	INTF	RBIF	R = Readable bit						
bit7							bit0	W = Writable bit						
bit 7:	GIE: Global Interrupt Enable bit 1 = Enables all un-masked interrupts 0 = Disables all interrupts													
bit 6:	PEIE : Peripheral Interrupt Enable bit 1 = Enables all un-masked peripheral interrupts 0 = Disables all peripheral interrupts													
bit 5:	TOIE : TMR0 Overflow Interrupt Enable bit 1 = Enables the TMR0 interrupt 0 = Disables the TMR0 interrupt													
bit 4:	IINTE: RB0/INT External Interrupt Enable bit 1 = Enables the RB0/INT external interrupt 0 = Disables the RB0/INT external interrupt													
bit 3:	RBIE : RB 1 = Enabl 0 = Disab	Port Cha es the RB les the RE	nge Interr port char port cha	upt Enable ige interru nge interru	e bit pt ıpt									
bit 2:	TOIF : TMF 1 = TMRC 0 = TMRC	R0 Overflo) register h) register o	ow Interrup nas overflo did not ove	ot Flag bit owed (softw erflow	ware must o	clear bit)								
bit 1:	INTF : RB 1 = The F 0 = The F	0/INT Exte 8B0/INT ex 8B0/INT ex	ernal Inter kternal inte kternal inte	rupt Flag b errupt occu errupt did i	bit urred (softw not occur	are must c	clear bit)							
bit 0:	RBIF : RB 1 = At lea 0 = None	Port Cha st one of t of the RB	nge Intern he RB7:R 7:RB4 inp	upt Flag bi B4 input p ut pins ha	t ins have ch ve changed	anged sta state	te (clear by	reading PORTB)						

PIC16C62B/72A

2.2.2.6 PCON REGISTER

The Power Control register (PCON) contains flag bits to allow differentiation between a Power-on Reset (POR), Brown-Out Reset (BOR) and resets from other sources.

Note: On Power-on Reset, the state of the BOR bit is unknown and is not predictable. If the BODEN bit in the configuration word is set, the user must first set the BOR bit on a POR, and check it on subsequent resets. If BOR is cleared while POR remains set, a Brown-out reset has occurred. If the BODEN bit is clear, the BOR bit may be ignored.

REGISTER 2-6: PCON REGISTER (ADDRESS 8Eh)



4.0 TIMER0 MODULE

The Timer0 module timer/counter has the following features:

- 8-bit timer/counter
 - Read and write
 - INT on overflow
- 8-bit software programmable prescaler
- INT or EXT clock select
 - EXT clock edge select

Figure 4-1 is a simplified block diagram of the Timer0 module.

Additional information on timer modules is available in the PIC[®] MCU Mid-Range Reference Manual, (DS33023).

4.1 <u>Timer0 Operation</u>

Timer0 can operate as a timer or as a counter.

Timer mode is selected by clearing bit TOCS (OPTION_REG<5>). In timer mode, the Timer0 module will increment every instruction cycle (without prescaler). If the TMR0 register is written, the increment is inhibited for the following two instruction cycles. The user can work around this by writing an adjusted value to the TMR0 register.

Counter mode is selected by setting bit T0CS (OPTION_REG<5>). In counter mode, Timer0 will increment either on every rising or falling edge of pin RA4/T0CKI. The incrementing edge is determined by the Timer0 Source Edge Select bit T0SE (OPTION_REG<4>). Clearing bit T0SE selects the rising edge. Restrictions on the external clock input are discussed below.

When an external clock input is used for Timer0, it must meet certain requirements. The requirements ensure the external clock can be synchronized with the internal phase clock (Tosc). Also, there is a delay in the actual incrementing of Timer0 after synchronization. Additional information on external clock requirements is available in the Electrical Specifications section of this manual, and in the PIC[®] MCU Mid-Range Reference Manual, (DS33023).

4.2 <u>Prescaler</u>

An 8-bit counter is available as a prescaler for the Timer0 module, or as a postscaler for the Watchdog Timer, respectively (Figure 4-2). For simplicity, this counter is being referred to as "prescaler" throughout this data sheet. There is only one prescaler available which is shared between the Timer0 module and the Watchdog Timer. A prescaler assignment for the Timer0 module means that there is no prescaler for the Watchdog Timer, and vice-versa.

The prescaler is not readable or writable.

The PSA and PS2:PS0 bits (OPTION_REG<3:0>) determine the prescaler assignment and prescale ratio.

Clearing bit PSA will assign the prescaler to the Timer0 module. When the prescaler is assigned to the Timer0 module, prescale values of 1:2, 1:4, ..., 1:256 are selectable.

Setting bit PSA will assign the prescaler to the Watchdog Timer (WDT). When the prescaler is assigned to the WDT, prescale values of 1:1, 1:2, ..., 1:128 are selectable.

When assigned to the Timer0 module, all instructions writing to the TMR0 register (e.g. CLRF 1, MOVWF 1, BSF 1, x....etc.) will clear the prescaler. When assigned to WDT, a CLRWDT instruction will clear the prescaler along with the WDT.

Note: Writing to TMR0 when the prescaler is assigned to Timer0 will clear the prescaler count, but will not change the prescaler assignment or ratio.



FIGURE 4-1: TIMER0 BLOCK DIAGRAM

4.2.1 SWITCHING PRESCALER ASSIGNMENT

The prescaler assignment is fully under software control, (i.e., it can be changed "on-the-fly" during program execution).

Note: To avoid an unintended device RESET, a specific instruction sequence (shown in the PIC[®] MCU Mid-Range Reference Manual, DS33023) must be executed when changing the prescaler assignment from Timer0 to the WDT. This sequence must be followed even if the WDT is disabled.

4.3 <u>Timer0 Interrupt</u>

The TMR0 interrupt is generated when the TMR0 register overflows from FFh to 00h. This overflow sets bit T0IF (INTCON<2>). The interrupt can be masked by clearing bit T0IE (INTCON<5>). Bit T0IF must be cleared in software by the Timer0 module interrupt service routine before re-enabling this interrupt. The TMR0 interrupt cannot awaken the processor from SLEEP since the timer is shut off during SLEEP.

FIGURE 4-2: BLOCK DIAGRAM OF THE TIMER0/WDT PRESCALER



TABLE 4-1 REGISTERS ASSOCIATED WITH TIMER0

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other resets
01h	TMR0	Timer0	module's r	egister		xxxx xxxx	uuuu uuuu				
0Bh,8Bh	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000u
81h	OPTION_REG	RBPU	INTEDG	TOCS	T0SE	PSA	PS0	1111 1111	1111 1111		
85h	TRISA	_	—	PORTA	Data Di	rection R	11 1111	11 1111			

Legend: x = unknown, u = unchanged, - = unimplemented locations read as '0'. Shaded cells are not used by Timer0.

6.0 TIMER2 MODULE

The Timer2 module timer has the following features:

- 8-bit timer (TMR2 register)
- Readable and writable
- 8-bit period register (PR2)
 - Readable and writable
- Software programmable prescaler (1:1, 1:4, 1:16)
- Software programmable postscaler (1:1 to 1:16)
- Interrupt on match (TMR2 = PR2)
- Timer2 can be used by SSP and CCP

Timer2 has a control register, shown in Register 6-1. Timer2 can be shut off by clearing control bit TMR2ON (T2CON<2>) to minimize power consumption.

Figure 6-1 is a simplified block diagram of the Timer2 module.

Additional information on timer modules is available in the PIC[®] MCU Mid-Range Reference Manual, (DS33023).

FIGURE 6-1: TIMER2 BLOCK DIAGRAM



REGISTER 6-1:T2CON: TIMER2 CONTROL REGISTER (ADDRESS 12h)



6.1 <u>Timer2 Operation</u>

The Timer2 output is also used by the CCP module to generate the PWM "On-Time", and the PWM period with a match with PR2.

The TMR2 register is readable and writable, and is cleared on any device reset.

The input clock (Fosc/4) has a prescale option of 1:1, 1:4 or 1:16, selected by control bits T2CKPS1:T2CKPS0 (T2CON<1:0>).

The match output of TMR2 goes through a 4-bit postscaler (which gives a 1:1 to 1:16 scaling) to generate a TMR2 interrupt (latched in flag bit TMR2IF, (PIR1<1>)).

The prescaler and postscaler counters are cleared when any of the following occurs:

- a write to the TMR2 register
- a write to the T2CON register
- any device reset (Power-on Reset, MCLR reset, Watchdog Timer reset or Brown-out Reset)

TMR2 is not cleared when T2CON is written.

6.2 <u>Timer2 Interrupt</u>

The Timer2 module has an 8-bit period register PR2. Timer2 increments from 00h until it matches PR2 and then resets to 00h on the next increment cycle. PR2 is a readable and writable register. The PR2 register is initialized to FFh upon reset.

6.3 Output of TMR2

The output of TMR2 (before the postscaler) is fed to the Synchronous Serial Port module, which optionally uses it to generate shift clock.

TABLE 6-1 REGISTERS ASSOCIATED WITH TIMER2 AS A TIMER/COUNTER

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other resets
0Bh,8Bh	INTCON	GIE	PEIE	TOIE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000u
0Ch	PIR1	-	ADIF			SSPIF	CCP1IF	TMR2IF	TMR1IF	-00-0000	0000 0000
8Ch	PIE1	_	ADIE	_	_	SSPIE	CCP1IE	TMR2IE	TMR1IE	-0 0000	0000 0000
11h	TMR2	Timer2 mod	lule's registe	r						0000 0000	0000 0000
12h	T2CON	_	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0	-000 0000	-000 0000
92h	PR2	Timer2 Peri	od Register		1111 1111	1111 1111					

Legend: x = unknown, u = unchanged, - = unimplemented read as '0'. Shaded cells are not used by the Timer2 module.

7.3.3 SET-UP FOR PWM OPERATION

The following steps should be taken when configuring the CCP module for PWM operation:

- 1. Set the PWM period by writing to the PR2 register.
- 2. Set the PWM on-time by writing to the CCPR1L register and CCP1CON<5:4> bits.
- 3. Make the CCP1 pin an output by clearing the TRISC<2> bit.
- 4. Set the TMR2 prescale value and enable Timer2 by writing to T2CON.
- 5. Configure the CCP1 module for PWM operation.

TABLE 7-4 EXAMPLE PWM FREQUENCIES AND RESOLUTIONS AT 20 MHz

PWM Frequency	1.22 kHz	4.88 kHz	19.53 kHz	78.12 kHz	156.3 kHz	208.3 kHz
Timer Prescaler (1, 4, 16)	16	4	1	1	1	1
PR2 Value	0xFF	0xFF	0xFF	0x3F	0x1F	0x17
Maximum Resolution (bits)	10	10	10	8	7	5.5

TABLE 7-5 REGISTERS ASSOCIATED WITH PWM AND TIMER2

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other resets
0Bh,8Bh	INTCON	GIE	PEIE	TOIE	INTE	RBIE	TOIF	INTF	RBIF	0000 000x	0000 000u
0Ch	PIR1	—	ADIF	_	—	SSPIF	CCP1IF	TMR2IF	TMR1IF	-0 0000	-0 0000
8Ch	PIE1	—	ADIE	—	—	SSPIE	CCP1IE	TMR2IE	TMR1IE	-0 0000	-0 0000
87h	TRISC	PORTC D	ata Directio	on Register	r					1111 1111	1111 1111
11h	TMR2	Timer2 mo	odule's regis	ter						0000 0000	0000 0000
92h	PR2	Timer2 mo	odule's perio	d register						1111 1111	1111 1111
12h	T2CON	—	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0	-000 0000	-000 0000
15h	CCPR1L	Capture/C	ompare/PW		xxxx xxxx	uuuu uuuu					
16h	CCPR1H	Capture/C	ompare/PW		xxxx xxxx	uuuu uuuu					
17h	CCP1CON	_		CCP1X	CCP1Y	CCP1M3	CCP1M2	CCP1M1	CCP1M0	00 0000	00 0000

Legend: x = unknown, u = unchanged, - = unimplemented read as '0'. Shaded cells are not used by PWM and Timer2.

9.4 <u>A/D Conversions</u>

Note:	The GO/DONE bit should NOT be set in
	the same instruction that turns on the A/D.

9.5 Use of the CCP Trigger

An A/D conversion can be started by the "special event trigger" of the CCP1 module. This requires that the CCP1M3:CCP1M0 bits (CCP1CON<3:0>) be programmed as 1011 and that the A/D module be enabled (ADON bit is set). When the trigger occurs, the

TABLE 9-2 SUMMARY OF A/D REGISTERS

GO/DONE bit will be set, starting the A/D conversion, and the Timer1 counter will be reset to zero. Timer1 is reset to automatically repeat the A/D acquisition period with minimal software overhead. The appropriate analog input channel must be selected and the minimum acquisition time must pass before the "special event trigger" sets the GO/DONE bit (starts a conversion).

If the A/D module is not enabled (ADON is cleared), then the "special event trigger" will be ignored by the A/D module, but will still reset the Timer1 counter.

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
0Bh,8Bh	INTCON	GIE	PEIE	TOIE	INTE	RBIE	TOIF	INTF	RBIF	0000 000x	0000 000u
0Ch	PIR1	_	ADIF	—	_	SSPIF	CCP1IF	TMR2IF	TMR1IF	-0 0000	-0 0000
8Ch	PIE1	_	ADIE	—	—	SSPIE	CCP1IE	TMR2IE	TMR1IE	-0 0000	-0 0000
1Eh	ADRES	A/D Res	ult Regist	ter						XXXX XXXX	uuuu uuuu
1Fh	ADCON0	ADCS1	ADCS0	CHS2	CHS1	CHS0	GO/DONE	—	ADON	0000 00-0	0000 00-0
9Fh	ADCON1	_	—	—	-	—	PCFG2	PCFG1	PCFG0	000	000
05h	PORTA	_	—	RA5	RA4	RA3	RA2	RA1	RA0	0x 0000	0u 0000
85h	TRISA	_	_	PORTA [Data Direct	11 1111	11 1111				

Legend: x = unknown, u = unchanged, - = unimplemented read as '0'. Shaded cells are not used for A/D conversion.

10.10 Interrupts

The interrupt control register (INTCON) records individual interrupt requests in flag bits. It also has individual and global interrupt enable bits.

Note:	Individual interrupt flag bits are set regard-
	less of the status of their corresponding
	mask bit or the GIE bit.

A global interrupt enable bit, GIE (INTCON<7>) enables or disables all interrupts. When bit GIE is enabled, and an interrupt's flag bit and mask bit are set, the interrupt will vector immediately. Individual interrupts can be disabled through their corresponding enable bits in various registers. Individual interrupt flag bits are set regardless of the status of the GIE bit. The GIE bit is cleared on reset.

The "return from interrupt" instruction, RETFIE, exits the interrupt routine and sets the GIE bit, which reenables interrupts.

The RB0/INT pin interrupt, the RB port change interrupt and the TMR0 overflow interrupt flags are contained in the INTCON register. The peripheral interrupt flags are contained in the special function registers PIR1 and PIR2. The corresponding interrupt enable bits are contained in special function registers PIE1 and PIE2, and the peripheral interrupt enable bit is contained in special function register INTCON.

When an interrupt is responded to, the GIE bit is cleared to disable any further interrupts, the return address is pushed onto the stack and the PC is loaded with 0004h. Once in the interrupt service routine, the source of the interrupt can be determined by polling the interrupt flag bits. The interrupt flag bit must be cleared in software before re-enabling interrupts to avoid recursive interrupts.

For external interrupt events, such as the INT pin or PORTB change interrupt, the interrupt latency will be three or four instruction cycles, depending on when the interrupt event occurs. The latency is the same for one or two cycle instructions. Individual interrupt flag bits are set regardless of the status of their corresponding mask bit or the GIE bit



FIGURE 10-7: INTERRUPT LOGIC

10.10.1 INT INTERRUPT

The external interrupt on RB0/INT pin is edge triggered: either rising, if bit INTEDG (OPTION_REG<6>) is set, or falling, if the INTEDG bit is clear. When a valid edge appears on the RB0/INT pin, flag bit INTF (INTCON<1>) is set. This interrupt can be disabled by clearing enable bit INTE (INTCON<4>). Flag bit INTF must be cleared in software in the interrupt service routine before re-enabling this interrupt. The INT interrupt can wake-up the processor from SLEEP, if bit INTE was set prior to going into SLEEP. The status of global interrupt enable bit GIE decides whether or not the processor branches to the interrupt vector following wake-up. See Section 10.13 for details on SLEEP mode.

10.10.2 TMR0 INTERRUPT

An overflow (FFh \rightarrow 00h) in the TMR0 register will set flag bit T0IF (INTCON<2>). The interrupt can be enabled/disabled by setting/clearing enable bit T0IE (INTCON<5>). (Section 4.0)

10.10.3 PORTB INTCON CHANGE

An input change on PORTB<7:4> sets flag bit RBIF (INTCON<0>). The interrupt can be enabled/disabled by setting/clearing enable bit RBIE (INTCON<4>). (Section 3.2)

10.11 Context Saving During Interrupts

During an interrupt, only the return PC value is saved on the stack. Typically, users may wish to save key registers during an interrupt, (i.e., W register and STATUS register). This will have to be implemented in software.

Example 10-1 stores and restores the W and STATUS registers. The register, W_TEMP, must be defined in each bank and must be defined at the same offset from the bank base address (i.e., if W_TEMP is defined at 0x20 in bank 0, it must also be defined at 0xA0 in bank 1).

The example:

- a) Stores the W register.
- b) Stores the STATUS register in bank 0.
- c) Stores the PCLATH register.
- d) Executes the interrupt service routine code (User-generated).
- e) Restores the STATUS register (and bank select bit).
- f) Restores the W and PCLATH registers.

EXAMPLE 10-1: SAVING STATUS, W, AND PCLATH REGISTERS IN RAM

MOVWF	W_TEMP	;Copy W to TEMP register, could be bank one or zero
SWAPF	STATUS,W	;Swap status to be saved into W
CLRF	STATUS	;bank 0, regardless of current bank, Clears IRP,RP1,RP0
MOVWF	STATUS_TEMP	;Save status to bank zero STATUS_TEMP register
:		
:(ISR)		
:		
SWAPF	STATUS_TEMP,W	;Swap STATUS_TEMP register into W
		;(sets bank to original state)
MOVWF	STATUS	;Move W into STATUS register
SWAPF	W_TEMP,F	;Swap W_TEMP
SWAPF	W_TEMP,W	;Swap W_TEMP into W

stand-alone mode the PRO MATE II can read, verify or program PIC devices. It can also set code-protect bits in this mode.

12.11 <u>PICSTART Plus Entry Level</u> <u>Development System</u>

The PICSTART programmer is an easy-to-use, lowcost prototype programmer. It connects to the PC via one of the COM (RS-232) ports. MPLAB Integrated Development Environment software makes using the programmer simple and efficient.

PICSTART Plus supports all PIC devices with up to 40 pins. Larger pin count devices such as the PIC16C92X, and PIC17C76X may be supported with an adapter socket. PICSTART Plus is CE compliant.

12.12 <u>SIMICE Entry-Level</u> <u>Hardware Simulator</u>

SIMICE is an entry-level hardware development system designed to operate in a PC-based environment with Microchip's simulator MPLAB-SIM. Both SIMICE and MPLAB-SIM run under Microchip Technology's MPLAB Integrated Development Environment (IDE) software. Specifically, SIMICE provides hardware simulation for Microchip's PIC12C5XX, PIC12CE5XX, and PIC16C5X families of PIC 8-bit microcontrollers. SIM-ICE works in conjunction with MPLAB-SIM to provide non-real-time I/O port emulation. SIMICE enables a developer to run simulator code for driving the target system. In addition, the target system can provide input to the simulator code. This capability allows for simple and interactive debugging without having to manually generate MPLAB-SIM stimulus files. SIMICE is a valuable debugging tool for entry-level system development.

12.13 <u>PICDEM-1 Low-Cost PIC MCU</u> <u>Demonstration Board</u>

The PICDEM-1 is a simple board which demonstrates the capabilities of several of Microchip's microcontrollers. The microcontrollers supported are: PIC16C5X (PIC16C54 to PIC16C58A), PIC16C61, PIC16C62X, PIC16C71, PIC16C8X, PIC17C42, PIC17C43 and PIC17C44. All necessary hardware and software is included to run basic demo programs. The users can program the sample microcontrollers provided with the PICDEM-1 board, on a PRO MATE II or PICSTART-Plus programmer, and easily test firmware. The user can also connect the PICDEM-1 board to the MPLAB-ICE emulator and download the firmware to the emulator for testing. Additional prototype area is available for the user to build some additional hardware and connect it to the microcontroller socket(s). Some of the features include an RS-232 interface, a potentiometer for simulated analog input, push-button switches and eight LEDs connected to PORTB.

12.14 PICDEM-2 Low-Cost PIC16CXX Demonstration Board

The PICDEM-2 is a simple demonstration board that supports the PIC16C62, PIC16C64, PIC16C65, PIC16C73 and PIC16C74 microcontrollers. All the necessary hardware and software is included to run the basic demonstration programs. The user can program the sample microcontrollers provided with the PICDEM-2 board, on a PRO MATE II programmer or PICSTART-Plus, and easily test firmware. The MPLAB-ICE emulator may also be used with the PICDEM-2 board to test firmware. Additional prototype area has been provided to the user for adding additional hardware and connecting it to the microcontroller socket(s). Some of the features include a RS-232 interface, push-button switches, a potentiometer for simulated analog input, a Serial EEPROM to demonstrate usage of the I²C bus and separate headers for connection to an LCD module and a keypad.

12.15 <u>PICDEM-3 Low-Cost PIC16CXXX</u> <u>Demonstration Board</u>

The PICDEM-3 is a simple demonstration board that supports the PIC16C923 and PIC16C924 in the PLCC package. It will also support future 44-pin PLCC microcontrollers with a LCD Module. All the necessary hardware and software is included to run the basic demonstration programs. The user can program the sample microcontrollers provided with the PICDEM-3 board, on a PRO MATE II programmer or PICSTART Plus with an adapter socket, and easily test firmware. The MPLAB-ICE emulator may also be used with the PICDEM-3 board to test firmware. Additional prototype area has been provided to the user for adding hardware and connecting it to the microcontroller socket(s). Some of the features include an RS-232 interface, push-button switches, a potentiometer for simulated analog input, a thermistor and separate headers for connection to an external LCD module and a keypad. Also provided on the PICDEM-3 board is an LCD panel, with 4 commons and 12 segments, that is capable of displaying time, temperature and day of the week. The PICDEM-3 provides an additional RS-232 interface and Windows 3.1 software for showing the demultiplexed LCD signals on a PC. A simple serial interface allows the user to construct a hardware demultiplexer for the LCD signals.

12.16 PICDEM-17

The PICDEM-17 is an evaluation board that demonstrates the capabilities of several Microchip microcontrollers, including PIC17C752, PIC17C756, PIC17C762, and PIC17C766. All necessary hardware is included to run basic demo programs, which are supplied on a 3.5-inch disk. A programmed sample is included, and the user may erase it and program it with the other sample programs using the PRO MATE II or PICSTART Plus device programmers and easily debug

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and test the sample code. In addition, PICDEM-17 supports down-loading of programs to and executing out of external FLASH memory on board. The PICDEM-17 is also usable with the MPLAB-ICE or PICMASTER emulator, and all of the sample programs can be run and modified using either emulator. Additionally, a generous prototype area is available for user hardware.

12.17 <u>SEEVAL Evaluation and Programming</u> <u>System</u>

The SEEVAL SEEPROM Designer's Kit supports all Microchip 2-wire and 3-wire Serial EEPROMs. The kit includes everything necessary to read, write, erase or program special features of any Microchip SEEPROM product including Smart Serials[™] and secure serials. The Total Endurance[™] Disk is included to aid in tradeoff analysis and reliability calculations. The total kit can significantly reduce time-to-market and result in an optimized system.

12.18 <u>KEELOQ Evaluation and</u> <u>Programming Tools</u>

KEELOQ evaluation and programming tools support Microchips HCS Secure Data Products. The HCS evaluation kit includes an LCD display to show changing codes, a decoder to decode transmissions, and a programming interface to program test transmitters.

13.4.2 TIMING CONDITIONS

The temperature and voltages specified in Table 13-1 apply to all timing specifications unless otherwise noted. Figure 13-4 specifies the load conditions for the timing specifications.

TABLE 13-1: TEMPERATURE AND VOLTAGE SPECIFICATIONS - AC

AC CHARACTERISTICS	Standard Operating Conditions (unless otherwise stated)					
	Operating temperature $0^{\circ}C \leq TA \leq +70^{\circ}C$ for commercial					
	-40°C \leq TA \leq +85°C for industrial					
	-40°C \leq TA \leq +125°C for extended					
	Operating voltage VDD range as described in DC spec Section 13.1 and Section 13.2. LC parts operate for commercial/industrial temp's only.					

FIGURE 13-4: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS



FIGURE 13-12: EXAMPLE SPI MASTER MODE TIMING (CKE = 1)



TABLE 13-8: EXAMPLE SPI MODE REQUIREMENTS (MASTER MODE, CKE = 1)

Param. No.	Symbol	Characteristic		Min	Тур†	Max	Units	Conditions
71	TscH	SCK input high time	Continuous	1.25Tcy + 30	—		ns	
71A		(slave mode)	Single Byte	40	—	_	ns	Note 1
72	TscL	SCK input low time	Continuous	1.25Tcy + 30	—	-	ns	
72A		(slave mode)	Single Byte	40	—		ns	Note 1
73	TdiV2scH, TdiV2scL	Setup time of SDI data input to SCK edge		100	_	—	ns	
73A	Тв2в	Last clock edge of Byte1 to the 1st clock edge of Byte2		1.5Tcy + 40	_	—	ns	Note 1
74	TscH2diL, TscL2diL	Hold time of SDI data input to SCK edge		100	_	_	ns	
75	TdoR	SDO data output rise time	PIC16CXX	—	10	25	ns	
			PIC16LCXX		20	45	ns	
76	TdoF	SDO data output fall time		—	10	25	ns	
78	TscR	SCK output rise time (master mode)	PIC16CXX	_	10	25	ns	
			PIC16LCXX		20	45	ns	
79	TscF	SCK output fall time (master mode)		—	10	25	ns	
80	TscH2doV, TscL2doV	SDO data output valid after SCK edge	PIC16CXX	_	—	50	ns	
			PIC16LCXX		—	100	ns	
81	TdoV2scH, TdoV2scL	SDO data output setup to	SCK edge	Тсү	_	_	ns	

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Specification 73A is only required if specifications 71A and 72A are used.

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FIGURE 13-16: I²C BUS DATA TIMING



TABLE 13-12: I²C BUS DATA REQUIREMENTS

Param. No.	Sym	Characteristic		Min	Max	Units	Conditions
100*	Тнідн	Clock high time	100 kHz mode	4.0	—	μS	Device must operate at a min- imum of 1.5 MHz
			400 kHz mode	0.6	—	μS	Device must operate at a min- imum of 10 MHz
			SSP Module	1.5TCY			
101*	TLOW	Clock low time	100 kHz mode	4.7	_	μS	Device must operate at a min- imum of 1.5 MHz
			400 kHz mode	1.3		μs	Device must operate at a min- imum of 10 MHz
			SSP Module	1.5TCY			
102*	TR	SDA and SCL rise	100 kHz mode	—	1000	ns	
		time	400 kHz mode	20 + 0.1Cb	300	ns	Cb is specified to be from 10-400 pF
103*	TF	SDA and SCL fall time	100 kHz mode	—	300	ns	
			400 kHz mode	20 + 0.1Cb	300	ns	Cb is specified to be from 10-400 pF
90*	TSU:STA	START condition setup time	100 kHz mode	4.7		μs	Only relevant for repeated
			400 kHz mode	0.6	—	μs	START condition
91*	THD:STA	START condition hold	100 kHz mode	4.0		μs	After this period the first clock
		time	400 kHz mode	0.6		μs	pulse is generated
106*	Thd:dat	Data input hold time	100 kHz mode	0	—	ns	
			400 kHz mode	0	0.9	μs	
107*	TSU:DAT	Data input setup time	100 kHz mode	250	—	ns	Note 2
			400 kHz mode	100	—	ns	
92*	Tsu:sto	STOP condition setup time	100 kHz mode	4.7	—	μs	
			400 kHz mode	0.6	—	μs	
109*	ΤΑΑ	Output valid from	100 kHz mode	—	3500	ns	Note 1
		clock	400 kHz mode	—	—	ns	
110*	TBUF	Bus free time	100 kHz mode	4.7	—	μs	Time the bus must be free
			400 kHz mode	1.3	—	μS	before a new transmission can start
	Cb	Bus capacitive loading			400	pF	

* These parameters are characterized but not tested.

Note 1: As a transmitter, the device must provide this internal minimum delay time to bridge the undefined region (min. 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

2: A fast-mode (400 kHz) I²C-bus device can be used in a standard-mode (100 kHz) I²C-bus system, but the requirement Tsu:DAT ≥ 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line TR max.+tsu;DAT = 1000 + 250 = 1250 ns (according to the standard-mode I²C bus specification) before the SCL line is released.

PIC16C62B/72A PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery refer to the factory or the listed sales office.



* JW Devices are UV erasable and can be programmed to any device configuration. JW Devices meet the electrical requirement of each oscillator type (including LC devices).

Sales and Support

Data Sheets

Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office

- 2. The Microchip Corporate Literature Center U.S. FAX: (480) 786-7277
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