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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

E·XFI

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	I ² C, SPI
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	22
Program Memory Size	3.5KB (2K x 14)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	A/D 5x8b
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lc72at-04-so

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

2.0 MEMORY ORGANIZATION

There are two memory blocks in each of these microcontrollers. Each block (Program Memory and Data Memory) has its own bus, so that concurrent access can occur.

Additional information on device memory may be found in the PICmicro[™] Mid-Range Reference Manual, (DS33023).

2.1 Program Memory Organization

The PIC16C62B/72A devices have a 13-bit program counter capable of addressing an 8K x 14 program memory space. Each device has 2K x 14 words of program memory. Accessing a location above 07FFh will cause a wraparound.

The reset vector is at 0000h and the interrupt vector is at 0004h.

FIGURE 2-1: PROGRAM MEMORY MAP AND STACK



2.2.2.1 STATUS REGISTER

The STATUS register, shown in Register 2-1, contains the arithmetic status of the ALU, the RESET status and the bank select bits for data memory.

The STATUS register can be the destination for any instruction, as with any other register. If the STATUS register is the destination for an instruction that affects the Z, DC or C bits, the write to these three bits is disabled. These bits are set or cleared according to the device logic. The TO and PD bits are not writable. The result of an instruction with the STATUS register as destination may be different than intended.

For example, CLRF STATUS will clear the upper-three bits and set the Z bit. This leaves the STATUS register as 000u uluu (where u = unchanged).

It is recommended, therefore, that only BCF, BSF, SWAPF and MOVWF instructions are used to alter the STATUS register, because these instructions do not affect the Z, C or DC bits from the STATUS register. For other instructions, not affecting any status bits, see the "Instruction Set Summary."

- **Note 1:** The IRP and RP1 bits are reserved. Maintain these bits clear to ensure upward compatibility with future products.
- Note 2: The C and DC bits operate as a borrow and digit borrow bit, respectively, in subtraction. See the SUBLW and SUBWF instructions.

REGISTER 2-1: STATUS REGISTER (ADDRESS 03h, 83h)



8.0 SYNCHRONOUS SERIAL PORT (SSP) MODULE

8.1 <u>SSP Module Overview</u>

The Synchronous Serial Port (SSP) module is a serial interface useful for communicating with other peripheral or microcontroller devices. These peripheral devices may be Serial EEPROMs, shift registers, display drivers, A/D converters, etc. The SSP module can operate in one of two modes:

- Serial Peripheral Interface (SPI)
- Inter-Integrated Circuit (I²C)

For more information on SSP operation (including an I²C Overview), refer to the PIC[®] MCU Mid-Range Reference Manual, (DS33023). Also, refer to Application Note AN578, *"Use of the SSP Module in the I²C Multi-Master Environment."*

8.2 SPI Mode

This section contains register definitions and operational characteristics of the SPI module.

Additional information on SPI operation may be found in the PIC[®] MCU Mid-Range Reference Manual, (DS33023).

8.2.1 OPERATION OF SSP MODULE IN SPI MODE

A block diagram of the SSP Module in SPI Mode is shown in Figure 8-1.

The SPI mode allows 8-bits of data to be synchronously transmitted and received simultaneously. To accomplish communication, three pins are used:

- Serial Data Out (SDO)RC5/SDO
- Serial Data In (SDI)RC4/SDI/SDA
- Serial Clock (SCK)RC3/SCK/SCL

Additionally, a fourth pin may be used when in a slave mode of operation:

Slave Select (SS)RA5/SS/AN4

When initializing the SPI, several options need to be specified. This is done by programming the appropriate control bits in the SSPCON register (SSPCON<5:0>) and SSPSTAT<7:6>. These control bits allow the following to be specified:

- Master Operation (SCK is the clock output)
- Slave Mode (SCK is the clock input)
- Clock Polarity (Idle state of SCK)
- Clock Edge (Output data on rising/falling edge of SCK)
- Clock Rate (master operation only)
- Slave Select Mode (Slave mode only)

To enable the serial port, SSP Enable bit, SSPEN (SSPCON<5>) must be set. To reset or reconfigure SPI mode, clear bit SSPEN, re-initialize the SSPCON reg-

ister, and then set bit SSPEN. This configures the SDI, SDO, SCK and \overline{SS} pins as serial port pins. For the pins to behave as the serial port function, they must have their data direction bits (in the TRISC register) appropriately programmed. That is:

- SDI must have TRISC<4> set
- SDO must have TRISC<5> cleared
- SCK (master operation) must have TRISC<3> cleared
- SCK (Slave mode) must have TRISC<3> set
- SS must have TRISA<5> set (if used)

Note: When the SPI is in Slave Mode with \overline{SS} pin control enabled, (SSPCON<3:0> = 0100) the SPI module will reset if the \overline{SS} pin is set to VDD.

Note: If the SPI is used in Slave Mode with CKE = '1', then the \overline{SS} pin control must be enabled.

FIGURE 8-1: SSP BLOCK DIAGRAM (SPI MODE)



8.3.2 MASTER OPERATION

Master operation is supported in firmware using interrupt generation on the detection of the START and STOP conditions. The STOP (P) and START (S) bits are cleared by a reset or when the SSP module is disabled. The STOP (P) and START (S) bits will toggle based on the START and STOP conditions. Control of the I^2C bus may be taken when the P bit is set, or the bus is idle and both the S and P bits are clear.

In master operation, the SCL and SDA lines are manipulated in software by clearing the corresponding TRISC<4:3> bit(s). The output level is always low, irrespective of the value(s) in PORTC<4:3>. So when transmitting data, a '1' data bit must have the TRISC<4> bit set (input) and a '0' data bit must have the TRISC<4> bit cleared (output). The same scenario is true for the SCL line with the TRISC<3> bit.

The following events will cause SSP Interrupt Flag bit, SSPIF, to be set (SSP Interrupt if enabled):

- START condition
- STOP condition
- Byte transfer completed

Master operation can be done with either the slave mode idle (SSPM3:SSPM0 = 1011) or with the slave active. When both master operation and slave modes are used, the software needs to differentiate the source(s) of the interrupt.

For more information on master operation, see AN554 - Software Implementation of I^2C Bus Master.

8.3.3 MULTI-MASTER OPERATION

In multi-master operation, the interrupt generation on the detection of the START and STOP conditions allows the determination of when the bus is free. The STOP (P) and START (S) bits are cleared from a reset or when the SSP module is disabled. The STOP (P) and START (S) bits will toggle based on the START and STOP conditions. Control of the I^2C bus may be taken when bit P (SSPSTAT<4>) is set, or the bus is idle and both the S and P bits clear. When the bus is busy, enabling the SSP Interrupt will generate the interrupt when the STOP condition occurs.

In multi-master operation, the SDA line must be monitored to see if the signal level is the expected output level. This check only needs to be done when a high level is output. If a high level is expected and a low level is present, the device needs to release the SDA and SCL lines (set TRISC<4:3>). There are two stages where this arbitration can be lost, these are:

- Address Transfer
- Data Transfer

When the slave logic is enabled, the slave continues to receive. If arbitration was lost during the address transfer stage, communication to the device may be in progress. If addressed, an ACK pulse will be generated. If arbitration was lost during the data transfer stage, the device will need to re-transfer the data at a later time.

For more information on master operation, see AN578 - Use of the SSP Module in the of l^2C Multi-Master Environment.

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other resets
0Bh, 8Bh	INTCON	GIE	PEIE	TOIE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000u
0Ch	PIR1	_	ADIF	_	_	SSPIF	CCP1IF	TMR2IF	TMR1IF	-0 0000	-0 0000
8Ch	PIE1	—	ADIE	_	_	SSPIE	CCP1IE	TMR2IE	TMR1IE	-0 0000	-0 0000
13h	SSPBUF	Synchronous Serial Port Receive Buffer/Transmit Register								xxxx xxxx	uuuu uuuu
93h	SSPADD	Synchronou	Synchronous Serial Port (I ² C mode) Address Register							0000 0000	0000 0000
14h	SSPCON	WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0	0000 0000	0000 0000
94h	SSPSTAT	SMP ⁽¹⁾	CKE ⁽¹⁾	D/A	Р	S	R/W	UA	BF	0000 0000	0000 0000
87h	TRISC	PORTC Data Direction register							1111 1111	1111 1111	

TABLE 8-3REGISTERS ASSOCIATED WITH I²C OPERATION

Legend: x = unknown, u = unchanged, - = unimplemented locations read as '0'. Shaded cells are not used by SSP module in SPI mode.

Note 1: Maintain these bits clear in I^2C mode.

REGISTER 8-1: SSPSTAT: SYNC SERIAL PORT STATUS REGISTER (ADDRESS 94h)

R/W-0	R/W-0	R-0	R-0	R-0	R-0	R-0	R-0	
SMP	CKE	D/A	Р	S	R/W	UA	BF	R = Readable bit
bit7							bitO	W = Writable bit U = Unimplemented bit, read as '0' - n =Value at POR reset
bit 7:	SMP: S SPI Ma: $1 = Inpu 0 = Inpu SPI SIa SMP mi I^2 C MooThis bit$	PI data ir ster Oper ut data sa ut data sa ve Mode ust be cle de must be	nput sampl ration umpled at e umpled at r eared wher maintained	e phase and of data niddle of d n SPI is us d clear	output time ata output tin ed in slave n	me node		
bit 6:	CKE : SPI Clock Edge Select <u>SPI Mode</u> <u>CKP = 0</u> 1 = Data transmitted on rising edge of SCK 0 = Data transmitted on falling edge of SCK <u>CKP = 1</u> 1 = Data transmitted on falling edge of SCK 0 = Data transmitted on rising edge of SCK $\frac{I^2C Mode}{I}$							
bit 5:	D/A : Da 1 = Indi 0 = Indi	ata/Addre cates tha cates tha	ss bit (I ² C t the last b t the last b	mode only yte receive yte receive) ed or transm ed or transm	itted was da itted was ac	ata ddress	
bit 4:	 P: Stop bit (I²C mode only. This bit is cleared when the SSP module is disabled, or when the Start bit is detected last, SSPEN is cleared) 1 = Indicates that a stop bit has been detected last (this bit is '0' on RESET) 0 = Stop bit was not detected last 							
bit 3:	 Start bit (I²C mode only. This bit is cleared when the SSP module is disabled, or when the Stop bit is detected last, SSPEN is cleared) 1 = Indicates that a start bit has been detected last (this bit is '0' on RESET) 2 = Start bit was not detected last 							
bit 2:	R/W : Read/Write bit information (I^2C mode only) This bit holds the R/W bit information following the last address match. This bit is only valid from the address match to the next start bit, stop bit, or ACK bit. 1 = Read 0 = Write							
bit 1:	UA : Update Address (10-bit I ² C mode only) 1 = Indicates that the user needs to update the address in the SSPADD register 0 = Address does not need to be updated							
bit 0:	BF: Buf	fer Full S	tatus bit					
	$\frac{\text{Receive}}{1 = \text{Rec}}$ $0 = \text{Rec}$	e (SPI and ceive com ceive not	d I ² C mode plete, SSF complete,	es) PBUF is ful SSPBUF is	l s empty			
	1 = Transm 1 = Transm 0 = Transm	ת (ו−C mc nsmit in p nsmit con	ae only) rogress, S 1plete, SSI	SPBUF is PBUF is er	full npty			

NOTES:

9.1 A/D Acquisition Requirements

For the A/D converter to meet its specified accuracy, the charge holding capacitor (CHOLD) must be allowed to fully charge to the input channel voltage level. The analog input model is shown in Figure 9-2. The source impedance (Rs) and the internal sampling switch (Rss) impedance directly affect the time required to charge the capacitor CHOLD. The sampling switch (Rss) impedance varies over the device voltage (VDD). The source impedance affects the offset voltage at the analog input (due to pin leakage current). The maximum recommended impedance for analog sources is 10 k Ω . After the analog input channel is selected (changed), this acquisition must pass before the conversion can be started.

To calculate the minimum acquisition time, TACQ, see Equation 9-1. This equation calculates the acquisition time to within 1/2 LSb error (512 steps for the A/D). The 1/2 LSb error is the maximum error allowed for the A/D to meet its specified accuracy.

Note:	When the conversion is started, the hold-					
	ing capacitor is disconnected from the input pin.					

In general;

Assuming Rs = $10k\Omega$

Vdd =
$$3.0V$$
 (Rss = $10k\Omega$)

TACQ $\approx~13.0~\mu Sec$

By increasing VDD and reducing Rs and Temp., TACQ can be substantially reduced.



FIGURE 9-2: ANALOG INPUT MODEL

EQUATION 9-1: ACQUISITION TIME

- TACQ = Amplifier Settling Time + Hold Capacitor Charging Time + Temperature Coefficient
 - = TAMP + TC + TCOFF TAMP = $5\mu S$ TC = - (51.2pF)($1k\Omega$ + Rss + Rs) In(1/511) TCOFF = (Temp - $25^{\circ}C$)($0.05\mu S/^{\circ}C$)

9.4 <u>A/D Conversions</u>

Note:	The GO/DONE bit should NOT be set in
	the same instruction that turns on the A/D.

9.5 Use of the CCP Trigger

An A/D conversion can be started by the "special event trigger" of the CCP1 module. This requires that the CCP1M3:CCP1M0 bits (CCP1CON<3:0>) be programmed as 1011 and that the A/D module be enabled (ADON bit is set). When the trigger occurs, the

TABLE 9-2 SUMMARY OF A/D REGISTERS

GO/DONE bit will be set, starting the A/D conversion, and the Timer1 counter will be reset to zero. Timer1 is reset to automatically repeat the A/D acquisition period with minimal software overhead. The appropriate analog input channel must be selected and the minimum acquisition time must pass before the "special event trigger" sets the GO/DONE bit (starts a conversion).

If the A/D module is not enabled (ADON is cleared), then the "special event trigger" will be ignored by the A/D module, but will still reset the Timer1 counter.

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
0Bh,8Bh	INTCON	GIE	PEIE	TOIE	INTE	RBIE	TOIF	INTF	RBIF	0000 000x	0000 000u
0Ch	PIR1	_	ADIF	—	_	SSPIF	CCP1IF	TMR2IF	TMR1IF	-0 0000	-0 0000
8Ch	PIE1	_	ADIE	—	—	SSPIE	CCP1IE	TMR2IE	TMR1IE	-0 0000	-0 0000
1Eh	ADRES	A/D Res	A/D Result Register						xxxx xxxx	uuuu uuuu	
1Fh	ADCON0	ADCS1	ADCS0	CHS2	CHS1	CHS0	GO/DONE	—	ADON	0000 00-0	0000 00-0
9Fh	ADCON1	_	—	—	-	—	PCFG2	PCFG1	PCFG0	000	000
05h	PORTA	_	—	RA5	RA4	RA3	RA2	RA1	RA0	0x 0000	0u 0000
85h	TRISA	_	_	PORTA [PORTA Data Direction Register				11 1111	11 1111	

Legend: x = unknown, u = unchanged, - = unimplemented read as '0'. Shaded cells are not used for A/D conversion.



FIGURE 10-5: SIMPLIFIED BLOCK DIAGRAM OF ON-CHIP RESET CIRCUIT

10.13 Power-down Mode (SLEEP)

Power-down mode is entered by executing a $\ensuremath{\mathtt{SLEEP}}$ instruction.

If enabled, the Watchdog Timer will be cleared but keeps running, the \overline{PD} bit (STATUS<3>) is cleared, the \overline{TO} (STATUS<4>) bit is set, and the oscillator driver is turned off. The I/O ports maintain the status they had, before the SLEEP instruction was executed (driving high, low or hi-impedance).

For lowest current consumption in this mode, place all I/O pins at either VDD or VSS, ensure no external circuitry is drawing current from the I/O pin, power-down the A/D and disable external clocks. Pull all I/O pins that are hi-impedance inputs, high or low externally, to avoid switching currents caused by floating inputs. The TOCKI input should also be at VDD or VSS for lowest current consumption. The contribution from on-chip pull-ups on PORTB should be considered.

The MCLR pin must be at a logic high level (VIHMC, parameter D042).

10.13.1 WAKE-UP FROM SLEEP

The device can wake up from SLEEP through one of the following events:

- 1. External reset input on $\overline{\text{MCLR}}$ pin.
- 2. Watchdog Timer Wake-up (if WDT was enabled).
- 3. Interrupt from INT pin, RB port change, or some Peripheral Interrupts.

External $\overline{\text{MCLR}}$ Reset will cause a device reset. All other events are considered a continuation of program execution and cause a "wake-up". The $\overline{\text{TO}}$ and $\overline{\text{PD}}$ bits in the STATUS register can be used to determine the cause of device reset. The $\overline{\text{PD}}$ bit, which is set on power-up, is cleared when SLEEP is invoked. The $\overline{\text{TO}}$ bit is cleared if a WDT time-out occurred (and caused wake-up).

The following peripheral interrupts can wake the device from SLEEP:

- 1. TMR1 interrupt. Timer1 must be operating as an asynchronous counter.
- 2. CCP capture mode interrupt.
- 3. Special event trigger (Timer1 in asynchronous mode using an external clock. CCP1 is in compare mode).
- 4. SSP (Start/Stop) bit detect interrupt.
- 5. SSP transmit or receive in slave mode (SPI/I²C).
- 6. USART RX or TX (synchronous slave mode).

Other peripherals cannot generate interrupts since during SLEEP, no on-chip clocks are present.

When the SLEEP instruction is being executed, the next instruction (PC + 1) is pre-fetched. For the device to wake-up through an interrupt event, the corresponding interrupt enable bit must be set (enabled). Wake-up is

regardless of the state of the GIE bit. If the GIE bit is clear (disabled), the device resumes execution at the instruction after the SLEEP instruction. If the GIE bit is set (enabled), the device executes the instruction after the SLEEP instruction and then branches to the interrupt address (0004h). In cases where the execution of the instruction following SLEEP is not desirable, a NOP should follow the SLEEP instruction.

10.13.2 WAKE-UP USING INTERRUPTS

When global interrupts are disabled (GIE cleared) and any interrupt source has both its interrupt enable bit and interrupt flag bit set, one of the following will occur:

- If the interrupt occurs **before** the execution of a SLEEP instruction, the SLEEP instruction will complete as a NOP. Therefore, the WDT and WDT postscaler will not be cleared, the TO bit will not be set and PD bits will not be cleared.
- If the interrupt occurs during or after the execution of a SLEEP instruction, the device will immediately wake up from sleep. The SLEEP instruction will be completely executed before the wake-up. Therefore, the WDT and WDT postscaler will be cleared, the TO bit will be set and the PD bit will be cleared.

Even if the flag bits were checked before executing a SLEEP instruction, it may be possible for flag bits to become set before the SLEEP instruction completes. To determine whether a SLEEP instruction executed, test the \overline{PD} bit. If the \overline{PD} bit is set, the SLEEP instruction was executed as a NOP.

To ensure that the WDT is cleared, a CLRWDT instruction should be executed before a SLEEP instruction.

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11.1 Instruction Descriptions

ADDLW	Add Literal and W
Syntax:	[<i>label</i>] ADDLW k
Operands:	$0 \leq k \leq 255$
Operation:	$(W) + k \to (W)$
Status Affected:	C, DC, Z
Description:	The contents of the W register are added to the eight bit literal 'k' and the result is placed in the W register.

ANDWF	AND W with f
Syntax:	[<i>label</i>] ANDWF f,d
Operands:	$\begin{array}{l} 0\leq f\leq 127\\ d\in[0,1] \end{array}$
Operation:	(W) .AND. (f) \rightarrow (destination)
Status Affected:	Z
Description:	AND the W register with register 'f'. If 'd' is 0, the result is stored in the W register. If 'd' is 1, the result is stored back in register 'f'.

ADDWF	Add W and f
Syntax:	[<i>label</i>] ADDWF f,d
Operands:	$\begin{array}{l} 0 \leq f \leq 127 \\ d \in [0,1] \end{array}$
Operation:	(W) + (f) \rightarrow (destination)
Status Affected:	C, DC, Z
Description:	Add the contents of the W register with register 'f'. If 'd' is 0, the result is stored in the W register. If 'd' is 1, the result is stored back in register 'f'.

BCF	Bit Clear f
Syntax:	[<i>label</i>] BCF f,b
Operands:	$\begin{array}{l} 0 \leq f \leq 127 \\ 0 \leq b \leq 7 \end{array}$
Operation:	$0 \rightarrow (f < b >)$
Status Affected:	None
Description:	Bit 'b' in register 'f' is cleared.

ANDLW	AND Literal with W
Syntax:	[<i>label</i>] ANDLW k
Operands:	$0 \leq k \leq 255$
Operation:	(W) .AND. (k) \rightarrow (W)
Status Affected:	Z
Description:	The contents of W register are AND'ed with the eight bit literal 'k'. The result is placed in the W register.

BSF	Bit Set f
Syntax:	[<i>label</i>] BSF f,b
Operands:	$\begin{array}{l} 0 \leq f \leq 127 \\ 0 \leq b \leq 7 \end{array}$
Operation:	$1 \rightarrow (f < b >)$
Status Affected:	None
Description:	Bit 'b' in register 'f' is set.

12.0 DEVELOPMENT SUPPORT

The PIC[®] microcontrollers are supported with a full range of hardware and software development tools:

- Integrated Development Environment
 - MPLAB™ IDE Software
- Assemblers/Compilers/Linkers
 - MPASM Assembler
 - MPLAB-C17 and MPLAB-C18 C Compilers
 - MPLINK/MPLIB Linker/Librarian
- Simulators
 - MPLAB-SIM Software Simulator
- Emulators
 - MPLAB-ICE Real-Time In-Circuit Emulator
 - PICMASTER[®]/PICMASTER-CE In-Circuit Emulator
 - ICEPIC™
- In-Circuit Debugger
 - MPLAB-ICD for PIC16F877
- Device Programmers
 - PRO MATE[®] II Universal Programmer
 - PICSTART[®] Plus Entry-Level Prototype Programmer
- Low-Cost Demonstration Boards
 - SIMICE
 - PICDEM-1
 - PICDEM-2
 - PICDEM-3
 - PICDEM-17
 - SEEVAL®
 - KEELOQ[®]

12.1 <u>MPLAB Integrated Development</u> <u>Environment Software</u>

- The MPLAB IDE software brings an ease of software development previously unseen in the 8-bit microcontroller market. MPLAB is a Windows[®]-based application which contains:
- Multiple functionality
 - editor
 - simulator
 - programmer (sold separately)
 - emulator (sold separately)
- A full featured editor
- A project manager
- · Customizable tool bar and key mapping
- · A status bar
- On-line help

MPLAB allows you to:

- Edit your source files (either assembly or 'C')
- One touch assemble (or compile) and download to PIC MCU tools (automatically updates all project information)
- Debug using:
 - source files
 - absolute listing file
 - object code

The ability to use MPLAB with Microchip's simulator, MPLAB-SIM, allows a consistent platform and the ability to easily switch from the cost-effective simulator to the full featured emulator with minimal retraining.

12.2 MPASM Assembler

MPASM is a full featured universal macro assembler for all PIC MCUs. It can produce absolute code directly in the form of HEX files for device programmers, or it can generate relocatable objects for MPLINK.

MPASM has a command line interface and a Windows shell and can be used as a standalone application on a Windows 3.x or greater system. MPASM generates relocatable object files, Intel standard HEX files, MAP files to detail memory usage and symbol reference, an absolute LST file which contains source lines and generated machine code, and a COD file for MPLAB debugging.

MPASM features include:

- MPASM and MPLINK are integrated into MPLAB projects.
- MPASM allows user defined macros to be created for streamlined assembly.
- MPASM allows conditional assembly for multi purpose source files.
- MPASM directives allow complete control over the assembly process.

12.3 <u>MPLAB-C17 and MPLAB-C18</u> <u>C Compilers</u>

The MPLAB-C17 and MPLAB-C18 Code Development Systems are complete ANSI 'C' compilers and integrated development environments for Microchip's PIC17CXXX and PIC18CXXX family of microcontrollers, respectively. These compilers provide powerful integration capabilities and ease of use not found with other compilers.

For easier source level debugging, the compilers provide symbol information that is compatible with the MPLAB IDE memory display.

12.4 MPLINK/MPLIB Linker/Librarian

MPLINK is a relocatable linker for MPASM and MPLAB-C17 and MPLAB-C18. It can link relocatable objects from assembly or C source files along with precompiled libraries using directives from a linker script.

PIC16C62B/72A

MPLIB is a librarian for pre-compiled code to be used with MPLINK. When a routine from a library is called from another source file, only the modules that contains that routine will be linked in with the application. This allows large libraries to be used efficiently in many different applications. MPLIB manages the creation and modification of library files.

MPLINK features include:

- MPLINK works with MPASM and MPLAB-C17 and MPLAB-C18.
- MPLINK allows all memory areas to be defined as sections to provide link-time flexibility.

MPLIB features include:

- MPLIB makes linking easier because single libraries can be included instead of many smaller files.
- MPLIB helps keep code maintainable by grouping related modules together.
- MPLIB commands allow libraries to be created and modules to be added, listed, replaced, deleted, or extracted.

12.5 MPLAB-SIM Software Simulator

The MPLAB-SIM Software Simulator allows code development in a PC host environment by simulating the PIC series microcontrollers on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a file or user-defined key press to any of the pins. The execution can be performed in single step, execute until break, or trace mode.

MPLAB-SIM fully supports symbolic debugging using MPLAB-C17 and MPLAB-C18 and MPASM. The Software Simulator offers the flexibility to develop and debug code outside of the laboratory environment making it an excellent multi-project software development tool.

12.6 <u>MPLAB-ICE High Performance</u> <u>Universal In-Circuit Emulator with</u> <u>MPLAB IDE</u>

The MPLAB-ICE Universal In-Circuit Emulator is intended to provide the product development engineer with a complete microcontroller design tool set for PIC microcontrollers (MCUs). Software control of MPLAB-ICE is provided by the MPLAB Integrated Development Environment (IDE), which allows editing, "make" and download, and source debugging from a single environment.

Interchangeable processor modules allow the system to be easily reconfigured for emulation of different processors. The universal architecture of the MPLAB-ICE allows expansion to support new PIC microcontrollers.

The MPLAB-ICE Emulator System has been designed as a real-time emulation system with advanced features that are generally found on more expensive development tools. The PC platform and Microsoft[®] Windows 3.x/95/98 environment were chosen to best make these features available to you, the end user.

MPLAB-ICE 2000 is a full-featured emulator system with enhanced trace, trigger, and data monitoring features. Both systems use the same processor modules and will operate across the full operating speed range of the PIC MCU.

12.7 PICMASTER/PICMASTER CE

The PICMASTER system from Microchip Technology is a full-featured, professional quality emulator system. This flexible in-circuit emulator provides a high-quality, universal platform for emulating Microchip 8-bit PIC microcontrollers (MCUs). PICMASTER systems are sold worldwide, with a CE compliant model available for European Union (EU) countries.

12.8 <u>ICEPIC</u>

ICEPIC is a low-cost in-circuit emulation solution for the Microchip Technology PIC16C5X, PIC16C6X, PIC16C7X, and PIC16CXXX families of 8-bit one-timeprogrammable (OTP) microcontrollers. The modular system can support different subsets of PIC16C5X or PIC16CXXX products through the use of interchangeable personality modules or daughter boards. The emulator is capable of emulating without target application circuitry being present.

12.9 MPLAB-ICD In-Circuit Debugger

Microchip's In-Circuit Debugger, MPLAB-ICD, is a powerful, low-cost run-time development tool. This tool is based on the flash PIC16F877 and can be used to develop for this and other PIC microcontrollers from the PIC16CXXX family. MPLAB-ICD utilizes the In-Circuit Debugging capability built into the PIC16F87X. This feature, along with Microchip's In-Circuit Serial Programming protocol, offers cost-effective in-circuit flash programming and debugging from the graphical user interface of the MPLAB Integrated Development Environment. This enables a designer to develop and debug source code by watching variables, single-stepping and setting break points. Running at full speed enables testing hardware in real-time. The MPLAB-ICD is also a programmer for the flash PIC16F87X family.

12.10 PRO MATE II Universal Programmer

The PRO MATE II Universal Programmer is a full-featured programmer capable of operating in stand-alone mode as well as PC-hosted mode. PRO MATE II is CE compliant.

The PRO MATE II has programmable VDD and VPP supplies which allows it to verify programmed memory at VDD min and VDD max for maximum reliability. It has an LCD display for instructions and error messages, keys to enter commands and a modular detachable socket assembly to support various package types. In

stand-alone mode the PRO MATE II can read, verify or program PIC devices. It can also set code-protect bits in this mode.

12.11 <u>PICSTART Plus Entry Level</u> <u>Development System</u>

The PICSTART programmer is an easy-to-use, lowcost prototype programmer. It connects to the PC via one of the COM (RS-232) ports. MPLAB Integrated Development Environment software makes using the programmer simple and efficient.

PICSTART Plus supports all PIC devices with up to 40 pins. Larger pin count devices such as the PIC16C92X, and PIC17C76X may be supported with an adapter socket. PICSTART Plus is CE compliant.

12.12 <u>SIMICE Entry-Level</u> <u>Hardware Simulator</u>

SIMICE is an entry-level hardware development system designed to operate in a PC-based environment with Microchip's simulator MPLAB-SIM. Both SIMICE and MPLAB-SIM run under Microchip Technology's MPLAB Integrated Development Environment (IDE) software. Specifically, SIMICE provides hardware simulation for Microchip's PIC12C5XX, PIC12CE5XX, and PIC16C5X families of PIC 8-bit microcontrollers. SIM-ICE works in conjunction with MPLAB-SIM to provide non-real-time I/O port emulation. SIMICE enables a developer to run simulator code for driving the target system. In addition, the target system can provide input to the simulator code. This capability allows for simple and interactive debugging without having to manually generate MPLAB-SIM stimulus files. SIMICE is a valuable debugging tool for entry-level system development.

12.13 <u>PICDEM-1 Low-Cost PIC MCU</u> <u>Demonstration Board</u>

The PICDEM-1 is a simple board which demonstrates the capabilities of several of Microchip's microcontrollers. The microcontrollers supported are: PIC16C5X (PIC16C54 to PIC16C58A), PIC16C61, PIC16C62X, PIC16C71, PIC16C8X, PIC17C42, PIC17C43 and PIC17C44. All necessary hardware and software is included to run basic demo programs. The users can program the sample microcontrollers provided with the PICDEM-1 board, on a PRO MATE II or PICSTART-Plus programmer, and easily test firmware. The user can also connect the PICDEM-1 board to the MPLAB-ICE emulator and download the firmware to the emulator for testing. Additional prototype area is available for the user to build some additional hardware and connect it to the microcontroller socket(s). Some of the features include an RS-232 interface, a potentiometer for simulated analog input, push-button switches and eight LEDs connected to PORTB.

12.14 PICDEM-2 Low-Cost PIC16CXX Demonstration Board

The PICDEM-2 is a simple demonstration board that supports the PIC16C62, PIC16C64, PIC16C65, PIC16C73 and PIC16C74 microcontrollers. All the necessary hardware and software is included to run the basic demonstration programs. The user can program the sample microcontrollers provided with the PICDEM-2 board, on a PRO MATE II programmer or PICSTART-Plus, and easily test firmware. The MPLAB-ICE emulator may also be used with the PICDEM-2 board to test firmware. Additional prototype area has been provided to the user for adding additional hardware and connecting it to the microcontroller socket(s). Some of the features include a RS-232 interface, push-button switches, a potentiometer for simulated analog input, a Serial EEPROM to demonstrate usage of the I²C bus and separate headers for connection to an LCD module and a keypad.

12.15 <u>PICDEM-3 Low-Cost PIC16CXXX</u> <u>Demonstration Board</u>

The PICDEM-3 is a simple demonstration board that supports the PIC16C923 and PIC16C924 in the PLCC package. It will also support future 44-pin PLCC microcontrollers with a LCD Module. All the necessary hardware and software is included to run the basic demonstration programs. The user can program the sample microcontrollers provided with the PICDEM-3 board, on a PRO MATE II programmer or PICSTART Plus with an adapter socket, and easily test firmware. The MPLAB-ICE emulator may also be used with the PICDEM-3 board to test firmware. Additional prototype area has been provided to the user for adding hardware and connecting it to the microcontroller socket(s). Some of the features include an RS-232 interface, push-button switches, a potentiometer for simulated analog input, a thermistor and separate headers for connection to an external LCD module and a keypad. Also provided on the PICDEM-3 board is an LCD panel, with 4 commons and 12 segments, that is capable of displaying time, temperature and day of the week. The PICDEM-3 provides an additional RS-232 interface and Windows 3.1 software for showing the demultiplexed LCD signals on a PC. A simple serial interface allows the user to construct a hardware demultiplexer for the LCD signals.

12.16 PICDEM-17

The PICDEM-17 is an evaluation board that demonstrates the capabilities of several Microchip microcontrollers, including PIC17C752, PIC17C756, PIC17C762, and PIC17C766. All necessary hardware is included to run basic demo programs, which are supplied on a 3.5-inch disk. A programmed sample is included, and the user may erase it and program it with the other sample programs using the PRO MATE II or PICSTART Plus device programmers and easily debug

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13.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings (†)

Ambient temperature under bias	55°C to +125°C
Storage temperature	65°C to +150°C
Voltage on any pin with respect to Vss (except VDD, MCLR, and RA4)	-0.3V to (VDD + 0.3V)
Voltage on VDD with respect to Vss	-0.3V to +7.5V
Voltage on MCLR with respect to Vss (Note 2)	0V to +13.25V
Voltage on RA4 with respect to Vss	0V to +8.5V
Total power dissipation (Note 1)	
Maximum current out of Vss pin	
Maximum current into VDD pin	
Input clamp current, IIK (VI < 0 or VI > VDD)	±20 mA
Output clamp current, Ioк (Vo < 0 or Vo > VDD)	±20 mA
Maximum output current sunk by any I/O pin	25 mA
Maximum output current sourced by any I/O pin	25 mA
Maximum current sunk by PORTA and PORTB (combined)	
Maximum current sourced by PORTA and PORTB (combined)	
Maximum current sunk by PORTC	
Maximum current sourced by PORTC	
Note 1: Power dissipation is calculated as follows: Pdis = VDD x {IDD - \sum IOH} + \sum {((VDD-VOH) x IOH} + Σ (VOI x IOL)

2: Voltage spikes below Vss at the MCLR/VPP pin, inducing currents greater than 80 mA, may cause latch-up. Thus, a series resistor of 50-100Ω should be used when applying a "low" level to the MCLR/VPP pin, rather than pulling this pin directly to Vss.

† NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

FIGURE 13-9: TIMER0 AND TIMER1 EXTERNAL CLOCK TIMINGS



TARI E 12-5.	TIMEDO AND TIMEDI EXTERNAL CLOCK DECLIIDEMENTS
IADLE 13-3.	TIMENU AND TIMENT EXTERNAL CLOCK REQUIREMENTS

Param No.	Sym	Characteristic			Min	Typ†	Max	Units	Conditions	
40*	Tt0H	T0CKI High Pulse Width		No Prescaler	0.5Tcy + 20	—	_	ns	Must also meet parameter 42	
				With Prescaler	10	—		ns		
41*	Tt0L	T0CKI Low Pulse Width		No Prescaler	0.5Tcy + 20	—		ns	Must also meet parameter 42	
				With Prescaler	10	—	-	ns		
42*	Tt0P	T0CKI Period		No Prescaler	Tcy + 40	—		ns		
				With Prescaler	Greater of: 20 or <u>Tcy + 40</u> N	_	_	ns	N = prescale value (2, 4,, 256)	
45*	Tt1H	T1CKI High Time	Synchronous, P	rescaler = 1	0.5TCY + 20	—	—	ns	Must also meet parameter 47	
			Synchronous, Prescaler = 2,4,8	PIC16CXX	15	—		ns		
				PIC16LCXX	25	—	—	ns		
			Asynchronous	PIC16CXX	30	—	-	ns		
				PIC16LCXX	50	—	-	ns		
46*	Tt1L	T1CKI Low Time	Synchronous, P	rescaler = 1	0.5TCY + 20	—		ns	Must also meet	
			Synchronous, Prescaler = 2,4,8	PIC16CXX	15	—	—	ns	parameter 47	
				PIC16LCXX	25	—	—	ns		
			Asynchronous	PIC16CXX	30	—	—	ns		
				PIC16LCXX	50	—	—	ns		
47*	Tt1P	T1CKI input period	Synchronous	PIC16CXX	GREATER OF: 30 OR <u>TCY + 40</u> N	-	_	ns	N = prescale value (1, 2, 4, 8)	
				PIC16LCXX	GREATER OF: 50 OR <u>TCY + 40</u> N				N = prescale value $(1, 2, 4, 8)$	
		Asynchronou	Asynchronous	PIC16CXX	60	—		ns		
				PIC16LCXX	100	—	-	ns		
	Ft1	Timer1 oscillator input frequency range (oscillator enabled by setting bit T1OSCEN)		DC	-	200	kHz			
48	TCKEZtmr1	Delay from external clock edge to timer increment			2Tosc	—	7Tosc	_		

* These parameters are characterized but not tested.
 † Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

PIC16C62B/72A

FIGURE 13-14: EXAMPLE SPI SLAVE MODE TIMING (CKE = 1)



TABLE 13-10: EXAMPLE SPI SLAVE MODE REQUIREMENTS (CKE = 1)

Param. No.	Symbol	Characteristic		Min	Тур†	Мах	Units	Conditions
70	TssL2scH, TssL2scL	$\overline{\text{SS}}\downarrow$ to SCK \downarrow or SCK \uparrow input		Тсү	—	—	ns	
71	TscH	SCK input high time	Continuous	1.25Tcy + 30	_		ns	
71A		(slave mode)	Single Byte	40	_	_	ns	Note 1
72	TscL	SCK input low time	Continuous	1.25Tcy + 30	_		ns	
72A		(slave mode)	Single Byte	40	_		ns	Note 1
73A	Тв2в	Last clock edge of Byte1 to the 1st clock edge of Byte2		1.5Tcy + 40	_	_	ns	Note 1
74	TscH2diL, TscL2diL	Hold time of SDI data input to SCK edge		100	-	—	ns	
75	TdoR	SDO data output rise	PIC16CXX	—	10	25	ns	
		time	PIC16LCXX		20	45	ns	
76	TdoF	SDO data output fall time		_	10	25	ns	
77	TssH2doZ	SS↑ to SDO output hi-impedance		10	_	50	ns	
78 TscR	TscR	SCK output rise time	PIC16CXX	_	10	25	ns	
		(master mode)	PIC16LCXX	_	20	45	ns	
79	TscF	SCK output fall time (master mode)		—	10	25	ns	
80	TscH2doV,	SDO data output valid	PIC16CXX	_	_	50	ns	
	TscL2doV after SCK edge	after SCK edge	PIC16LCXX	_	_	100	ns	
82	TssL2doV	SDO data output valid	PIC16CXX	_	_	50	ns	
		after SS↓ edge	PIC16LCXX	—	—	100	ns	
83	TscH2ssH, TscL2ssH	\overline{SS} \uparrow after SCK edge		1.5TCY + 40	-	—	ns	

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Specification 73A is only required if specifications 71A and 72A are used.

14.0 DC AND AC CHARACTERISTICS GRAPHS AND TABLES

The graphs and tables provided in this section are for **design guidance** and are **not tested**.

In some graphs or tables, the data presented are **outside specified operating range** (i.e., outside specified VDD range). This is for **information only** and devices are guaranteed to operate properly only within the specified range.

The data presented in this section is a **statistical summary** of data collected on units from different lots over a period of time and matrix samples. 'Typical' represents the mean of the distribution at 25° C. 'Max' or 'min' represents (mean + 3σ) or (mean - 3σ) respectively, where σ is standard deviation, over the whole temperature range.

Graphs and Tables not available at this time.

Data is not available at this time but you may reference the *PIC16C72 Series Data Sheet* (DS39016,) DC and AC characteristic section, which contains data similar to what is expected.

SSP	
Enable (SSPIE Bit)	14
Flag (SSPIF Bit)	
RA5/SS/AN4 Pin	6
RC3/SCK/SCL Pin	6
RC4/SDI/SDA Pin	6
RC5/SDO Pin	6
SSPADD Register	
SSPBUF Register	
SSPCON Register	
SSPSTAT Register	
TMR2 Output for Clock Shift	
Write Collision Detect (WCOL Bit)	
SSPCON Register	
CKP Bit	
SSPEN Bit	
SSPM3:SSPM0 Bits	
SSPOV Bit	
WCOL Bit	
SSPSTAT Register	
BF Bit	
CKE Bit	46
D/Ā Bit	46
P bit	
R/W Bit	42, 43, 44, 46
S Bit	
SMP Bit	
UA Bit	
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DC Bit	11
IRP Bit	11
PD Bit	11, 57
RP1:RP0 Bits	
TO Bit	
Z Bit	

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T1CON Register	
T1CKPS1:T1CKPS0 Bits	
T10SCEN Bit	27
T1SYNC Bit	
TMB1CS Bit	
TMR10N Bit	27
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Overflow Flag (T0IF Bit)	
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Power-up Timer (PWRT)	92 20
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Watchdog Timer (WDT)	
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