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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	I ² C, IrDA, LINbus, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	24
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.85V ~ 3.8V
Data Converters	A/D 24x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TJ)
Mounting Type	Surface Mount
Package / Case	32-VFQFN Exposed Pad
Supplier Device Package	32-QFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32pg1b100f256im32-c0r

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

3.2 Power

The EFM32PG1 has an Energy Management Unit (EMU) and efficient integrated regulators to generate internal supply voltages. Only a single external supply voltage is required, from which all internal voltages are created. An optional integrated dc-dc buck regulator can be utilized to further reduce the current consumption. The dc-dc regulator requires one external inductor and one external capacitor.

AVDD and VREGVDD need to be 1.85 V or higher for the MCU to operate across all conditions; however the rest of the system will operate down to 1.62 V, including the digital supply and I/O. This means that the device is fully compatible with 1.8 V components. Running from a sufficiently high supply, the device can use the dc-dc to regulate voltage not only for itself, but also for other PCB components, supplying up to a total of 200 mA.

3.2.1 Energy Management Unit (EMU)

The Energy Management Unit manages transitions of energy modes in the device. Each energy mode defines which peripherals and features are available and the amount of current the device consumes. The EMU can also be used to turn off the power to unused RAM blocks, and it contains control registers for the dc-dc regulator and the Voltage Monitor (VMON). The VMON is used to monitor multiple supply voltages. It has multiple channels which can be programmed individually by the user to determine if a sensed supply has fallen below a chosen threshold.

3.2.2 DC-DC Converter

The DC-DC buck converter covers a wide range of load currents and provides up to 90% efficiency in energy modes EM0, EM1, EM2 and EM3, and can supply up to 200 mA to the device and surrounding PCB components. Protection features include programmable current limiting, short-circuit protection, and dead-time protection. The DC-DC converter may also enter bypass mode when the input voltage is too low for efficient operation. In bypass mode, the DC-DC input supply is internally connected directly to its output through a low resistance switch. Bypass mode also supports in-rush current limiting to prevent input supply voltage droops due to excessive output current transients.

3.3 General Purpose Input/Output (GPIO)

EFM32PG1 has up to 32 General Purpose Input/Output pins. Each GPIO pin can be individually configured as either an output or input. More advanced configurations including open-drain, open-source, and glitch-filtering can be configured for each individual GPIO pin. The GPIO pins can be overridden by peripheral connections, like SPI communication. Each peripheral connection can be routed to several GPIO pins on the device. The input value of a GPIO pin can be routed through the Peripheral Reflex System to other peripherals. The GPIO subsystem supports asynchronous external pin interrupts.

3.4 Clocking

3.4.1 Clock Management Unit (CMU)

The Clock Management Unit controls oscillators and clocks in the EFM32PG1. Individual enabling and disabling of clocks to all peripheral modules is performed by the CMU. The CMU also controls enabling and configuration of the oscillators. A high degree of flexibility allows software to optimize energy consumption in any specific application by minimizing power dissipation in unused peripherals and oscillators.

3.4.2 Internal and External Oscillators

The EFM32PG1 supports two crystal oscillators and fully integrates four RC oscillators, listed below.

- A high frequency crystal oscillator (HFXO) with integrated load capacitors, tunable in small steps, provides a precise timing reference for the MCU. Crystal frequencies in the range from 38 to 40 MHz are supported. An external clock source such as a TCXO can also be applied to the HFXO input for improved accuracy over temperature.
- A 32.768 kHz crystal oscillator (LFXO) provides an accurate timing reference for low energy modes.
- An integrated high frequency RC oscillator (HFRCO) is available for the MCU system, when crystal accuracy is not required. The HFRCO employs fast startup at minimal energy consumption combined with a wide frequency range.
- An integrated auxilliary high frequency RC oscillator (AUXHFRCO) is available for timing the general-purpose ADC and the Serial Wire debug port with a wide frequency range.
- An integrated low frequency 32.768 kHz RC oscillator (LFRCO) can be used as a timing reference in low energy modes, when crystal accuracy is not required.
- An integrated ultra-low frequency 1 kHz RC oscillator (ULFRCO) is available to provide a timing reference at the lowest energy consumption in low energy modes.

3.6.3 Inter-Integrated Circuit Interface (I²C)

The I²C module provides an interface between the MCU and a serial I²C bus. It is capable of acting as both a master and a slave and supports multi-master buses. Standard-mode, fast-mode and fast-mode plus speeds are supported, allowing transmission rates from 10 kbit/s up to 1 Mbit/s. Slave arbitration and timeouts are also available, allowing implementation of an SMBus-compliant system. The interface provided to software by the I²C module allows precise timing control of the transmission process and highly automated transfers. Automatic recognition of slave addresses is provided in active and low energy modes.

3.6.4 Peripheral Reflex System (PRS)

The Peripheral Reflex System provides a communication network between different peripheral modules without software involvement. Peripheral modules producing Reflex signals are called producers. The PRS routes Reflex signals from producers to consumer peripherals which in turn perform actions in response. Edge triggers and other functionality can be applied by the PRS. The PRS allows peripheral to act autonomously without waking the MCU core, saving power.

3.7 Security Features

3.7.1 GPCRC (General Purpose Cyclic Redundancy Check)

The GPCRC module implements a Cyclic Redundancy Check (CRC) function. It supports both 32-bit and 16-bit polynomials. The supported 32-bit polynomial is 0x04C11DB7 (IEEE 802.3), while the 16-bit polynomial can be programmed to any value, depending on the needs of the application.

3.7.2 Crypto Accelerator (CRYPTO)

The Crypto Accelerator is a fast and energy-efficient autonomous hardware encryption and decryption accelerator. EFM32PG1 devices support AES encryption and decryption with 128- or 256-bit keys, ECC over both GF(P) and GF(2^m), and SHA-1 and SHA-2 (SHA-224 and SHA-256).

Supported block cipher modes of operation for AES include: ECB, CTR, CBC, PCBC, CFB, OFB, GCM, CBC-MAC, GMAC and CCM.

Supported ECC NIST recommended curves include P-192, P-224, P-256, K-163, K-233, B-163 and B-233.

The CRYPTO module allows fast processing of GCM (AES), ECC and SHA with little CPU intervention. CRYPTO also provides trigger signals for DMA read and write operations.

3.8 Analog

3.8.1 Analog Port (APORT)

The Analog Port (APORT) is an analog interconnect matrix allowing access to many analog modules on a flexible selection of pins. Each APORT bus consists of analog switches connected to a common wire. Since many clients can operate differentially, buses are grouped by X/Y pairs.

3.8.2 Analog Comparator (ACMP)

The Analog Comparator is used to compare the voltage of two analog inputs, with a digital output indicating which input voltage is higher. Inputs are selected from among internal references and external pins. The tradeoff between response time and current consumption is configurable by software. Two 6-bit reference dividers allow for a wide range of internally-programmable reference sources. The ACMP can also be used to monitor the supply voltage. An interrupt can be generated when the supply falls below or rises above the programmable threshold.

3.8.3 Analog to Digital Converter (ADC)

The ADC is a Successive Approximation Register (SAR) architecture, with a resolution of up to 12 bits at up to 1 Msps. The output sample resolution is configurable and additional resolution is possible using integrated hardware for averaging over multiple samples. The ADC includes integrated voltage references and an integrated temperature sensor. Inputs are selectable from a wide range of sources, including pins configurable as either single-ended or differential.

4.1.2 Operating Conditions

When assigning supply sources, the following requirements must be observed:

- VREGVDD must be the highest voltage in the system
- VREGVDD = AVDD
- DVDD ≤ AVDD
- IOVDD ≤ AVDD

4.1.2.1 General Operating Conditions

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
Operating temperature range	T _{OP}	-G temperature grade, Ambient Temperature	-40	25	85	°C
		-I temperature grade, Junction Temperature	-40	25	125	°C
AVDD Supply voltage ¹	V _{AVDD}		1.85	3.3	3.8	V
VREGVDD Operating supply	V _{VREGVDD}	DCDC in regulation	2.4	3.3	3.8	V
voltage ^{1 2}		DCDC in bypass, 50mA load	1.85	3.3	3.8	V
		DCDC not in use. DVDD external- ly shorted to VREGVDD	1.85	3.3	3.8	V
VREGVDD Current	IVREGVDD	DCDC in bypass, T _{amb} ≤ 85 °C	_	—	200	mA
		DCDC in bypass, T _{amb} > 85 °C	_	_	100	mA
DVDD Operating supply volt- age	V _{DVDD}		1.62	_	V _{VREGVDD}	V
IOVDD Operating supply voltage	VIOVDD		1.62	_	V _{VREGVDD}	V
Difference between AVDD and VREGVDD, ABS(AVDD- VREGVDD)	dV _{DD}		_	_	0.1	V
HFCLK frequency	f _{CORE}	0 wait-states (MODE = WS0) ³	—	—	26	MHz
		1 wait-states (MODE = WS1) ³	—	_	40	MHz

Table 4.2. General Operating Conditions

Note:

1. VREGVDD must be tied to AVDD. Both VREGVDD and AVDD minimum voltages must be satisfied for the part to operate.

2. The minimum voltage required in bypass mode is calculated using R_{BYP} from the DCDC specification table. Requirements for other loads can be calculated as V_{DVDD_min}+I_{LOAD} * R_{BYP_max}

3. In MSC_READCTRL register

4.1.4 DC-DC Converter

Test conditions: L_{DCDC} =4.7 µH (Murata LQH3NPN4R7MM0L), C_{DCDC} =1.0 µF (Murata GRM188R71A105KA61D), $V_{DCDC_{-1}}$ =3.3 V, $V_{DCDC_{-0}}$ =1.8 V, $I_{DCDC_{-LOAD}}$ =50 mA, Heavy Drive configuration, $F_{DCDC_{-LN}}$ =7 MHz, unless otherwise indicated.

Table 4.4. DC-DC Converter

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
Input voltage range	V _{DCDC_I}	Bypass mode, I _{DCDC_LOAD} = 50 mA	1.85	_	V _{VREGVDD} MAX	V
		Low noise (LN) mode, 1.8 V out- put, I_{DCDC_LOAD} = 100 mA, or Low power (LP) mode, 1.8 V out- put, I_{DCDC_LOAD} = 10 mA	2.4	_	V _{VREGVDD} MAX	V
		Low noise (LN) mode, 1.8 V out- put, I _{DCDC_LOAD} = 200 mA	2.6	_	V _{VREGVDD} MAX	V
Output voltage programma- ble range ¹	V _{DCDC_O}		1.8	_	V _{VREGVDD}	V
Regulation DC Accuracy	ACC _{DC}	Low noise (LN) mode, 1.8 V target output	1.7	_	1.9	V
Regulation Window ²	WIN _{REG}	Low power (LP) mode, LPCMPBIAS ³ = 0, 1.8 V target output, I _{DCDC_LOAD} ≤ 75 µA	1.63	_	2.2	V
		Low power (LP) mode, LPCMPBIAS ³ = 3, 1.8 V target output, I _{DCDC_LOAD} ≤ 10 mA	1.63	_	2.1	V
Steady-state output ripple	V _R		_	3	_	mVpp
Output voltage under/over- shoot	V _{OV}	CCM Mode (LNFORCECCM ³ = 1), Load changes between 0 mA and 100 mA	_	_	150	mV
		DCM Mode (LNFORCECCM ³ = 0), Load changes between 0 mA and 10 mA	_	_	150	mV
		Overshoot during LP to LN CCM/DCM mode transitions com- pared to DC level in LN mode	_	200	_	mV
		Undershoot during BYP/LP to LN CCM (LNFORCECCM ³ = 1) mode transitions compared to DC level in LN mode	_	50	_	mV
		Undershoot during BYP/LP to LN DCM (LNFORCECCM ³ = 0) mode transitions compared to DC level in LN mode	-	125	_	mV
DC line regulation	V _{REG}	Input changes between V _{VREGVDD_MAX} and 2.4 V	_	0.1	-	%
DC load regulation	I _{REG}	Load changes between 0 mA and 100 mA in CCM mode	_	0.1	_	%

4.1.5.2 Current Consumption 3.3 V using DC-DC Converter

Unless otherwise indicated, typical conditions are: VREGVDD = AVDD = IOVDD = 3.3 V, DVDD = 1.8 V DC-DC output. T_{OP} = 25 °C. Minimum and maximum values in this table represent the worst conditions across supply voltage and process variation at T_{OP} = 25 °C. See Figure 5.2 EFM32PG1 Typical Application Circuit Using the DC-DC Converter on page 47.

Parameter	Symbol	Test Condition	Min	Тур	Мах	Unit
Current consumption in EM0 Active mode with all periph-	IACTIVE	38.4 MHz crystal, CPU running while loop from flash ²	_	86	_	µA/MHz
Noise DCM mode ¹ .		38 MHz HFRCO, CPU running Prime from flash		63	_	µA/MHz
		38 MHz HFRCO, CPU running while loop from flash		71	_	µA/MHz
		38 MHz HFRCO, CPU running CoreMark from flash		78	_	µA/MHz
		26 MHz HFRCO, CPU running while loop from flash		76	_	µA/MHz
Current consumption in EM0 Active mode with all periph-		38.4 MHz crystal, CPU running while loop from flash ²	—	96	—	µA/MHz
Noise CCM mode ³ .		38 MHz HFRCO, CPU running Prime from flash		75	_	µA/MHz
		38 MHz HFRCO, CPU running while loop from flash		81	_	µA/MHz
		38 MHz HFRCO, CPU running CoreMark from flash	—	88	_	µA/MHz
		26 MHz HFRCO, CPU running while loop from flash	—	94	—	µA/MHz
Current consumption in EM1	I _{EM1}	38.4 MHz crystal ²	—	47	_	µA/MHz
als disabled, DCDC in Low		38 MHz HFRCO	—	32	_	µA/MHz
Noise DCM mode ¹ .		26 MHz HFRCO	_	38		µA/MHz
Current consumption in EM1		38.4 MHz crystal ²		59	_	µA/MHz
als disabled, DCDC in Low		38 MHz HFRCO	_	45	_	µA/MHz
Noise CCM mode ³ .		26 MHz HFRCO	—	58	_	µA/MHz
Current consumption in EM2 Deep Sleep mode. DCDC in	I _{EM2}	Full RAM retention and RTCC running from LFXO	—	2.5	_	μA
Low Power mode ⁴ .		4 kB RAM retention and RTCC running from LFRCO		2.2	_	μA
Current consumption in EM3 Stop mode	I _{EM3}	Full RAM retention and CRYO- TIMER running from ULFRCO	—	2.1	—	μA
Current consumption in EM4H Hibernate mode	I _{EM4}	128 byte RAM retention, RTCC running from LFXO	_	0.86		μA
		128 byte RAM retention, CRYO- TIMER running from ULFRCO	_	0.58		μA
		128 byte RAM retention, no RTCC		0.58	_	μΑ

Table 4.6. Current Consumption 3.3V with DC-DC

Table 4.18. ADC

Parameter	Symbol	Test Condition	Min	Тур	Мах	Unit
Resolution	VRESOLUTION		6	_	12	Bits
Input voltage range	V _{ADCIN}	Single ended	0	_	2*V _{REF}	V
		Differential	-V _{REF}		V _{REF}	V
Input range of external refer- ence voltage, single ended and differential	V _{ADCREFIN_P}		1	_	V _{AVDD}	V
Power supply rejection ¹	PSRR _{ADC}	At DC	_	80	_	dB
Analog input common mode rejection ratio	CMRR _{ADC}	At DC	_	80		dB
Current from all supplies, us-	IADC_CONTI-	1 Msps / 16 MHz ADCCLK,	_	301	350	μA
Continous operation. WAR- MUPMODE ² = KEEPADC-	NOUS_LP	BIASPROG = 0, GPBIASACC = 1 3				
WARM		250 ksps / 4 MHz ADCCLK, BIA- SPROG = 6, GPBIASACC = 1 ³	—	149	_	μA
		62.5 ksps / 1 MHz ADCCLK,	_	91	_	μA
		BIASPROG = 15, GPBIASACC = 1 ³				
Current from all supplies, us-	IADC_NORMAL_LP	35 ksps / 16 MHz ADCCLK,	_	51		μA
Duty-cycled operation. WAR- MUPMODE ² = NORMAL		BIASPROG = 0, GPBIASACC = 1 3				
		5 ksps / 16 MHz ADCCLK		9	_	μA
		BIASPROG = 0, GPBIASACC = 1 3				
Current from all supplies, us-	IADC_STAND-	125 ksps / 16 MHz ADCCLK,	_	117	_	μA
Duty-cycled operation. AWARMUPMODE ² = KEEP-	BY_LP	BIASPROG = 0, GPBIASACC = 1 3				
INSTANDBY or KEEPIN- SLOWACC		35 ksps / 16 MHz ADCCLK,	—	79	_	μA
		BIASPROG = 0, GPBIASACC = 1 3				
Current from all supplies, us-	IADC_CONTI-	1 Msps / 16 MHz ADCCLK,	—	345	_	μA
Continous operation. WAR- MUPMODE ² = KEEPADC-	NOUS_HP	BIASPROG = 0, GPBIASACC = 0 3				
WARM		250 ksps / 4 MHz ADCCLK, BIA- SPROG = 6, GPBIASACC = 0 ³	—	191	_	μA
		62.5 ksps / 1 MHz ADCCLK,	_	132		μA
		BIASPROG = 15, GPBIASACC = 0^{3}				

4.1.14 Analog Comparator (ACMP)

Table 4.20. ACMP

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
Input voltage range	V _{ACMPIN}	ACMPVDD = ACMPn_CTRL_PWRSEL ¹	0	_	V _{ACMPVDD}	V
Supply Voltage	VACMPVDD	BIASPROG ² \leq 0x10 or FULL- BIAS ² = 0	1.85		V _{VREGVDD} MAX	V
		$0x10 < BIASPROG^2 \le 0x20$ and FULLBIAS ² = 1	2.1		V _{VREGVDD} MAX	V
Active current not including	I _{ACMP}	$BIASPROG^2 = 1$, $FULLBIAS^2 = 0$	—	50	—	nA
voltage relefence		$BIASPROG^{2} = 0x10, FULLBIAS^{2} = 0$	_	306	_	nA
		$BIASPROG^{2} = 0x20, FULLBIAS^{2}$ $= 1$	_	74	95	μA
Current consumption of inter- nal voltage reference	IACMPREF	VLP selected as input using 2.5 V Reference / 4 (0.625 V)	—	50	_	nA
		VLP selected as input using VDD		20	—	nA
		VBDIV selected as input using 1.25 V reference / 1	—	4.1	—	μA
		VADIV selected as input using VDD/1	_	2.4	_	μA
Hysteresis (V _{CM} = 1.25 V,	V _{ACMPHYST}	HYSTSEL ³ = HYST0	-1.75	0	1.75	mV
$BIASPROG^{2} = 0x10, FULL-BIAS^{2} = 1)$		HYSTSEL ³ = HYST1	10	18	26	mV
		HYSTSEL ³ = HYST2	21	32	46	mV
		HYSTSEL ³ = HYST3	27	44	63	mV
		HYSTSEL ³ = HYST4	32	55	80	mV
		HYSTSEL ³ = HYST5	38	65	100	mV
		HYSTSEL ³ = HYST6	43	77	121	mV
		HYSTSEL ³ = HYST7	47	86	148	mV
		HYSTSEL ³ = HYST8	-4	0	4	mV
		HYSTSEL ³ = HYST9	-27	-18	-10	mV
		HYSTSEL ³ = HYST10	-47	-32	-18	mV
		HYSTSEL ³ = HYST11	-64	-43	-27	mV
		HYSTSEL ³ = HYST12	-78	-54	-32	mV
		HYSTSEL ³ = HYST13	-93	-64	-37	mV
		HYSTSEL ³ = HYST14	-113	-74	-42	mV
		HYSTSEL ³ = HYST15	-135	-85	-47	mV

4.1.16 USART SPI

SPI Master Timing

Table 4.24.	SPI	Master	Timing
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Parameter	Symbol	Test Condition	Min	Тур	Max	Unit		
SCLK period ^{1 2}	t _{SCLK}		2 * t _{HFPERCLK}	_	_	ns		
CS to MOSI ^{1 2}	t _{CS_MO}		0		8	ns		
SCLK to MOSI ^{1 2}	t _{SCLK_MO}		3		20	ns		
MISO setup time ^{1 2}	t _{SU_MI}	IOVDD = 1.62 V	56	_	_	ns		
		IOVDD = 3.0 V	37	_	_	ns		
MISO hold time ^{1 2}	t _{H_MI}		6			ns		
Note:								

1. Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0)

2. Measurement done with 8 pF output loading at 10% and 90% of V_{DD} (figure shows 50% of $V_{\text{DD}})$



Figure 4.1. SPI Master Timing Diagram



Figure 4.18. LFRCO Typical Performance at 32.768 kHz



Figure 4.19. ULFRCO Typical Performance at 1 kHz

5. Typical Connection Diagrams

5.1 Power

Typical power supply connections for direct supply, without using the internal dc-dc converter, are shown in Figure 5.1 EFM32PG1 Typical Application Circuit, Direct Supply, No DC-DC Converter on page 47.



Figure 5.1. EFM32PG1 Typical Application Circuit, Direct Supply, No DC-DC Converter

A typical application circuit using the internal dc-dc converter is shown in Figure 5.2 EFM32PG1 Typical Application Circuit Using the DC-DC Converter on page 47. The MCU operates from the dc-dc converter supply.



Figure 5.2. EFM32PG1 Typical Application Circuit Using the DC-DC Converter

5.2 Other Connections

Other components or connections may be required to meet the system-level requirements. Application Note AN0002: "Hardware Design Considerations" contains detailed information on these connections. Application Notes can be accessed on the Silicon Labs website (www.silabs.com/32bit-appnotes).

6. Pin Definitions

6.1 EFM32PG1 QFN48 with DC-DC Definition



Figure 6.1. EFM32PG1 QFN48 with DC-DC Pinout

QFN	48 Pin# and Name		Pin Alternate Functi	onality / Description	
Pin #	Pin Name	Analog	Timers	Communication	Other
0	RFVSS	Radio Ground			I
1	PF0	BUSAX BUSBY	TIM0_CC0 #24 TIM0_CC1 #23 TIM0_CC2 #22 TIM0_CDTI0 #21 TIM0_CDTI1 #20 TIM0_CDTI2 #19 TIM1_CC0 #24 TIM1_CC1 #23 TIM1_CC2 #22 TIM1_CC3 #21 LE- TIM0_OUT0 #24 LE- TIM0_OUT1 #23 PCNT0_S0IN #24 PCNT0_S1IN #23	US0_TX #24 US0_RX #23 US0_CLK #22 US0_CS #21 US0_CTS #20 US0_RTS #19 US1_TX #24 US1_RX #23 US1_CLK #22 US1_CS #21 US1_CTS #20 US1_RTS #19 LEU0_TX #24 LEU0_RX #23 I2C0_SDA #24 I2C0_SCL #23	PRS_CH0 #0 PRS_CH1 #7 PRS_CH2 #6 PRS_CH3 #5 ACMP0_O #24 ACMP1_O #24 DBG_SWCLKTCK #0 BOOT_TX
2	PF1	BUSAY BUSBX	TIM0_CC0 #25 TIM0_CC1 #24 TIM0_CC2 #23 TIM0_CDTI0 #22 TIM0_CDTI1 #21 TIM0_CDTI2 #20 TIM1_CC0 #25 TIM1_CC1 #24 TIM1_CC2 #23 TIM1_CC3 #22 LE- TIM0_OUT0 #25 LE- TIM0_OUT1 #24 PCNT0_S0IN #25 PCNT0_S1IN #24	US0_TX #25 US0_RX #24 US0_CLK #23 US0_CS #22 US0_CTS #21 US0_RTS #20 US1_TX #25 US1_RX #24 US1_CLK #23 US1_CS #22 US1_CTS #21 US1_RTS #20 LEU0_TX #25 LEU0_RX #24 I2C0_SDA #25 I2C0_SCL #24	PRS_CH0 #1 PRS_CH1 #0 PRS_CH2 #7 PRS_CH3 #6 ACMP0_O #25 ACMP1_O #25 DBG_SWDIOTMS #0 BOOT_RX
3	PF2	BUSAX BUSBY	TIM0_CC0 #26 TIM0_CC1 #25 TIM0_CC2 #24 TIM0_CDTI0 #23 TIM0_CDTI1 #22 TIM0_CDTI2 #21 TIM1_CC0 #26 TIM1_CC1 #25 TIM1_CC2 #24 TIM1_CC3 #23 LE- TIM0_OUT0 #26 LE- TIM0_OUT1 #25 PCNT0_S0IN #26 PCNT0_S1IN #25	US0_TX #26 US0_RX #25 US0_CLK #24 US0_CS #23 US0_CTS #22 US0_RTS #21 US1_TX #26 US1_RX #25 US1_CLK #24 US1_CS #23 US1_CTS #22 US1_RTS #21 LEU0_TX #26 LEU0_RX #25 I2C0_SDA #26 I2C0_SCL #25	CMU_CLK0 #6 PRS_CH0 #2 PRS_CH1 #1 PRS_CH2 #0 PRS_CH3 #7 ACMP0_O #26 ACMP1_O #26 DBG_TDO #0 DBG_SWO #0 GPIO_EM4WU0

Table 6.1. QFN48 with DC-DC Device Pinout

QFN	48 Pin# and Name		Pin Alternate Functi	Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other		
46	PC9	BUSAY BUSBX	TIM0_CC0 #14 TIM0_CC1 #13 TIM0_CC2 #12 TIM0_CDTI0 #11 TIM0_CDTI1 #10 TIM0_CDTI2 #9 TIM1_CC0 #14 TIM1_CC1 #13 TIM1_CC2 #12 TIM1_CC3 #11 LE- TIM0_OUT0 #14 LE- TIM0_OUT1 #13 PCNT0_S0IN #14 PCNT0_S1IN #13	US0_TX #14 US0_RX #13 US0_CLK #12 US0_CS #11 US0_CTS #10 US0_RTS #9 US1_TX #14 US1_RX #13 US1_CLK #12 US1_CS #11 US1_CTS #10 US1_RTS #9 LEU0_TX #14 LEU0_RX #13 I2C0_SDA #14 I2C0_SCL #13	PRS_CH0 #11 PRS_CH9 #14 PRS_CH10 #3 PRS_CH11 #2 ACMP0_O #14 ACMP1_O #14		
47	PC10	BUSAX BUSBY	TIM0_CC0 #15 TIM0_CC1 #14 TIM0_CC2 #13 TIM0_CDTI0 #12 TIM0_CDTI1 #11 TIM0_CDTI2 #10 TIM1_CC0 #15 TIM1_CC1 #14 TIM1_CC2 #13 TIM1_CC3 #12 LE- TIM0_OUT0 #15 LE- TIM0_OUT0 #15 LE- TIM0_OUT1 #14 PCNT0_S0IN #15 PCNT0_S1IN #14	US0_TX #15 US0_RX #14 US0_CLK #13 US0_CS #12 US0_CTS #11 US0_RTS #10 US1_TX #15 US1_RX #14 US1_CLK #13 US1_CS #12 US1_CTS #11 US1_RTS #10 LEU0_TX #15 LEU0_RX #14 I2C0_SDA #15 I2C0_SCL #14	CMU_CLK1 #3 PRS_CH0 #12 PRS_CH9 #15 PRS_CH10 #4 PRS_CH11 #3 ACMP0_O #15 ACMP1_O #15 GPIO_EM4WU12		
48	PC11	BUSAY BUSBX	TIM0_CC0 #16 TIM0_CC1 #15 TIM0_CC2 #14 TIM0_CDTI0 #13 TIM0_CDT11 #12 TIM0_CDT12 #11 TIM1_CC0 #16 TIM1_CC1 #15 TIM1_CC2 #14 TIM1_CC3 #13 LE- TIM0_OUT0 #16 LE- TIM0_OUT0 #16 LE- TIM0_OUT1 #15 PCNT0_S0IN #16 PCNT0_S1IN #15	US0_TX #16 US0_RX #15 US0_CLK #14 US0_CS #13 US0_CTS #12 US0_RTS #11 US1_TX #16 US1_RX #15 US1_CLK #14 US1_CS #13 US1_CTS #12 US1_RTS #11 LEU0_TX #16 LEU0_RX #15 I2C0_SDA #16 I2C0_SCL #15	CMU_CLK0 #3 PRS_CH0 #13 PRS_CH9 #16 PRS_CH10 #5 PRS_CH11 #4 ACMP0_O #16 ACMP1_O #16 DBG_SWO #3		

QFN	32 Pin# and Name		Pin Alternate Functi	onality / Description	
Pin #	Pin Name	Analog	Timers	Communication	Other
4	PF3	BUSAY BUSBX	TIM0_CC0 #27 TIM0_CC1 #26 TIM0_CC2 #25 TIM0_CDTI0 #24 TIM0_CDTI1 #23 TIM0_CDTI2 #22 TIM1_CC0 #27 TIM1_CC1 #26 TIM1_CC2 #25 TIM1_CC3 #24 LE- TIM0_OUT0 #27 LE- TIM0_OUT1 #26 PCNT0_S0IN #27 PCNT0_S1IN #26	US0_TX #27 US0_RX #26 US0_CLK #25 US0_CS #24 US0_CTS #23 US0_RTS #22 US1_TX #27 US1_RX #26 US1_CLK #25 US1_CS #24 US1_CTS #23 US1_RTS #22 LEU0_TX #27 LEU0_RX #26 I2C0_SDA #27 I2C0_SCL #26	CMU_CLK1 #6 PRS_CH0 #3 PRS_CH1 #2 PRS_CH2 #1 PRS_CH3 #0 ACMP0_O #27 ACMP1_O #27 DBG_TDI #0
5	PF4	BUSAX BUSBY	TIM0_CC0 #28 TIM0_CC1 #27 TIM0_CC2 #26 TIM0_CDT10 #25 TIM0_CDT11 #24 TIM0_CDT12 #23 TIM1_CC0 #28 TIM1_CC1 #27 TIM1_CC2 #26 TIM1_CC3 #25 LE- TIM0_OUT0 #28 LE- TIM0_OUT0 #28 LE- TIM0_OUT1 #27 PCNT0_S0IN #28 PCNT0_S1IN #27	US0_TX #28 US0_RX #27 US0_CLK #26 US0_CS #25 US0_CTS #24 US0_RTS #23 US1_TX #28 US1_RX #27 US1_CLK #26 US1_CS #25 US1_CTS #24 US1_RTS #23 LEU0_TX #28 LEU0_RX #27 I2C0_SDA #28 I2C0_SCL #27	PRS_CH0 #4 PRS_CH1 #3 PRS_CH2 #2 PRS_CH3 #1 ACMP0_O #28 ACMP1_O #28
6	AVDD_1	Analog power supply 1.			
7	HFXTAL_N	High Frequency Crystal in	put pin.		
8	HFXTAL_P	High Frequency Crystal or	utput pin.		
9	RESETn	Reset input, active low.To during reset, and let the in	apply an external reset so ternal pull-up ensure that r	urce to this pin, it is required eset is released.	d to only drive this pin low
10	PD9	BUSCY BUSDX	TIM0_CC0 #17 TIM0_CC1 #16 TIM0_CC2 #15 TIM0_CDT10 #14 TIM0_CDT11 #13 TIM0_CDT12 #12 TIM1_CC0 #17 TIM1_CC1 #16 TIM1_CC2 #15 TIM1_CC3 #14 LE- TIM0_OUT0 #17 LE- TIM0_OUT0 #17 LE- TIM0_OUT1 #16 PCNT0_S0IN #17 PCNT0_S1IN #16	US0_TX #17 US0_RX #16 US0_CLK #15 US0_CS #14 US0_CTS #13 US0_RTS #12 US1_TX #17 US1_RX #16 US1_CLK #15 US1_CS #14 US1_CTS #13 US1_RTS #12 LEU0_TX #17 LEU0_RX #16 I2C0_SDA #17 I2C0_SCL #16	CMU_CLK0 #4 PRS_CH3 #8 PRS_CH4 #0 PRS_CH5 #6 PRS_CH6 #11 ACMP0_O #17 ACMP1_O #17

QFN	32 Pin# and Name		Pin Alternate Functi	ionality / Description	
Pin #	Pin Name	Analog	Timers	Communication	Other
19	PB11	BUSCY BUSDX	TIM0_CC0 #6 TIM0_CC1 #5 TIM0_CC2 #4 TIM0_CDTI0 #3 TIM0_CDTI1 #2 TIM0_CDTI2 #1 TIM1_CC0 #6 TIM1_CC1 #5 TIM1_CC2 #4 TIM1_CC3 #3 LE- TIM0_OUT0 #6 LE- TIM0_OUT0 #6 LE- TIM0_OUT1 #5 PCNT0_S0IN #6 PCNT0_S1IN #5	US0_TX #6 US0_RX #5 US0_CLK #4 US0_CS #3 US0_CTS #2 US0_RTS #1 US1_TX #6 US1_RX #5 US1_CLK #4 US1_CS #3 US1_CTS #2 US1_RTS #1 LEU0_TX #6 LEU0_RX #5 I2C0_SDA #6 I2C0_SCL #5	PRS_CH6 #6 PRS_CH7 #5 PRS_CH8 #4 PRS_CH9 #3 ACMP0_O #6 ACMP1_O #6
20	PB12	BUSCX BUSDY	TIM0_CC0 #7 TIM0_CC1 #6 TIM0_CC2 #5 TIM0_CDTI0 #4 TIM0_CDTI1 #3 TIM0_CDT12 #2 TIM1_CC0 #7 TIM1_CC1 #6 TIM1_CC2 #5 TIM1_CC3 #4 LE- TIM0_OUT0 #7 LE- TIM0_OUT1 #6 PCNT0_S0IN #7 PCNT0_S1IN #6	US0_TX #7 US0_RX #6 US0_CLK #5 US0_CS #4 US0_CTS #3 US0_RTS #2 US1_TX #7 US1_RX #6 US1_CLK #5 US1_CS #4 US1_CTS #3 US1_RTS #2 LEU0_TX #7 LEU0_RX #6 I2C0_SDA #7 I2C0_SCL #6	PRS_CH6 #7 PRS_CH7 #6 PRS_CH8 #5 PRS_CH9 #4 ACMP0_O #7 ACMP1_O #7
21	PB13	BUSCY BUSDX	TIM0_CC0 #8 TIM0_CC1 #7 TIM0_CC2 #6 TIM0_CDTI0 #5 TIM0_CDTI1 #4 TIM0_CDTI2 #3 TIM1_CC0 #8 TIM1_CC1 #7 TIM1_CC2 #6 TIM1_CC3 #5 LE- TIM0_OUT0 #8 LE- TIM0_OUT0 #8 LE- TIM0_OUT1 #7 PCNT0_S0IN #8 PCNT0_S1IN #7	US0_TX #8 US0_RX #7 US0_CLK #6 US0_CS #5 US0_CTS #4 US0_RTS #3 US1_TX #8 US1_RX #7 US1_CLK #6 US1_CS #5 US1_CTS #4 US1_RTS #3 LEU0_TX #8 LEU0_RX #7 I2C0_SDA #8 I2C0_SCL #7	PRS_CH6 #8 PRS_CH7 #7 PRS_CH8 #6 PRS_CH9 #5 ACMP0_O #8 ACMP1_O #8 DBG_SWO #1 GPIO_EM4WU9
22	AVDD_0	Analog power supply 0.			
23	PB14	LFXTAL_N BUSCX BUSDY	TIM0_CC0 #9 TIM0_CC1 #8 TIM0_CC2 #7 TIM0_CDTI0 #6 TIM0_CDTI1 #5 TIM0_CDTI2 #4 TIM1_CC0 #9 TIM1_CC1 #8 TIM1_CC2 #7 TIM1_CC3 #6 LE- TIM0_OUT0 #9 LE- TIM0_OUT0 #9 LE- TIM0_OUT1 #8 PCNT0_S0IN #9 PCNT0_S1IN #8	US0_TX #9 US0_RX #8 US0_CLK #7 US0_CS #6 US0_CTS #5 US0_RTS #4 US1_TX #9 US1_RX #8 US1_CLK #7 US1_CS #6 US1_CTS #5 US1_RTS #4 LEU0_TX #9 LEU0_RX #8 I2C0_SDA #9 I2C0_SCL #8	CMU_CLK1 #1 PRS_CH6 #9 PRS_CH7 #8 PRS_CH8 #7 PRS_CH9 #6 ACMP0_O #9 ACMP1_O #9

QFN32 Pin# and Name		Pin Alternate Functionality / Description								
Pin #	Pin Name	Analog	Timers	Communication	Other					
0	VSS	Ground			1					
1	PF0	BUSAX BUSBY	TIM0_CC0 #24 TIM0_CC1 #23 TIM0_CC2 #22 TIM0_CDTI0 #21 TIM0_CDTI1 #20 TIM0_CDTI2 #19 TIM1_CC0 #24 TIM1_CC1 #23 TIM1_CC2 #22 TIM1_CC3 #21 LE- TIM0_OUT0 #24 LE- TIM0_OUT1 #23 PCNT0_S0IN #24 PCNT0_S1IN #23	US0_TX #24 US0_RX #23 US0_CLK #22 US0_CS #21 US0_CTS #20 US0_RTS #19 US1_TX #24 US1_RX #23 US1_CLK #22 US1_CS #21 US1_CTS #20 US1_RTS #19 LEU0_TX #24 LEU0_RX #23 I2C0_SDA #24 I2C0_SCL #23	PRS_CH0 #0 PRS_CH1 #7 PRS_CH2 #6 PRS_CH3 #5 ACMP0_O #24 ACMP1_O #24 DBG_SWCLKTCK #0 BOOT_TX					
2	PF1	BUSAY BUSBX	TIM0_CC0 #25 TIM0_CC1 #24 TIM0_CC2 #23 TIM0_CDTI0 #22 TIM0_CDTI1 #21 TIM0_CDTI2 #20 TIM1_CC0 #25 TIM1_CC1 #24 TIM1_CC2 #23 TIM1_CC3 #22 LE- TIM0_OUT0 #25 LE- TIM0_OUT1 #24 PCNT0_S0IN #25 PCNT0_S1IN #24	US0_TX #25 US0_RX #24 US0_CLK #23 US0_CS #22 US0_CTS #21 US0_RTS #20 US1_TX #25 US1_RX #24 US1_CLK #23 US1_CS #22 US1_CTS #21 US1_RTS #20 LEU0_TX #25 LEU0_RX #24 I2C0_SDA #25 I2C0_SCL #24	PRS_CH0 #1 PRS_CH1 #0 PRS_CH2 #7 PRS_CH3 #6 ACMP0_O #25 ACMP1_O #25 DBG_SWDIOTMS #0 BOOT_RX					
3	PF2	BUSAX BUSBY	TIM0_CC0 #26 TIM0_CC1 #25 TIM0_CC2 #24 TIM0_CDTI0 #23 TIM0_CDTI1 #22 TIM0_CDTI2 #21 TIM1_CC0 #26 TIM1_CC1 #25 TIM1_CC2 #24 TIM1_CC3 #23 LE- TIM0_OUT0 #26 LE- TIM0_OUT1 #25 PCNT0_S0IN #26 PCNT0_S1IN #25	US0_TX #26 US0_RX #25 US0_CLK #24 US0_CS #23 US0_CTS #22 US0_RTS #21 US1_TX #26 US1_RX #25 US1_CLK #24 US1_CS #23 US1_CTS #22 US1_RTS #21 LEU0_TX #26 LEU0_RX #25 I2C0_SDA #26 I2C0_SCL #25	CMU_CLK0 #6 PRS_CH0 #2 PRS_CH1 #1 PRS_CH2 #0 PRS_CH3 #7 ACMP0_O #26 ACMP1_O #26 DBG_TDO #0 DBG_SWO #0 GPIO_EM4WU0					

Table 6.5. QFN32 with DC-DC Device Pinout

6.3.1 EFM32PG1 QFN32 with DC-DC GPIO Overview

The GPIO pins are organized as 16-bit ports indicated by letters (A, B, C...), and the individual pins on each port are indicated by a number from 15 down to 0.

Port	Pin 15	Pin 14	Pin 13	Pin 12	Pin 11	Pin 10	Pin 9	Pin 8	Pin 7	Pin 6	Pin 5	Pin 4	Pin 3	Pin 2	Pin 1	Pin 0
Port A	-	-	-	-	-	-	-	-	-	-	-	-	-	-	PA1	PA0
Port B	PB15	PB14	PB13 (5V)	PB12 (5V)	PB11 (5V)	-	-	-	-	-	-	-	-	-	-	-
Port C	-	-	-	-	PC11 (5V)	PC10 (5V)	-	-	-	-	-	-	-	-	-	-
Port D	PD15 (5V)	PD14 (5V)	PD13 (5V)	PD12 (5V)	PD11 (5V)	PD10 (5V)	PD9 (5V)	-	-	-	-	-	-	-	-	-
Port F	-	-	-	-	-	-	-	-	-	-	-	-	PF3 (5V)	PF2 (5V)	PF1 (5V)	PF0 (5V)

Table 6.6. QFN32 with DC-DC GPIO Pinout

Note:

1. GPIO with 5V tolerance are indicated by (5V).

2. The pins PB13, PB12, PB11, PD15, PD14, and PD13 will not be 5V tolerant on all future devices. In order to preserve upgrade options with full hardware compatibility, do not use these pins with 5V domains.

Alternate	LOCATION										
Functionality	0 - 3	4 - 7	8 - 11	12 - 15	16 - 19	20 - 23	24 - 27	28 - 31	Description		
TIM0_CC2	0: PA2 1: PA3 2: PA4 3: PA5	4: PB11 5: PB12 6: PB13 7: PB14	8: PB15 9: PC6 10: PC7 11: PC8	12: PC9 13: PC10 14: PC11 15: PD9	16: PD10 17: PD11 18: PD12 19: PD13	20: PD14 21: PD15 22: PF0 23: PF1	24: PF2 25: PF3 26: PF4 27: PF5	28: PF6 29: PF7 30: PA0 31: PA1	Timer 0 Capture Compare input / output channel 2.		
TIM0_CDTI0	0: PA3 1: PA4 2: PA5 3: PB11	4: PB12 5: PB13 6: PB14 7: PB15	8: PC6 9: PC7 10: PC8 11: PC9	12: PC10 13: PC11 14: PD9 15: PD10	16: PD11 17: PD12 18: PD13 19: PD14	20: PD15 21: PF0 22: PF1 23: PF2	24: PF3 25: PF4 26: PF5 27: PF6	28: PF7 29: PA0 30: PA1 31: PA2	Timer 0 Compli- mentary Dead Time Insertion channel 0.		
TIM0_CDTI1	0: PA4 1: PA5 2: PB11 3: PB12	4: PB13 5: PB14 6: PB15 7: PC6	8: PC7 9: PC8 10: PC9 11: PC10	12: PC11 13: PD9 14: PD10 15: PD11	16: PD12 17: PD13 18: PD14 19: PD15	20: PF0 21: PF1 22: PF2 23: PF3	24: PF4 25: PF5 26: PF6 27: PF7	28: PA0 29: PA1 30: PA2 31: PA3	Timer 0 Compli- mentary Dead Time Insertion channel 1.		
TIM0_CDTI2	0: PA5 1: PB11 2: PB12 3: PB13	4: PB14 5: PB15 6: PC6 7: PC7	8: PC8 9: PC9 10: PC10 11: PC11	12: PD9 13: PD10 14: PD11 15: PD12	16: PD13 17: PD14 18: PD15 19: PF0	20: PF1 21: PF2 22: PF3 23: PF4	24: PF5 25: PF6 26: PF7 27: PA0	28: PA1 29: PA2 30: PA3 31: PA4	Timer 0 Compli- mentary Dead Time Insertion channel 2.		
TIM1_CC0	0: PA0 1: PA1 2: PA2 3: PA3	4: PA4 5: PA5 6: PB11 7: PB12	8: PB13 9: PB14 10: PB15 11: PC6	12: PC7 13: PC8 14: PC9 15: PC10	16: PC11 17: PD9 18: PD10 19: PD11	20: PD12 21: PD13 22: PD14 23: PD15	24: PF0 25: PF1 26: PF2 27: PF3	28: PF4 29: PF5 30: PF6 31: PF7	Timer 1 Capture Compare input / output channel 0.		
TIM1_CC1	0: PA1 1: PA2 2: PA3 3: PA4	4: PA5 5: PB11 6: PB12 7: PB13	8: PB14 9: PB15 10: PC6 11: PC7	12: PC8 13: PC9 14: PC10 15: PC11	16: PD9 17: PD10 18: PD11 19: PD12	20: PD13 21: PD14 22: PD15 23: PF0	24: PF1 25: PF2 26: PF3 27: PF4	28: PF5 29: PF6 30: PF7 31: PA0	Timer 1 Capture Compare input / output channel 1.		
TIM1_CC2	0: PA2 1: PA3 2: PA4 3: PA5	4: PB11 5: PB12 6: PB13 7: PB14	8: PB15 9: PC6 10: PC7 11: PC8	12: PC9 13: PC10 14: PC11 15: PD9	16: PD10 17: PD11 18: PD12 19: PD13	20: PD14 21: PD15 22: PF0 23: PF1	24: PF2 25: PF3 26: PF4 27: PF5	28: PF6 29: PF7 30: PA0 31: PA1	Timer 1 Capture Compare input / output channel 2.		
TIM1_CC3	0: PA3 1: PA4 2: PA5 3: PB11	4: PB12 5: PB13 6: PB14 7: PB15	8: PC6 9: PC7 10: PC8 11: PC9	12: PC10 13: PC11 14: PD9 15: PD10	16: PD11 17: PD12 18: PD13 19: PD14	20: PD15 21: PF0 22: PF1 23: PF2	24: PF3 25: PF4 26: PF5 27: PF6	28: PF7 29: PA0 30: PA1 31: PA2	Timer 1 Capture Compare input / output channel 3.		
US0_CLK	0: PA2 1: PA3 2: PA4 3: PA5	4: PB11 5: PB12 6: PB13 7: PB14	8: PB15 9: PC6 10: PC7 11: PC8	12: PC9 13: PC10 14: PC11 15: PD9	16: PD10 17: PD11 18: PD12 19: PD13	20: PD14 21: PD15 22: PF0 23: PF1	24: PF2 25: PF3 26: PF4 27: PF5	28: PF6 29: PF7 30: PA0 31: PA1	USART0 clock in- put / output.		
US0_CS	0: PA3 1: PA4 2: PA5 3: PB11	4: PB12 5: PB13 6: PB14 7: PB15	8: PC6 9: PC7 10: PC8 11: PC9	12: PC10 13: PC11 14: PD9 15: PD10	16: PD11 17: PD12 18: PD13 19: PD14	20: PD15 21: PF0 22: PF1 23: PF2	24: PF3 25: PF4 26: PF5 27: PF6	28: PF7 29: PA0 30: PA1 31: PA2	USART0 chip se- lect input / output.		
US0_CTS	0: PA4 1: PA5 2: PB11 3: PB12	4: PB13 5: PB14 6: PB15 7: PC6	8: PC7 9: PC8 10: PC9 11: PC10	12: PC11 13: PD9 14: PD10 15: PD11	16: PD12 17: PD13 18: PD14 19: PD15	20: PF0 21: PF1 22: PF2 23: PF3	24: PF4 25: PF5 26: PF6 27: PF7	28: PA0 29: PA1 30: PA2 31: PA3	USART0 Clear To Send hardware flow control input.		
US0_RTS	0: PA5 1: PB11 2: PB12 3: PB13	4: PB14 5: PB15 6: PC6 7: PC7	8: PC8 9: PC9 10: PC10 11: PC11	12: PD9 13: PD10 14: PD11 15: PD12	16: PD13 17: PD14 18: PD15 19: PF0	20: PF1 21: PF2 22: PF3 23: PF4	24: PF5 25: PF6 26: PF7 27: PA0	28: PA1 29: PA2 30: PA3 31: PA4	USART0 Request To Send hardware flow control output.		

8.2 QFN32 PCB Land Pattern



Figure 8.2. QFN32 PCB Land Pattern Drawing





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