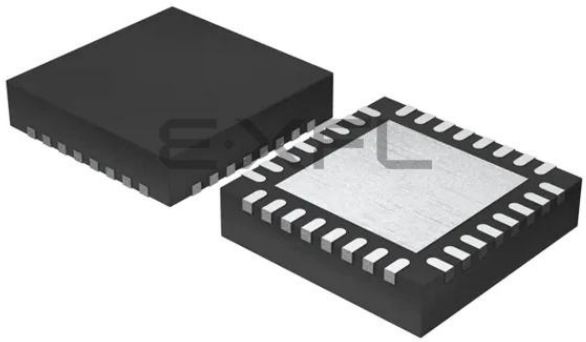
Silicon Labs - EFM32PG1B200F256GM32-B0R Datasheet



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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	I²C, IrDA, LINbus, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	20
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.85V ~ 3.8V
Data Converters	A/D 20x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-VFQFN Exposed Pad
Supplier Device Package	32-QFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32pg1b200f256gm32-b0r

3.6.3 Inter-Integrated Circuit Interface (I^2C)

The I^2C module provides an interface between the MCU and a serial I^2C bus. It is capable of acting as both a master and a slave and supports multi-master buses. Standard-mode, fast-mode and fast-mode plus speeds are supported, allowing transmission rates from 10 kbit/s up to 1 Mbit/s. Slave arbitration and timeouts are also available, allowing implementation of an SMBus-compliant system. The interface provided to software by the I^2C module allows precise timing control of the transmission process and highly automated transfers. Automatic recognition of slave addresses is provided in active and low energy modes.

3.6.4 Peripheral Reflex System (PRS)

The Peripheral Reflex System provides a communication network between different peripheral modules without software involvement. Peripheral modules producing Reflex signals are called producers. The PRS routes Reflex signals from producers to consumer peripherals which in turn perform actions in response. Edge triggers and other functionality can be applied by the PRS. The PRS allows peripheral to act autonomously without waking the MCU core, saving power.

3.7 Security Features

3.7.1 GPCRC (General Purpose Cyclic Redundancy Check)

The GPCRC module implements a Cyclic Redundancy Check (CRC) function. It supports both 32-bit and 16-bit polynomials. The supported 32-bit polynomial is 0x04C11DB7 (IEEE 802.3), while the 16-bit polynomial can be programmed to any value, depending on the needs of the application.

3.7.2 Crypto Accelerator (CRYPTO)

The Crypto Accelerator is a fast and energy-efficient autonomous hardware encryption and decryption accelerator. EFM32PG1 devices support AES encryption and decryption with 128- or 256-bit keys, ECC over both GF(P) and GF(2^m), and SHA-1 and SHA-2 (SHA-224 and SHA-256).

Supported block cipher modes of operation for AES include: ECB, CTR, CBC, PCBC, CFB, OFB, GCM, CBC-MAC, GMAC and CCM.

Supported ECC NIST recommended curves include P-192, P-224, P-256, K-163, K-233, B-163 and B-233.

The CRYPTO module allows fast processing of GCM (AES), ECC and SHA with little CPU intervention. CRYPTO also provides trigger signals for DMA read and write operations.

3.8 Analog

3.8.1 Analog Port (APORT)

The Analog Port (APORT) is an analog interconnect matrix allowing access to many analog modules on a flexible selection of pins. Each APORT bus consists of analog switches connected to a common wire. Since many clients can operate differentially, buses are grouped by X/Y pairs.

3.8.2 Analog Comparator (ACMP)

The Analog Comparator is used to compare the voltage of two analog inputs, with a digital output indicating which input voltage is higher. Inputs are selected from among internal references and external pins. The tradeoff between response time and current consumption is configurable by software. Two 6-bit reference dividers allow for a wide range of internally-programmable reference sources. The ACMP can also be used to monitor the supply voltage. An interrupt can be generated when the supply falls below or rises above the programmable threshold.

3.8.3 Analog to Digital Converter (ADC)

The ADC is a Successive Approximation Register (SAR) architecture, with a resolution of up to 12 bits at up to 1 Msps. The output sample resolution is configurable and additional resolution is possible using integrated hardware for averaging over multiple samples. The ADC includes integrated voltage references and an integrated temperature sensor. Inputs are selectable from a wide range of sources, including pins configurable as either single-ended or differential.

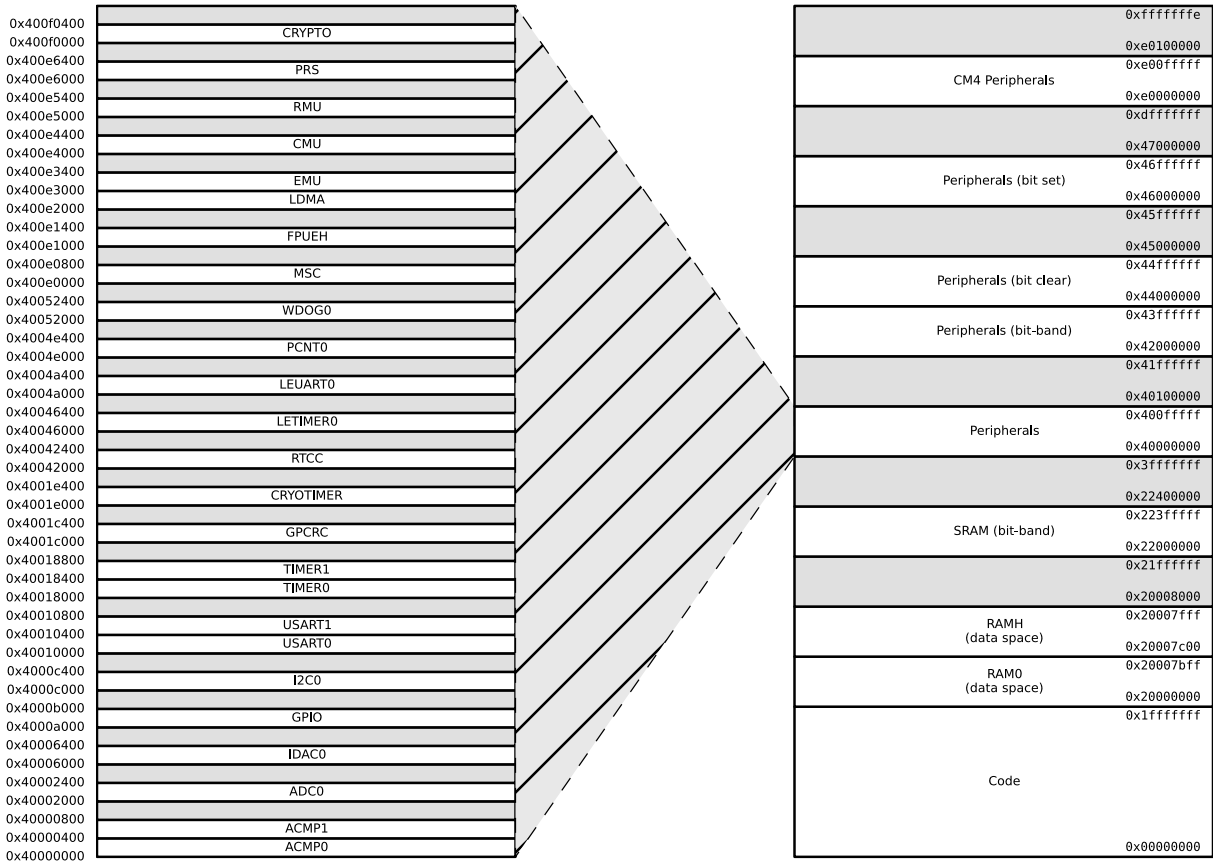

Figure 3.3. EFM32PG1 Memory Map — Peripherals

3.12 Configuration Summary

The features of the EFM32PG1 are a subset of the feature set described in the device reference manual. The table below describes device specific implementation of the features. Remaining modules support full configuration.

Table 3.1. Configuration Summary

Module	Configuration	Pin Connections
USART0	IrDA SmartCard	US0_TX, US0_RX, US0_CLK, US0_CS
USART1	IrDA I^2S SmartCard	US1_TX, US1_RX, US1_CLK, US1_CS
TIMER0	with DTI	TIM0_CC[2:0], TIM0_CDTI[2:0]
TIMER1		TIM1_CC[3:0]

4. Electrical Specifications

4.1 Electrical Characteristics

All electrical parameters in all tables are specified under the following conditions, unless stated otherwise:

- Typical values are based on T_{AMB}=25 °C and V_{DD}= 3.3 V, by production test and/or technology characterization.
- Minimum and maximum values represent the worst conditions across supply voltage, process variation, and operating temperature, unless stated otherwise.

Refer to Table 4.2 General Operating Conditions on page 11 for more details about operational supply and temperature limits.

4.1.1 Absolute Maximum Ratings

Stresses above those listed below may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. For more information on the available quality and reliability data, see the Quality and Reliability Monitor Report at http://www.silabs.com/support/quality/pages/default.aspx.

Table 4.1. Absolute Maximum Ratings

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Storage temperature range	T_{STG}		-50	—	150	°C
External main supply voltage	V_{DDMAX}		0	—	3.8	V
External main supply voltage ramp rate	$V_{DDRAMPMAX}$		—	—	1	V / µs
Voltage on any 5V tolerant GPIO pin[1]	V_{DIGPIN}		-0.3	—	Min of 5.25 and IOVDD +2	V
Voltage on non-5V tolerant GPIO pins			-0.3	—	IOVDD+0.3	V
Voltage on HFXO pins	$V_{HFXOPIN}$		-0.3	—	1.4	V
Total current into VDD power lines (source)	I_{VDDMAX}		—	—	200	mA
Total current into VSS ground lines (sink)	I_{VSSMAX}		—	—	200	mA
Current per I/O pin (sink)	I_{IOMAX}		—	—	50	mA
Current per I/O pin (source)			—	—	50	mA
Current for all I/O pins (sink)	$I_{IOALLMAX}$		—	—	200	mA
Current for all I/O pins (source)			—	—	200	mA
Voltage difference between AVDD and VREGVDD	ΔV_{DD}		—	—	0.3	V
Junction Temperature for -G grade devices	T_J		-40	—	105	°C
Junction Temperature for -I grade devices			-40	—	125	°C

Note:

1. When a GPIO pin is routed to the analog module through the APORT, the maximum voltage = IOVDD.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM4S Shutoff mode	I_{EM4S}	no RAM retention, no RTCC	—	0.04	—	µA

Note:

1. DCDC Low Noise DCM Mode = Light Drive (PFETCNT=NFETCNT=3), F=3.0 MHz (RCOBAND=0), ANASW=DVDD
2. CMU_HFXOCTRL_LOWPOWER=1
3. DCDC Low Noise CCM Mode = Light Drive (PFETCNT=NFETCNT=3), F=6.4 MHz (RCOBAND=4), ANASW=DVDD
4. DCDC Low Power Mode = Medium Drive (PFETCNT=NFETCNT=7), LPOSCDIV=1, LPBIAS=3, LPCILIMSEL=1, ANASW=DVDD

4.1.5.3 Current Consumption 1.85 V without DC-DC Converter

Unless otherwise indicated, typical conditions are: VREGVDD = AVDD = DVDD = 1.85 V. T_{OP} = 25 °C. EMU_PWRCFG_PWRCG=NODCDC. EMU_DCDCCTRL_DCDCMODE=BYPASS. Minimum and maximum values in this table represent the worst conditions across supply voltage and process variation at T_{OP} = 25 °C. See Figure 5.1 EFM32PG1 Typical Application Circuit, Direct Supply, No DC-DC Converter on page 47.

Table 4.7. Current Consumption 1.85V without DC/DC

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM0 Active mode with all peripherals disabled	I_{ACTIVE}	38.4 MHz crystal, CPU running while loop from flash[1]	—	127	—	µA/MHz
		38 MHz HFRCO, CPU running Prime from flash	—	88	—	µA/MHz
		38 MHz HFRCO, CPU running while loop from flash	—	100	—	µA/MHz
		38 MHz HFRCO, CPU running CoreMark from flash	—	112	—	µA/MHz
		26 MHz HFRCO, CPU running while loop from flash	—	102	—	µA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	220	—	µA/MHz
Current consumption in EM1 Sleep mode with all peripherals disabled	I_{EM1}	38.4 MHz crystal[1]	—	61	—	µA/MHz
		38 MHz HFRCO	—	35	—	µA/MHz
		26 MHz HFRCO	—	37	—	µA/MHz
		1 MHz HFRCO	—	154	—	µA/MHz
Current consumption in EM2 Deep Sleep mode	I_{EM2}	Full RAM retention and RTCC running from LFXO	—	3.2	—	µA
		4 kB RAM retention and RTCC running from LFRCO	—	2.8	—	µA
Current consumption in EM3 Stop mode	I_{EM3}	Full RAM retention and CRYOTIMER running from ULFRCO	—	2.7	—	µA
Current consumption in EM4H Hibernate mode	I_{EM4}	128 byte RAM retention, RTCC running from LFXO	—	1	—	µA
		128 byte RAM retention, CRYOTIMER running from ULFRCO	—	0.62	—	µA
		128 byte RAM retention, no RTCC	—	0.62	—	µA
Current consumption in EM4S Shutoff mode	I_{EM4S}	No RAM retention, no RTCC	—	0.02	—	µA

Note:
1. CMU_HFXOCTRL_LOWPOWER=1

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current from all supplies, using internal reference buffer. Duty-cycled operation. WARMUPMODE[2] = NORMAL	$I_{ADC\_NORMAL\_HP}$	35 ksps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 0 [3]	—	102	—	µA
		5 ksps / 16 MHz ADCCLK BIASPROG = 0, GPBIASACC = 0 [3]	—	17	—	µA
Current from all supplies, using internal reference buffer. Duty-cycled operation. AWARMUPMODE[2] = KEEPINSTANDBY or KEEPINSLOWACC	$I_{ADC\_STANDBY\_HP}$	125 ksps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 0 [3]	—	162	—	µA
		35 ksps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 0 [3]	—	123	—	µA
Current from HFPERCLK	I_{ADC_CLK}	HFPERCLK = 16 MHz	—	140	—	µA
ADC Clock Frequency	f_{ADCCLK}		—	—	16	MHz
Throughput rate	$f_{ADCRATE}$		—	—	1	Msps
Conversion time[4]	$t_{ADCCONV}$	6 bit	—	7	—	cycles
		8 bit	—	9	—	cycles
		12 bit	—	13	—	cycles
Startup time of reference generator and ADC core	$t_{ADCSTART}$	WARMUPMODE[2] = NORMAL	—	—	5	µs
		WARMUPMODE[2] = KEEPINSTANDBY	—	—	2	µs
		WARMUPMODE[2] = KEEPINSLOWACC	—	—	1	µs
SNDR at 1Msps and f_{in} = 10kHz	$SNDR_{ADC}$	Internal reference, 2.5 V full-scale, differential (-1.25, 1.25)	58	67	—	dB
		vrefp_in = 1.25 V direct mode with 2.5 V full-scale, differential	—	68	—	dB
Spurious-Free Dynamic Range (SFDR)	$SFDR_{ADC}$	1 MSamples/s, 10 kHz full-scale sine wave	—	75	—	dB
Input referred ADC noise, rms	V_{REF_NOISE}	Including quantization noise and distortion	—	380	—	µV
Offset Error	$V_{ADCOFFSETERR}$		-3	0.25	3	LSB
Gain error in ADC	V_{ADC_GAIN}	Using internal reference	—	-0.2	5	%
		Using external reference	—	-1	—	%
Differential non-linearity (DNL)	DNL_{ADC}	12 bit resolution, No Missing Codes	-1	—	2	LSB
Integral non-linearity (INL), End point method	INL_{ADC}	12 bit resolution	-6	—	6	LSB
Temperature Sensor Slope	V_{TS_SLOPE}		—	-1.84	—	mV/°C

SPI Slave Timing

Table 4.25. SPI Slave Timing

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCKL period [1] [2]	t_{SCLK_sl}		2 * $t_{HFPERCLK}$	—	—	ns
SCLK high period[1] [2]	t_{SCLK_hi}		3 * $t_{HFPERCLK}$	—	—	ns
SCLK low period [1] [2]	t_{SCLK_lo}		3 * $t_{HFPERCLK}$	—	—	ns
CS active to MISO [1] [2]	$t_{CS\_ACT\_MI}$		4	—	50	ns
CS disable to MISO [1] [2]	$t_{CS\_DIS\_MI}$		4	—	50	ns
MOSI setup time [1] [2]	t_{SU_MO}		4	—	—	ns
MOSI hold time [1] [2]	t_{H_MO}		3 + 2 * $t_{HFPERCLK}$	—	—	ns
SCLK to MISO [1] [2]	t_{SCLK_MI}		16 + $t_{HFPERCLK}$	—	66 + 2 * $t_{HFPERCLK}$	ns

Note:
1. Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0)
2. Measurement done with 8 pF output loading at 10% and 90% of V_{DD} (figure shows 50% of V_{DD})

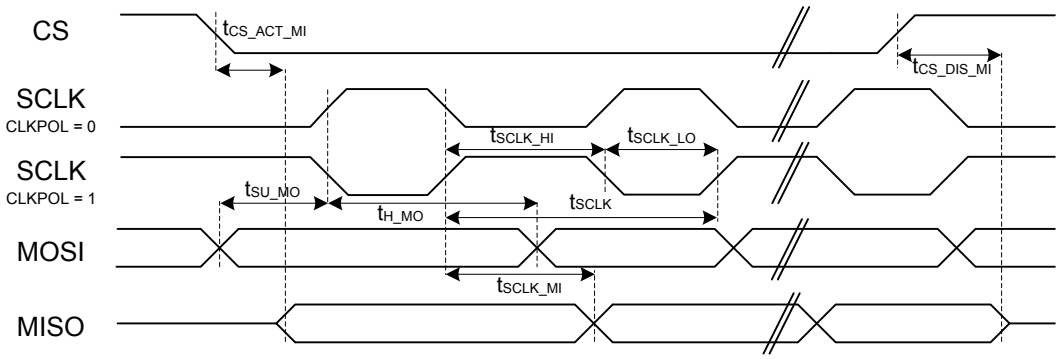

Figure 4.2. SPI Slave Timing Diagram

4.2 Typical Performance Curves

Typical performance curves indicate typical characterized performance under the stated conditions.

4.2.1 Supply Current

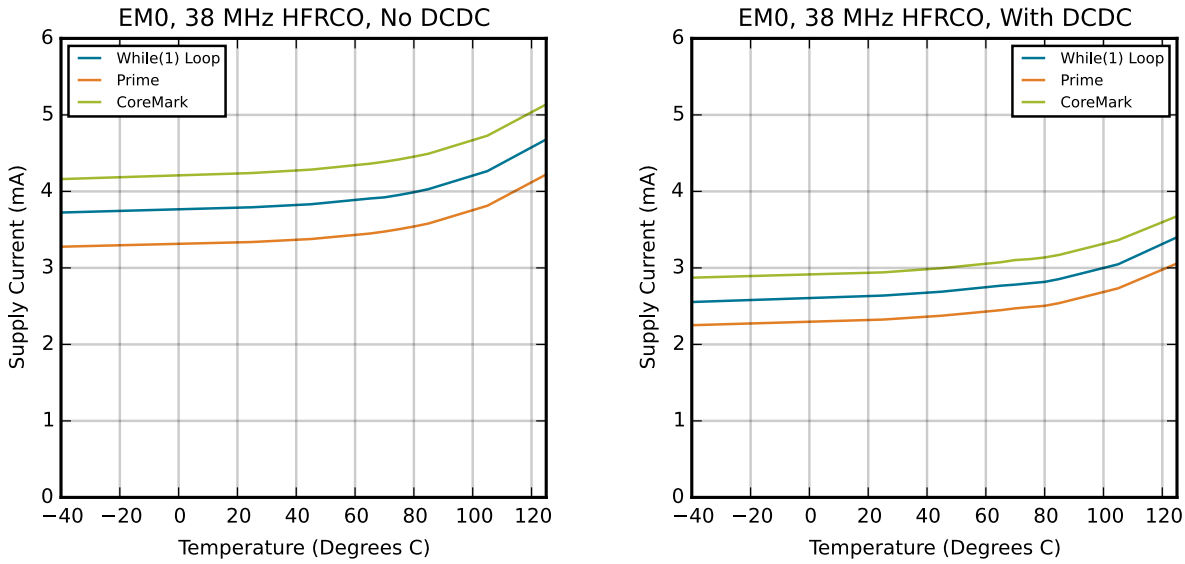

Figure 4.3. EM0 Active Mode Typical Supply Current

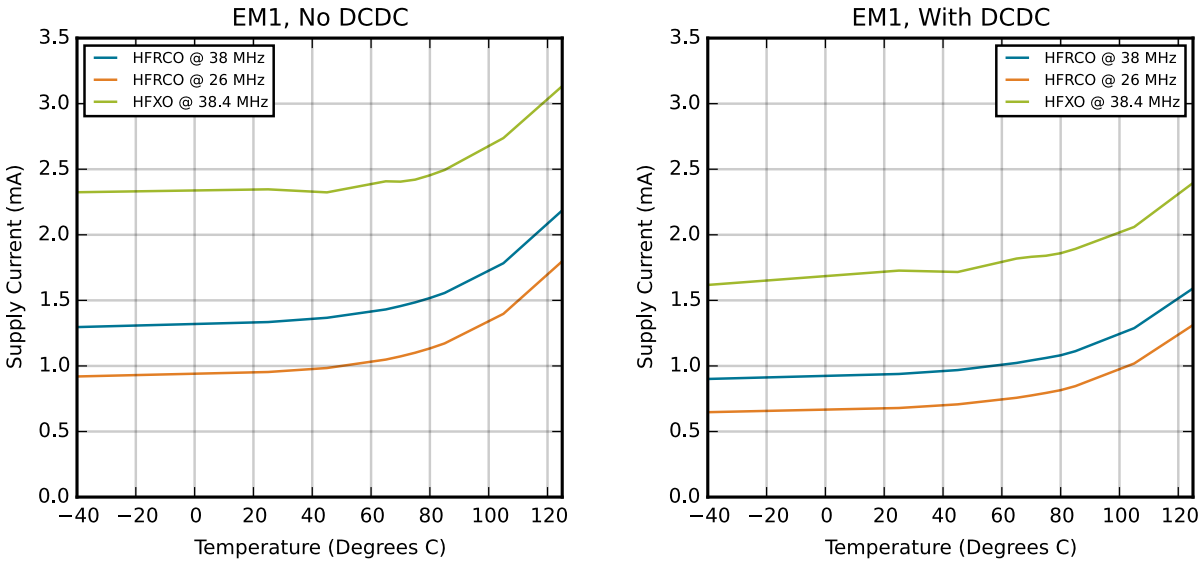

Figure 4.4. EM1 Sleep Mode Typical Supply Current

Typical supply current for EM2, EM3 and EM4H using standard software libraries from Silicon Laboratories.

6. Pin Definitions

6.1 EFM32PG1 QFN48 with DC-DC Definition

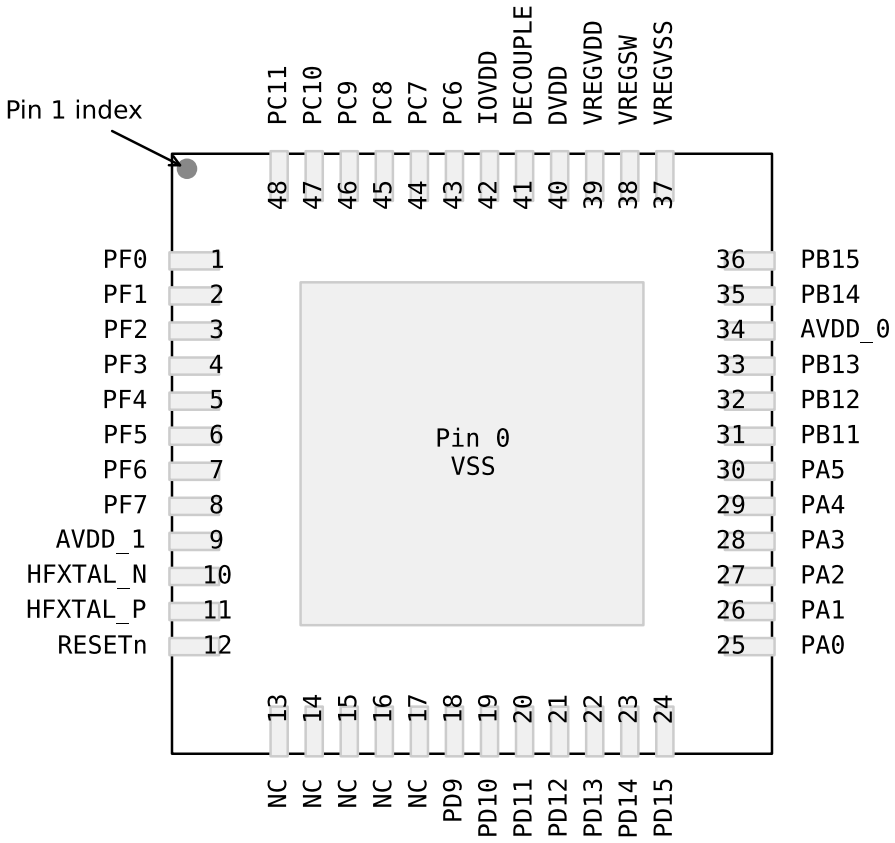

Figure 6.1. EFM32PG1 QFN48 with DC-DC Pinout

Table 6.1. QFN48 with DC-DC Device Pinout

QFN48 Pin# and Name		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
0	RFVSS	Radio Ground			
1	PF0	BUSAX BUSBY	TIM0_CC0 #24 TIM0_CC1 #23 TIM0_CC2 #22 TIM0_CDTI0 #21 TIM0_CDTI1 #20 TIM0_CDTI2 #19 TIM1_CC0 #24 TIM1_CC1 #23 TIM1_CC2 #22 TIM1_CC3 #21 LE- TIM0_OUT0 #24 LE- TIM0_OUT1 #23 PCNT0_S0IN #24 PCNT0_S1IN #23	US0_TX #24 US0_RX #23 US0_CLK #22 US0_CS #21 US0_CTS #20 US0_RTS #19 US1_TX #24 US1_RX #23 US1_CLK #22 US1_CS #21 US1_CTS #20 US1_RTS #19 LEU0_TX #24 LEU0_RX #23 I2C0_SDA #24 I2C0_SCL #23	PRS_CH0 #0 PRS_CH1 #7 PRS_CH2 #6 PRS_CH3 #5 ACMP0_O #24 ACMP1_O #24 DBG_SWCLKTCK #0 BOOT_TX
2	PF1	BUSAY BUSBX	TIM0_CC0 #25 TIM0_CC1 #24 TIM0_CC2 #23 TIM0_CDTI0 #22 TIM0_CDTI1 #21 TIM0_CDTI2 #20 TIM1_CC0 #25 TIM1_CC1 #24 TIM1_CC2 #23 TIM1_CC3 #22 LE- TIM0_OUT0 #25 LE- TIM0_OUT1 #24 PCNT0_S0IN #25 PCNT0_S1IN #24	US0_TX #25 US0_RX #24 US0_CLK #23 US0_CS #22 US0_CTS #21 US0_RTS #20 US1_TX #25 US1_RX #24 US1_CLK #23 US1_CS #22 US1_CTS #21 US1_RTS #20 LEU0_TX #25 LEU0_RX #24 I2C0_SDA #25 I2C0_SCL #24	PRS_CH0 #1 PRS_CH1 #0 PRS_CH2 #7 PRS_CH3 #6 ACMP0_O #25 ACMP1_O #25 DBG_SWDIOTMS #0 BOOT_RX
3	PF2	BUSAX BUSBY	TIM0_CC0 #26 TIM0_CC1 #25 TIM0_CC2 #24 TIM0_CDTI0 #23 TIM0_CDTI1 #22 TIM0_CDTI2 #21 TIM1_CC0 #26 TIM1_CC1 #25 TIM1_CC2 #24 TIM1_CC3 #23 LE- TIM0_OUT0 #26 LE- TIM0_OUT1 #25 PCNT0_S0IN #26 PCNT0_S1IN #25	US0_TX #26 US0_RX #25 US0_CLK #24 US0_CS #23 US0_CTS #22 US0_RTS #21 US1_TX #26 US1_RX #25 US1_CLK #24 US1_CS #23 US1_CTS #22 US1_RTS #21 LEU0_TX #26 LEU0_RX #25 I2C0_SDA #26 I2C0_SCL #25	CMU_CLK0 #6 PRS_CH0 #2 PRS_CH1 #1 PRS_CH2 #0 PRS_CH3 #7 ACMP0_O #26 ACMP1_O #26 DBG_TDO #0 DBG_SWO #0 GPIO_EM4WU0

QFN48 Pin# and Name		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
8	PF7	BUSAY BUSBX	TIM0_CC0 #31 TIM0_CC1 #30 TIM0_CC2 #29 TIM0_CDTI0 #28 TIM0_CDTI1 #27 TIM0_CDTI2 #26 TIM1_CC0 #31 TIM1_CC1 #30 TIM1_CC2 #29 TIM1_CC3 #28 LE-TIM0_OUT0 #31 LE-TIM0_OUT1 #30 PCNT0_S0IN #31 PCNT0_S1IN #30	US0_TX #31 US0_RX #30 US0_CLK #29 US0_CS #28 US0_CTS #27 US0_RTS #26 US1_TX #31 US1_RX #30 US1_CLK #29 US1_CS #28 US1_CTS #27 US1_RTS #26 LEU0_TX #31 LEU0_RX #30 I2C0_SDA #31 I2C0_SCL #30	CMU_CLK0 #7 PRS_CH0 #7 PRS_CH1 #6 PRS_CH2 #5 PRS_CH3 #4 ACMP0_O #31 ACMP1_O #31 GPIO_EM4WU1
9	AVDD_1	Analog power supply 1.			
10	HFXTAL_N	High Frequency Crystal input pin.			
11	HFXTAL_P	High Frequency Crystal output pin.			
12	RESETn	Reset input, active low.To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.			
13	NC	No Connect.			
14	NC	No Connect.			
15	NC	No Connect.			
16	NC	No Connect.			
17	NC	No Connect.			
18	PD9	BUSCY BUSDX	TIM0_CC0 #17 TIM0_CC1 #16 TIM0_CC2 #15 TIM0_CDTI0 #14 TIM0_CDTI1 #13 TIM0_CDTI2 #12 TIM1_CC0 #17 TIM1_CC1 #16 TIM1_CC2 #15 TIM1_CC3 #14 LE-TIM0_OUT0 #17 LE-TIM0_OUT1 #16 PCNT0_S0IN #17 PCNT0_S1IN #16	US0_TX #17 US0_RX #16 US0_CLK #15 US0_CS #14 US0_CTS #13 US0_RTS #12 US1_TX #17 US1_RX #16 US1_CLK #15 US1_CS #14 US1_CTS #13 US1_RTS #12 LEU0_TX #17 LEU0_RX #16 I2C0_SDA #17 I2C0_SCL #16	CMU_CLK0 #4 PRS_CH3 #8 PRS_CH4 #0 PRS_CH5 #6 PRS_CH6 #11 ACMP0_O #17 ACMP1_O #17
19	PD10	BUSCX BUSDY	TIM0_CC0 #18 TIM0_CC1 #17 TIM0_CC2 #16 TIM0_CDTI0 #15 TIM0_CDTI1 #14 TIM0_CDTI2 #13 TIM1_CC0 #18 TIM1_CC1 #17 TIM1_CC2 #16 TIM1_CC3 #15 LE-TIM0_OUT0 #18 LE-TIM0_OUT1 #17 PCNT0_S0IN #18 PCNT0_S1IN #17	US0_TX #18 US0_RX #17 US0_CLK #16 US0_CS #15 US0_CTS #14 US0_RTS #13 US1_TX #18 US1_RX #17 US1_CLK #16 US1_CS #15 US1_CTS #14 US1_RTS #13 LEU0_TX #18 LEU0_RX #17 I2C0_SDA #18 I2C0_SCL #17	CMU_CLK1 #4 PRS_CH3 #9 PRS_CH4 #1 PRS_CH5 #0 PRS_CH6 #12 ACMP0_O #18 ACMP1_O #18

QFN48 Pin# and Name		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
37	VREGVSS	Voltage regulator VSS			
38	VREGSW	DCDC regulator switching node			
39	VREGVDD	Voltage regulator VDD input			
40	DVDD	Digital power supply.			
41	DECOUPLE	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin.			
42	IOVDD	Digital IO power supply.			
43	PC6	BUSAX BUSBY	TIM0_CC0 #11 TIM0_CC1 #10 TIM0_CC2 #9 TIM0_CDTI0 #8 TIM0_CDTI1 #7 TIM0_CDTI2 #6 TIM1_CC0 #11 TIM1_CC1 #10 TIM1_CC2 #9 TIM1_CC3 #8 LE- TIM0_OUT0 #11 LE- TIM0_OUT1 #10 PCNT0_S0IN #11 PCNT0_S1IN #10	US0_TX #11 US0_RX #10 US0_CLK #9 US0_CS #8 US0_CTS #7 US0_RTS #6 US1_TX #11 US1_RX #10 US1_CLK #9 US1_CS #8 US1_CTS #7 US1_RTS #6 LEU0_TX #11 LEU0_RX #10 I2C0_SDA #11 I2C0_SCL #10	CMU_CLK0 #2 PRS_CH0 #8 PRS_CH9 #11 PRS_CH10 #0 PRS_CH11 #5 ACMP0_O #11 ACMP1_O #11
44	PC7	BUSAY BUSBX	TIM0_CC0 #12 TIM0_CC1 #11 TIM0_CC2 #10 TIM0_CDTI0 #9 TIM0_CDTI1 #8 TIM0_CDTI2 #7 TIM1_CC0 #12 TIM1_CC1 #11 TIM1_CC2 #10 TIM1_CC3 #9 LE- TIM0_OUT0 #12 LE- TIM0_OUT1 #11 PCNT0_S0IN #12 PCNT0_S1IN #11	US0_TX #12 US0_RX #11 US0_CLK #10 US0_CS #9 US0_CTS #8 US0_RTS #7 US1_TX #12 US1_RX #11 US1_CLK #10 US1_CS #9 US1_CTS #8 US1_RTS #7 LEU0_TX #12 LEU0_RX #11 I2C0_SDA #12 I2C0_SCL #11	CMU_CLK1 #2 PRS_CH0 #9 PRS_CH9 #12 PRS_CH10 #1 PRS_CH11 #0 ACMP0_O #12 ACMP1_O #12
45	PC8	BUSAX BUSBY	TIM0_CC0 #13 TIM0_CC1 #12 TIM0_CC2 #11 TIM0_CDTI0 #10 TIM0_CDTI1 #9 TIM0_CDTI2 #8 TIM1_CC0 #13 TIM1_CC1 #12 TIM1_CC2 #11 TIM1_CC3 #10 LE- TIM0_OUT0 #13 LE- TIM0_OUT1 #12 PCNT0_S0IN #13 PCNT0_S1IN #12	US0_TX #13 US0_RX #12 US0_CLK #11 US0_CS #10 US0_CTS #9 US0_RTS #8 US1_TX #13 US1_RX #12 US1_CLK #11 US1_CS #10 US1_CTS #9 US1_RTS #8 LEU0_TX #13 LEU0_RX #12 I2C0_SDA #13 I2C0_SCL #12	PRS_CH0 #10 PRS_CH9 #13 PRS_CH10 #2 PRS_CH11 #1 ACMP0_O #13 ACMP1_O #13

QFN48 Pin# and Name		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
46	PC9	BUSAY BUSBX	TIM0_CC0 #14 TIM0_CC1 #13 TIM0_CC2 #12 TIM0_CDTI0 #11 TIM0_CDTI1 #10 TIM0_CDTI2 #9 TIM1_CC0 #14 TIM1_CC1 #13 TIM1_CC2 #12 TIM1_CC3 #11 LE- TIM0_OUT0 #14 LE- TIM0_OUT1 #13 PCNT0_S0IN #14 PCNT0_S1IN #13	US0_TX #14 US0_RX #13 US0_CLK #12 US0_CS #11 US0_CTS #10 US0_RTS #9 US1_TX #14 US1_RX #13 US1_CLK #12 US1_CS #11 US1_CTS #10 US1_RTS #9 LEU0_TX #14 LEU0_RX #13 I2C0_SDA #14 I2C0_SCL #13	PRS_CH0 #11 PRS_CH9 #14 PRS_CH10 #3 PRS_CH11 #2 ACMP0_O #14 ACMP1_O #14
47	PC10	BUSAX BUSBY	TIM0_CC0 #15 TIM0_CC1 #14 TIM0_CC2 #13 TIM0_CDTI0 #12 TIM0_CDTI1 #11 TIM0_CDTI2 #10 TIM1_CC0 #15 TIM1_CC1 #14 TIM1_CC2 #13 TIM1_CC3 #12 LE- TIM0_OUT0 #15 LE- TIM0_OUT1 #14 PCNT0_S0IN #15 PCNT0_S1IN #14	US0_TX #15 US0_RX #14 US0_CLK #13 US0_CS #12 US0_CTS #11 US0_RTS #10 US1_TX #15 US1_RX #14 US1_CLK #13 US1_CS #12 US1_CTS #11 US1_RTS #10 LEU0_TX #15 LEU0_RX #14 I2C0_SDA #15 I2C0_SCL #14	CMU_CLK1 #3 PRS_CH0 #12 PRS_CH9 #15 PRS_CH10 #4 PRS_CH11 #3 ACMP0_O #15 ACMP1_O #15 GPIO_EM4WU12
48	PC11	BUSAY BUSBX	TIM0_CC0 #16 TIM0_CC1 #15 TIM0_CC2 #14 TIM0_CDTI0 #13 TIM0_CDTI1 #12 TIM0_CDTI2 #11 TIM1_CC0 #16 TIM1_CC1 #15 TIM1_CC2 #14 TIM1_CC3 #13 LE- TIM0_OUT0 #16 LE- TIM0_OUT1 #15 PCNT0_S0IN #16 PCNT0_S1IN #15	US0_TX #16 US0_RX #15 US0_CLK #14 US0_CS #13 US0_CTS #12 US0_RTS #11 US1_TX #16 US1_RX #15 US1_CLK #14 US1_CS #13 US1_CTS #12 US1_RTS #11 LEU0_TX #16 LEU0_RX #15 I2C0_SDA #16 I2C0_SCL #15	CMU_CLK0 #3 PRS_CH0 #13 PRS_CH9 #16 PRS_CH10 #5 PRS_CH11 #4 ACMP0_O #16 ACMP1_O #16 DBG_SWO #3

QFN32 Pin# and Name		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
4	PF3	BUSAY BUSBX	TIM0_CC0 #27 TIM0_CC1 #26 TIM0_CC2 #25 TIM0_CDTI0 #24 TIM0_CDTI1 #23 TIM0_CDTI2 #22 TIM1_CC0 #27 TIM1_CC1 #26 TIM1_CC2 #25 TIM1_CC3 #24 LE-TIM0_OUT0 #27 LE-TIM0_OUT1 #26 PCNT0_S0IN #27 PCNT0_S1IN #26	US0_TX #27 US0_RX #26 US0_CLK #25 US0_CS #24 US0_CTS #23 US0_RTS #22 US1_TX #27 US1_RX #26 US1_CLK #25 US1_CS #24 US1_CTS #23 US1_RTS #22 LEU0_TX #27 LEU0_RX #26 I2C0_SDA #27 I2C0_SCL #26	CMU_CLK1 #6 PRS_CH0 #3 PRS_CH1 #2 PRS_CH2 #1 PRS_CH3 #0 ACMP0_O #27 ACMP1_O #27 DBG_TDI #0
5	PF4	BUSAX BUSBY	TIM0_CC0 #28 TIM0_CC1 #27 TIM0_CC2 #26 TIM0_CDTI0 #25 TIM0_CDTI1 #24 TIM0_CDTI2 #23 TIM1_CC0 #28 TIM1_CC1 #27 TIM1_CC2 #26 TIM1_CC3 #25 LE-TIM0_OUT0 #28 LE-TIM0_OUT1 #27 PCNT0_S0IN #28 PCNT0_S1IN #27	US0_TX #28 US0_RX #27 US0_CLK #26 US0_CS #25 US0_CTS #24 US0_RTS #23 US1_TX #28 US1_RX #27 US1_CLK #26 US1_CS #25 US1_CTS #24 US1_RTS #23 LEU0_TX #28 LEU0_RX #27 I2C0_SDA #28 I2C0_SCL #27	PRS_CH0 #4 PRS_CH1 #3 PRS_CH2 #2 PRS_CH3 #1 ACMP0_O #28 ACMP1_O #28
6	AVDD_1	Analog power supply 1.			
7	HFXTAL_N	High Frequency Crystal input pin.			
8	HFXTAL_P	High Frequency Crystal output pin.			
9	RESETn	Reset input, active low.To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.			
10	PD9	BUSCY BUSDX	TIM0_CC0 #17 TIM0_CC1 #16 TIM0_CC2 #15 TIM0_CDTI0 #14 TIM0_CDTI1 #13 TIM0_CDTI2 #12 TIM1_CC0 #17 TIM1_CC1 #16 TIM1_CC2 #15 TIM1_CC3 #14 LE-TIM0_OUT0 #17 LE-TIM0_OUT1 #16 PCNT0_S0IN #17 PCNT0_S1IN #16	US0_TX #17 US0_RX #16 US0_CLK #15 US0_CS #14 US0_CTS #13 US0_RTS #12 US1_TX #17 US1_RX #16 US1_CLK #15 US1_CS #14 US1_CTS #13 US1_RTS #12 LEU0_TX #17 LEU0_RX #16 I2C0_SDA #17 I2C0_SCL #16	CMU_CLK0 #4 PRS_CH3 #8 PRS_CH4 #0 PRS_CH5 #6 PRS_CH6 #11 ACMP0_O #17 ACMP1_O #17

6.4 Alternate Functionality Pinout

A wide selection of alternate functionality is available for multiplexing to various pins. The following table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

Note: Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

Table 6.7. Alternate functionality overview

Alternate	LOCATION								
Functionality	0 - 3	4 - 7	8 - 11	12 - 15	16 - 19	20 - 23	24 - 27	28 - 31	Description
ACMP0_O	0: PA0 1: PA1 2: PA2 3: PA3	4: PA4 5: PA5 6: PB11 7: PB12	8: PB13 9: PB14 10: PB15 11: PC6	12: PC7 13: PC8 14: PC9 15: PC10	16: PC11 17: PD9 18: PD10 19: PD11	20: PD12 21: PD13 22: PD14 23: PD15	24: PF0 25: PF1 26: PF2 27: PF3	28: PF4 29: PF5 30: PF6 31: PF7	Analog comparator ACMP0, digital output.
ACMP1_O	0: PA0 1: PA1 2: PA2 3: PA3	4: PA4 5: PA5 6: PB11 7: PB12	8: PB13 9: PB14 10: PB15 11: PC6	12: PC7 13: PC8 14: PC9 15: PC10	16: PC11 17: PD9 18: PD10 19: PD11	20: PD12 21: PD13 22: PD14 23: PD15	24: PF0 25: PF1 26: PF2 27: PF3	28: PF4 29: PF5 30: PF6 31: PF7	Analog comparator ACMP1, digital output.
ADC0_EXTN	0: PA0								Analog to digital converter ADC0 external reference input negative pin
ADC0_EXTP	0: PA1								Analog to digital converter ADC0 external reference input positive pin
BOOT_RX	0: PF1								Bootloader RX
BOOT_TX	0: PF0								Bootloader TX
CMU_CLK0	0: PA1 1: PB15 2: PC6 3: PC11	4: PD9 5: PD14 6: PF2 7: PF7							Clock Management Unit, clock output number 0.
CMU_CLK1	0: PA0 1: PB14 2: PC7 3: PC10	4: PD10 5: PD15 6: PF3 7: PF6							Clock Management Unit, clock output number 1.
DBG_SWCLKTCK	0: PF0								Debug-interface Serial Wire clock input and JTAG Test Clock. Note that this function is enabled to the pin out of reset, and has a built-in pull down.

Alternate	LOCATION								
Functionality	0 - 3	4 - 7	8 - 11	12 - 15	16 - 19	20 - 23	24 - 27	28 - 31	Description
GPIO_EM4WU12	0: PC10								Pin can be used to wake the system up from EM4
I2C0_SCL	0: PA1 1: PA2 2: PA3 3: PA4	4: PA5 5: PB11 6: PB12 7: PB13	8: PB14 9: PB15 10: PC6 11: PC7	12: PC8 13: PC9 14: PC10 15: PC11	16: PD9 17: PD10 18: PD11 19: PD12	20: PD13 21: PD14 22: PD15 23: PF0	24: PF1 25: PF2 26: PF3 27: PF4	28: PF5 29: PF6 30: PF7 31: PA0	I2C0 Serial Clock Line input / output.
I2C0_SDA	0: PA0 1: PA1 2: PA2 3: PA3	4: PA4 5: PA5 6: PB11 7: PB12	8: PB13 9: PB14 10: PB15 11: PC6	12: PC7 13: PC8 14: PC9 15: PC10	16: PC11 17: PD9 18: PD10 19: PD11	20: PD12 21: PD13 22: PD14 23: PD15	24: PF0 25: PF1 26: PF2 27: PF3	28: PF4 29: PF5 30: PF6 31: PF7	I2C0 Serial Data input / output.
LETIM0_OUT0	0: PA0 1: PA1 2: PA2 3: PA3	4: PA4 5: PA5 6: PB11 7: PB12	8: PB13 9: PB14 10: PB15 11: PC6	12: PC7 13: PC8 14: PC9 15: PC10	16: PC11 17: PD9 18: PD10 19: PD11	20: PD12 21: PD13 22: PD14 23: PD15	24: PF0 25: PF1 26: PF2 27: PF3	28: PF4 29: PF5 30: PF6 31: PF7	Low Energy Timer LETIM0, output channel 0.
LETIM0_OUT1	0: PA1 1: PA2 2: PA3 3: PA4	4: PA5 5: PB11 6: PB12 7: PB13	8: PB14 9: PB15 10: PC6 11: PC7	12: PC8 13: PC9 14: PC10 15: PC11	16: PD9 17: PD10 18: PD11 19: PD12	20: PD13 21: PD14 22: PD15 23: PF0	24: PF1 25: PF2 26: PF3 27: PF4	28: PF5 29: PF6 30: PF7 31: PA0	Low Energy Timer LETIM0, output channel 1.
LEU0_RX	0: PA1 1: PA2 2: PA3 3: PA4	4: PA5 5: PB11 6: PB12 7: PB13	8: PB14 9: PB15 10: PC6 11: PC7	12: PC8 13: PC9 14: PC10 15: PC11	16: PD9 17: PD10 18: PD11 19: PD12	20: PD13 21: PD14 22: PD15 23: PF0	24: PF1 25: PF2 26: PF3 27: PF4	28: PF5 29: PF6 30: PF7 31: PA0	LEUART0 Receive input.
LEU0_TX	0: PA0 1: PA1 2: PA2 3: PA3	4: PA4 5: PA5 6: PB11 7: PB12	8: PB13 9: PB14 10: PB15 11: PC6	12: PC7 13: PC8 14: PC9 15: PC10	16: PC11 17: PD9 18: PD10 19: PD11	20: PD12 21: PD13 22: PD14 23: PD15	24: PF0 25: PF1 26: PF2 27: PF3	28: PF4 29: PF5 30: PF6 31: PF7	LEUART0 Transmit output. Also used as receive input in half duplex communication.
LFXTAL_N	0: PB14								Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin.
LFXTAL_P	0: PB15								Low Frequency Crystal (typically 32.768 kHz) positive pin.
PCNT0_S0IN	0: PA0 1: PA1 2: PA2 3: PA3	4: PA4 5: PA5 6: PB11 7: PB12	8: PB13 9: PB14 10: PB15 11: PC6	12: PC7 13: PC8 14: PC9 15: PC10	16: PC11 17: PD9 18: PD10 19: PD11	20: PD12 21: PD13 22: PD14 23: PD15	24: PF0 25: PF1 26: PF2 27: PF3	28: PF4 29: PF5 30: PF6 31: PF7	Pulse Counter PCNT0 input number 0.
PCNT0_S1IN	0: PA1 1: PA2 2: PA3 3: PA4	4: PA5 5: PB11 6: PB12 7: PB13	8: PB14 9: PB15 10: PC6 11: PC7	12: PC8 13: PC9 14: PC10 15: PC11	16: PD9 17: PD10 18: PD11 19: PD12	20: PD13 21: PD14 22: PD15 23: PF0	24: PF1 25: PF2 26: PF3 27: PF4	28: PF5 29: PF6 30: PF7 31: PA0	Pulse Counter PCNT0 input number 1.
PRS_CH0	0: PF0 1: PF1 2: PF2 3: PF3	4: PF4 5: PF5 6: PF6 7: PF7	8: PC6 9: PC7 10: PC8 11: PC9	12: PC10 13: PC11					Peripheral Reflex System PRS, channel 0.

7. QFN48 Package Specifications

7.1 QFN48 Package Dimensions

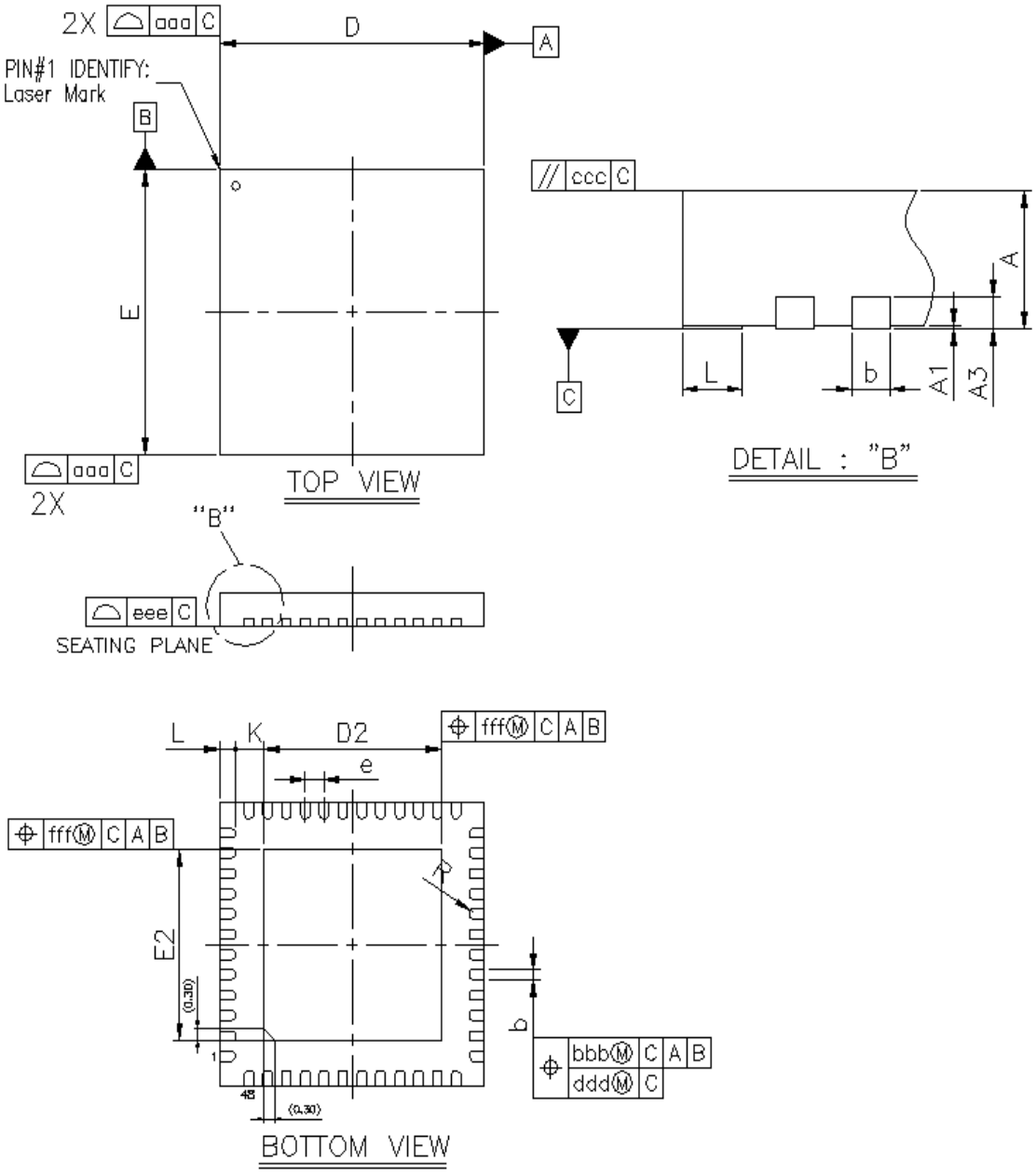

Figure 7.1. QFN48 Package Drawing

Table 7.1. QFN48 Package Dimensions

Dimension	Min	Typ	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3		0.20 REF	
b	0.18	0.25	0.30
D	6.90	7.00	7.10
E	6.90	7.00	7.10
D2	4.60	4.70	4.80
E2	4.60	4.70	4.80
e		0.50 BSC	
L	0.30	0.40	0.50
K	0.20	—	—
R	0.09	—	0.14
aaa		0.15	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-220, Variation VKKD-4.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

Table 7.2. QFN48 PCB Land Pattern Dimensions

Dimension	Typ
S1	6.01
S	6.01
L1	4.70
W1	4.70
e	0.50
W	0.26
L	0.86

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.
4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
5. The stencil thickness should be 0.125 mm (5 mils).
6. The ratio of stencil aperture to land pad size can be 1:1 for all perimeter pads.
7. A 4x4 array of 0.75 mm square openings on a 1.00 mm pitch can be used for the center ground pad.
8. A No-Clean, Type-3 solder paste is recommended.
9. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

9.7 Revision 0.1

Initial release.