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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	I ² C, IrDA, LINbus, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	20
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.85V ~ 3.8V
Data Converters	A/D 20x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TJ)
Mounting Type	Surface Mount
Package / Case	32-VFQFN Exposed Pad
Supplier Device Package	32-QFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32pg1b200f256im32-c0

3.6.3 Inter-Integrated Circuit Interface (I²C)

The I²C module provides an interface between the MCU and a serial I²C bus. It is capable of acting as both a master and a slave and supports multi-master buses. Standard-mode, fast-mode and fast-mode plus speeds are supported, allowing transmission rates from 10 kbit/s up to 1 Mbit/s. Slave arbitration and timeouts are also available, allowing implementation of an SMBus-compliant system. The interface provided to software by the I²C module allows precise timing control of the transmission process and highly automated transfers. Automatic recognition of slave addresses is provided in active and low energy modes.

3.6.4 Peripheral Reflex System (PRS)

The Peripheral Reflex System provides a communication network between different peripheral modules without software involvement. Peripheral modules producing Reflex signals are called producers. The PRS routes Reflex signals from producers to consumer peripherals which in turn perform actions in response. Edge triggers and other functionality can be applied by the PRS. The PRS allows peripheral to act autonomously without waking the MCU core, saving power.

3.7 Security Features

3.7.1 GPCRC (General Purpose Cyclic Redundancy Check)

The GPCRC module implements a Cyclic Redundancy Check (CRC) function. It supports both 32-bit and 16-bit polynomials. The supported 32-bit polynomial is 0x04C11DB7 (IEEE 802.3), while the 16-bit polynomial can be programmed to any value, depending on the needs of the application.

3.7.2 Crypto Accelerator (CRYPTO)

The Crypto Accelerator is a fast and energy-efficient autonomous hardware encryption and decryption accelerator. EFM32PG1 devices support AES encryption and decryption with 128- or 256-bit keys, ECC over both GF(P) and GF(2^m), and SHA-1 and SHA-2 (SHA-224 and SHA-256).

Supported block cipher modes of operation for AES include: ECB, CTR, CBC, PCBC, CFB, OFB, GCM, CBC-MAC, GMAC and CCM.

Supported ECC NIST recommended curves include P-192, P-224, P-256, K-163, K-233, B-163 and B-233.

The CRYPTO module allows fast processing of GCM (AES), ECC and SHA with little CPU intervention. CRYPTO also provides trigger signals for DMA read and write operations.

3.8 Analog

3.8.1 Analog Port (APORT)

The Analog Port (APORT) is an analog interconnect matrix allowing access to many analog modules on a flexible selection of pins. Each APORT bus consists of analog switches connected to a common wire. Since many clients can operate differentially, buses are grouped by X/Y pairs.

3.8.2 Analog Comparator (ACMP)

The Analog Comparator is used to compare the voltage of two analog inputs, with a digital output indicating which input voltage is higher. Inputs are selected from among internal references and external pins. The tradeoff between response time and current consumption is configurable by software. Two 6-bit reference dividers allow for a wide range of internally-programmable reference sources. The ACMP can also be used to monitor the supply voltage. An interrupt can be generated when the supply falls below or rises above the programmable threshold.

3.8.3 Analog to Digital Converter (ADC)

The ADC is a Successive Approximation Register (SAR) architecture, with a resolution of up to 12 bits at up to 1 Msps. The output sample resolution is configurable and additional resolution is possible using integrated hardware for averaging over multiple samples. The ADC includes integrated voltage references and an integrated temperature sensor. Inputs are selectable from a wide range of sources, including pins configurable as either single-ended or differential.

3.8.4 Digital to Analog Current Converter (IDAC)

The Digital to Analog Current Converter can source or sink a configurable constant current. This current can be driven on an output pin or routed to the selected ADC input pin for capacitive sensing. The full-scale current is programmable between 0.05 μA and 64 μA with several ranges consisting of various step sizes.

3.9 Reset Management Unit (RMU)

The RMU is responsible for handling reset of the EFM32PG1. A wide range of reset sources are available, including several power supply monitors, pin reset, software controlled reset, core lockup reset, and watchdog reset.

3.10 Core and Memory

3.10.1 Processor Core

The ARM Cortex-M processor includes a 32-bit RISC processor integrating the following features and tasks in the system:

- ARM Cortex-M4 RISC processor achieving 1.25 Dhrystone MIPS/MHz
- DSP instruction support and Floating Point Unit
- Memory Protection Unit (MPU) supporting up to 8 memory segments
- Up to 256 kB flash program memory
- Up to 32 kB RAM data memory
- Configuration and event handling of all modules
- 2-pin Serial-Wire debug interface

3.10.2 Memory System Controller (MSC)

The Memory System Controller (MSC) is the program memory unit of the microcontroller. The flash memory is readable and writable from both the Cortex-M and DMA. The flash memory is divided into two blocks; the main block and the information block. Program code is normally written to the main block, whereas the information block is available for special user data and flash lock bits. There is also a read-only page in the information block containing system and device calibration data. Read and write operations are supported in energy modes EM0 Active and EM1 Sleep.

3.10.3 Linked Direct Memory Access Controller (LDMA)

The Linked Direct Memory Access (LDMA) controller features 8 channels capable of performing memory operations independently of software. This reduces both energy consumption and software workload. The LDMA allows operations to be linked together and staged, enabling sophisticated operations to be implemented.

3.11 Memory Map

The EFM32PG1 memory map is shown in the figures below. RAM and flash sizes are for the largest memory configuration.

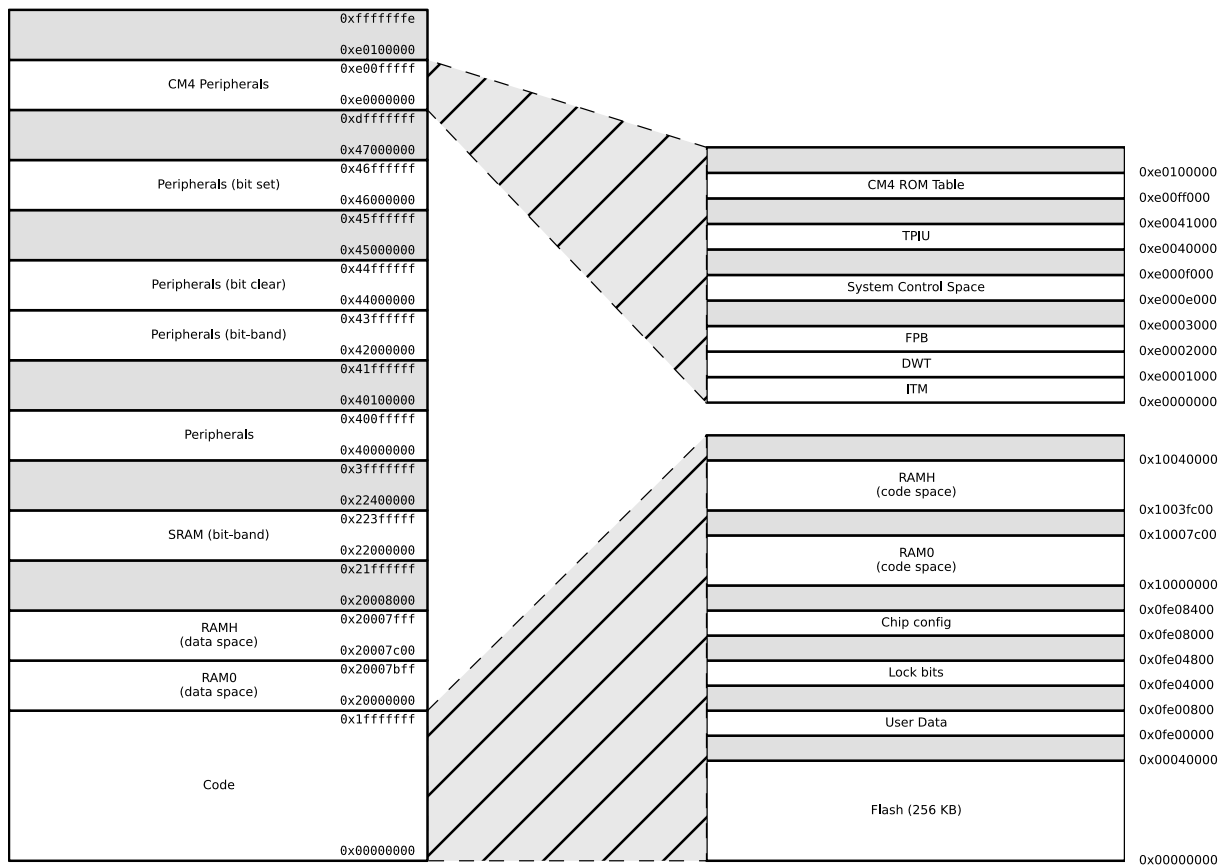


Figure 3.2. EFM32PG1 Memory Map — Core Peripherals and Code Space

4.1.3 Thermal Characteristics

Table 4.3. Thermal Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Thermal Resistance	THETA _{JA}	QFN32 Package, 2-Layer PCB, Air velocity = 0 m/s	—	79	—	°C/W
		QFN32 Package, 2-Layer PCB, Air velocity = 1 m/s	—	62.2	—	°C/W
		QFN32 Package, 2-Layer PCB, Air velocity = 2 m/s	—	54.1	—	°C/W
		QFN32 Package, 4-Layer PCB, Air velocity = 0 m/s	—	32	—	°C/W
		QFN32 Package, 4-Layer PCB, Air velocity = 1 m/s	—	28.1	—	°C/W
		QFN32 Package, 4-Layer PCB, Air velocity = 2 m/s	—	26.9	—	°C/W
		QFN48 Package, 2-Layer PCB, Air velocity = 0 m/s	—	64.5	—	°C/W
		QFN48 Package, 2-Layer PCB, Air velocity = 1 m/s	—	51.6	—	°C/W
		QFN48 Package, 2-Layer PCB, Air velocity = 2 m/s	—	47.7	—	°C/W
		QFN48 Package, 4-Layer PCB, Air velocity = 0 m/s	—	26.2	—	°C/W
		QFN48 Package, 4-Layer PCB, Air velocity = 1 m/s	—	23.1	—	°C/W
		QFN48 Package, 4-Layer PCB, Air velocity = 2 m/s	—	22.1	—	°C/W

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM4S Shutoff mode	I_{EM4S}	no RAM retention, no RTCC	—	0.04	—	μA

Note:

1. DCDC Low Noise DCM Mode = Light Drive (PFETCNT=NFETCNT=3), F=3.0 MHz (RCOBAND=0), ANASW=DVDD
2. CMU_HFXOCTRL_LOWPOWER=1
3. DCDC Low Noise CCM Mode = Light Drive (PFETCNT=NFETCNT=3), F=6.4 MHz (RCOBAND=4), ANASW=DVDD
4. DCDC Low Power Mode = Medium Drive (PFETCNT=NFETCNT=7), LPOSCDIV=1, LPBIAS=3, LPCILIMSEL=1, ANASW=DVDD

4.1.8 Oscillators

4.1.8.1 LFXO

Table 4.10. LFXO

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Crystal frequency	f_{LFXO}		—	32.768	—	kHz
Supported crystal equivalent series resistance (ESR)	ESR_{LFXO}		—	—	70	k Ω
Supported range of crystal load capacitance ¹	$C_{\text{LFXO_CL}}$		6	—	18	pF
On-chip tuning cap range ²	$C_{\text{LFXO_T}}$	On each of LFX TAL_N and LFX TAL_P pins	8	—	40	pF
On-chip tuning cap step size	SS_{LFXO}		—	0.25	—	pF
Current consumption after startup ³	I_{LFXO}	ESR = 70 k Ω , C_L = 7 pF, GAIN ⁴ = 3, AGC ⁴ = 1	—	273	—	nA
Start- up time	t_{LFXO}	ESR=70 k Ω , C_L = 7 pF, GAIN ⁴ = 2	—	308	—	ms

Note:

1. Total load capacitance as seen by the crystal
2. The effective load capacitance seen by the crystal will be $C_{\text{LFXO_T}}/2$. This is because each XTAL pin has a tuning cap and the two caps will be seen in series by the crystal.
3. Block is supplied by AVDD if ANASW = 0, or DVDD if ANASW=1 in EMU_PWRCTRL register
4. In CMU_LFXOCTRL register

4.1.8.4 HFRCO and AUXHFRCO

Table 4.13. HFRCO and AUXHFRCO

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Frequency Accuracy	$f_{\text{HFRCO_ACC}}$	Any frequency band, across supply voltage and temperature	-2.5	—	2.5	%
Start-up time	t_{HFRCO}	$f_{\text{HFRCO}} \geq 19 \text{ MHz}$	—	300	—	ns
		$4 < f_{\text{HFRCO}} < 19 \text{ MHz}$	—	1	—	μs
		$f_{\text{HFRCO}} \leq 4 \text{ MHz}$	—	2.5	—	μs
Current consumption on all supplies	I_{HFRCO}	$f_{\text{HFRCO}} = 38 \text{ MHz}$	—	204	228	μA
		$f_{\text{HFRCO}} = 32 \text{ MHz}$	—	171	190	μA
		$f_{\text{HFRCO}} = 26 \text{ MHz}$	—	147	164	μA
		$f_{\text{HFRCO}} = 19 \text{ MHz}$	—	126	138	μA
		$f_{\text{HFRCO}} = 16 \text{ MHz}$	—	110	120	μA
		$f_{\text{HFRCO}} = 13 \text{ MHz}$	—	100	110	μA
		$f_{\text{HFRCO}} = 7 \text{ MHz}$	—	81	91	μA
		$f_{\text{HFRCO}} = 4 \text{ MHz}$	—	33	35	μA
		$f_{\text{HFRCO}} = 2 \text{ MHz}$	—	31	35	μA
		$f_{\text{HFRCO}} = 1 \text{ MHz}$	—	30	35	μA
Step size	SS_{HFRCO}	Coarse (% of period)	—	0.8	—	%
		Fine (% of period)	—	0.1	—	%
Period Jitter	PJ_{HFRCO}		—	0.2	—	% RMS

4.1.8.5 ULFRCO

Table 4.14. ULFRCO

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Oscillation frequency	f_{ULFRCO}		0.95	1	1.07	kHz

4.1.16 USART SPI

SPI Master Timing

Table 4.24. SPI Master Timing

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK period ^{1 2}	t_{SCLK}		2 * t_{HFPERCLK}	—	—	ns
CS to MOSI ^{1 2}	$t_{\text{CS_MO}}$		0	—	8	ns
SCLK to MOSI ^{1 2}	$t_{\text{SCLK_MO}}$		3	—	20	ns
MISO setup time ^{1 2}	$t_{\text{SU_MI}}$	IOVDD = 1.62 V	56	—	—	ns
		IOVDD = 3.0 V	37	—	—	ns
MISO hold time ^{1 2}	$t_{\text{H_MI}}$		6	—	—	ns

Note:

1. Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0)
2. Measurement done with 8 pF output loading at 10% and 90% of V_{DD} (figure shows 50% of V_{DD})

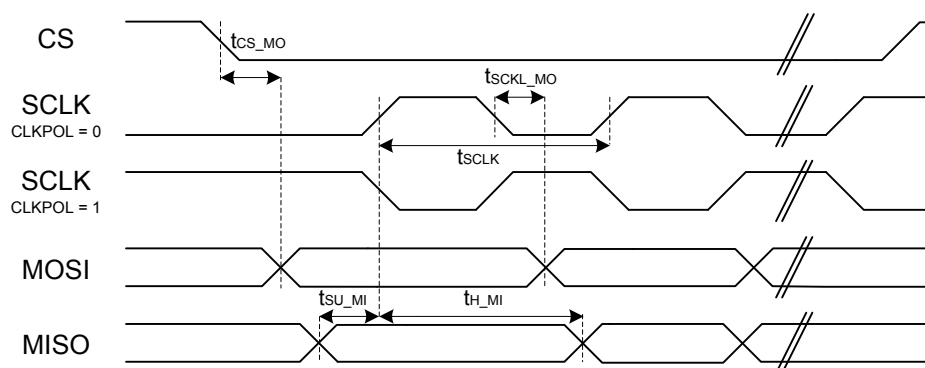


Figure 4.1. SPI Master Timing Diagram

4.2.2 DC-DC Converter

Default test conditions: CCM mode, LDCDC = 4.7 μ H, CDCDC = 1.0 μ F, VDCDC_I = 3.3 V, VDCDC_O = 1.8 V, FDCDC_LN = 7 MHz

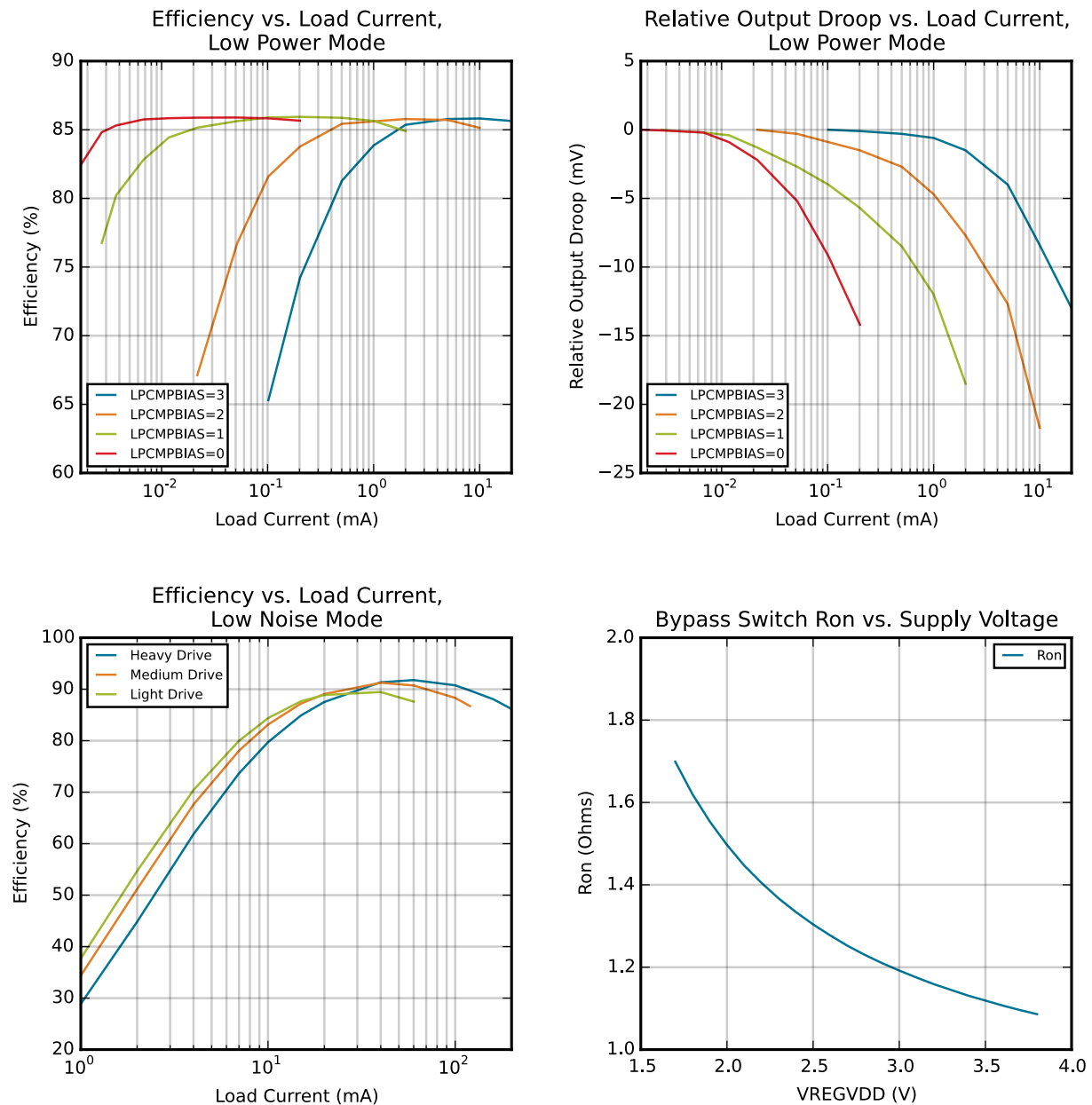


Figure 4.6. DC-DC Converter Typical Performance Characteristics

4.2.3 Internal Oscillators

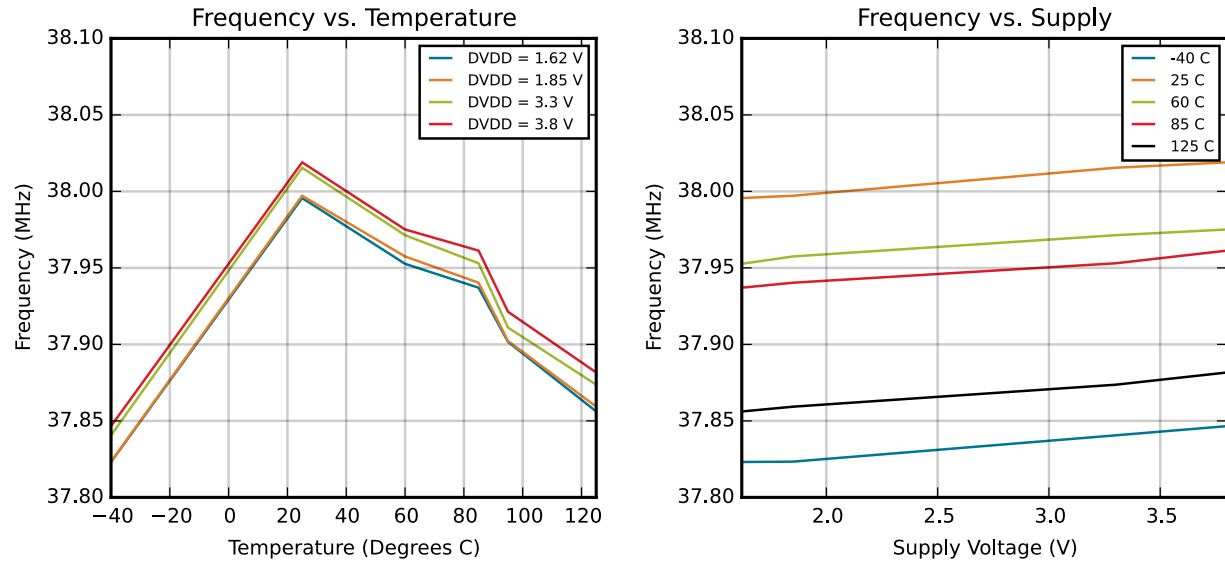


Figure 4.8. HFCO and AUXHFCO Typical Performance at 38 MHz

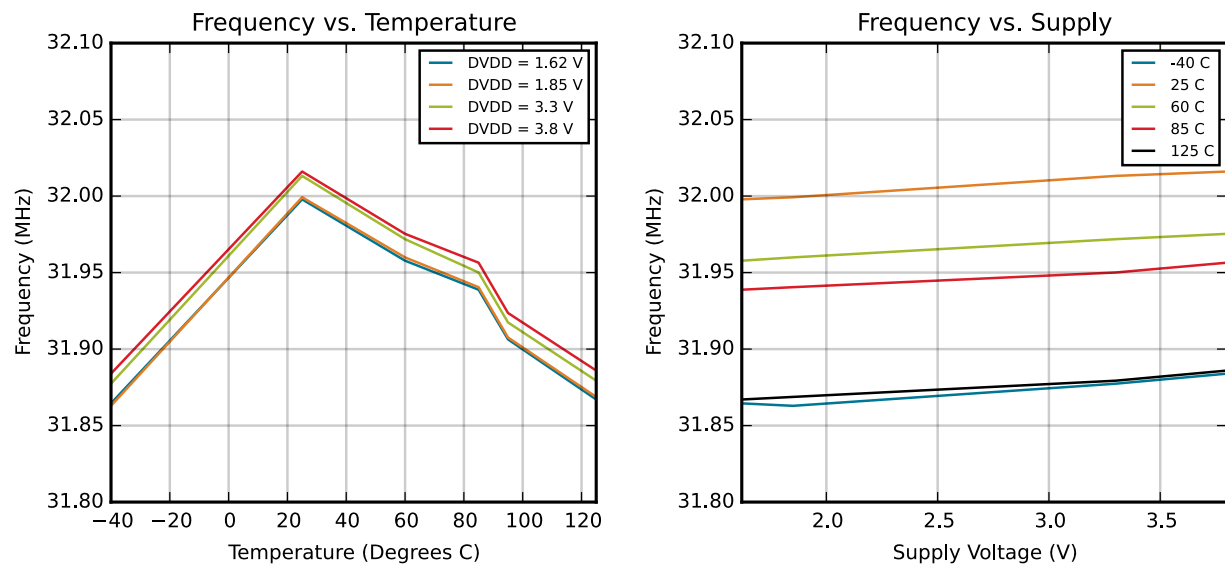


Figure 4.9. HFCO and AUXHFCO Typical Performance at 32 MHz

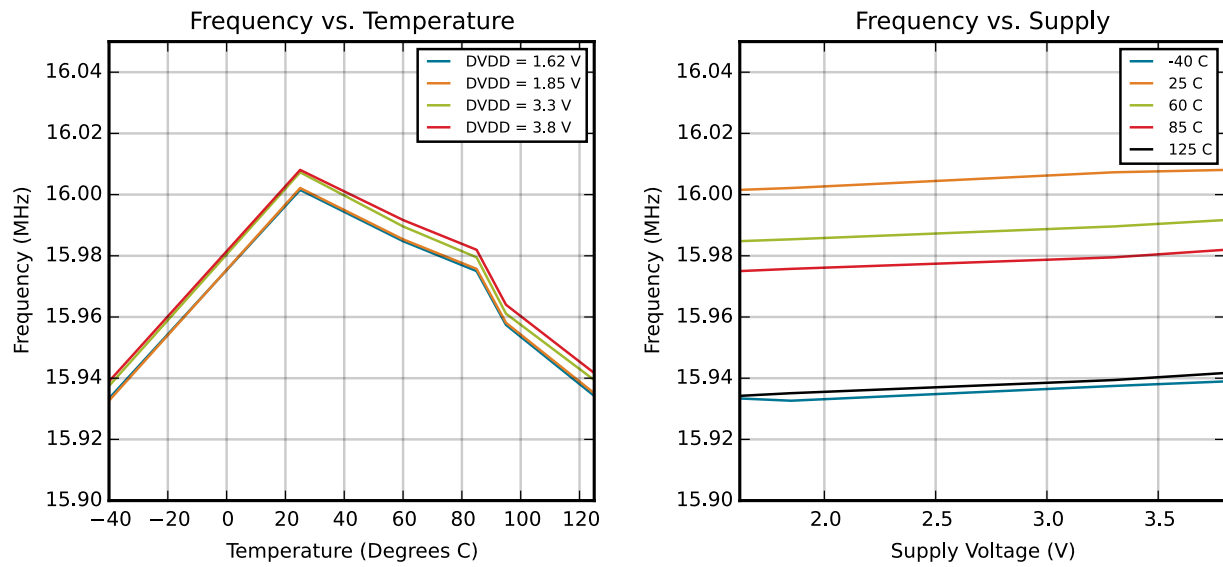


Figure 4.12. HFRCO and AUXHFRCO Typical Performance at 16 MHz

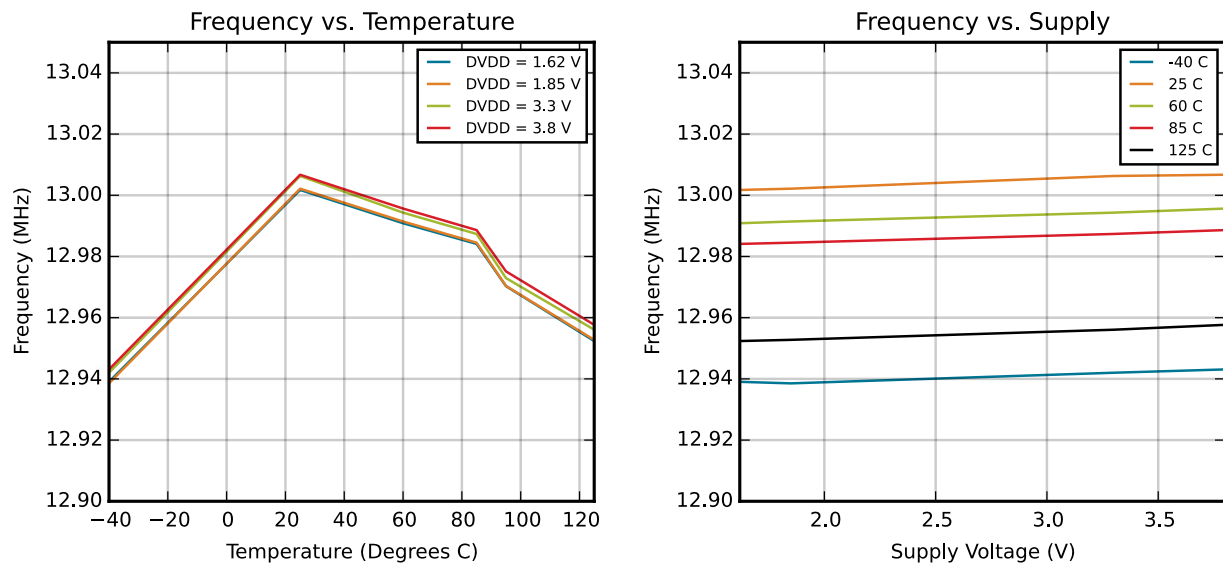


Figure 4.13. HFRCO and AUXHFRCO Typical Performance at 13 MHz

QFN48 Pin# and Name		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
24	PD15	BUSCY BUSDX	TIM0_CC0 #23 TIM0_CC1 #22 TIM0_CC2 #21 TIM0_CDTI0 #20 TIM0_CDTI1 #19 TIM0_CDTI2 #18 TIM1_CC0 #23 TIM1_CC1 #22 TIM1_CC2 #21 TIM1_CC3 #20 LE- TIM0_OUT0 #23 LE- TIM0_OUT1 #22 PCNT0_S0IN #23 PCNT0_S1IN #22	US0_TX #23 US0_RX #22 US0_CLK #21 US0_CS #20 US0_CTS #19 US0_RTS #18 US1_TX #23 US1_RX #22 US1_CLK #21 US1_CS #20 US1_CTS #19 US1_RTS #18 LEU0_TX #23 LEU0_RX #22 I2C0_SDA #23 I2C0_SCL #22	CMU_CLK1 #5 PRS_CH3 #14 PRS_CH4 #6 PRS_CH5 #5 PRS_CH6 #17 ACMP0_O #23 ACMP1_O #23 DBG_SWO #2
25	PA0	ADC0_EXTN BUSCX BUSDY	TIM0_CC0 #0 TIM0_CC1 #31 TIM0_CC2 #30 TIM0_CDTI0 #29 TIM0_CDTI1 #28 TIM0_CDTI2 #27 TIM1_CC0 #0 TIM1_CC1 #31 TIM1_CC2 #30 TIM1_CC3 #29 LE- TIM0_OUT0 #0 LE- TIM0_OUT1 #31 PCNT0_S0IN #0 PCNT0_S1IN #31	US0_TX #0 US0_RX #31 US0_CLK #30 US0_CS #29 US0_CTS #28 US0_RTS #27 US1_TX #0 US1_RX #31 US1_CLK #30 US1_CS #29 US1_CTS #28 US1_RTS #27 LEU0_TX #0 LEU0_RX #31 I2C0_SDA #0 I2C0_SCL #31	CMU_CLK1 #0 PRS_CH6 #0 PRS_CH7 #10 PRS_CH8 #9 PRS_CH9 #8 ACMP0_O #0 ACMP1_O #0
26	PA1	ADC0_EXTP BUSCY BUSDX	TIM0_CC0 #1 TIM0_CC1 #0 TIM0_CC2 #31 TIM0_CDTI0 #30 TIM0_CDTI1 #29 TIM0_CDTI2 #28 TIM1_CC0 #1 TIM1_CC1 #0 TIM1_CC2 #31 TIM1_CC3 #30 LE- TIM0_OUT0 #1 LE- TIM0_OUT1 #0 PCNT0_S0IN #1 PCNT0_S1IN #0	US0_TX #1 US0_RX #0 US0_CLK #31 US0_CS #30 US0_CTS #29 US0_RTS #28 US1_TX #1 US1_RX #0 US1_CLK #31 US1_CS #30 US1_CTS #29 US1_RTS #28 LEU0_TX #1 LEU0_RX #0 I2C0_SDA #1 I2C0_SCL #0	CMU_CLK0 #0 PRS_CH6 #1 PRS_CH7 #0 PRS_CH8 #10 PRS_CH9 #9 ACMP0_O #1 ACMP1_O #1
27	PA2	BUSCX BUSDY	TIM0_CC0 #2 TIM0_CC1 #1 TIM0_CC2 #0 TIM0_CDTI0 #31 TIM0_CDTI1 #30 TIM0_CDTI2 #29 TIM1_CC0 #2 TIM1_CC1 #1 TIM1_CC2 #0 TIM1_CC3 #31 LE- TIM0_OUT0 #2 LE- TIM0_OUT1 #1 PCNT0_S0IN #2 PCNT0_S1IN #1	US0_TX #2 US0_RX #1 US0_CLK #0 US0_CS #31 US0_CTS #30 US0_RTS #29 US1_TX #2 US1_RX #1 US1_CLK #0 US1_CS #31 US1_CTS #30 US1_RTS #29 LEU0_TX #2 LEU0_RX #1 I2C0_SDA #2 I2C0_SCL #1	PRS_CH6 #2 PRS_CH7 #1 PRS_CH8 #0 PRS_CH9 #10 ACMP0_O #2 ACMP1_O #2

QFN48 Pin# and Name		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
46	PC9	BUSAY BUSBX	TIM0_CC0 #14 TIM0_CC1 #13 TIM0_CC2 #12 TIM0_CDTI0 #11 TIM0_CDTI1 #10 TIM0_CDTI2 #9 TIM1_CC0 #14 TIM1_CC1 #13 TIM1_CC2 #12 TIM1_CC3 #11 LE- TIM0_OUT0 #14 LE- TIM0_OUT1 #13 PCNT0_S0IN #14 PCNT0_S1IN #13	US0_TX #14 US0_RX #13 US0_CLK #12 US0_CS #11 US0_CTS #10 US0_RTS #9 US1_TX #14 US1_RX #13 US1_CLK #12 US1_CS #11 US1_CTS #10 US1_RTS #9 LEU0_TX #14 LEU0_RX #13 I2C0_SDA #14 I2C0_SCL #13	PRS_CH0 #11 PRS_CH9 #14 PRS_CH10 #3 PRS_CH11 #2 ACMP0_O #14 ACMP1_O #14
47	PC10	BUSAX BUSBY	TIM0_CC0 #15 TIM0_CC1 #14 TIM0_CC2 #13 TIM0_CDTI0 #12 TIM0_CDTI1 #11 TIM0_CDTI2 #10 TIM1_CC0 #15 TIM1_CC1 #14 TIM1_CC2 #13 TIM1_CC3 #12 LE- TIM0_OUT0 #15 LE- TIM0_OUT1 #14 PCNT0_S0IN #15 PCNT0_S1IN #14	US0_TX #15 US0_RX #14 US0_CLK #13 US0_CS #12 US0_CTS #11 US0_RTS #10 US1_TX #15 US1_RX #14 US1_CLK #13 US1_CS #12 US1_CTS #11 US1_RTS #10 LEU0_TX #15 LEU0_RX #14 I2C0_SDA #15 I2C0_SCL #14	CMU_CLK1 #3 PRS_CH0 #12 PRS_CH9 #15 PRS_CH10 #4 PRS_CH11 #3 ACMP0_O #15 ACMP1_O #15 GPIO_EM4WU12
48	PC11	BUSAY BUSBX	TIM0_CC0 #16 TIM0_CC1 #15 TIM0_CC2 #14 TIM0_CDTI0 #13 TIM0_CDTI1 #12 TIM0_CDTI2 #11 TIM1_CC0 #16 TIM1_CC1 #15 TIM1_CC2 #14 TIM1_CC3 #13 LE- TIM0_OUT0 #16 LE- TIM0_OUT1 #15 PCNT0_S0IN #16 PCNT0_S1IN #15	US0_TX #16 US0_RX #15 US0_CLK #14 US0_CS #13 US0_CTS #12 US0_RTS #11 US1_TX #16 US1_RX #15 US1_CLK #14 US1_CS #13 US1_CTS #12 US1_RTS #11 LEU0_TX #16 LEU0_RX #15 I2C0_SDA #16 I2C0_SCL #15	CMU_CLK0 #3 PRS_CH0 #13 PRS_CH9 #16 PRS_CH10 #5 PRS_CH11 #4 ACMP0_O #16 ACMP1_O #16 DBG_SWO #3

QFN32 Pin# and Name		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
11	PD10	BUSCX BUSDY	TIM0_CC0 #18 TIM0_CC1 #17 TIM0_CC2 #16 TIM0_CDTI0 #15 TIM0_CDTI1 #14 TIM0_CDTI2 #13 TIM1_CC0 #18 TIM1_CC1 #17 TIM1_CC2 #16 TIM1_CC3 #15 LE- TIM0_OUT0 #18 LE- TIM0_OUT1 #17 PCNT0_S0IN #18 PCNT0_S1IN #17	US0_TX #18 US0_RX #17 US0_CLK #16 US0_CS #15 US0_CTS #14 US0_RTS #13 US1_TX #18 US1_RX #17 US1_CLK #16 US1_CS #15 US1_CTS #14 US1_RTS #13 LEU0_TX #18 LEU0_RX #17 I2C0_SDA #18 I2C0_SCL #17	CMU_CLK1 #4 PRS_CH3 #9 PRS_CH4 #1 PRS_CH5 #0 PRS_CH6 #12 ACMP0_O #18 ACMP1_O #18
12	PD11	BUSCY BUSDX	TIM0_CC0 #19 TIM0_CC1 #18 TIM0_CC2 #17 TIM0_CDTI0 #16 TIM0_CDTI1 #15 TIM0_CDTI2 #14 TIM1_CC0 #19 TIM1_CC1 #18 TIM1_CC2 #17 TIM1_CC3 #16 LE- TIM0_OUT0 #19 LE- TIM0_OUT1 #18 PCNT0_S0IN #19 PCNT0_S1IN #18	US0_TX #19 US0_RX #18 US0_CLK #17 US0_CS #16 US0_CTS #15 US0_RTS #14 US1_TX #19 US1_RX #18 US1_CLK #17 US1_CS #16 US1_CTS #15 US1_RTS #14 LEU0_TX #19 LEU0_RX #18 I2C0_SDA #19 I2C0_SCL #18	PRS_CH3 #10 PRS_CH4 #2 PRS_CH5 #1 PRS_CH6 #13 ACMP0_O #19 ACMP1_O #19
13	PD12	BUSCX BUSDY	TIM0_CC0 #20 TIM0_CC1 #19 TIM0_CC2 #18 TIM0_CDTI0 #17 TIM0_CDTI1 #16 TIM0_CDTI2 #15 TIM1_CC0 #20 TIM1_CC1 #19 TIM1_CC2 #18 TIM1_CC3 #17 LE- TIM0_OUT0 #20 LE- TIM0_OUT1 #19 PCNT0_S0IN #20 PCNT0_S1IN #19	US0_TX #20 US0_RX #19 US0_CLK #18 US0_CS #17 US0_CTS #16 US0_RTS #15 US1_TX #20 US1_RX #19 US1_CLK #18 US1_CS #17 US1_CTS #16 US1_RTS #15 LEU0_TX #20 LEU0_RX #19 I2C0_SDA #20 I2C0_SCL #19	PRS_CH3 #11 PRS_CH4 #3 PRS_CH5 #2 PRS_CH6 #14 ACMP0_O #20 ACMP1_O #20
14	PD13	BUSCY BUSDX	TIM0_CC0 #21 TIM0_CC1 #20 TIM0_CC2 #19 TIM0_CDTI0 #18 TIM0_CDTI1 #17 TIM0_CDTI2 #16 TIM1_CC0 #21 TIM1_CC1 #20 TIM1_CC2 #19 TIM1_CC3 #18 LE- TIM0_OUT0 #21 LE- TIM0_OUT1 #20 PCNT0_S0IN #21 PCNT0_S1IN #20	US0_TX #21 US0_RX #20 US0_CLK #19 US0_CS #18 US0_CTS #17 US0_RTS #16 US1_TX #21 US1_RX #20 US1_CLK #19 US1_CS #18 US1_CTS #17 US1_RTS #16 LEU0_TX #21 LEU0_RX #20 I2C0_SDA #21 I2C0_SCL #20	PRS_CH3 #12 PRS_CH4 #4 PRS_CH5 #3 PRS_CH6 #15 ACMP0_O #21 ACMP1_O #21

QFN32 Pin# and Name		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
25	VREGVSS	Voltage regulator VSS			
26	VREGSW	DCDC regulator switching node			
27	VREGVDD	Voltage regulator VDD input			
28	DVDD	Digital power supply.			
29	DECOUPLE	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin.			
30	IOVDD	Digital IO power supply.			
31	PC10	BUSAX BUSBY	TIM0_CC0 #15 TIM0_CC1 #14 TIM0_CC2 #13 TIM0_CDTI0 #12 TIM0_CDTI1 #11 TIM0_CDTI2 #10 TIM1_CC0 #15 TIM1_CC1 #14 TIM1_CC2 #13 TIM1_CC3 #12 LE- TIM0_OUT0 #15 LE- TIM0_OUT1 #14 PCNT0_S0IN #15 PCNT0_S1IN #14	US0_TX #15 US0_RX #14 US0_CLK #13 US0_CS #12 US0_CTS #11 US0_RTS #10 US1_TX #15 US1_RX #14 US1_CLK #13 US1_CS #12 US1_CTS #11 US1_RTS #10 LEU0_TX #15 LEU0_RX #14 I2C0_SDA #15 I2C0_SCL #14	CMU_CLK1 #3 PRS_CH0 #12 PRS_CH9 #15 PRS_CH10 #4 PRS_CH11 #3 ACMP0_O #15 ACMP1_O #15 GPIO_EM4WU12
32	PC11	BUSAY BUSBX	TIM0_CC0 #16 TIM0_CC1 #15 TIM0_CC2 #14 TIM0_CDTI0 #13 TIM0_CDTI1 #12 TIM0_CDTI2 #11 TIM1_CC0 #16 TIM1_CC1 #15 TIM1_CC2 #14 TIM1_CC3 #13 LE- TIM0_OUT0 #16 LE- TIM0_OUT1 #15 PCNT0_S0IN #16 PCNT0_S1IN #15	US0_TX #16 US0_RX #15 US0_CLK #14 US0_CS #13 US0_CTS #12 US0_RTS #11 US1_TX #16 US1_RX #15 US1_CLK #14 US1_CS #13 US1_CTS #12 US1_RTS #11 LEU0_TX #16 LEU0_RX #15 I2C0_SDA #16 I2C0_SCL #15	CMU_CLK0 #3 PRS_CH0 #13 PRS_CH9 #16 PRS_CH10 #5 PRS_CH11 #4 ACMP0_O #16 ACMP1_O #16 DBG_SWO #3

6.3.1 EFM32PG1 QFN32 with DC-DC GPIO Overview

The GPIO pins are organized as 16-bit ports indicated by letters (A, B, C...), and the individual pins on each port are indicated by a number from 15 down to 0.

Table 6.6. QFN32 with DC-DC GPIO Pinout

Port	Pin 15	Pin 14	Pin 13	Pin 12	Pin 11	Pin 10	Pin 9	Pin 8	Pin 7	Pin 6	Pin 5	Pin 4	Pin 3	Pin 2	Pin 1	Pin 0
Port A	-	-	-	-	-	-	-	-	-	-	-	-	-	-	PA1	PA0
Port B	PB15	PB14	PB13 (5V)	PB12 (5V)	PB11 (5V)	-	-	-	-	-	-	-	-	-	-	-
Port C	-	-	-	-	PC11 (5V)	PC10 (5V)	-	-	-	-	-	-	-	-	-	-
Port D	PD15 (5V)	PD14 (5V)	PD13 (5V)	PD12 (5V)	PD11 (5V)	PD10 (5V)	PD9 (5V)	-	-	-	-	-	-	-	-	-
Port F	-	-	-	-	-	-	-	-	-	-	-	-	PF3 (5V)	PF2 (5V)	PF1 (5V)	PF0 (5V)

Note:

- GPIO with 5V tolerance are indicated by (5V).
- The pins PB13, PB12, PB11, PD15, PD14, and PD13 will not be 5V tolerant on all future devices. In order to preserve upgrade options with full hardware compatibility, do not use these pins with 5V domains.

6.4 Alternate Functionality Pinout

A wide selection of alternate functionality is available for multiplexing to various pins. The following table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

Note: Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

Table 6.7. Alternate functionality overview

Alternate	LOCATION								
Functionality	0 - 3	4 - 7	8 - 11	12 - 15	16 - 19	20 - 23	24 - 27	28 - 31	Description
ACMP0_O	0: PA0 1: PA1 2: PA2 3: PA3	4: PA4 5: PA5 6: PB11 7: PB12	8: PB13 9: PB14 10: PB15 11: PC6	12: PC7 13: PC8 14: PC9 15: PC10	16: PC11 17: PD9 18: PD10 19: PD11	20: PD12 21: PD13 22: PD14 23: PD15	24: PF0 25: PF1 26: PF2 27: PF3	28: PF4 29: PF5 30: PF6 31: PF7	Analog comparator ACMP0, digital output.
ACMP1_O	0: PA0 1: PA1 2: PA2 3: PA3	4: PA4 5: PA5 6: PB11 7: PB12	8: PB13 9: PB14 10: PB15 11: PC6	12: PC7 13: PC8 14: PC9 15: PC10	16: PC11 17: PD9 18: PD10 19: PD11	20: PD12 21: PD13 22: PD14 23: PD15	24: PF0 25: PF1 26: PF2 27: PF3	28: PF4 29: PF5 30: PF6 31: PF7	Analog comparator ACMP1, digital output.
ADC0_EXTN	0: PA0								Analog to digital converter ADC0 external reference input negative pin
ADC0_EXTP	0: PA1								Analog to digital converter ADC0 external reference input positive pin
BOOT_RX	0: PF1								Bootloader RX
BOOT_TX	0: PF0								Bootloader TX
CMU_CLK0	0: PA1 1: PB15 2: PC6 3: PC11	4: PD9 5: PD14 6: PF2 7: PF7							Clock Management Unit, clock output number 0.
CMU_CLK1	0: PA0 1: PB14 2: PC7 3: PC10	4: PD10 5: PD15 6: PF3 7: PF6							Clock Management Unit, clock output number 1.
DBG_SWCLKTCK	0: PF0								Debug-interface Serial Wire clock input and JTAG Test Clock. Note that this function is enabled to the pin out of reset, and has a built-in pull down.

Alternate	LOCATION								
Functionality	0 - 3	4 - 7	8 - 11	12 - 15	16 - 19	20 - 23	24 - 27	28 - 31	Description
US0_RX	0: PA1 1: PA2 2: PA3 3: PA4	4: PA5 5: PB11 6: PB12 7: PB13	8: PB14 9: PB15 10: PC6 11: PC7	12: PC8 13: PC9 14: PC10 15: PC11	16: PD9 17: PD10 18: PD11 19: PD12	20: PD13 21: PD14 22: PD15 23: PF0	24: PF1 25: PF2 26: PF3 27: PF4	28: PF5 29: PF6 30: PF7 31: PA0	USART0 Asynchronous Receive. USART0 Synchronous mode Master Input / Slave Output (MISO).
US0_TX	0: PA0 1: PA1 2: PA2 3: PA3	4: PA4 5: PA5 6: PB11 7: PB12	8: PB13 9: PB14 10: PB15 11: PC6	12: PC7 13: PC8 14: PC9 15: PC10	16: PC11 17: PD9 18: PD10 19: PD11	20: PD12 21: PD13 22: PD14 23: PD15	24: PF0 25: PF1 26: PF2 27: PF3	28: PF4 29: PF5 30: PF6 31: PF7	USART0 Asynchronous Transmit. Also used as receive input in half duplex communication. USART0 Synchronous mode Master Output / Slave Input (MOSI).
US1_CLK	0: PA2 1: PA3 2: PA4 3: PA5	4: PB11 5: PB12 6: PB13 7: PB14	8: PB15 9: PC6 10: PC7 11: PC8	12: PC9 13: PC10 14: PC11 15: PD9	16: PD10 17: PD11 18: PD12 19: PD13	20: PD14 21: PD15 22: PF0 23: PF1	24: PF2 25: PF3 26: PF4 27: PF5	28: PF6 29: PF7 30: PA0 31: PA1	USART1 clock input / output.
US1_CS	0: PA3 1: PA4 2: PA5 3: PB11	4: PB12 5: PB13 6: PB14 7: PB15	8: PC6 9: PC7 10: PC8 11: PC9	12: PC10 13: PC11 14: PD9 15: PD10	16: PD11 17: PD12 18: PD13 19: PD14	20: PD15 21: PF0 22: PF1 23: PF2	24: PF3 25: PF4 26: PF5 27: PF6	28: PF7 29: PA0 30: PA1 31: PA2	USART1 chip select input / output.
US1_CTS	0: PA4 1: PA5 2: PB11 3: PB12	4: PB13 5: PB14 6: PB15 7: PC6	8: PC7 9: PC8 10: PC9 11: PC10	12: PC11 13: PD9 14: PD10 15: PD11	16: PD12 17: PD13 18: PD14 19: PD15	20: PF0 21: PF1 22: PF2 23: PF3	24: PF4 25: PF5 26: PF6 27: PF7	28: PA0 29: PA1 30: PA2 31: PA3	USART1 Clear To Send hardware flow control input.
US1_RTS	0: PA5 1: PB11 2: PB12 3: PB13	4: PB14 5: PB15 6: PC6 7: PC7	8: PC8 9: PC9 10: PC10 11: PC11	12: PD9 13: PD10 14: PD11 15: PD12	16: PD13 17: PD14 18: PD15 19: PF0	20: PF1 21: PF2 22: PF3 23: PF4	24: PF5 25: PF6 26: PF7 27: PA0	28: PA1 29: PA2 30: PA3 31: PA4	USART1 Request To Send hardware flow control output.
US1_RX	0: PA1 1: PA2 2: PA3 3: PA4	4: PA5 5: PB11 6: PB12 7: PB13	8: PB14 9: PB15 10: PC6 11: PC7	12: PC8 13: PC9 14: PC10 15: PC11	16: PD9 17: PD10 18: PD11 19: PD12	20: PD13 21: PD14 22: PD15 23: PF0	24: PF1 25: PF2 26: PF3 27: PF4	28: PF5 29: PF6 30: PF7 31: PA0	USART1 Asynchronous Receive. USART1 Synchronous mode Master Input / Slave Output (MISO).
US1_TX	0: PA0 1: PA1 2: PA2 3: PA3	4: PA4 5: PA5 6: PB11 7: PB12	8: PB13 9: PB14 10: PB15 11: PC6	12: PC7 13: PC8 14: PC9 15: PC10	16: PC11 17: PD9 18: PD10 19: PD11	20: PD12 21: PD13 22: PD14 23: PD15	24: PF0 25: PF1 26: PF2 27: PF3	28: PF4 29: PF5 30: PF6 31: PF7	USART1 Asynchronous Transmit. Also used as receive input in half duplex communication. USART1 Synchronous mode Master Output / Slave Input (MOSI).

6.5 Analog Port (APORT) Client Maps

The Analog Port (APORT) is an infrastructure used to connect chip pins with on-chip analog clients such as analog comparators, ADCs, DACs, etc. The APORT consists of a set of shared buses, switches, and control logic needed to configurably implement the signal routing. A complete description of APORT functionality can be found in the Reference Manual.

Client maps for each analog circuit using the APORT are shown in the following tables. The maps are organized by bus, and show the peripheral's port connection, the shared bus, and the connection from specific bus channel numbers to GPIO pins.

In general, enumerations for the pin selection field in an analog peripheral's register can be determined by finding the desired pin connection in the table and then combining the value in the Port column (APORT__), and the channel identifier (CH__). For example, if pin PF7 is available on port APORT2X as CH23, the register field enumeration to connect to PF7 would be APORT2XCH23. The shared bus used by this connection is indicated in the Bus column.

Table 6.8. ACMP0 Bus and Pin Mapping

Port	Bus	CH31	CH30	CH29	CH28	CH27	CH26	CH25	CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
APORT1X	BUSAX										PF6		PF4		PF2		PF0						PC10		PC8		PC6						
APORT1Y	BUSAY									PF7		PF5		PF3		PF1						PC11			PC9		PC7						
APORT2X	BUSBX									PF7		PF5		PF3		PF1							PC11		PC9		PC7						
APORT2Y	BUSBY										PF6		PF4		PF2		PF0						PC10		PC8		PC6						
APORT3X	BUSCX		PB14		PB12																PA4		PA2		PA0		PD14		PD12		PD10		
APORT3Y	BUSCY	PB15		PB13		PB11														PA5		PA3		PA1		PD15		PD13		PD11		PD9	
APORT4X	BUSDX	PB15		PB13		PB11														PA5		PA3		PA1		PD15		PD13		PD11		PD9	
APORT4Y	BUSDY		PB14		PB12																PA4		PA2		PA0		PD14		PD12		PD10		

Table 6.10. ADC0 Bus and Pin Mapping

APORT4Y	APORT4X	APORT3Y	APORT3X	APORT2Y	APORT2X	APORT1Y	APORT1X	Port
BUSDY	BUSDX	BUSCY	BUSCX	BUSBY	BUSBX	BUSAY	BUSAX	Bus
	PB15	PB15						CH31
PB14			PB14					CH30
	PB13	PB13						CH29
PB12			PB12					CH28
	PB11	PB11						CH27
								CH26
								CH25
								CH24
					PF7	PF7		CH23
				PF6			PF6	CH22
					PF5	PF5		CH21
				PF4			PF4	CH20
					PF3	PF3		CH19
				PF2			PF2	CH18
					PF1	PF1		CH17
				PF0			PF0	CH16
								CH15
								CH14
	PA5	PA5						CH13
PA4			PA4					CH12
	PA3	PA3			PC11	PC11		CH11
PA2			PA2	PC10			PC10	CH10
	PA1	PA1			PC9	PC9		CH9
PA0			PA0	PC8			PC8	CH8
	PD15	PD15			PC7	PC7		CH7
PD14			PD14	PC6			PC6	CH6
	PD13	PD13						CH5
PD12			PD12					CH4
	PD11	PD11						CH3
PD10			PD10					CH2
	PD9	PD9						CH1
								CH0

Table 6.11. IDAC0 Bus and Pin Mapping

APORT1Y	APORT1X	Port
BUSCY	BUSCX	Bus
PB15		CH31
	PB14	CH30
PB13		CH29
	PB12	CH28
PB11		CH27
		CH26
		CH25
		CH24
		CH23
		CH22
		CH21
		CH20
		CH19
		CH18
		CH17
		CH16
		CH15
		CH14
PA5		CH13
	PA4	CH12
PA3		CH11
	PA2	CH10
PA1		CH9
	PA0	CH8
PD15		CH7
	PD14	CH6
PD13		CH5
	PD12	CH4
PD11		CH3
	PD10	CH2
PD9		CH1
		CH0