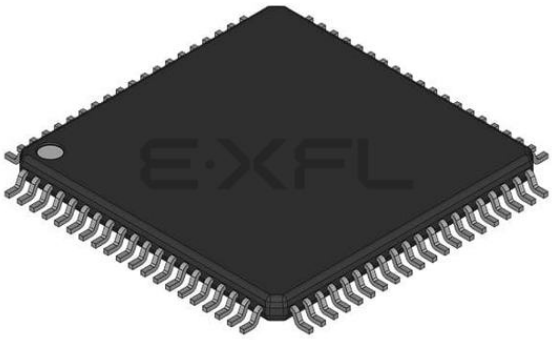

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, I²C, IrDA, SD, SPI, UART/USART
Peripherals	DMA, I²S, LCD, LVD, POR, PWM, WDT
Number of I/O	56
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 64x16b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mk30dn512zvlk10

3.1.1 Example

This is an example of an operating requirement:

Symbol	Description	Min.	Max.	Unit
V_{DD}	1.0 V core supply voltage	0.9	1.1	V

3.2 Definition: Operating behavior

An *operating behavior* is a specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions.

3.2.1 Example

This is an example of an operating behavior:

Symbol	Description	Min.	Max.	Unit
I_{WP}	Digital I/O weak pullup/ pulldown current	10	130	µA

3.3 Definition: Attribute

An *attribute* is a specified value or range of values for a technical characteristic that are guaranteed, regardless of whether you meet the operating requirements.

3.3.1 Example

This is an example of an attribute:

Symbol	Description	Min.	Max.	Unit
CIN_D	Input capacitance: digital pins	—	7	pF

4 Ratings

4.1 Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T_{STG}	Storage temperature	–55	150	°C	1
T_{SDR}	Solder temperature, lead-free	—	260	°C	2
	Solder temperature, leaded	—	245		

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

4.2 Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

4.3 ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V_{HBM}	Electrostatic discharge voltage, human body model	-2000	+2000	V	1
V_{CDM}	Electrostatic discharge voltage, charged-device model	-500	+500	V	2
I_{LAT}	Latch-up current at ambient temperature of 105°C	-100	+100	mA	3

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.
3. Determined according to JEDEC Standard JESD78, *IC Latch-Up Test*.

4.4 Voltage and current operating ratings

5.2.3 Voltage and current operating behaviors

Table 4. Voltage and current operating behaviors

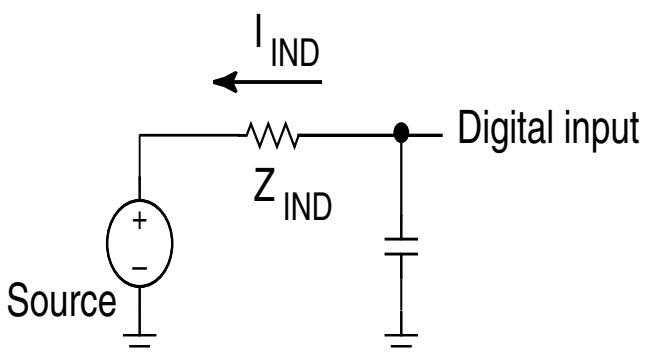
Symbol	Description	Min.	Typ.[1]	Max.	Unit	Notes
V_{OH}	Output high voltage — high drive strength					
	• 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OH} = -9mA	V_{DD} – 0.5	—	—	V	
	• 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OH} = -3mA	V_{DD} – 0.5	—	—	V	
	Output high voltage — low drive strength					
	• 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OH} = -2mA	V_{DD} – 0.5	—	—	V	
	• 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OH} = -0.6mA	V_{DD} – 0.5	—	—	V	
I_{OHT}	Output high current total for all ports	—	—	100	mA	
V_{OL}	Output low voltage — high drive strength					2
	• 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OL} = 9mA	—	—	0.5	V	
	• 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OL} = 3mA	—	—	0.5	V	
	Output low voltage — low drive strength					
	• 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OL} = 2mA	—	—	0.5	V	
	• 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OL} = 0.6mA	—	—	0.5	V	
I_{OLT}	Output low current total for all ports	—	—	100	mA	
I_{INA}	Input leakage current, analog pins and digital pins configured as analog inputs					3, 4
	• V_{SS} ≤ V_{IN} ≤ V_{DD}					
	— All pins except EXTAL32, XTAL32, EXTAL, XTAL	—	0.002	0.5	µA	
	— EXTAL (PTA18) and XTAL (PTA19)	—	0.004	1.5	µA	
	— EXTAL32, XTAL32	—	0.075	10	µA	
I_{IND}	Input leakage current, digital pins					4, 5
	• V_{SS} ≤ V_{IN} ≤ V_{IL}					
	— All digital pins	—	0.002	0.5	µA	
	• V_{IN} = V_{DD}					
	— All digital pins except PTD7	—	0.002	0.5	µA	
	— PTD7	—	0.004	1	µA	
I_{IND}	Input leakage current, digital pins					4, 5, 6
	• V_{IL} < V_{IN} < V_{DD}					
	— V_{DD} = 3.6 V	—	18	26	µA	
	— V_{DD} = 3.0 V	—	12	49	µA	
	— V_{DD} = 2.5 V	—	8	13	µA	
	— V_{DD} = 1.7 V	—	3	6	µA	

Table continues on the next page...

Table 4. Voltage and current operating behaviors (continued)

Symbol	Description	Min.	Typ.[1]	Max.	Unit	Notes
I_{IND}	Input leakage current, digital pins • $V_{DD} < V_{IN} < 5.5$ V	— —	 1	 50	 μA	4, 5
Z_{IND}	Input impedance examples, digital pins • V_{DD} = 3.6 V • V_{DD} = 3.0 V • V_{DD} = 2.5 V • V_{DD} = 1.7 V	 — — — —	 — — — —	 48 55 57 85	 kΩ kΩ kΩ kΩ	4, 7
R_{PU}	Internal pullup resistors	20	35	50	kΩ	8
R_{PD}	Internal pulldown resistors	20	35	50	kΩ	9

1. Typical values characterized at 25°C and VDD = 3.6 V unless otherwise noted.
2. Open drain outputs must be pulled to V_{DD}.
3. Analog pins are defined as pins that do not have an associated general purpose I/O port function.
4. Digital pins have an associated GPIO port function and have 5V tolerant inputs, except EXTAL and XTAL.
5. Internal pull-up/pull-down resistors disabled.
6. Characterized, not tested in production.
7. Examples calculated using V_{IL} relation, V_{DD}, and max I_{IND}: $Z_{IND}=V_{IL}/I_{IND}$. This is the impedance needed to pull a high signal to a level below V_{IL} due to leakage when $V_{IL} < V_{IN} < V_{DD}$. These examples assume signal source low = 0 V.
8. Measured at V_{DD} supply voltage = V_{DD} min and Vinput = V_{SS}
9. Measured at V_{DD} supply voltage = V_{DD} min and Vinput = V_{DD}



5.2.4 Power mode transition operating behaviors

All specifications except t_{POR}, and VLLSx→RUN recovery times in the following table assume this clock configuration:

- CPU and system clocks = 100 MHz
- Bus clock = 50 MHz
- Flash clock = 25 MHz
- MCG mode: FEI

Table 6. Power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DD_VLPR}	Very-low-power run mode current at 3.0 V — all peripheral clocks enabled	—	N/A	—	mA	7
I_{DD_VLPW}	Very-low-power wait mode current at 3.0 V — all peripheral clocks disabled	—	N/A	—	mA	8
I_{DD_STOP}	Stop mode current at 3.0 V					
	• @ –40 to 25°C	—	0.59	1.4	mA	
	• @ 70°C	—	2.26	7.9	mA	
	• @ 105°C	—	5.94	19.2	mA	
I_{DD_VLPS}	Very-low-power stop mode current at 3.0 V					
	• @ –40 to 25°C	—	93	435	µA	
	• @ 70°C	—	520	2000	µA	
	• @ 105°C	—	1350	4000	µA	
I_{DD_LLS}	Low leakage stop mode current at 3.0 V					9
	• @ –40 to 25°C	—	4.8	20	µA	
	• @ 70°C	—	28	68	µA	
	• @ 105°C	—	126	270	µA	
I_{DD_VLLS3}	Very low-leakage stop mode 3 current at 3.0 V					9
	• @ –40 to 25°C	—	3.1	8.9	µA	
	• @ 70°C	—	17	35	µA	
	• @ 105°C	—	82	148	µA	
I_{DD_VLLS2}	Very low-leakage stop mode 2 current at 3.0 V					
	• @ –40 to 25°C	—	2.2	5.4	µA	
	• @ 70°C	—	7.1	12.5	µA	
	• @ 105°C	—	41	125	µA	
I_{DD_VLLS1}	Very low-leakage stop mode 1 current at 3.0 V					
	• @ –40 to 25°C	—	2.1	7.6	µA	
	• @ 70°C	—	6.2	13.5	µA	
	• @ 105°C	—	30	46	µA	
I_{DD_VBAT}	Average current with RTC and 32kHz disabled at 3.0 V					
	• @ –40 to 25°C	—	0.33	0.39	µA	
	• @ 70°C	—	0.60	0.78	µA	
	• @ 105°C	—	1.97	2.9	µA	

Table continues on the next page...

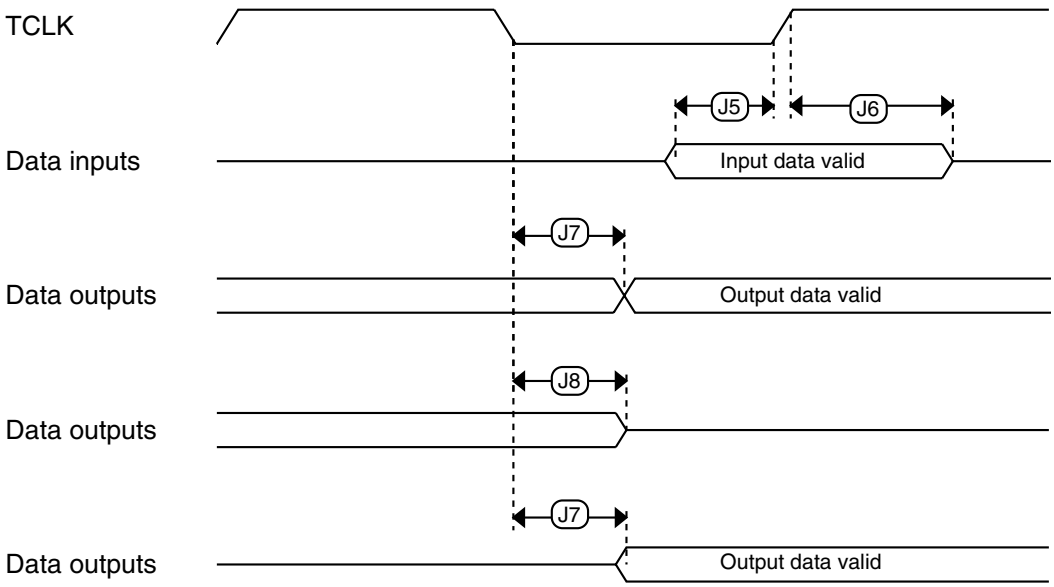


Figure 6. Boundary scan (JTAG) timing

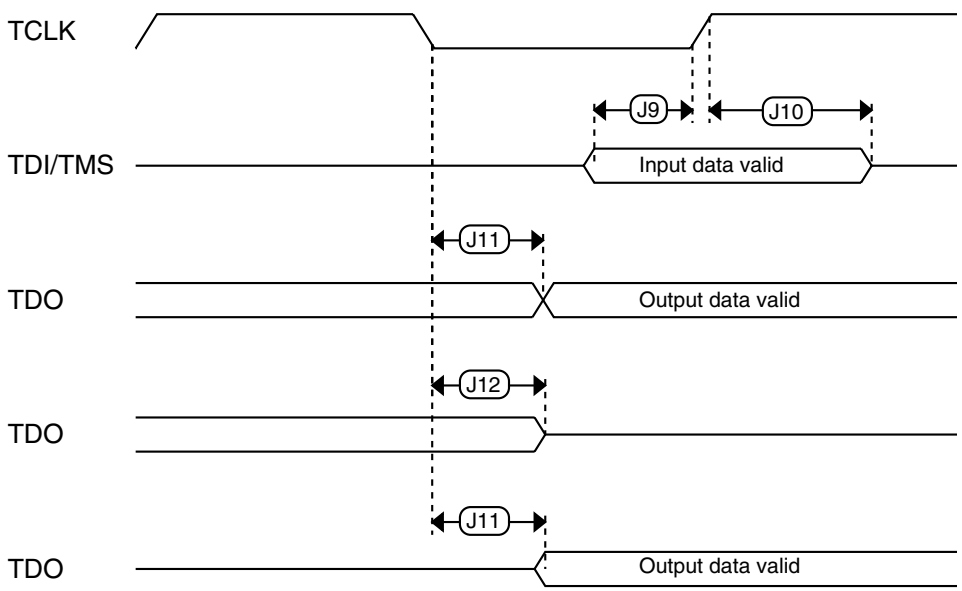


Figure 7. Test Access Port timing

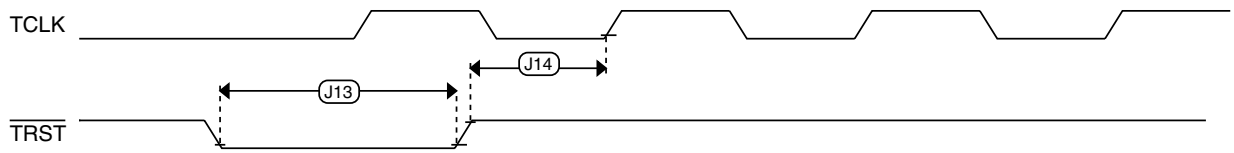


Figure 8. $\overline{\text{TRST}}$ timing

6.2 System modules

There are no specifications necessary for the device's system modules.

6.3 Clock modules

6.3.1 MCG specifications

Table 15. MCG specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{ints_ft}	Internal reference frequency (slow clock) — factory trimmed at nominal VDD and 25 °C	—	32.768	—	kHz	
f_{ints_t}	Internal reference frequency (slow clock) — user trimmed — over fixed voltage and temperature range of 0–70°C	31.25	—	38.2	kHz	
$\Delta_{fdco\_res\_t}$	Resolution of trimmed average DCO output frequency at fixed voltage and temperature — using SCTRIM and SCFTRIM	—	± 0.3	± 0.6	$\%f_{dco}$	1
Δf_{dco_t}	Total deviation of trimmed average DCO output frequency over fixed voltage and temperature range of 0–70°C	—	± 1.5	± 4.5	$\%f_{dco}$	1
f_{intf_ft}	Internal reference frequency (fast clock) — factory trimmed at nominal VDD and 25°C	—	4	—	MHz	
f_{intf_t}	Internal reference frequency (fast clock) — user trimmed at nominal VDD and 25 °C	3	—	5	MHz	
f_{loc_low}	Loss of external clock minimum frequency — RANGE = 00	(3/5) x f_{ints_t}	—	—	kHz	
f_{loc_high}	Loss of external clock minimum frequency — RANGE = 01, 10, or 11	(16/5) x f_{ints_t}	—	—	kHz	
FLL						
f_{fll_ref}	FLL reference frequency range	31.25	—	39.0625	kHz	

Table continues on the next page...

Table 21. Flash command timing specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
t_{pgmchk}	Program Check execution time	—	—	45	µs	1
t_{rdrsrc}	Read Resource execution time	—	—	30	µs	1
t_{pgm4}	Program Longword execution time	—	65	145	µs	
$t_{ersblk256k}$	Erase Flash Block execution time • 256 KB program/data flash	—	435	3700	ms	2
t_{ersscr}	Erase Flash Sector execution time	—	14	114	ms	2
	Program Section execution time					
$t_{pgmsec512}$	• 512 bytes flash	—	2.4	—	ms	
$t_{pgmsec1k}$	• 1 KB flash	—	4.7	—	ms	
$t_{pgmsec2k}$	• 2 KB flash	—	9.3	—	ms	
t_{rd1all}	Read 1s All Blocks execution time	—	—	1.8	ms	
t_{rdonce}	Read Once execution time	—	—	25	µs	1
$t_{pgmonce}$	Program Once execution time	—	65	—	µs	
t_{ersall}	Erase All Blocks execution time	—	870	7400	ms	2
t_{vfykey}	Verify Backdoor Access Key execution time	—	—	30	µs	1
	Swap Control execution time					
$t_{swapx01}$	• control code 0x01	—	200	—	µs	
$t_{swapx02}$	• control code 0x02	—	70	150	µs	
$t_{swapx04}$	• control code 0x04	—	70	150	µs	
$t_{swapx08}$	• control code 0x08	—	—	30	µs	

1. Assumes 25 MHz flash clock frequency.
2. Maximum times for erase parameters based on expectations at cycling end-of-life.

6.4.1.3 Flash high voltage current behaviors

Table 22. Flash high voltage current behaviors

Symbol	Description	Min.	Typ.	Max.	Unit
I_{DD_PGM}	Average current adder during high voltage flash programming operation	—	2.5	6.0	mA
I_{DD_ERS}	Average current adder during high voltage flash erase operation	—	1.5	4.0	mA

6.4.1.4 Reliability specifications

Table 23. NVM reliability specifications

Symbol	Description	Min.	Typ.[1]	Max.	Unit	Notes
	Program Flash					

Table continues on the next page...

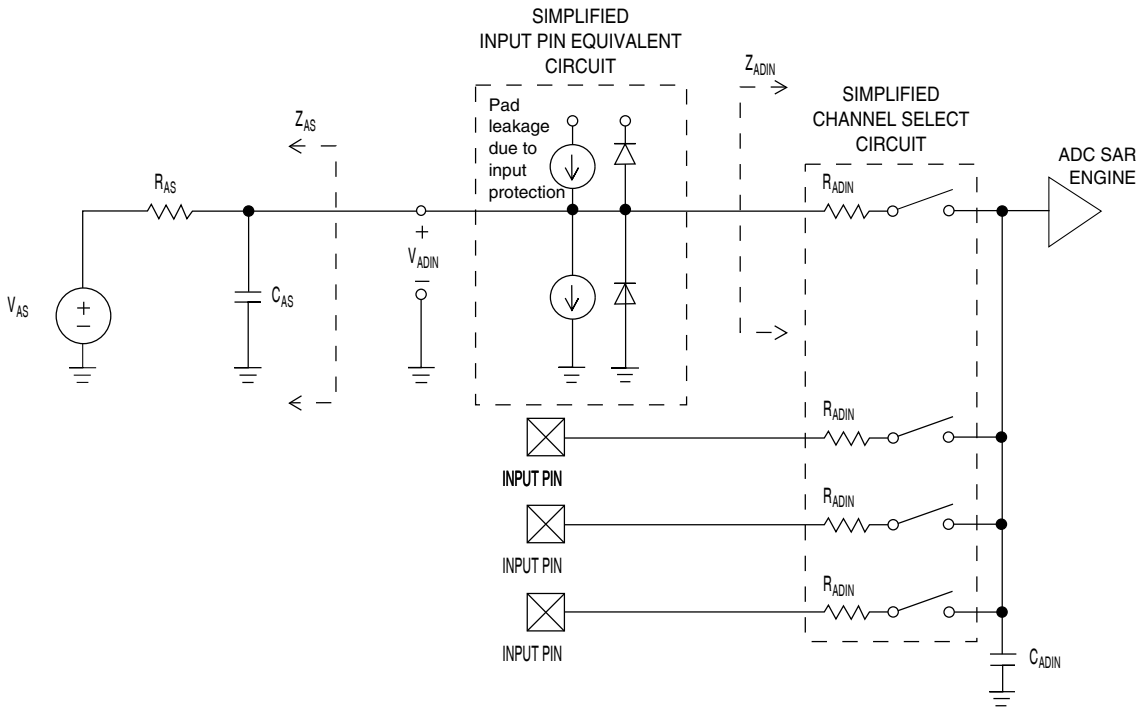


Figure 10. ADC input impedance equivalency diagram

6.6.1.2 16-bit ADC electrical characteristics

Table 26. 16-bit ADC characteristics (V_{REFH} = V_{DDA}, V_{REFL} = V_{SSA})

Symbol	Description	Conditions[1]	Min.	Typ.[2]	Max.	Unit	Notes
I_{DDA_ADC}	Supply current		0.215	—	1.7	mA	3
f_{ADACK}	ADC asynchronous clock source	• ADLPC = 1, ADHSC = 0 • ADLPC = 1, ADHSC = 1 • ADLPC = 0, ADHSC = 0 • ADLPC = 0, ADHSC = 1	1.2 2.4 3.0 4.4	2.4 4.0 5.2 6.2	3.9 6.1 7.3 9.5	MHz MHz MHz MHz	t_{ADACK} = 1/ f_{ADACK}
	Sample Time	See Reference Manual chapter for sample times					
TUE	Total unadjusted error	• 12-bit modes • <12-bit modes	— —	±4 ±1.4	±6.8 ±2.1	LSB[4]	5
DNL	Differential non-linearity	• 12-bit modes • <12-bit modes	— —	±0.7 ±0.2	-1.1 to +1.9 -0.3 to 0.5	LSB[4]	5
INL	Integral non-linearity	• 12-bit modes • <12-bit modes	— —	±1.0 ±0.5	-2.7 to +1.9 -0.7 to +0.5	LSB[4]	5
E_{FS}	Full-scale error	• 12-bit modes • <12-bit modes	— —	-4 -1.4	-5.4 -1.8	LSB[4]	V_{ADIN} = V_{DDA} 5

Table continues on the next page...

Table 29. Comparator and 6-bit DAC electrical specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit
V_H	Analog comparator hysteresis[1]				
	• CR0[HYSTCTR] = 00	—	5	—	mV
	• CR0[HYSTCTR] = 01	—	10	—	mV
	• CR0[HYSTCTR] = 10	—	20	—	mV
	• CR0[HYSTCTR] = 11	—	30	—	mV
V_{CMPOh}	Output high	V_{DD} – 0.5	—	—	V
V_{CMPOl}	Output low	—	—	0.5	V
t_{DHS}	Propagation delay, high-speed mode (EN=1, PMODE=1)	20	50	200	ns
t_{DLS}	Propagation delay, low-speed mode (EN=1, PMODE=0)	80	250	600	ns
	Analog comparator initialization delay[2]	—	—	40	µs
I_{DAC6b}	6-bit DAC current adder (enabled)	—	7	—	µA
INL	6-bit DAC integral non-linearity	–0.5	—	0.5	LSB[3]
DNL	6-bit DAC differential non-linearity	–0.3	—	0.3	LSB

1. Typical hysteresis is measured with input voltage range limited to 0.6 to V_{DD}-0.6 V.
2. Comparator initialization delay is defined as the time between software writes to change control inputs (Writes to DACEN, VRSEL, PSEL, MSEL, VOSEL) and the comparator output settling to a stable level.
3. 1 LSB = $V_{reference}$/64

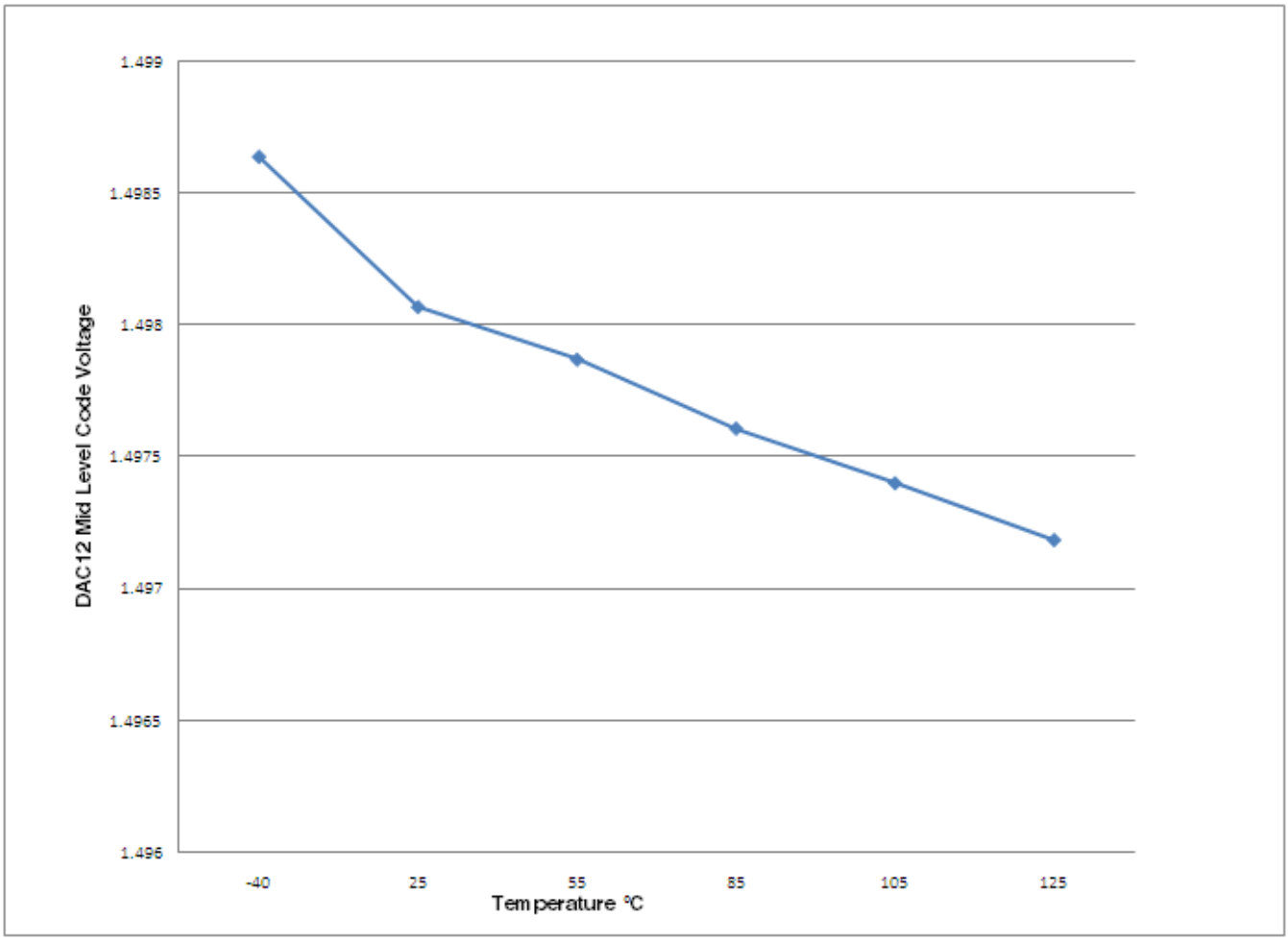


Figure 16. Offset at half scale vs. temperature

6.6.4 Voltage reference electrical specifications

Table 32. VREF full-range operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
V_{DDA}	Supply voltage	1.71	3.6	V	
T_A	Temperature	Operating temperature range of the device		°C	
C_L	Output load capacitance	100		nF	1, 2

1. C_L must be connected to VREF_OUT if the VREF_OUT functionality is being used for either an internal or external reference.
2. The load capacitance should not exceed +/-25% of the nominal specified C_L value over the operating temperature range of the device.

Table 37. Slave mode DSPI timing (limited voltage range)

Num	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
	Frequency of operation		12.5	MHz
DS9	DSPI_SCK input cycle time	4 x t_{BUS}	—	ns
DS10	DSPI_SCK input high/low time	(t_{SCK}/2) – 2	(t_{SCK}/2) + 2	ns
DS11	DSPI_SCK to DSPI_SOUT valid	—	10	ns
DS12	DSPI_SCK to DSPI_SOUT invalid	0	—	ns
DS13	DSPI_SIN to DSPI_SCK input setup	2	—	ns
DS14	DSPI_SCK to DSPI_SIN input hold	7	—	ns
DS15	$\overline{\text{DSPI\_SS}}$ active to DSPI_SOUT driven	—	14	ns
DS16	$\overline{\text{DSPI\_SS}}$ inactive to DSPI_SOUT not driven	—	14	ns

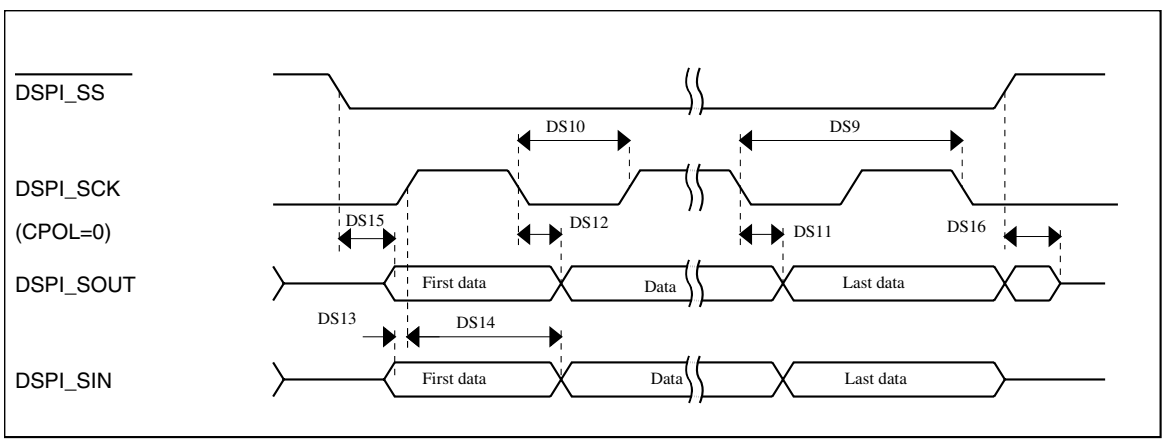


Figure 18. DSPI classic SPI timing — slave mode

6.8.3 DSPI switching specifications (full voltage range)

The DMA Serial Peripheral Interface (DSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The tables below provides DSPI timing characteristics for classic SPI timing modes. Refer to the DSPI chapter of the Reference Manual for information on the modified transfer formats used for communicating with slower peripheral devices.

Table 38. Master mode DSPI timing (full voltage range)

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	1.71	3.6	V	1
	Frequency of operation	—	12.5	MHz	
DS1	DSPI_SCK output cycle time	4 x t_{BUS}	—	ns	

Table continues on the next page...

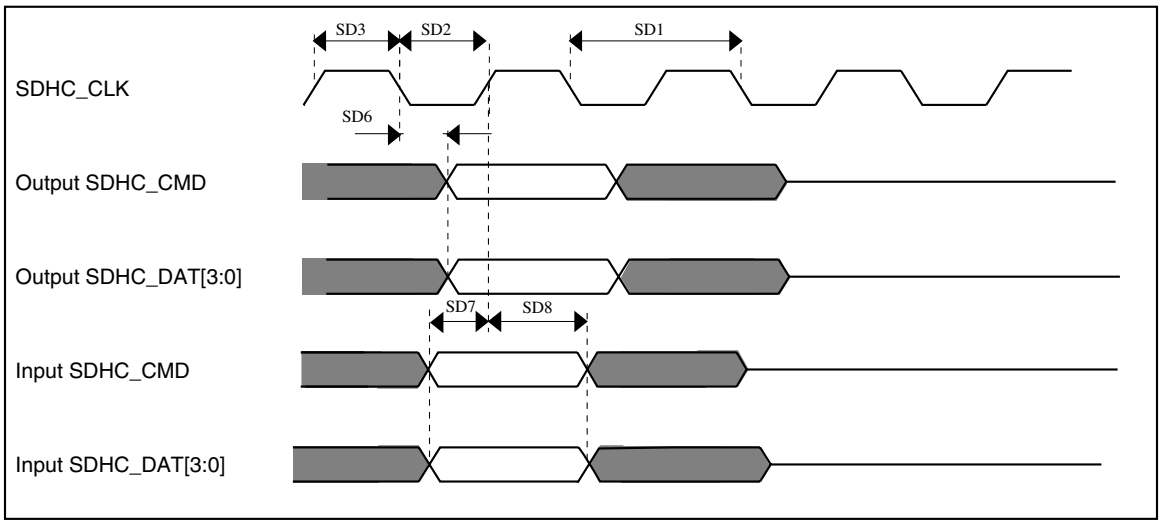


Figure 22. SDHC timing

6.8.7 I²S switching specifications

This section provides the AC timings for the I²S in master (clocks driven) and slave modes (clocks input). All timings are given for non-inverted serial clock polarity (TCR[TSCKP] = 0, RCR[RSCKP] = 0) and a non-inverted frame sync (TCR[TFSI] = 0, RCR[RFSI] = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timings remain valid by inverting the clock signal (I2S_BCLK) and/or the frame sync (I2S_FS) shown in the figures below.

Table 42. I²S master mode timing (limited voltage range)

Num	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
S1	I2S_MCLK cycle time	2 x t_{SYS}		ns
S2	I2S_MCLK pulse width high/low	45%	55%	MCLK period
S3	I2S_BCLK cycle time	5 x t_{SYS}	—	ns
S4	I2S_BCLK pulse width high/low	45%	55%	BCLK period
S5	I2S_BCLK to I2S_FS output valid	—	15	ns
S6	I2S_BCLK to I2S_FS output invalid	-2.5	—	ns
S7	I2S_BCLK to I2S_TXD valid	—	15	ns
S8	I2S_BCLK to I2S_TXD invalid	-3	—	ns
S9	I2S_RXD/I2S_FS input setup before I2S_BCLK	20	—	ns
S10	I2S_RXD/I2S_FS input hold after I2S_BCLK	0	—	ns

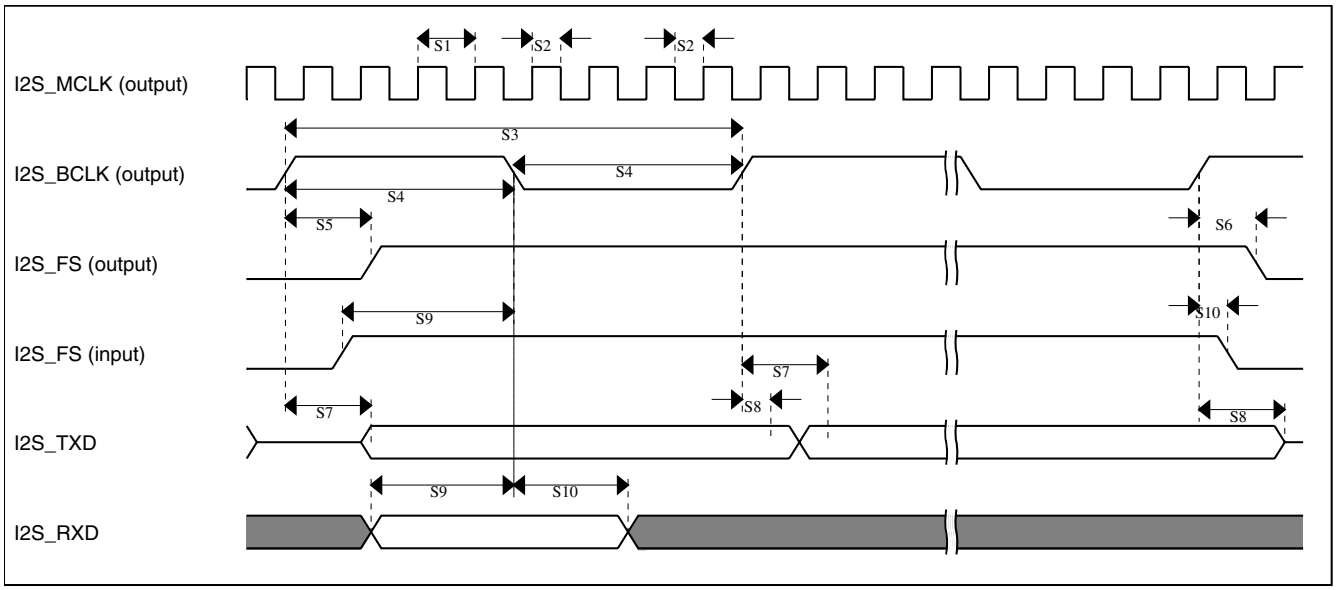


Figure 23. I²S timing — master mode

Table 43. I²S slave mode timing (limited voltage range)

Num	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
S11	I2S_BCLK cycle time (input)	8 x t_{SYS}	—	ns
S12	I2S_BCLK pulse width high/low (input)	45%	55%	MCLK period
S13	I2S_FS input setup before I2S_BCLK	10	—	ns
S14	I2S_FS input hold after I2S_BCLK	3	—	ns
S15	I2S_BCLK to I2S_TXD/I2S_FS output valid	—	20	ns
S16	I2S_BCLK to I2S_TXD/I2S_FS output invalid	0	—	ns
S17	I2S_RXD setup before I2S_BCLK	10	—	ns
S18	I2S_RXD hold after I2S_BCLK	2	—	ns

2. For highest glass capacitance values, LCD_GCR[LADJ] should be configured as specified in the LCD Controller chapter within the device's reference manual.
3. V_{IREG} maximum should never be externally driven to any level other than V_{DD} - 0.15 V
4. 2000 pF load LCD, 32 Hz frame frequency

7 Dimensions

7.1 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to freescale.com and perform a keyword search for the drawing's document number:

If you want the drawing for this package	Then use this document number
80-pin LQFP	98ASS23174W
81-pin MAPBGA	98ASA00344D

8 Pinout

8.1 K30 Signal Multiplexing and Pin Assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The Port Control Module is responsible for selecting which ALT functionality is available on each pin.

NOTE

The 81-pin ballmap assignments are currently being developed. The • in the entries in this package column indicate which signals are present on the package.

81 MAP BGA	80 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
E4	1	PTE0	ADC1_SE4a	ADC1_SE4a	PTE0	SPI1_PCS1	UART1_TX	SDHC0_D1		I2C1_SDA		
E3	2	PTE1/ LLWU_P0	ADC1_SE5a	ADC1_SE5a	PTE1/ LLWU_P0	SPI1_SOUT	UART1_RX	SDHC0_D0		I2C1_SCL		
E2	3	PTE2/ LLWU_P1	ADC1_SE6a	ADC1_SE6a	PTE2/ LLWU_P1	SPI1_SCK	UART1_CTS_ b	SDHC0_DCLK				
F4	4	PTE3	ADC1_SE7a	ADC1_SE7a	PTE3	SPI1_SIN	UART1_RTS_ b	SDHC0_CMD				

81 MAP BGA	80 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
C10	50	PTB11	LCD_P11/ ADC1_SE15	LCD_P11/ ADC1_SE15	PTB11	SPI1_SCK	UART3_TX			FTM0_FLT2	LCD_P11	
B10	51	PTB16	LCD_P12/ TSI0_CH9	LCD_P12/ TSI0_CH9	PTB16	SPI1_SOUT	UART0_RX			EWM_IN	LCD_P12	
E9	52	PTB17	LCD_P13/ TSI0_CH10	LCD_P13/ TSI0_CH10	PTB17	SPI1_SIN	UART0_TX			EWM_OUT_b	LCD_P13	
D9	53	PTB18	LCD_P14/ TSI0_CH11	LCD_P14/ TSI0_CH11	PTB18	CAN0_TX	FTM2_CH0	I2S0_TX_ BCLK		FTM2_QD_ PHA	LCD_P14	
C9	54	PTB19	LCD_P15/ TSI0_CH12	LCD_P15/ TSI0_CH12	PTB19	CAN0_RX	FTM2_CH1	I2S0_TX_FS		FTM2_QD_ PHB	LCD_P15	
B9	55	PTC0	LCD_P20/ ADC0_SE14/ TSI0_CH13	LCD_P20/ ADC0_SE14/ TSI0_CH13	PTC0	SPI0_PCS4	PDB0_EXTRG	I2S0_TXD			LCD_P20	
D8	56	PTC1/ LLWU_P6	LCD_P21/ ADC0_SE15/ TSI0_CH14	LCD_P21/ ADC0_SE15/ TSI0_CH14	PTC1/ LLWU_P6	SPI0_PCS3	UART1_RTS_ b	FTM0_CH0			LCD_P21	
C8	57	PTC2	LCD_P22/ ADC0_SE4b/ CMP1_IN0/ TSI0_CH15	LCD_P22/ ADC0_SE4b/ CMP1_IN0/ TSI0_CH15	PTC2	SPI0_PCS2	UART1_CTS_ b	FTM0_CH1			LCD_P22	
B8	58	PTC3/ LLWU_P7	LCD_P23/ CMP1_IN1	LCD_P23/ CMP1_IN1	PTC3/ LLWU_P7	SPI0_PCS1	UART1_RX	FTM0_CH2			LCD_P23	
—	59	VSS	VSS	VSS								
A11	60	VLL3	VLL3	VLL3								
A10	61	VLL2	VLL2	VLL2								
A9	62	VLL1	VLL1	VLL1								
B11	63	VCAP2	VCAP2	VCAP2								
C11	64	VCAP1	VCAP1	VCAP1								
A8	65	PTC4/ LLWU_P8	LCD_P24	LCD_P24	PTC4/ LLWU_P8	SPI0_PCS0	UART1_TX	FTM0_CH3		CMP1_OUT	LCD_P24	
D7	66	PTC5/ LLWU_P9	LCD_P25	LCD_P25	PTC5/ LLWU_P9	SPI0_SCK		LPT0_ALT2		CMP0_OUT	LCD_P25	
C7	67	PTC6/ LLWU_P10	LCD_P26/ CMP0_IN0	LCD_P26/ CMP0_IN0	PTC6/ LLWU_P10	SPI0_SOUT	PDB0_EXTRG				LCD_P26	
B7	68	PTC7	LCD_P27/ CMP0_IN1	LCD_P27/ CMP0_IN1	PTC7	SPI0_SIN					LCD_P27	
A7	69	PTC8	LCD_P28/ ADC1_SE4b/ CMP0_IN2	LCD_P28/ ADC1_SE4b/ CMP0_IN2	PTC8		I2S0_MCLK	I2S0_CLKIN			LCD_P28	
D6	70	PTC9	LCD_P29/ ADC1_SE5b/ CMP0_IN3	LCD_P29/ ADC1_SE5b/ CMP0_IN3	PTC9			I2S0_RX_ BCLK		FTM2_FLT0	LCD_P29	
C6	71	PTC10	LCD_P30/ ADC1_SE6b/ CMP0_IN4	LCD_P30/ ADC1_SE6b/ CMP0_IN4	PTC10	I2C1_SCL		I2S0_RX_FS			LCD_P30	
C5	72	PTC11/ LLWU_P11	LCD_P31/ ADC1_SE7b	LCD_P31/ ADC1_SE7b	PTC11/ LLWU_P11	I2C1_SDA		I2S0_RXD			LCD_P31	

81 MAP BGA	80 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
C4	—	NC	NC	NC								
B4	—	NC	NC	NC								
A4	—	NC	NC	NC								
B1	—	NC	NC	NC								
C1	—	NC	NC	NC								
D1	—	NC	NC	NC								
E1	—	NC	NC	NC								
C2	—	NC	NC	NC								
D2	—	NC	NC	NC								

8.2 K30 Pinouts

The below figure shows the pinout diagram for the devices supported by this document. Many signals may be multiplexed onto a single pin. To determine what signals can be used on which pin, see the previous section.

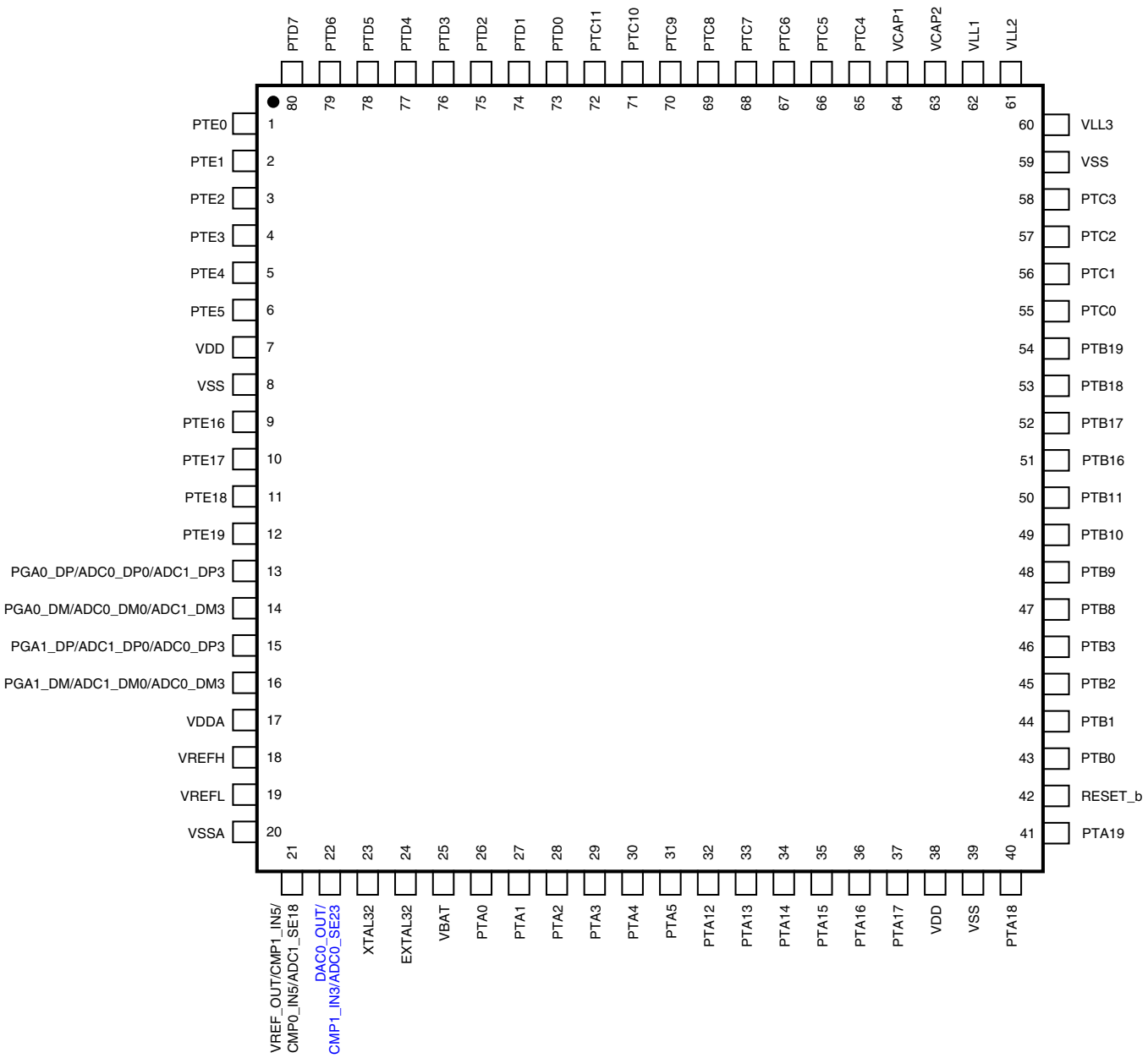


Figure 26. K30 80 LQFP Pinout Diagram

9 Revision History

The following table provides a revision history for this document.

Table 48. Revision History

Rev. No.	Date	Substantial Changes
1	11/2010	Initial public revision

Table continues on the next page...

Table 48. Revision History (continued)

Rev. No.	Date	Substantial Changes
2	3/2011	Many updates throughout Corrected 81- and 104-pin package codes
3	3/2011	Added sections that were inadvertently removed in previous revision
4	3/2011	Reworded I_{IC} footnote in "Voltage and Current Operating Requirements" table. Added paragraph to "Peripheral operating requirements and behaviors" section. Added "JTAG full voltage range electricals" table to the "JTAG electricals" section.
5	6/2011	• Changed supported part numbers per new part number scheme • Changed *DC injection current* specs in "Voltage and current operating requirements" table • Changed *Input leakage current* and *internal pullup/pulldown resistor* specs in "Voltage and current operating behaviors" table • Split *Low power stop mode current* specs by temperature range in "Power consumption operating behaviors" table • Changed typical I_{DD_VBAT} spec in "Power consumption operating behaviors" table • Added LPTMR clock specs to "Device clock specifications" table • Changed *Minimum external reset pulse width* in "General switching specifications" table • Changed *PLL operating current* in "MCG specifications" table • Added footnote to *PLL period jitter* in "MCG specifications" table • Changed *Supply current* in "Oscillator DC electrical specifications" table • Changed *Crystal startup time* in "Oscillator frequency specifications" table • Changed *Operating voltage* in "EzPort switching specifications" table • Changed *ADC asynchronous clock source* specs in "16-bit ADC characteristics" table • Changed *Gain* spec in "16-bit ADC with PGA characteristics" table • Added typical *Input DC current* to "16-bit ADC with PGA characteristics" table • Changed *Input offset voltage* and *ENOB* notes field in "16-bit ADC with PGA characteristics" table • Changed *Analog comparator initialization delay* in "Comparator and 6-bit DAC electrical specifications" • Changed *Code-to-code settling time*, *DAC output voltage range low*, and *Temperature coefficient offset voltage* in "12-bit DAC operating behaviors" table • Changed *Temperature drift* and *Load regulation* in "VREF full-range operating behaviors" table • Changed *DSPI_SCK cycle time* specs in "DSPI timing" tables • Changed $\overline{\text{DSPI\_SS}}$ specs in "Slave mode DSPI timing (low-speed mode)" table • Changed *DSPI_SCK to DSPI_SOUT valid* spec in "Slave mode DSPI timing (high-speed mode)" table • Changed *Reference oscillator current source base current* spec and added *Low-power current adder* footer in "TSI electrical specifications" table • Added *LCD glass capacitance* footnote

Table continues on the next page...

Table 48. Revision History (continued)

Rev. No.	Date	Substantial Changes
6	01/2012	• Added AC electrical specifications. • Replaced TBDs with silicon data throughout. • In "Power mode transition operating behaviors" table, removed entry times. • Updated "EMC radiated emissions operating behaviors" to remove SAE level and also added data for 144LQFP. • Clarified "EP7" in "EzPort switching specifications" table and "EzPort Timing Diagram". • Added "ENOB vs. ADC_CLK for 16-bit differential and 16-bit single-ended modes" figures. • Updated I_{DD_RUN} numbers in 'Power consumption operating behaviors' section. • Clarified 'Diagram: Typical IDD_RUN operating behavior' section and updated 'Run mode supply current vs. core frequency — all peripheral clocks disabled' figure. • In 'Voltage reference electrical specifications' section, updated C_L, V_{tdrift}, and V_{vdrift} values. • In 'LCD electrical characteristics' section, updated V_{IREG} and Δ_{RTRIM} values.
7	02/2013	• In "ESD handling ratings", added a note for I_{LAT}. • Updated "Voltage and current operating requirements". • Updated "Voltage and current operating behaviors". • Updated "Power mode transition operating behaviors". • Updated "EMC radiated emissions operating behaviors" to add MAPBGA data. • In "MCG specifications", updated the description of f_{ints_t}. • In "16-bit ADC operating conditions", updated the max spec of V_{ADIN}. • In "16-bit ADC electrical characteristics", updated the temp sensor slope and voltage specs. • Updated "I2C switching specifications". • In "SDHC specifications", removed the operating voltage limits and updated the SD1 and SD6 specs. • In "I2S switching specifications", added separate specification tables for the full operating voltage range.