Toshiba Semiconductor and Storage - TMPM362F10FG(C) Datasheet

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Details	
Product Status	Not For New Designs
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	64MHz
Connectivity	EBI/EMI, I²C, Microwire, SIO, SPI, SSP, UART/USART
Peripherals	DMA, WDT
Number of I/O	104
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 16x10b
Oscillator Type	External
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-FQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/toshiba-semiconductor-and-storage/tmpm362f10fg-c

9. DMA Controller(DMAC)

10. Static Memory Controller

8.2.1.3 PADATA (Port A data register)

	31	30	29	28	27	26	25	24
bit symbol	-	-	-	-	-	-	-	-
After reset	0	0	0	0	0	0	0	0
	23	22	21	20	19	18	17	16
bit symbol	-	-	-	-	-	-	-	-
After reset	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8
bit symbol	-	-	-	-	-	-	-	-
After reset	0	0	0	0	0	0	0	0
	7	6	5	4	3	2	1	0
bit symbol	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
After reset	0	0	0	0	0	0	0	0

Bit	Bit Symbol	Type	Function
31-8	−	R	Read as "0".
7-0	PA7 to PA0	R/W	Port A data register

8.2.1.4 PACR (Port A output control register)

	31	30	29	28	27	26	25	24
bit symbol	-	-	-	-	-	-	-	-
After reset	0	0	0	0	0	0	0	0
	23	22	21	20	19	18	17	16
bit symbol	-	-	-	-	-	-	-	-
After reset	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8
bit symbol	-	-	-	-	-	-	-	-
After reset	0	0	0	0	0	0	0	0
	7	6	5	4	3	2	1	0
bit symbol	PA7C	PA6C	PA5C	PA4C	PA3C	PA2C	PA1C	PA0C
After reset	0	0	0	0	0	0	0	0

Bit	Bit Symbol	Type	Function
31-8	−	R	Read as "0".
7-0	PA7C to PA0C	R/W	Output 0: Disable 1: Enable

8.2.3.7 PCFR3 (Port C function register 3)

	31	30	29	28	27	26	25	24
bit symbol	-	-	-	-	-	-	-	-
After reset	0	0	0	0	0	0	0	0
	23	22	21	20	19	18	17	16
bit symbol	-	-	-	-	-	-	-	-
After reset	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8
bit symbol	-	-	-	-	-	-	-	-
After reset	0	0	0	0	0	0	0	0
	7	6	5	4	3	2	1	0
bit symbol	-	PC6F3	-	-	-	PC2F3	-	-
After reset	0	0	0	0	0	0	0	0

Bit	Bit Symbol	Type	Function
31-7	−	R	Read as "0".
6	PC6F3	R/W	0 : PORT 1 : $\overline{\text{CTS9}}$
5-3	−	R	Read as "0".
2	PC2F3	R/W	0 : PORT 1 : $\overline{\text{CTS8}}$
1-0	−	R	Read as "0".

8.2.3.8 PCOD (Port C open drain control reigister)

	31	30	29	28	27	26	25	24
bit symbol	-	-	-	-	-	-	-	-
After reset	0	0	0	0	0	0	0	0
	23	22	21	20	19	18	17	16
bit symbol	-	-	-	-	-	-	-	-
After reset	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8
bit symbol	-	-	-	-	-	-	-	-
After reset	0	0	0	0	0	0	0	0
	7	6	5	4	3	2	1	0
bit symbol	PC7OD	PC6OD	PC5OD	PC4OD	PC3OD	PC2OD	PC1OD	PC0OD
After reset	0	0	0	0	0	0	0	0

Bit	Bit Symbol	Type	Function
31-8	−	R	Read as "0".
7-0	PC7OD to PC0OD	R/W	0 : CMOS 1 : Open-drain

8.4.5 Port E Setting

Table 8-8 Port Setting List (Port E)

Pin	Port Type	Function	After reset	PECR	PEFR1	PEFR2	PEFR3	PEOD	PEPUP	PEIE
PE0	T3	Input port		0	0	0	0	×	×	1
		Output port		1	0	0	0	×	×	0
		Address (Output)		1	1	0	0	×	×	0
		TB5IN0 (Input)		0	0	1	0	×	×	1
PE1	T3	Input port		0	0	0	0	×	×	1
		Output port		1	0	0	0	×	×	0
		Address (Output)		1	1	0	0	×	×	0
		TB5IN1 (Input)		0	0	1	0	×	×	1
PE2	T3	Input port		0	0	0	0	×	×	1
		Output port		1	0	0	0	×	×	0
		Address (Output)		1	1	0	0	×	×	0
		TB6IN0 (Input)		0	0	1	0	×	×	1
PE3	T3	Input port		0	0	0	0	×	×	1
		Output port		1	0	0	0	×	×	0
		Address (Output)		1	1	0	0	×	×	0
		TB6IN1 (Input)		0	0	1	0	×	×	1
PE4	T2	Input port		0	0	0	0	×	×	1
		Output port		1	0	0	0	×	×	0
		Address (Output)		1	1	0	0	×	×	0
		TXD0 (Output)		1	0	1	0	×	×	0
PE5	T3	Input port		0	0	0	0	×	×	1
		Output port		1	0	0	0	×	×	0
		Address (Output)		1	1	0	0	×	×	0
		RXD0 (Input)		0	0	1	0	×	×	1
PE6	T4	Input port		0	0	0	0	×	×	1
		Output port		1	0	0	0	×	×	0
		Address (Output)		1	1	0	0	×	×	0
		SCLK0 (Input)		0	0	1	0	×	×	1
		SCLK0 (Output)		1	0	1	0	×	×	0
		$\overline{\text{CTS0}}$ (Input)		0	0	0	1	×	×	1
PE7	T6	Input port		0	0	0	0	×	×	1
		Output port		1	0	0	0	×	×	0
		INT5 (Input)		0	0	1	0	×	×	1
		SCOUT (Output)		1	0	0	1	×	×	0

Bit	Bit Symbol	Type	Function
0	E	R/W	Channel enable 0 : Disable 1 : Enable This bit can be used to enable/disable the channels. (This bit works as start bit when "Memory to Memory" is selected.) Amount of transfer data specified by DMACxCnControl <TransferSize> is completed, the corresponding <E> is cleared to "0" automatically. Disabling channels during transfer loses the data in the FIFO. Initialize all the channels before restart. To pause the transfer, stop the DMA request by using the <HALT>, and poll the data until the <Active> becomes "0" and then disable the channel with the <E> bit.

Note 1: When "Memory to Memory" is selected, hardware start for DMA startup is not supported. Write "1" <E> for starting transfer.

Note 2: When DMACxENableChns<EnabledCHx> is enabled and the corresponding DMACxCnConfiguration<Halt> is set to "1", write them after channel enable bit (E:bit0) is clear to "0". Without this, in the case of the slave error is occurred when writing them, the error is recovered by reset. Regarding slave error, when the width and address of transfer have mismatch, this error is occurred.

10.3.5 smc_set_cycles (SMC Set Cycles Register)

	31	30	29	28	27	26	25	24
bit symbol	-	-	-	-	-	-	-	-
After reset	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined
	23	22	21	20	19	18	17	16
bit symbol	-	-	-	-	Set_t5			Set_t4
After reset	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined
	15	14	13	12	11	10	9	8
bit symbol	Set_t4		Set_t3			Set_t2		
After reset	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined
	7	6	5	4	3	2	1	0
bit symbol	Set_t1				Set_t0			
After reset	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined

Bit	Bit Symbol	Type	Function
31-20	−	W	Write as "0".
19-17	Set_t5[2:0]	W	Set value of t_{TR} 000 : Setting prohibition 001 to 111 : SMCCLK × 1 clock to SMCCLK × 7 clock
16-14	Set_t4[2:0]	W	Set value of t_{PC} 000 : Setting prohibition 001 to 111 : SMCCLK × 1 clock to SMCCLK × 7 clock Page access is not supported in multiplex bus mode. t_{PC} is effective only separate bus mode.
13-11	Set_t3[2:0]	W	Set value of t_{WP} (note) 000 : Setting prohibition 001 to 111 : SMCCLK × 1 clock to SMCCLK × 7 clock In multiplex mode, write pulse width (t_{WP}) increase for one more clock pulse against for value of <Set_t3>.
10-8	Set_t2[2:0]	W	Set value of t_{CEOE} (note) 000 : Setting prohibition 001 to 111 : SMCCLK × 1 clock to SMCCLK × 7 clock
7-4	Set_t1[3:0]	W	Set value of t_{WC} (note) 0000 : Setting prohibition 0011 to 1111 : SMCCLK × 3 clock to SMCCLK × 15 clock
3-0	Set_t0[3:0]	W	Set value of t_{RC} (note) 0000 : Setting prohibition 0010 to 1111 : SMCCLK × 2 clock to SMCCLK × 15 clock

This register is provided to adjust the access cycle of static memory and should be set to satisfy the A.C. specifications of the memory to be used. Adjust base clock is SMCCLK : fsys/2.

To validate SMC set cycles register setting, it is necessary to execute update register command on smc_direct_cmd register.

Note: It needs to keep below relation.

<Set_t3>,<Set_t1>	Separate bus mode	:(t_{WP} + SMCCLK × 2 clock) ≤ t_{WC}
	Multiplex bus mode	:(t_{WP} + SMCCLK × 3 clock) ≤ t_{WC}
<Set_t2>,<Set_t0>	Separate bus mode	:(t_{CEOE} + SMCCLK × 1 clock) ≤ t_{RC}
	Multiplex bus mode	:(t_{CEOE} + SMCCLK × 1 clock) ≤ t_{RC}

10.3.12 smc_opmode0_1 (SMC Opmode Registers 0<1>)

	31	30	29	28	27	26	25	24
bit symbol	address_match							
After reset	0	1	1	0	0	0	0	1
	23	22	21	20	19	18	17	16
bit symbol	-	-	-	-	-	-	-	-
After reset	1	1	1	1	1	1	1	1
	15	14	13	12	11	10	9	8
bit symbol	-	-	-	-	adv	-	-	-
After reset	Undefined	Undefined	Undefined	Undefined	1	Undefined	Undefined	Undefined
	7	6	5	4	3	2	1	0
bit symbol	-	-	rd_bl			-	mw	
After reset	Undefined	Undefined	0	0	0	Undefined	1	0

Bit	Bit Symbol	Type	Function
31-24	address_match [7:0]	R	Start address of CS1 area Read as "0x61".
23-16	−	R	Read as "0xFF".
15-12	−	R	Read as undefined.
11	adv	R	Address latch enable signal 0 : Address latch enable signal ($\overline{ALE}$) not used 1 : Address latch enable signal ($\overline{ALE}$) used
10-6	−	R	Read as undefined.
5-3	rd_bl[2:0]	R	Burst length of data read 000 : 1 beat 001 : 4 beats 010 to 111 : Don't care
2	−	R	Read as undefined.
1-0	mw[1:0]	R	Data bus width of CS1 01 : 16 bits Others : Don't care

Note: Do not access the external memory area except set CS area.

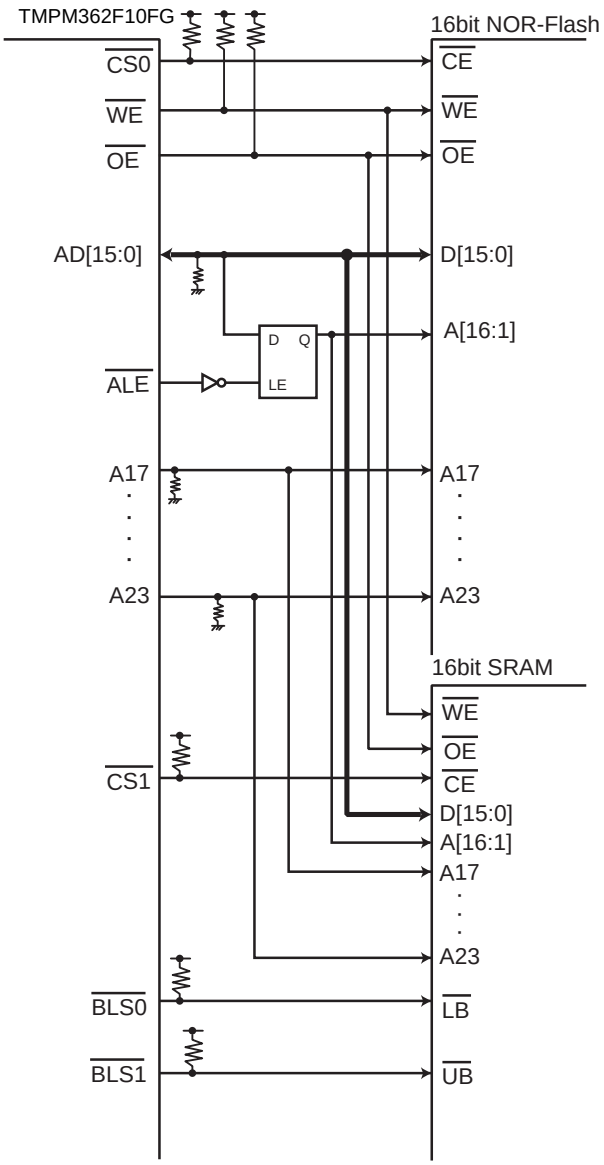


Figure 10-10 Connection example for external 16bit SRAM and NOR-Flash (Multiplex mode)

12.4.3 SCxBUF (Buffer Register)

SCxBUF works as a transmit buffer or FIFO for write operation and as a receive buffer or FIFO for read operation.

	31	30	29	28	27	26	25	24
bit symbol	-	-	-	-	-	-	-	-
After reset	0	0	0	0	0	0	0	0
	23	22	21	20	19	18	17	16
bit symbol	-	-	-	-	-	-	-	-
After reset	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8
bit symbol	-	-	-	-	-	-	-	-
After reset	0	0	0	0	0	0	0	0
	7	6	5	4	3	2	1	0
bit symbol	TB / RB							
After reset	0	0	0	0	0	0	0	0

Bit	Bit Symbol	Type	Function
31-8	−	R	Read as "0".
7-0	TB[7:0] / RB [7:0]	R/W	[write] TB :Transmit buffer / FIFO [read] RB : Receive buffer / FIFO

12.4.11 SCxTFC (TX FIFO Configuration Register) (Note2)

	31	30	29	28	27	26	25	24
bit symbol	-	-	-	-	-	-	-	-
After reset	0	0	0	0	0	0	0	0
	23	22	21	20	19	18	17	16
bit symbol	-	-	-	-	-	-	-	-
After reset	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8
bit symbol	-	-	-	-	-	-	-	-
After reset	0	0	0	0	0	0	0	0
	7	6	5	4	3	2	1	0
bit symbol	TFCS	TFIS	-	-	-	-	TIL	
After reset	0	0	0	0	0	0	0	0

Bit	Bit Symbol	Type	Function
31-8	−	R	Read as "0".
7	TFCS	W	TX FIFO clear (Note1) 1: Clear When SCxTST<TFCS> is set to "1", the transmit FIFO is cleared and SCxTST<TLVL> is "000". And also the write pointer is initialized.
6	TFIS	R/W	Selects interrupt generation condition. 0: An interrupt is generated when the data reaches to the specified fill level. 1: An interrupt is generated when the data reaches to the specified fill level or the data can not reach the specified fill level at the time data is read.
5-2	−	R	Read as "0".
1-0	TIL[1:0]	R/W	Fill level which transmit interrupt is occurred.

	Half duplex	Full duplex
00	Empty	Empty
01	1 byte	1 byte
10	2 bytes	Empty
11	3 bytes	1 byte

Note 1: **To use TX/RX FIFO buffer, TX/RX FIFO must be cleared after setting the SIO transfer mode (half duplex/full duplex) and enabling FIFO (SCxFCNF<CNFG> = "1").**

Note 2: **After you perform the following operations, configure the SCxTFC register again.**
SCxEN<SIOE> = "0" (SIO operation stop)
Conditions are as follows:SCxMOD1<I2SC> = "0" (operation is prohibited in IDLE mode) and releasing the low power consumption mode which is started by the WFI (Wait For Interrupt) instruction.

Note 3: **DMA transfer is not started by an interrupt generated in the fill level of FIFO.**

12.11 Receive

12.11.1 Receive Counter

The receive counter is a 4-bit binary counter and is up-counted by SIOCLK.

In the UART mode, sixteen SIOCLK clock pulses are used in receiving a single data bit and the data symbol is sampled at the seventh, eighth, and ninth pulses. From these three samples, majority logic is applied to decide the received data.

12.11.2 Receive Control Unit

12.11.2.1 I/O interface mode

In the SCLK output mode with SCxCR <IOC> set to "0", the RXD pin is sampled on the rising edge of the shift clock outputted to the SCLK pin.

In the SCLK input mode with SCxCR <IOC> set to "1", the serial receive data RXD pin is sampled on the rising or falling edge of SCLK input signal depending on the SCxCR <SCLKS> setting.

12.11.2.2 UART Mode

The receive control unit has a start bit detection circuit, which is used to initiate receive operation when a normal start bit is detected.

12.11.3 Receive Operation

12.11.3.1 Receive Buffer

The received data is stored by 1 bit in the receive shift register. When a complete set of bits has been stored, the interrupt INTTRX is generated.

When the double buffer is enabled, the data is moved to the receive buffer (SCxBUF) and the receive buffer full flag (SCxMOD2<RBFLL>) is set to "1". The receive buffer full flag is "0" cleared by reading the receive buffer. The receive buffer flag does not have any value for the single buffer.

12.12 Transmission

12.12.1 Transmission Counter

The transmit counter is a 4-bit binary counter and is counted by SIOCLK as in the case of the receive counter.

In UART mode, it generates a transmit clock (TXDCLK) on every 16th clock pulse.

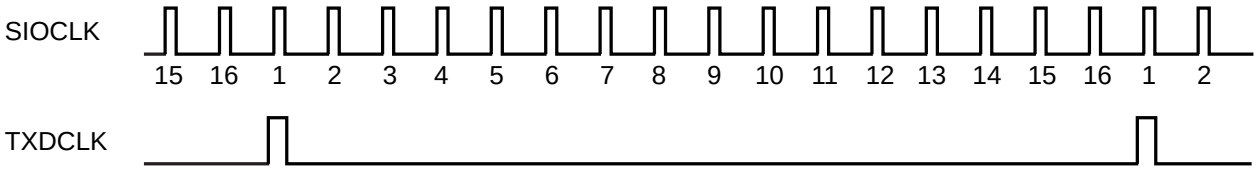


Figure 12-6 Generation of Transmission Clock in UART Mode

12.12.2 Transmission Control

12.12.2.1 I/O interface Mode

In the SCLK output mode with SCxCR<IOC> set to "0", each bit of data in the transmit buffer is outputted to the TXD pin on the falling edge of the shift clock outputted from the SCLK pin.

In the SCLK input mode with SCxCR<IOC> set to "1", each bit of data in the transmit buffer is outputted to the TXD pin on the rising or falling edge of the SCLK input signal according to the SCxCR<SCLKS> setting.

12.12.2.2 UART Mode

When the transmit data is written in the transmit buffer, data transmission is initiated on the rising edge of the next TXDCLK and the transmit shift clock signal is also generated.

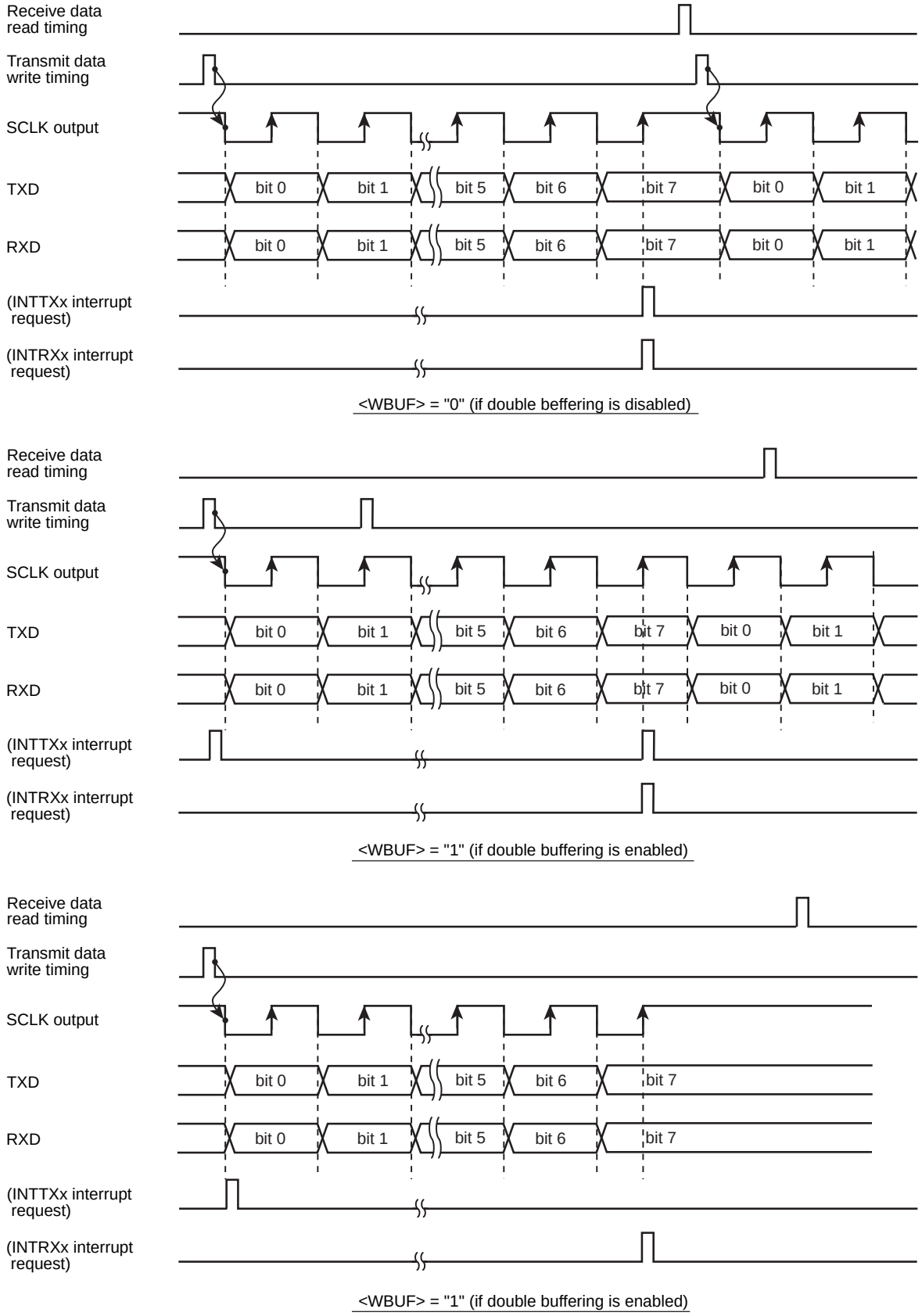


Figure 12-16 Transmit / Receive Operation in the I/O Interface Mode (SCLK Output Mode)

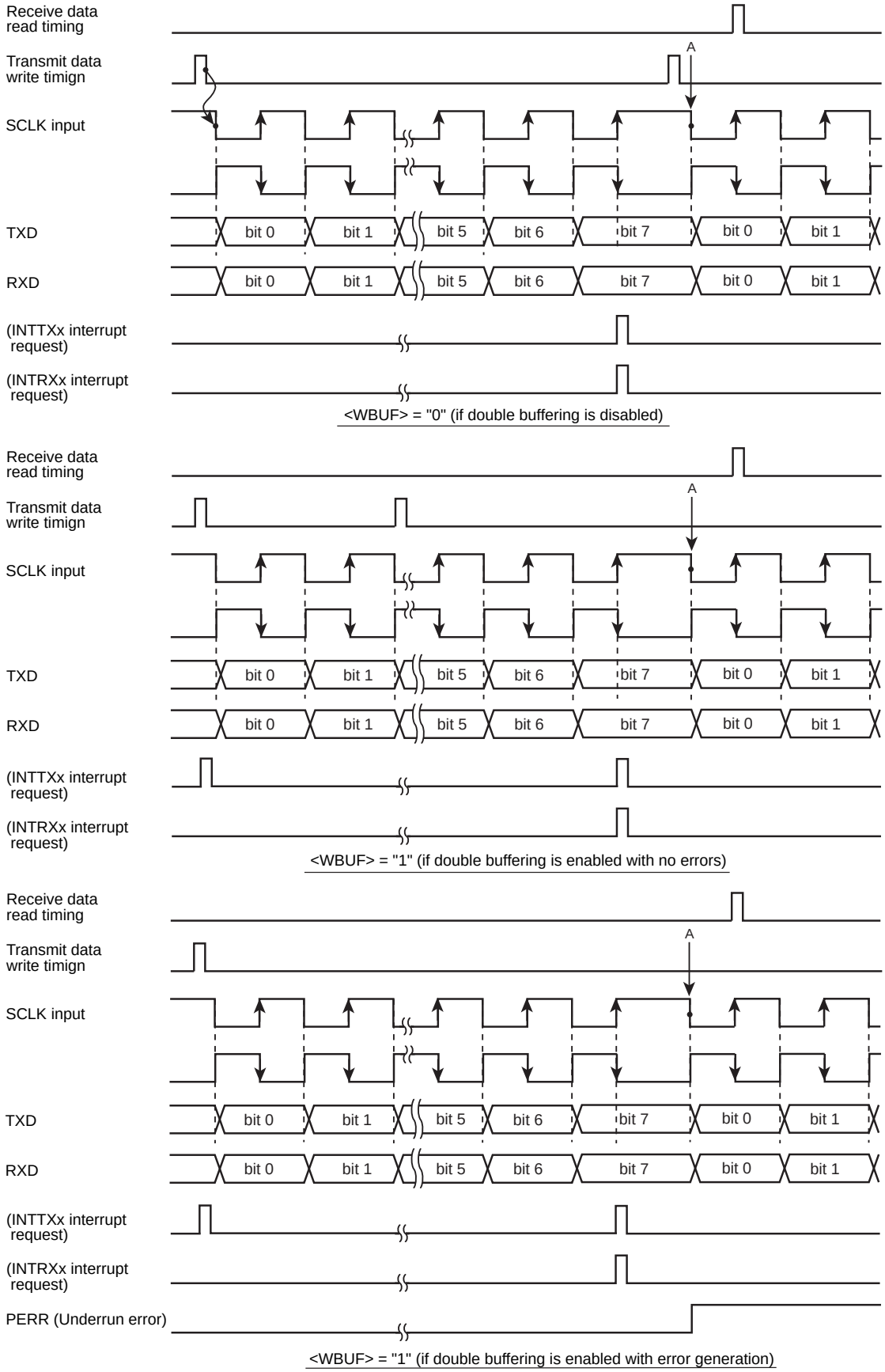


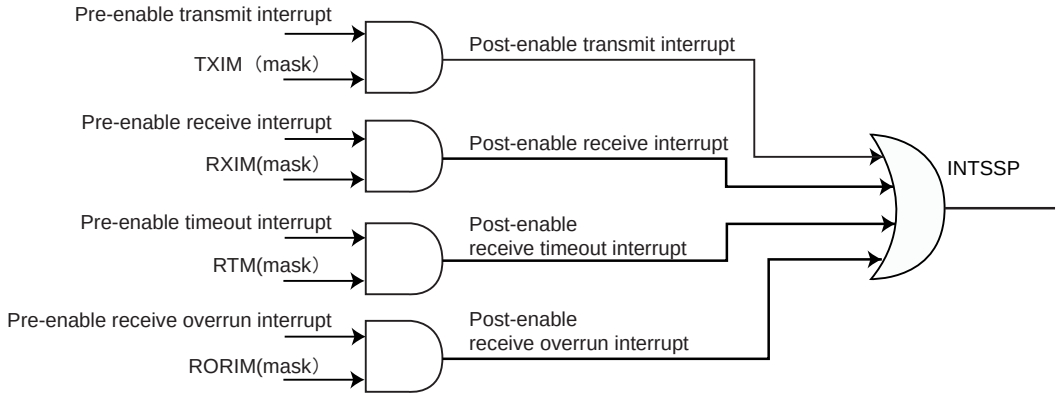
Figure 12-17 Transmit / Receive Operation in the I/O Interface Mode (SCLK Input Mode)

13.4.4 Interrupt generation logic

The interrupts, each of which can be masked separately, are generated.

Transmit interrupt	A conditional interrupt to occur when the transmit FIFO has free space more than (including half) of the entire capacity. (Number of valid data items in the transmit FIFO ≤ 4)
Receive interrupt	A conditional interrupt to occur when the receive FIFO has valid data more than half (including half) the entire capacity. (Number of valid data items in the receive FIFO ≥ 4)
Time-out interrupt	A conditional interrupt to indicate that the data exists in the receive FIFO to the time-out period.
Overrun interrupt	Conditional interrupts indicating that data is written to receive FIFO when it is full.

Also, The individual masked sources are combined into a single interrupt. When any of the above interrupts is asserted, the combined interrupt INTSSP is asserted.



a. Transmit interrupt

The transmit interrupt is asserted when there are four or fewer valid entries in the transmit FIFO. The transmit interrupt is also generated when the SSP operation is disabled (SSPCR1 <SSE> = "0").

The first transmitted data can be written in the FIFO by using this interrupt.

b. Receive interrupt

The receive interrupt is asserted when there are four or more valid entries in the receive FIFO.

c. Time-out interrupt

The time-out interrupt is asserted when the receive FIFO is not empty and the SSP has remained idle for a fixed 32-bit period (bit rate). This mechanism ensures that the user is aware that data is still present in the receive FIFO and requires servicing. This operation occurs in both master and slave modes. When the time-out interrupt is generated, read all data from the receive FIFO. Even if all the data is not read, data can be transmitted / received if the receive FIFO has a free space and the number of data to be transmitted does not exceed the free space of the receive FIFO. When transfer starts, the timeout interrupt will be cleared. If data is transmitted / received when the receive FIFO has no free space, the time-out interrupt will not be cleared and an overrun interrupt will be generated.

21.3.3.11 RTCRESTR (Reset register (for PAGE0/1))

	7	6	5	4	3	2	1	0
Bit symbol	DIS1HZ	DIS16HZ	RSTTMR	RSTALM	-	-	-	-
After reset	1	1	0	0	0	1	1	1

Bit	Bit Symbol	Type	Function
7	DIS1HZ	R/W	1 Hz 0:Enable 1: Disable
6	DIS16HZ	R/W	16 Hz 0: Enable 1: Disable
5	RSTTMR	R/W	[Write] 0: Don't care 1: Sec.counter reset Resets the sec counter. The equest is sampled using low-speed clock. [Read] 0: No reset request 1: RESET requested If "1" is read, it indicates that RESET is being executed. If "0" is read, it indicates that the execution is finished.
4	RSTALM	R/W	0:Don't care 1: Alarm reset Initializes alarm registers (Minute column, hour column, day column and day of the week column) as follows. MInute:00, Hour:00, Day:01, Day of the week:Sunday
3	−	R	Read as 0.
2-0	−	R/W	Write "1".

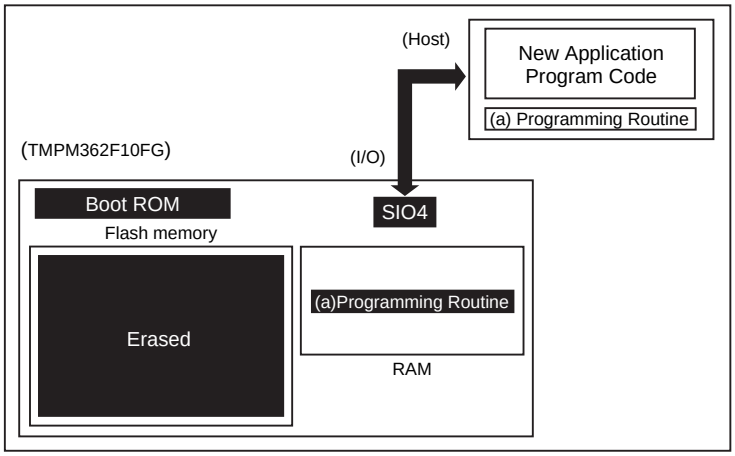
Note 1: A read-modify-write operation cannot be performed.

The setting of <DIS1HZ> and <DIS16MHZ>, RTCPAGER<ENAALM> used for alarm, 1Hz interrupt and 16Hz interrupt is shown as below.

<DIS1HZ>	<DIS16HZ>	RTCPAGER <ENAALM>	Interrupt source signal
1	1	1	Alarm
0	1	0	1 Hz
1	0	0	16 Hz
Others			Interrupt not generated.

(4) Step-4

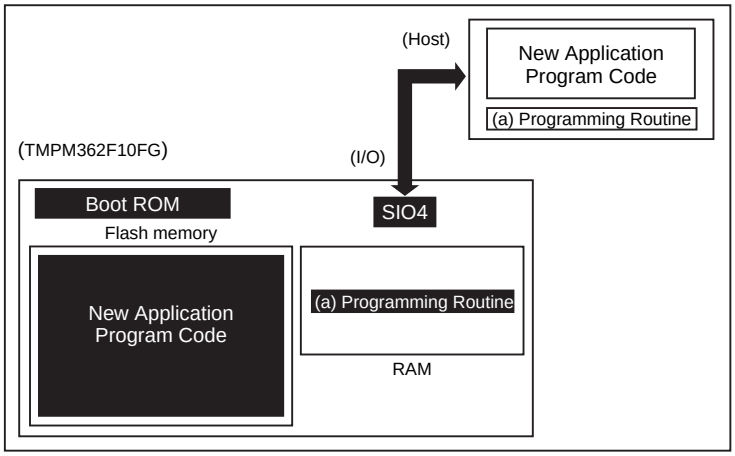
The CPU jumps to the programming routine (a) in the on-chip RAM to erase the flash block containing the old application program code. The Block Erase or Chip Erase command may be used.



(5) Step-5

Next, the programming routine (a) downloads new application program code from the host controller and programs it into the erased flash block. When the programming is completed, the writing or erase protection of that flash block in the user's program area must be set.

In the example below, new program code comes from the same host controller via the same SIO4 channel as for the programming routine. However, once the programming routine has begun to execute in the on-chip RAM, it is free to change the transfer path and the source of the transfer. Create board hardware and a programming routine to suit your particular needs.



8. The 19th to 22nd bytes, transmitted from the controller the target board, indicate the start address of the RAM region where subsequent data (e.g., a flash programming routine) should be stored. The 19th byte corresponds to bits 31 to 24 of the address and the 22nd byte corresponds to bits 7 to 0 of the address. The start address of the stored RAM must be even address.

9. The 23rd and 24th bytes, transmitted from the controller to the target board, indicate the number of bytes that will be transferred from the controller to be stored in the RAM. The 23rd byte corresponds to bits 15 to 8 of the number of bytes to be transferred, and the 24th byte corresponds to bits 7 to 0 of the number of bytes.

10. The 25th byte is a checksum value for the 19th to 24th bytes. To calculate the checksum value, add all these bytes together, ignore the carries and caluculate the 8-bit two's complement by using lower 8 bits then transmit this checksum value from the controller. The checksum calculation is described in detail in the later Section "22.2.10.9 Checksum Calculation".

11. The 26th byte, transmitted from the target board to the controller, is an acknowledge response to the 19th to 25th bytes of data. First, the RAM Transfer routine checks for a receive error in the 19th to 25th bytes. If there is a receive error, the RAM Transfer routine sends back 0x18 and returns to the command wait state (i.e., the 3rd byte) again. In this case, the upper four bits of the acknowledge response are the same as those of the previously issued command (i.e., 1). When the SIO4 is configured for I/O Interface mode, the RAM Transfer routine does not check for a receive error.

    Next, the RAM Transfer routine performs the checksum operation to ensure data integrity. Adding the series of the 19th to 24th bytes must result in 0x00 (with the carry dropped). In case of a checksum error, the RAM Transfer routine sends back 0x11 to the controller and returns to the state in which it waits for a command (i.e., the 3rd byte) again.

    - The 19th to 25th bytes data must be within the range of 0x2000_0400 to the end address of RAM.

    When the above checks have been successful, the RAM Transfer routine returns a normal acknowledge response (0x10) to the controller.

12. The 27th to mth bytes from the controller are stored in the on-chip RAM of the TMPM362F10FG. Storage begins at the address specified by the 19th to 22nd bytes and continues for the number of bytes specified by the 23rd to 24th bytes.

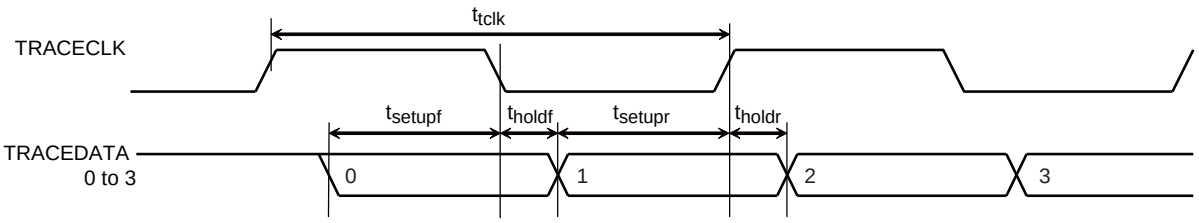
13. The (m+1) th byte is a checksum value. To calculate the checksum value, add the 27th to mth bytes together, ignore the carries and calculate the 8-bit two’s complement by using lower 8 bits then transmit this checksum value from the controller. The checksum calculation is described in detail in later Section "22.2.10.9 Checksum Calculation".

14. The (m+2) th byte is a acknowledge response to the 27th to (m+1) th bytes. First, the RAM Transfer routine checks for a receive error in the 27th to (m+1) th bytes. If there is a receive error, the RAM Transfer routine sends back 0x18 (bit 3) and returns to the state in which it waits for a command (i.e., the 3rd byte) again. In this case, the upper four bits of the acknowledge response are the same as those of the previously issued command (i.e., 1). When the SIO4 is configured for I/O Interface mode, the RAM Transfer routine does not check for a receive error.

    Next, the RAM Transfer routine performs the checksum operation to ensure data integrity. Adding the series of the 27th to (m+1) th bytes must result in 0x00 (with the carry dropped). In case of a checksum error, the RAM Transfer routine sends back 0x11 (bit 0) to the controller and returns to the command wait state (i.e., the 3rd byte) again. When the above checks have been completed successfully, the RAM Transfer routine returns a normal acknowledge response (0x10) to the controller.

26.6.11 ETM Trace

Parameter	Symbol	Min.	Max.	Unit
TRACECLK cycle	t_{tclk}	31.25	−	ns
TRACEDATA valid ← TRACECLK rise	t_{setupr}	2	−	ns
TRACECLK rise → TRACEDATA hold	t_{holdr}	1	−	ns
TRACEDATA valid ← TRACECLK rise	t_{setupf}	2	−	ns
TRACECLK fall → TRACEDATA hold	t_{holdf}	1	−	ns



26.7 Flash Characteristics

26.7.1 Erase / Write Characteristics

Parameter	Condition	Min.	Typ.	Max.	Unit
The number of E / W cycle	DVDD3 = AVDD3 = RVDD3 = 2.7 V to 3.6 V Ta = 0 to 70 °C	−	−	100	cycle