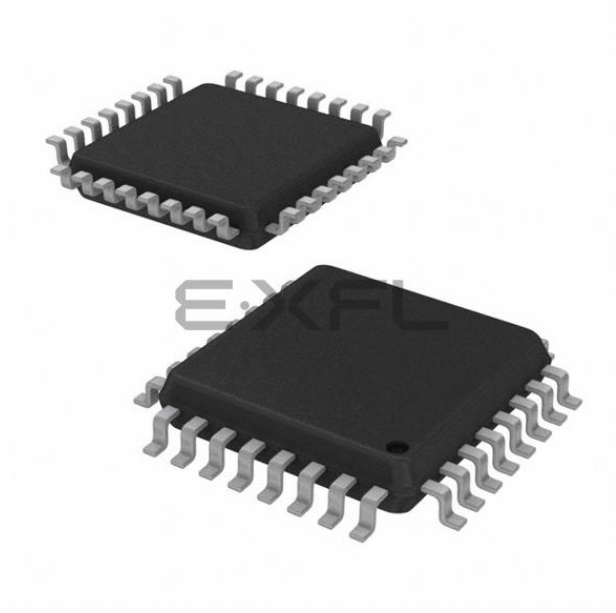

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Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, LVD, POR, PWM, WDT
Number of I/O	30
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z32f06410aks

Figure 1.2 and Figure 1.3 show the pin layouts.

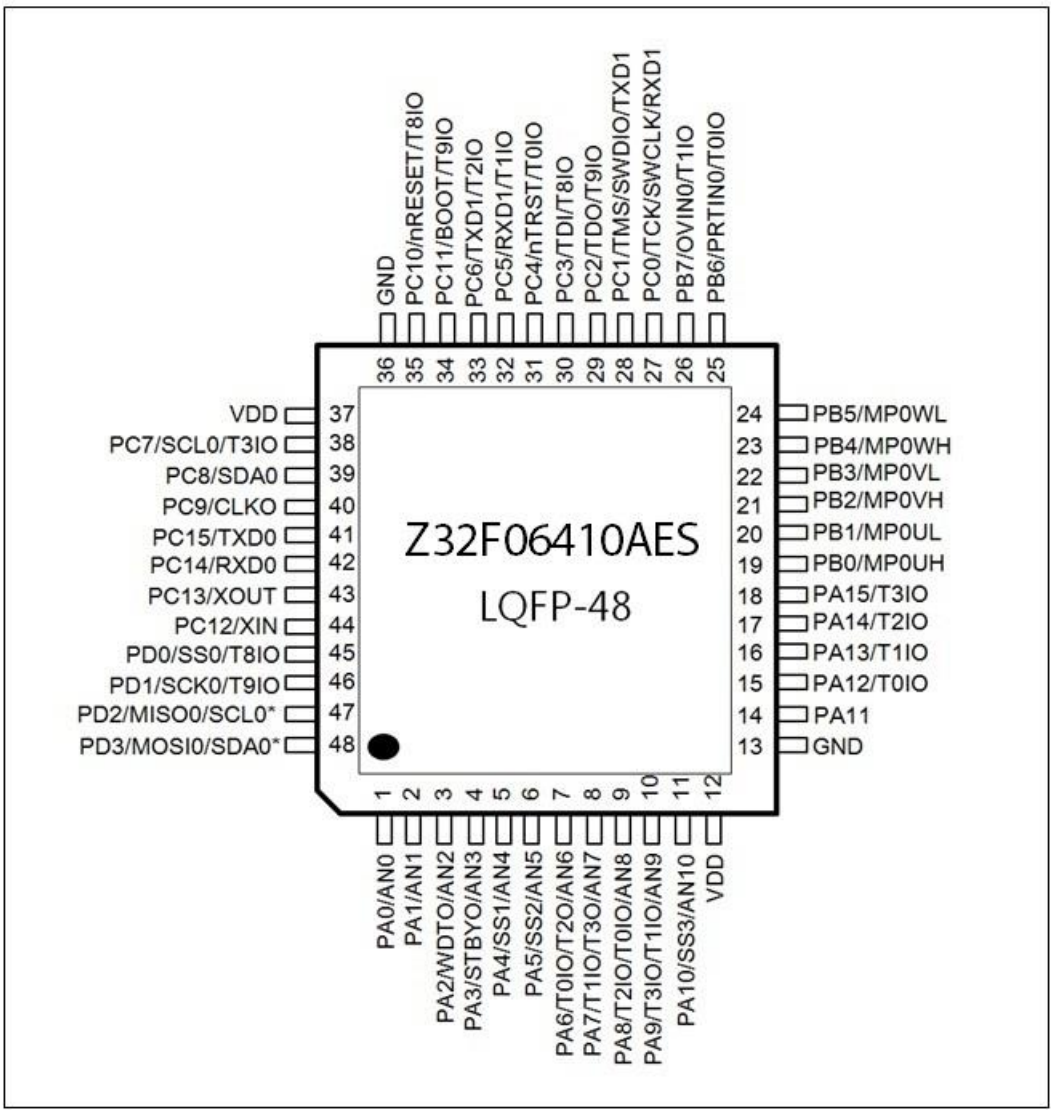

Figure 1.2 Pin Layout (LQFP-48)

PER2 Peripheral Enable Register 2

Prior to using a peripheral unit, it requires to be activated by writing **1** to the corresponding bit in the PER1/PER2 register. Until activation, the peripheral stays in Reset state.

To disable the peripheral unit, write **0** to the corresponding bit in the PER0/PER1 register, after which the peripheral enters the Reset state.

PER2=0x4000_002C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
										ADC1	ADC0				MWPM0							UART1	UART0				I2C0				SPI0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1
										RW	RW				RW							RW	RW				RW				RW

21	ADC1	ADC1 function enable
20	ADC0	ADC0 function enable
16	MPWM0	MPWM0 function enable
9	UART1	UART1 function enable
8	UART0	UART0 function enable
4	I2C0	I^2C0 function enable
0	SPI0	SPI0 function enable

DBCLK1 Debounce Clock Control Register 1

The Debounce Clock Control register 1 controls the debounce timing configuration for Port A and Port B.

DBCLK1=0x4000_009C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
					PBDCSEL			PBDDIV														PADCSEL			PADDIV							
0	0	0	0	0	000			0x01								0	0	0	0	0	000			0x01							
					RW			RW													RW			RW							

26 24	PBDCSEL	Debounce Clock for Port B source select bit 0xx RING OSC 1Mhz 100 MCLK (bus clock) 101 Reserved 110 External Main OSC (XTAL) 111 Reserved
23 16	PBDDIV	PORT B Debounce Clock N divider
10 8	PADCSEL	Debounce Clock for Port A source select bit 0xx RING OSC 1Mhz 100 MCLK (bus clock) 101 Reserved 110 External Main OSC (XTAL) 111 Reserved
7 0	PADDIV	PORT A Debounce Clock N divider

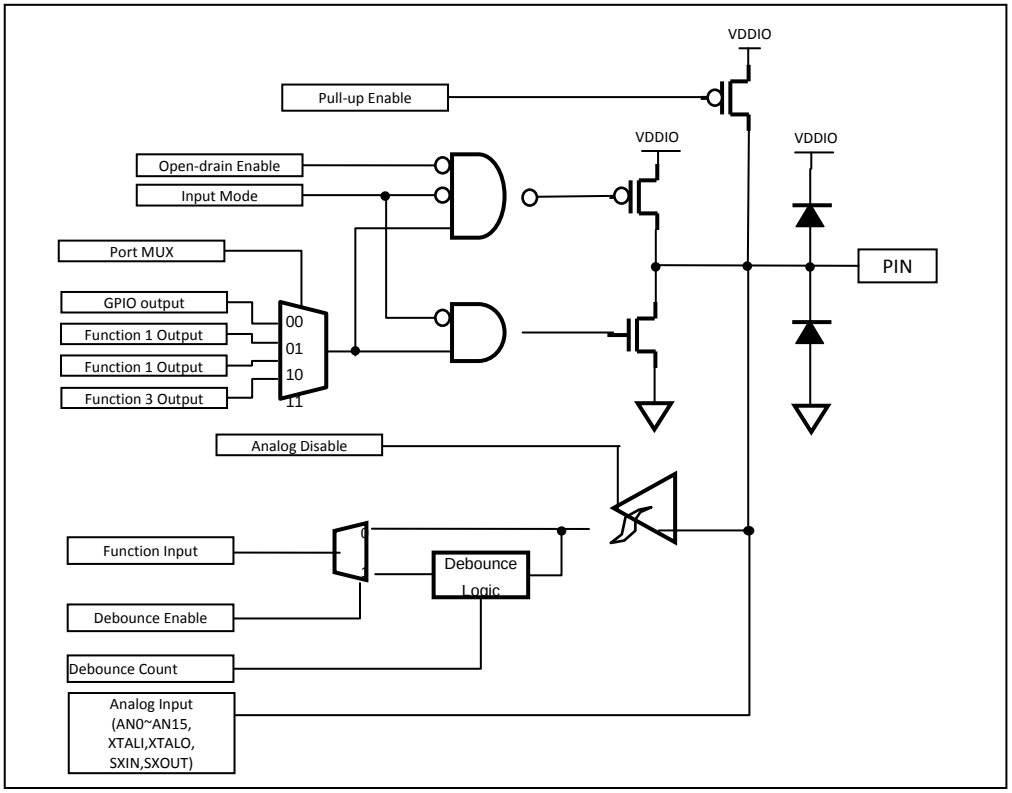

Figure 5.2 I/O Port Block Diagram (ADC and External Oscillator pins)

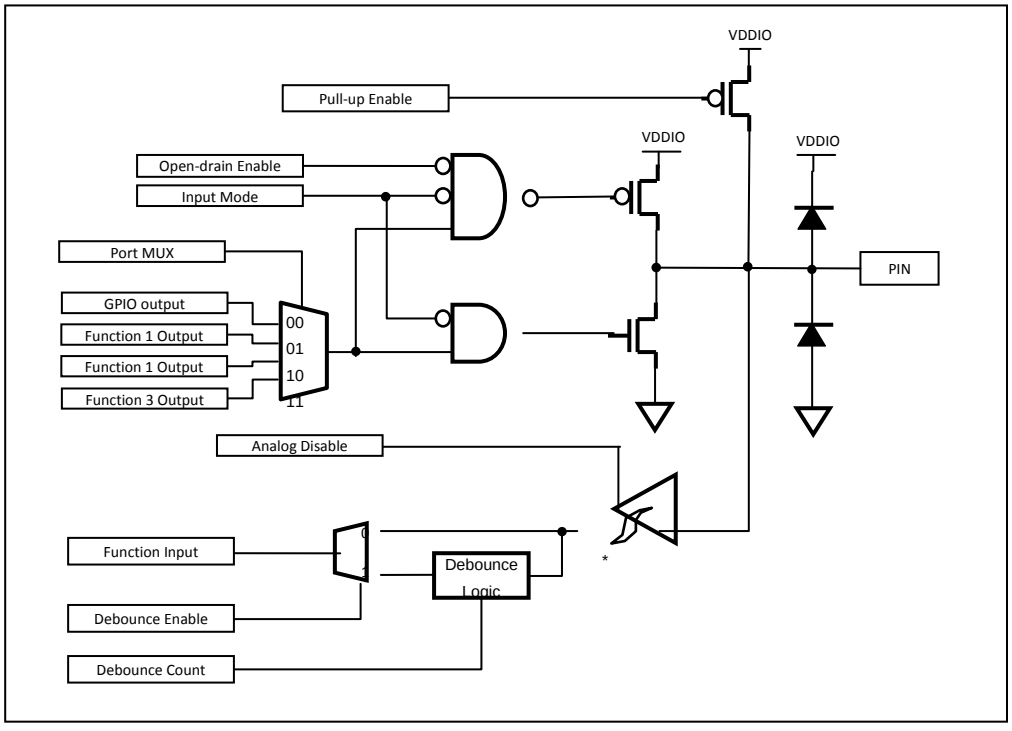

Figure 5.3 I/O Port Block Diagram (General I/O pins)

Pn.BSR PORT n Bit Set Register

Pn.BSR is a register for controlling each bit of the PnODR register. Writing a **1** into the specific bit will set a corresponding bit of PnODR to **1**. Writing **0** in this register has no effect.

PA.BSR=0x4000_2008, PB.BSR=0x4000_2108
PC.BSR=0x4000_2208, PD.BSR=0x4000_2308

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BSR															
0000															
WO															

BSR	Pin current level
0	Not effect
1	Set correspondent bit in PnODR register

Pn.BCR PORT n Bit Clear Register

Pn.BRR is a register for controlling each bit of the PnODR register. Writing a **1** into the specific bit will set a corresponding bit of PnODR to **0**. Writing **0** in this register has no effect.

PA.BCR=0x4000_200C, PB.BCR=0x4000_210C
PC.BCR=0x4000_220C, PD.BCR=0x4000_230C

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PnBCR															
0000															
WO															

BCR	Pin current level
0	Not effect
1	Clear correspondent bit in PnODR register

DC*n*.PAR DMA Controller Peripheral Address Register

This register represents the peripheral addresses.

DC0.PAR=0x4000_0408 , DC1.PAR=0x4000_0418
DC2.PAR=0x4000_0428 , DC3.PAR=0x4000_0438

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Peripheral BASE OFFSET																PAR															
0x4000																0x0000															
RO																RW															

31 0	PAR	Target Peripheral address of transmit buffer or receive buffer. User must set exact target peripheral buffer address in this field. If DIR is “0” this address is destination address of data transfer. If DIR is “1”, this address is source address of data transfer.

DC*n*.MAR DMA Controller Memory Address Register

This register represents the memory addresses.

DC0.MAR=0x4000_040C , DC1.MAR=0x4000_041C
DC2.MAR=0x4000_042C , DC3.MAR=0x4000_043C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
																MAR															
0x2000																0x0000															
RO																RW															

31 0	MAR	Target memory address of data transfer. Address is automatically incremented according to SIZE bits when each transfer is done. If DIR is “0” this address is source address of data tra nsfer. If DIR is “1”, this address is destination address of dat a transfer.

Registers

The base address of the watchdog timer is 0x4000_0200 and the register map is described in Table 10.1. The initial watchdog time-out period is set to 2,000-miliseconds.

Table 10.1 Watchdog Timer Register Map

NAME	OFFSET	TYPE	DESCRIPTION	RESET VALUE
WDT.LR	0x0000	W	WDT Load register	0x00000000
WDT.CNT	0x0004	R	WDT Current counter register	0x0000FFFF
WDT.CON	0x0008	RW	WDT Control register	0x0000805C

WDT.LR Watchdog Timer Load Register

The WDTLR register is used to update the WDTCVR register. To update the WDTCVR register, the WEN bit of WDTCON should be set to **1** and written to the WDTLR register with a target value of WDTCVR.

WDT.LR=0x4000_0200

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WDTLR																															
0x0000_0000																															
RW																															

31 0	WDTLR	Watchdog timer load value register Keeping WEN bit as '1', write WDTLR register will update WDTCVR value with written value

WDT.CNT Watchdog Timer Current Counter Register

The WDTCNT register represents the current count value of 32-bit down counter .When the counter value reaches 0, an interrupt or reset occurs.

WDT.LR=0x4000_0204

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WDTCNT																															
0x0000_FFFF																															
RW																															

31 0	WDTCNT	Watchdog timer current counter register 32-bit down counter will run from the written value.

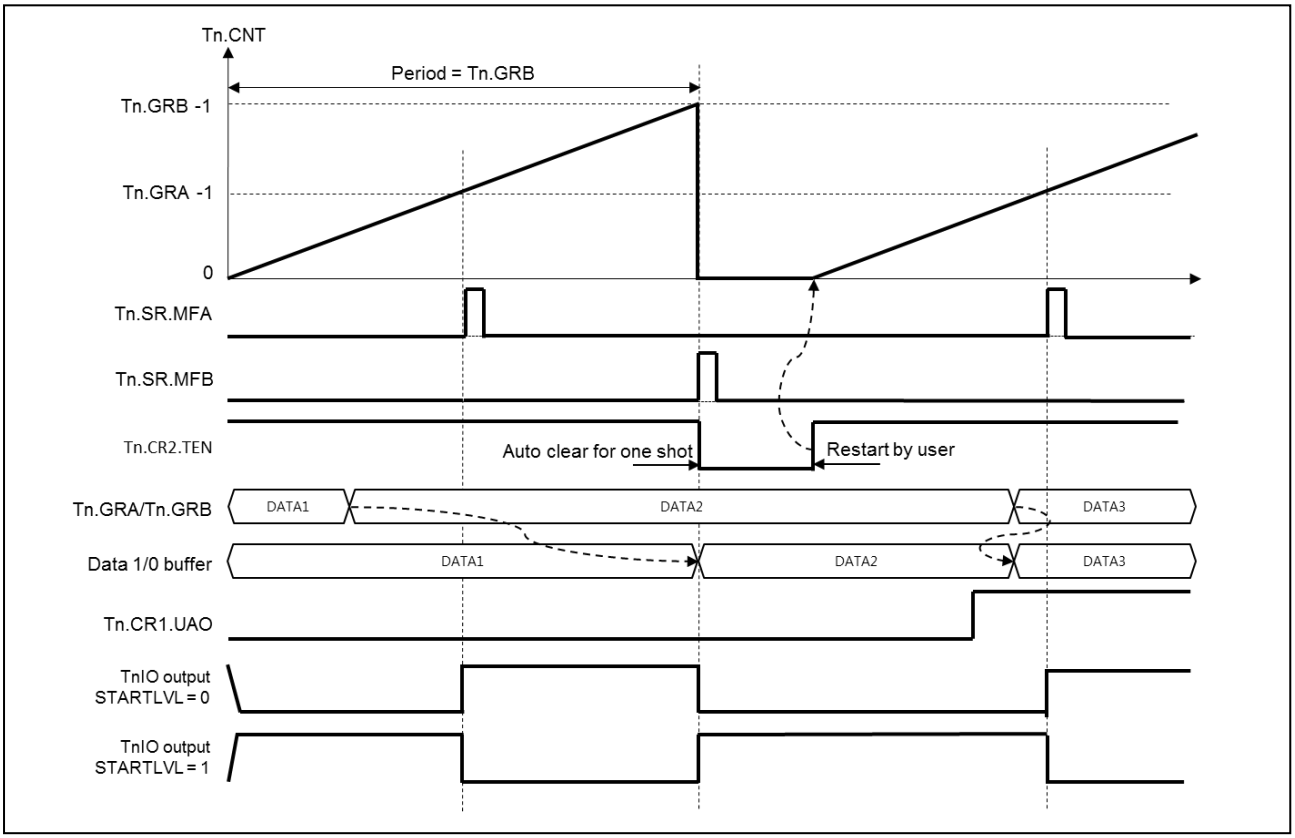

Figure 11.4. One Shot Mode Operation

The period of one shot count can be calculated as shown in the following equation:

The period = TMCLK Period * Tn.GRB value
Match A interrupt time = TMCLK Period * Tn.GRA value

If Tn.GRB = 0, the timer cannot be started even if TnCR2.TEN is “1” because the period is “0”.

The value in Tn.GRA and Tn.GRB is loaded into the internal compare data buffer 0 and 1 when the loading condition occurs. In this periodic mode with TnCR1.UAO =0, the Tn.CR2.TCLR write operation and the GRB match event will load the compare data buffers.

When TnCR1.UAO is 1, the internal compare data buffer is updated whenever the Tn.GRA or Tn.GRB data is updated.

The TnIO output signal format is the same as PWM mode. Tn.GRB value defines the output pulse period and the Tn.GRA value defines the pulse width of one shot pulse.

PWM Timer Output

Figure 11.5 shows the timing diagram in PWM output mode. The Tn.GRB value decides the PWM pulse period. An additional comparison point is provided by the Tn.GRA register value which defines the pulse width of PWM output.

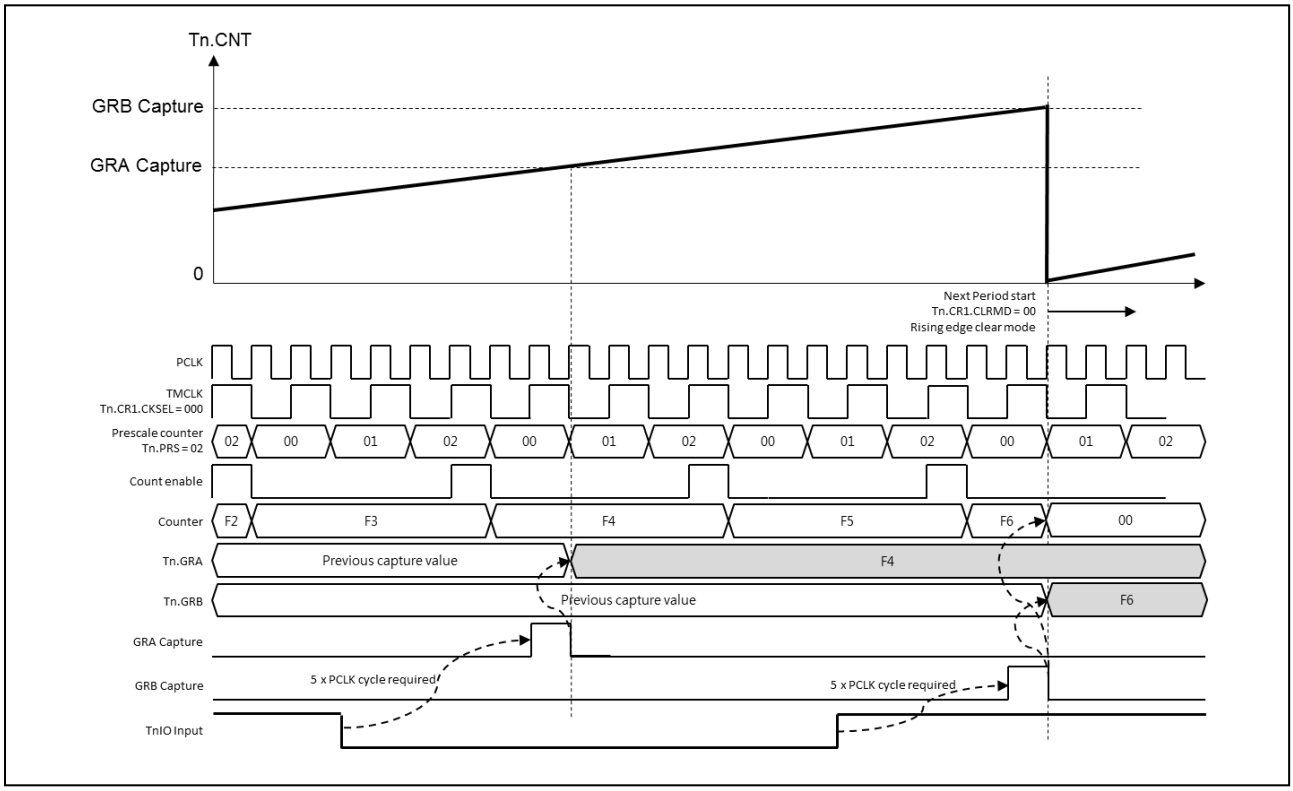

Figure 11.8. Capture Mode Operation

A 5 PCLK clock cycle is required internally. Therefore, the actual capture point is after 5 PCLK clock cycles from the rising or falling edge of the TnIO input signal.

The internal counter can be cleared in multiple modes. The TnCR1.CLRMD field controls the counter clear mode. The following clear modes are supported: Rising edge, Falling edge, Both edges, and None.

The example in Figure 11.8 is of Rising edge clear mode.

ADC Trigger Function

The timer module can generate ADC start trigger signals. One timer can be one trigger source of the ADC block. Trigger source control is performed by the ADC control register.

Figure 11.9 shows the ADC trigger function.

The conversion rate must be shorter than the timer period, else an overrun situation can occur. ADC acknowledge is not required because the trigger signal is automatically cleared after 3 PCLK clock pulses.

Un.IER UART Interrupt Enable Register

The UART Interrupt Enable Register is an 8-bit register.

U0.IER=0x4000_8004, U1.IER=0x4000_8104

7	6	5	4	3	2	1	0
-	-	DTXIEN	DRXIEN	TXIE	RLSIE	THREIE	DRIE
0	0	0	0	0	0	0	0
		RW	RW		RW	RW	RW

5	DTXIEN	DMA transmit done interrupt enable
		0 Receive line status interrupt is disabled
		1 Receive line status interrupt is enabled
4	DRXIEN	DMA receive done interrupt enable
		0 DMA receive done interrupt is disabled
		1 DMA receive done interrupt is enabled
3	TXIE	Transmit register empty interrupt enable
		0 Transmit register empty interrupt is disabled
		1 Transmit register empty interrupt is enabled
2	RLSIE	Receiver line status interrupt enable
		0 Receive line status interrupt is disabled
		1 Receive line status interrupt is enabled
1	THREIE	Transmit holding register empty interrupt enable
		0 Transmit holding register empty interrupt is disabled
		1 Transmit holding register empty interrupt is enabled
0	DRIE	Data receive interrupt enable
		0 Data receive interrupt is disabled
		1 Data receive interrupt is enabled

Un.IIR UART Interrupt ID Register

The UART Interrupt ID Register is an 8-bit register.

U0.IIR=0x4000_8008, U1.IIR=0x4000_8108

7	6	5	4	3	2	1	0
			TXE	IID			IPEN
0	0	0	0	000			0
			R	R			R

4	TXE	Interrupt source ID See interrupt source ID table
3 1	IID	Interrupt source ID See interrupt source ID table
0	IPEN	Interrupt pending bit
		0 Interrupt is pending
		1 No interrupt is pending.

Un.LCR UART Line Control Register

The UART Line Control Register is an 8-bit register.

U0.LCR=0x4000_800C, U1.LCR=0x4000_810C

7	6	5	4	3	2	1	0
	BREAK	STICKP	PARITY	PEN	STOPBIT	DLEN	
0	0	0	0	0	0	0	0
	RW	RW	RW	RW	RW	RW	RW

6	BREAK	When this bit is set, TxD pin will be driven at low state in order to notice the alert to the receiver.
		0 Normal transfer mode
		1 Break transmit mode
5	STICKP	Force parity and it will be effective when PEN bit is set.
		0 Parity stuck is disabled
		1 Parity stuck is enabled and parity always the bit of PARITY.
4	PARITY	Parity mode selection bit and stuck parity select bit
		0 Odd parity mode
		1 Even parity mode
3	PEN	Parity bit transfer enable
		0 The parity bit disabled
		1 The parity bit enabled
2	STOPBIT	The number of stop bit followed by data bits.
		0 1 stop bit
		1 1.5 / 2 stop bit In case of 5 bit data case, 1.5 stop bit is added. In case of 6,7 or 8 bit data, 2 stop bit is added
1 0	DLEN	The data length in one transfer word.
		00 5 bit data
		01 6 bit data
		10 7 bit data
		11 8 bit data

Parity bit is generated according to bit 3, 4, 5 of UnLCR register. The following table shows the variation of parity bit generation.

STICKP	PARITY	PEN	Parity
X	X	0	No Parity
0	0	1	Odd Parity
0	1	1	Even Parity
1	0	1	Force parity as “1”
1	1	1	Force parity as “0”

Un.DCR UART Data Control Register

The UART Data Control Register is an 8-bit register.

U0.DCR=0x4000_8010, U1.DCR=0x4000_8110

7	6	5	4	3	2	1	0
			LBON	RXINV	TXINV		
0	0	0	0	0	0	0	0
				RW	RW		

4	LBON	Local loopback test mode enable
		0 Normal mode
		1 Local loopback mode (TxD connected to RxD internally)
3	RXINV	Rx Data Inversion Selection
		0 Normal RxData Input
		1 Inverted RxData Input
2	TXINV	Tx Data Inversion Selection
		0 Normal TxData Output
		1 Inverted TxData Output

SP0.RDR SPI Receive Data Register

SP0.RDR is a 17-bit read/write register. It contains serial receive data.

SP0.RDR=0x4000_9000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
																RDR															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		0x00000															
																RW															

16	RDR	Receive Data Register
0		

SP0.CR SPI Control Register

SP0.CR is a 20-bit read/write register which can be set to configure SPI operation mode.

SP0.CR=0x4000_9004

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
											TXBC	RXBC	TXDIE	RXDIE	SSCIE	TXIE	RXIE	SSMOD	SSOUT	LBE	SSMASK	SSMO	SSPOL			MS	MSBF	CPHA	CPOL	BITSZ	
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0	00	
											RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW			RW	RW	RW	RW	RW		

20	TXBC	Tx buffer clear bit.
		0 No action
		1 Clear Tx buffer
19	RXBC	Rx buffer clear bit
		0 No action
		1 Clear Rx buffer
18	TXDIE	DMA Tx Done Interrupt Enable bit.
		0 DMA Tx Done Interrupt is disabled.
		1 DMA Tx Done Interrupt is enabled.
17	RXDIE	DMA Rx Done Interrupt Enable bit.
		0 DMA Rx Done Interrupt is disabled.
		1 DMA Rx Done Interrupt is enabled.
16	SSCIE	SS Edge Change Interrupt Enable bit.
		0 nSS interrupt is disabled.
		1 nSS interrupt is enabled for both edges (L→H, H→L)
15	TXIE	Transmit Interrupt Enable bit.
		0 Transmit Interrupt is disabled.
		1 Transmit Interrupt is enabled.
14	RXIE	Receive Interrupt Enable bit..
		0 Receive Interrupt is disabled.
		1 Receive Interrupt is enabled.
13	SSMOD	SS Auto/Manual output select bit.

ICn.DR I²C Data Register

ICn.DR is an 8-bit read/write register. It contains a byte of serial data to be transmitted or a byte which has just been received.

IC0.DR=0x4000_A000

7	6	5	4	3	2	1	0
DR							
0xFF							
RW							

7 0	DR	The most recently received data or data to be transmitted.

ICn.SR I²C Status Register

ICn.SR is an 8-bit read/write register. It contains the status of I²C bus interface. Writing to the register clears the status bits except for IMASTER.

IC0.SR=0x4000_A008

7	6	5	4	3	2	1	0
GCALL	TEND	STOP	SSEL	MLOST	BUSY	TMODE	RXACK
0	0	0	0	0	0	0	0
RW	RW	RW	RW	RW	RW	RW	RW

7	GCALL	General call flag	
		0	General call is not detected.
		1	General call detected or slave address (ID byte) was sent.
6	TEND	1 Byte transmission complete flag	
		0	The transmission is working or not completed.
		1	The transmission is completed.
5	STOP	STOP flag	
		0	STOP is not detected.
		1	STOP is detected.
4	SSEL	Slave flag	
		0	Slave is not selected.
		1	Slave is selected.
3	MLOST	Mastership lost flag	
		0	Mastership is not lost.
		1	Mastership is lost.
2	BUSY	BUSY flag	
		0	I²C bus is in IDLE state.
		1	I²C bus is busy.
1	TMODE	Transmitter/Receiver mode flag	
		0	Receiver mode.
		1	Transmitter mode.
0	RXACK	Rx ACK flag	
		0	Rx ACK is not received.
		1	Rx ACK is received.

MP0.PRD MPWM Period Register

The PWM Period Register is a 16-bit register.

MP0.PRD=0x4000400C

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PERIOD															
0x0002															
RW															

15 0	PERIOD	16-bit PWM period. It should be larger than 0x0010 (If Duty is 0x0000, PWM will not work)

MP0.DUH MPWM Duty UH Register

The PWM U channel duty register is a 16-bit register.

MP0.DUH=0x4000_4010

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DUTY UH															
0x0001															
RW															

15 0	DUTY UH	16-bit PWM Duty for UH output. It should be larger than 0x0001 (If Duty is 0x0000, PWM will not work)

MP0.DUL MPWM Duty UL Register

The PWM U channel duty register is a 16-bit register.

MP0.DUL=0x4000_401C

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DUTY UL															
0x0001															
RW															

15 0	DUTY UL	16-bit PWM Duty for UL output. It should be larger than 0x0001 (If Duty is 0x0000, PWM will not work)

MP0.DVL MPWM Duty VL Register

The PWM V channel duty register is a 16-bit register.

MP0.DVL=0x4000_4020

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DUTY VL															
0x0001															
RW															

15 0	DUTY VL	16-bit PWM Duty for VL output. It should be larger than 0x0001 (if Duty is 0x0000, PWM will not work)

Figure 15.9 is an example of dead-time operation in 1 channel symmetric mode.

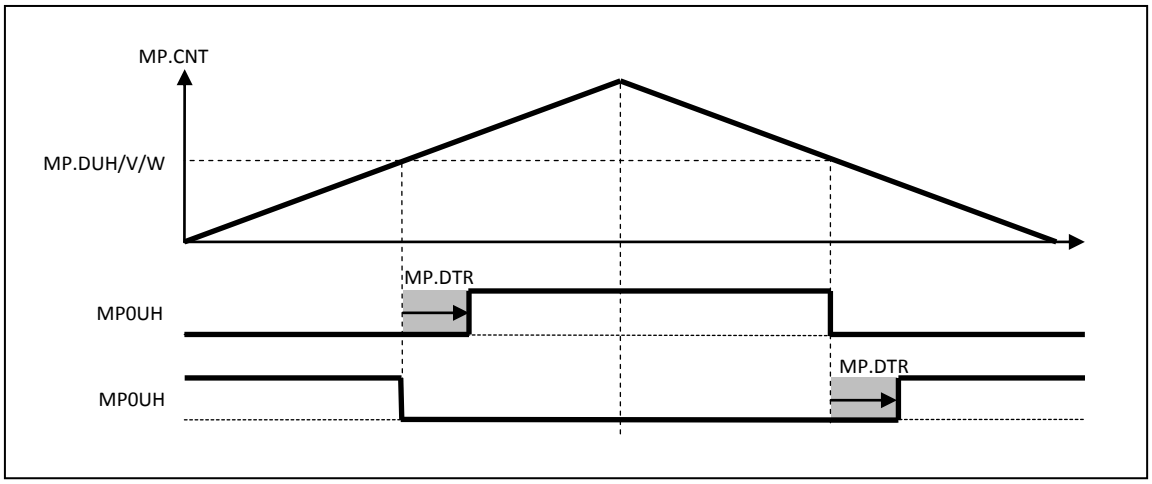

Figure 15.9. PWM Dead-time Operation Timing Diagram (Symmetric Mode)

Figure 15.10 displays an example of dead-time operation in 1-channel asymmetric mode.

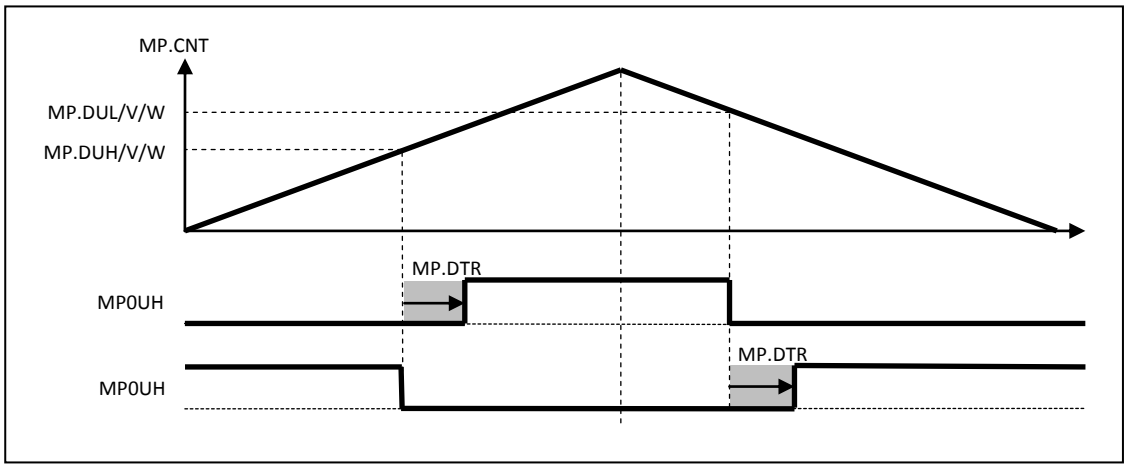

Figure 15.10. PWM Dead-Time Operation Timing Diagram (Asymmetric Mode)

The dead-time function is not available for 2-channel symmetric mode. Therefore, the dead condition is generated by each channel's duty control.

MPWM Dead-time Timing Examples for Special Conditions

Figure 15.11 shows the operation of dead-time.

In normal dead-time, dead-time masking is activated at duty match time and the dead-time counter runs. When the dead-time counter reaches the dead time value, the mask is disabled.

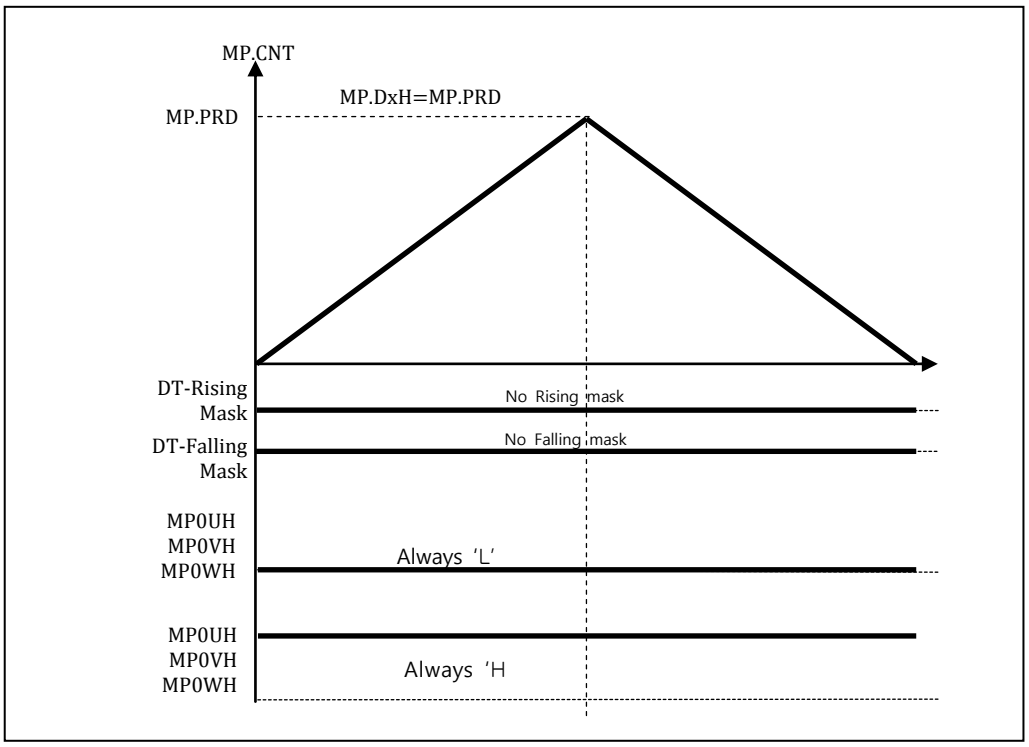

Figure 15.17. L-Side Always On (T_{DUTY}='0': Dead-Time Disabled)

Symmetrical Mode vs Asymmetrical Mode

In symmetrical mode, the waveform is symmetrical on both sides of the mid-point of the period. The duty comparison is performed twice in both up and down count period.

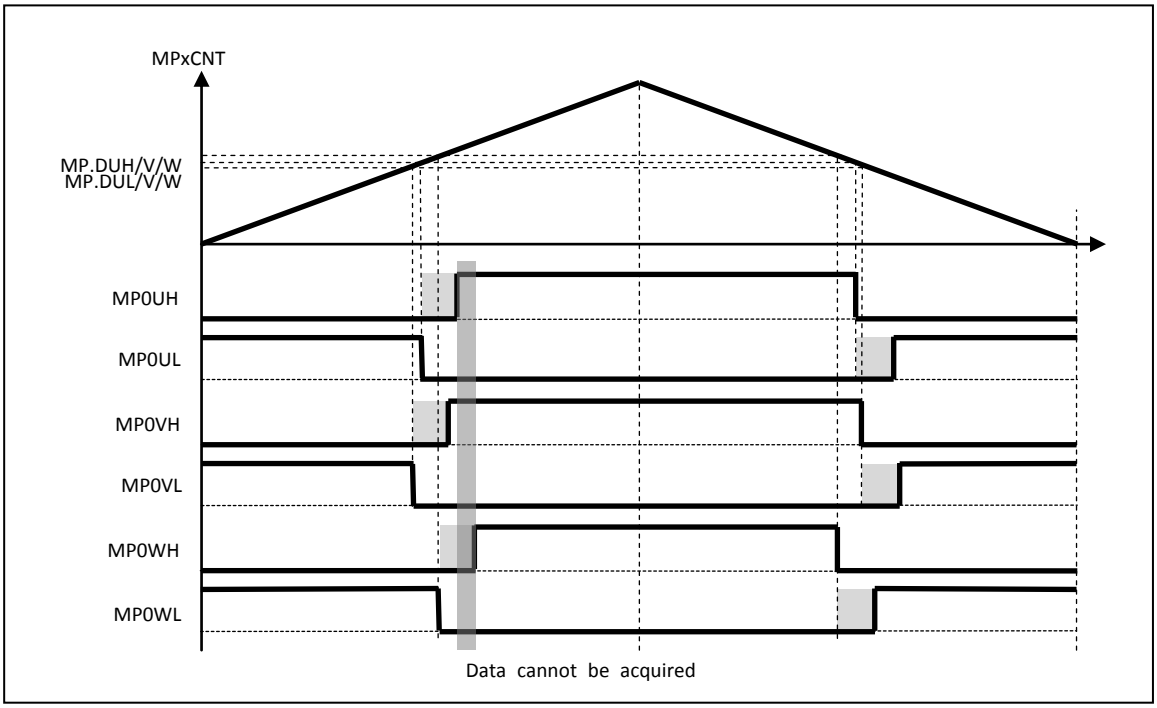

Figure 15.18. Symmetrical PWM Timing

Table 16.3 ADC Register Map

Name	Offset	Type	Description	Reset Value
ADn.MR	0x0000	RW	ADC Mode register	0x00
ADn.CSCR	0x0004	RW	ADC Current Sequence/Channel register	0x00
ADn.CCR	0x0008	RW	ADC Clock Control register	0x80
ADn.TRG	0x000C	RW	ADC Trigger Selection register	0x00
-	0x0010	-	Reserved	
-	0x0014	-	Reserved	
ADn.SCSR	0x0018	RW	ADC Burst mode channel select	0x00
ADn.CR	0x0020	RW	ADC Control register	0x00
ADn.SR	0x0024	RW	ADC Status register	0x00
ADn.IER	0x0028	RW	ADC Interrupt Enable register	0x00
ADn.DDR	0x002C	R	ADCn DMA Data Register	0x00
ADn.DR0	0x0030	R	ADCn Sequence 0 Data register	0x00
ADn.DR1	0x0034	R	ADCn Sequence 1 Data register	0x00
ADn.DR2	0x0038	R	ADCn Sequence 2 Data register	0x00
ADn.DR3	0x003C	R	ADCn Sequence 3 Data register	0x00
ADn.DR4	0x0040	R	ADCn Sequence 4 Data register	0x00
ADn.DR5	0x0044	R	ADCn Sequence 5 Data register	0x00
ADn.DR6	0x0048	R	ADCn Sequence 6 Data register	0x00
ADn.DR7	0x004C	R	ADCn Sequence 7 Data register	0x00

AD*n*.CR ADCn Control Register

The ADCn Control Register controls start or stop ADC conversion operations. This register is an 8-bit register.

AD0.CR=0x4000_B020, AD1.CR=0x4000_B120

7	6	5	4	3	2	1	0
ASTOP							ASTART
0							0
W							RW

7	ASTOP	0	No
		1	ADC conversion stop (will be clear next @ADC clock) If ASTOP set after conversion cycle start, present conversion would be completed.
0	ASTART	0	No ADC conversion
		1	ADC conversion start (will be clear next @ADC clock) ADCEN should be “1” to start ADC If ASTART is set as 1’h1 when ARST is 1’h0 in trigger event mode, ADC conversion will start once as SEQCNT set.

AD*n*.SR ADC*n* Status Register

The ADC Status Register is a 32-bit register.

AD0.SR=0x4000_B024, AD1.SR=0x4000_B124

7	6	5	4	3	2	1	0
EOC	ABUSY	DOVRUN	DMAIRQ	TRGIRQ	EOSIRQ	-	EOCIRQ
0	0	0	0	0	0	-	0
RO	RO	RO	RO	RC	RC	-	RC

7	EOC		ADC End-of-Conversion flag (Start-of-Conversion made by ADC_CLK clears this bit , not ASTART)
6	ABUSY		ADC conversion busy flag
5	DOVRUN		DMA overrun flag (not interrupt) (DMA ACK didn’t come until end of next conversion)
4	DMAIRQ		DMA done received (DMA transfer is completed)
3	TRGIRQ		ADC Trigger interrupt flag(Write “1” to clear flag) (0: no int / 1: int occurred)
2	EOSIRQ		This flag will be set upon final end of a sequence (Write “1” to clear flag)
		0	None.
		1	End-of-Sequence(burst) Interrupt occurred
0	EOCIRQ		This flag will be set upon each conversion when a sequence occurs. Use this bit when polling the ADC for completion in single conversion mode. (Write “1” to clear flag)
		0	None.
		1	End-of-Conversion Interrupt occurred