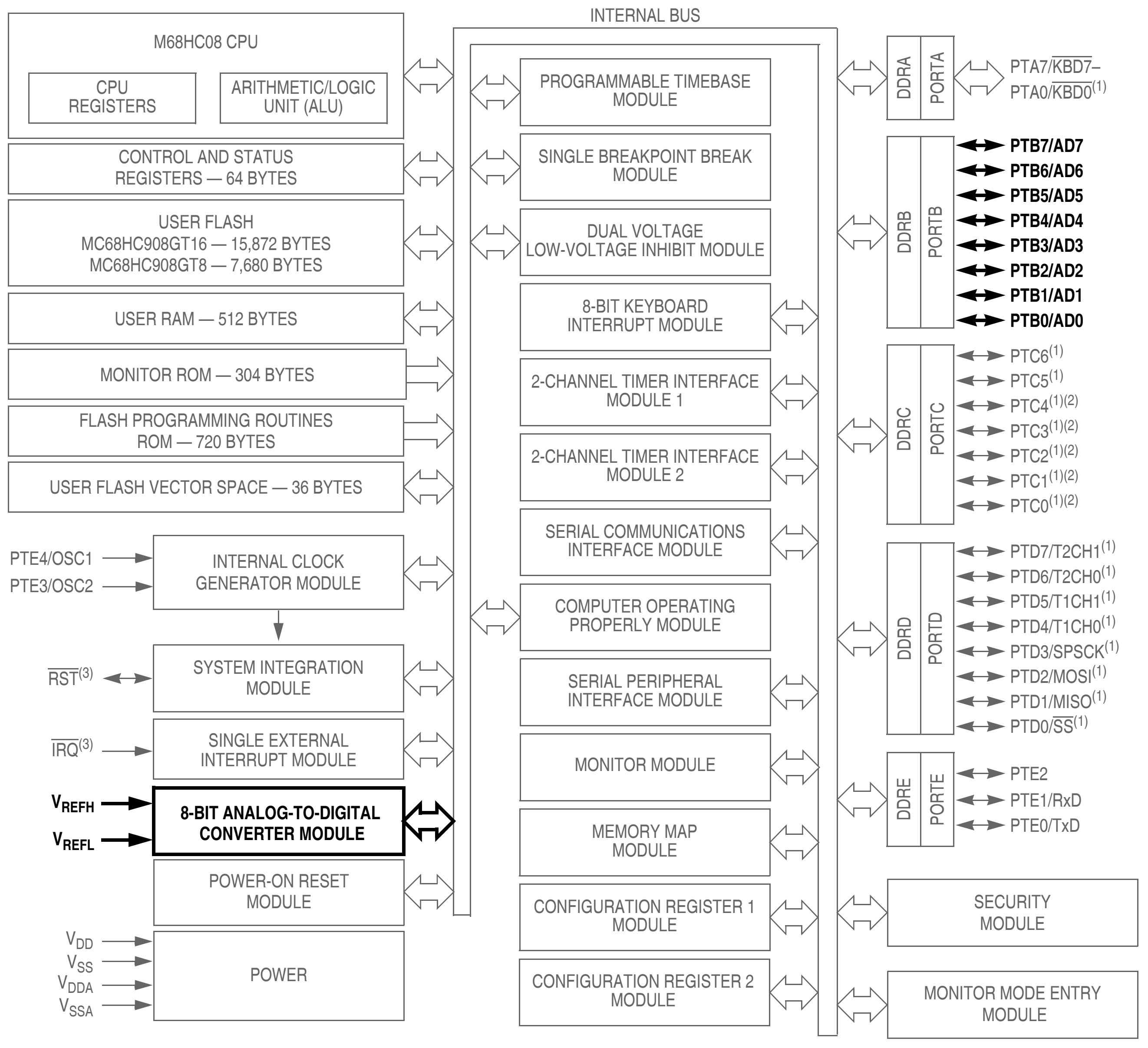
NXP USA Inc. - MC68HC908GT16CB Datasheet

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	HC08
Core Size	8-Bit
Speed	8MHz
Connectivity	SCI, SPI
Peripherals	LVD, POR, PWM
Number of I/O	36
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 8x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	42-SDIP (0.600", 15.24mm)
Supplier Device Package	42-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc68hc908gt16cb


INTERNAL BUS
M68HC08 CPU
CPU REGISTERS
ARITHMETIC/LOGIC UNIT (ALU)
CONTROL AND STATUS REGISTERS — 64 BYTES
USER FLASH MC68HC908GT16 — 15,872 BYTES MC68HC908GT8 — 7,680 BYTES
USER RAM — 512 BYTES
MONITOR ROM — 304 BYTES
FLASH PROGRAMMING ROUTINES ROM — 720 BYTES
USER FLASH VECTOR SPACE — 36 BYTES
PTE4/OSC1
PTE3/OSC2
INTERNAL CLOCK GENERATOR MODULE
RST(3)
SYSTEM INTEGRATION MODULE
IRQ(3)
SINGLE EXTERNAL INTERRUPT MODULE
VREFH
VREFL
8-BIT ANALOG-TO-DIGITAL CONVERTER MODULE
POWER-ON RESET MODULE
VDD
VSS
VDDA
VSSA
POWER
PROGRAMMABLE TIMEBASE MODULE
SINGLE BREAKPOINT BREAK MODULE
DUAL VOLTAGE LOW-VOLTAGE INHIBIT MODULE
8-BIT KEYBOARD INTERRUPT MODULE
2-CHANNEL TIMER INTERFACE MODULE 1
2-CHANNEL TIMER INTERFACE MODULE 2
SERIAL COMMUNICATIONS INTERFACE MODULE
COMPUTER OPERATING PROPERLY MODULE
SERIAL PERIPHERAL INTERFACE MODULE
MONITOR MODULE
MEMORY MAP MODULE
CONFIGURATION REGISTER 1 MODULE
CONFIGURATION REGISTER 2 MODULE
DDRA
PORTA
PTA7/KBD7–PTA0/KBD0(1)
DDRB
PORTB
PTB7/AD7
PTB6/AD6
PTB5/AD5
PTB4/AD4
PTB3/AD3
PTB2/AD2
PTB1/AD1
PTB0/AD0
DDRC
PORTC
PTC6(1)
PTC5(1)
PTC4(1)(2)
PTC3(1)(2)
PTC2(1)(2)
PTC1(1)(2)
PTC0(1)(2)
DDRD
PORTD
PTD7/T2CH1(1)
PTD6/T2CH0(1)
PTD5/T1CH1(1)
PTD4/T1CH0(1)
PTD3/SPSCK(1)
PTD2/MOSI(1)
PTD1/MISO(1)
PTD0/SS(1)
DDRE
PORTE
PTE2
PTE1/RxD
PTE0/TxD
SECURITY MODULE
MONITOR MODE ENTRY MODULE

1. Ports are software configurable with pullup device if input port.
2. Higher current drive port pins
3. Pin contains integrated pullup device

Figure 3-1. Block Diagram Highlighting ADC Block and Pins

Chapter 5
Computer Operating Properly (COP) Module

5.1 Introduction

The computer operating properly (COP) module contains a free-running counter that generates a reset if allowed to overflow. The COP module helps software recover from runaway code. Prevent a COP reset by clearing the COP counter periodically. The COP module can be disabled through the COPD bit in the CONFIG register.

5.2 Functional Description

Figure 5-1 shows the structure of the COP module.

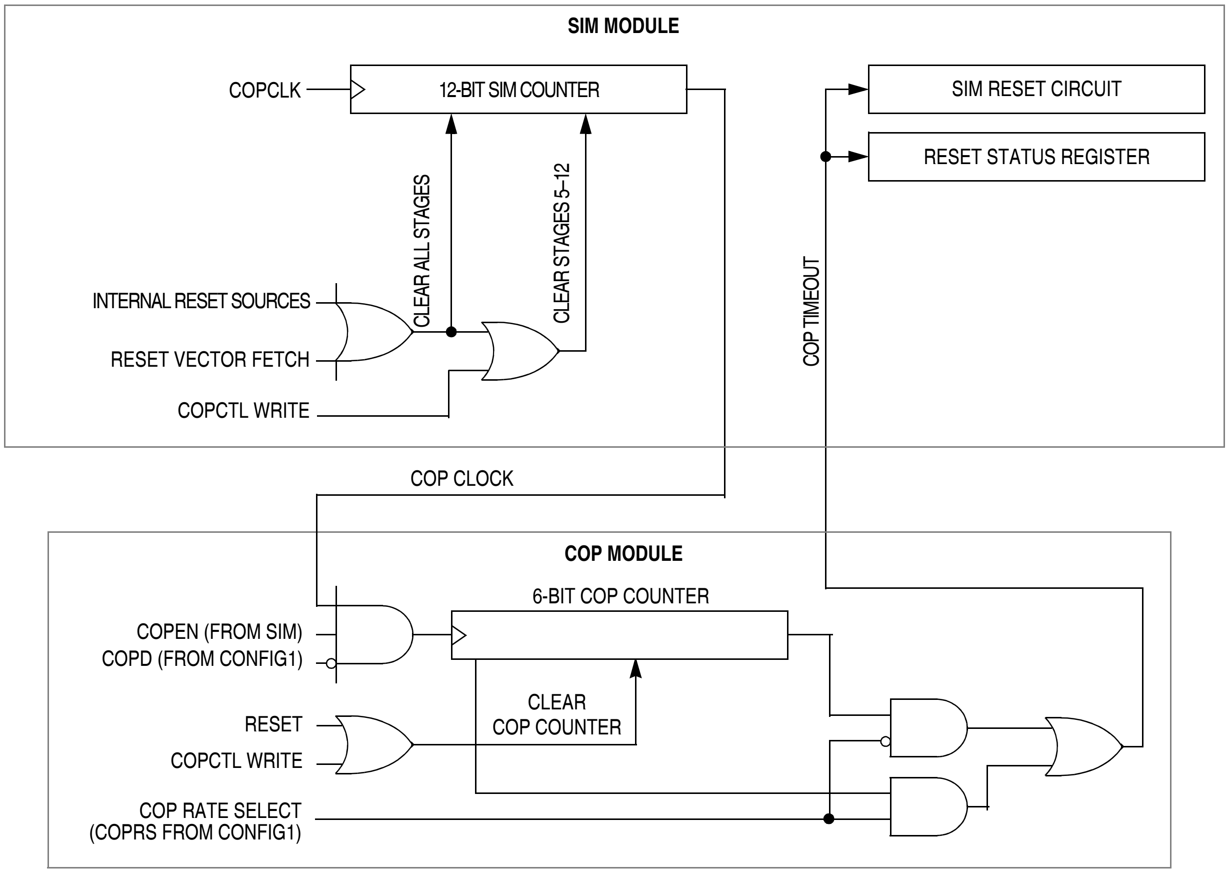


Figure 5-1. COP Block Diagram

The COP counter is a free-running 6-bit counter preceded by a 12-bit prescaler counter. If not cleared by software, the COP counter overflows and generates an asynchronous reset after 262,128 or 8176 COPCLK cycles, depending on the state of the COP rate select bit, COPRS, in the configuration register. With a 8176 COPCLK cycle overflow option, a 32.768-kHz crystal gives a COP timeout period of 250 ms. Writing any value to location $FFFF before an overflow occurs prevents a COP reset by clearing the COP counter and stages 12 through 5 of the prescaler.

NOTE

Service the COP immediately after reset and before entering or after exiting stop mode to guarantee the maximum time before the first COP counter overflow.

A COP reset pulls the $\overline{\text{RST}}$ pin low for 32 COPCLK cycles and sets the COP bit in the reset status register (RSR).

In monitor mode, the COP is disabled if the $\overline{\text{RST}}$ pin or the $\overline{\text{IRQ1}}$ is held at V_{TST}. During the break state, V_{TST} on the $\overline{\text{RST}}$ pin disables the COP.

NOTE

Place COP clearing instructions in the main program and not in an interrupt subroutine. Such an interrupt subroutine could keep the COP from generating a reset even while the main program is not working properly.

5.3 I/O Signals

The following paragraphs describe the signals shown in Figure 5-1.

5.3.1 COPCLK

COPCLK is a clock generated by the clock selection circuit in the internal clock generator (ICG). See 7.3.5 Clock Selection Circuit for more details.

5.3.2 STOP Instruction

The STOP instruction clears the COP prescaler.

5.3.3 COPCTL Write

Writing any value to the COP control register (COPCTL) (see 5.4 COP Control Register) clears the COP counter and clears bits 12 through 5 of the prescaler. Reading the COP control register returns the low byte of the reset vector.

5.3.4 Power-On Reset

The power-on reset (POR) circuit clears the COP prescaler 4096 CGMXCLK cycles after power-up.

5.3.5 Internal Reset

An internal reset clears the COP prescaler and the COP counter.

Settling time depends primarily on how many corrections it takes to change the clock period and the period of each correction. Since the corrections require four periods of the low-frequency base clock ($4^*\tau_{IBASE}$), and since ICLK is N (the ICG multiply factor for the desired frequency) times faster than IBASE, each correction takes $4^*N^*\tau_{ICLK}$. The period of ICLK, however, will vary as the corrections occur.

7.4.6.1 Settling to Within 15 Percent

When the error is greater than 15 percent, the filter takes eight corrections to double or halve the clock period. Due to how the DCO increases or decreases the clock period, the total period of these eight corrections is approximately 11 times the period of the fastest correction. (If the corrections were perfectly linear, the total period would be 11.5 times the minimum period; however, the ring must be slightly nonlinear.) Therefore, the total time it takes to double or halve the clock period is $44^*N^*\tau_{ICLKFAST}$.

If the clock period needs more than doubled or halved, the same relationship applies, only for each time the clock period needs doubled, the total number of cycles doubles. That is, when transitioning from fast to slow, going from the initial speed to half speed takes $44^*N^*\tau_{ICLKFAST}$; from half speed to quarter speed takes $88^*N^*\tau_{ICLKFAST}$; going from quarter speed to eighth speed takes $176^*N^*\tau_{ICLKFAST}$; and so on. This series can be expressed as $(2^x–1)^*44^*N^*\tau_{ICLKFAST}$, where x is the number of times the speed needs doubled or halved. Since 2^x happens to be equal to $\tau_{ICLKSLOW}/\tau_{ICLKFAST}$, the equation reduces to $44^*N^*(\tau_{ICLKSLOW}–\tau_{ICLKFAST})$.

Note that increasing speed takes much longer than decreasing speed since N is higher. This can be expressed in terms of the initial clock period (τ_1) minus the final clock period (τ_2) as such:

$$\tau_{15} = \mathrm{abs}[44N(\tau_1 - \tau_2)]$$

7.4.6.2 Settling to Within 5 Percent

Once the clock period is within 15 percent of the desired clock period, the filter starts making smaller adjustments. When between 15 percent and 5 percent error, each correction will adjust the clock period between 1.61 percent and 2.94 percent. In this mode, a maximum of eight corrections will be required to get to less than 5 percent error. Since the clock period is relatively close to desired, each correction takes approximately the same period of time, or $4^*\tau_{IBASE}$. At this point, the internal clock stable bit (ICGS) will be set and the clock frequency is usable, although the error will be as high as 5 percent. The total time to this point is:

$$\tau_5 = \mathrm{abs}[44N(\tau_1 - \tau_2)] + 32\tau_{IBASE}$$

7.4.6.3 Total Settling Time

Once the clock period is within 5 percent of the desired clock period, the filter starts making minimum adjustments. In this mode, each correction will adjust the frequency between 0.202 percent and 0.368 percent. A maximum of 24 corrections will be required to get to the minimum error. Each correction takes approximately the same period of time, or $4^*\tau_{IBASE}$. Added to the corrections for 15 percent to 5 percent, this makes 32 corrections ($128^*\tau_{IBASE}$) to get from 15 percent to the minimum error. The total time to the minimum error is:

$$\tau_{tot} = \mathrm{abs}[44N(\tau_1 - \tau_2)] + 128\tau_{IBASE}$$

The equations for τ_{15}, τ_5, and τ_{tot} are dependent on the actual initial and final clock periods τ_1 and τ_2, not the nominal. This means the variability in the ICLK frequency due to process, temperature, and voltage must be considered. Additionally, other process factors and noise can affect the actual tolerances of the points at which the filter changes modes. This means a worst case adjustment of up to 35 percent (ICLK clock period tolerance plus 10 percent) must be added. This adjustment can be reduced with trimming. Table 7-3 shows some typical values for settling time.

Table 7-3. Typical Settling Time Examples

τ_1	τ_2	N	τ_{15}	τ_5	τ_{tot}
1/ (6.45 MHz)	1/ (25.8 MHz)	84	430 µs	535 µs	850 µs
1/ (25.8 MHz)	1/ (6.45 MHz)	21	107 µs	212 µs	525 µs
1/ (25.8 MHz)	1/ (307.2 kHz)	1	141 µs	246 µs	560 µs
1/ (307.2 kHz)	1/ (25.8 MHz)	84	11.9 ms	12.0 ms	12.3 ms

7.4.7 Trimming Frequency on the Internal Clock Generator

The unadjusted frequency of the low-frequency base clock (IBASE), when the comparators in the frequency comparator indicate zero error, will vary as much as ±25 percent due to process, temperature, and voltage dependencies. These dependencies are in the voltage and current references, the offset of the comparators, and the internal capacitor.

The method of changing the unadjusted operating point is by changing the size of the capacitor. This capacitor is designed with 639 equally sized units. Of that number, 384 of these units are always connected. The remaining 255 units are put in by adjusting the ICG trim factor (TRIM). The default value for TRIM is $80, or 128 units, making the default capacitor size 512. Each unit added or removed will adjust the output frequency by about ±0.195 percent of the unadjusted frequency (adding to TRIM will decrease frequency). Therefore, the frequency of IBASE can be changed to ±25 percent of its unadjusted value, which is enough to cancel the process variability mentioned before.

The best way to trim the internal clock is to use the timer to measure the width of an input pulse on an input capture pin (this pulse must be supplied by the application and should be as long or wide as possible). Considering the prescale value of the timer and the theoretical (zero error) frequency of the bus (307.2 kHz *N/4), the error can be calculated. This error, expressed as a percentage, can be divided by 0.195 percent and the resultant factor added or subtracted from TRIM. This process should be repeated to eliminate any residual error.

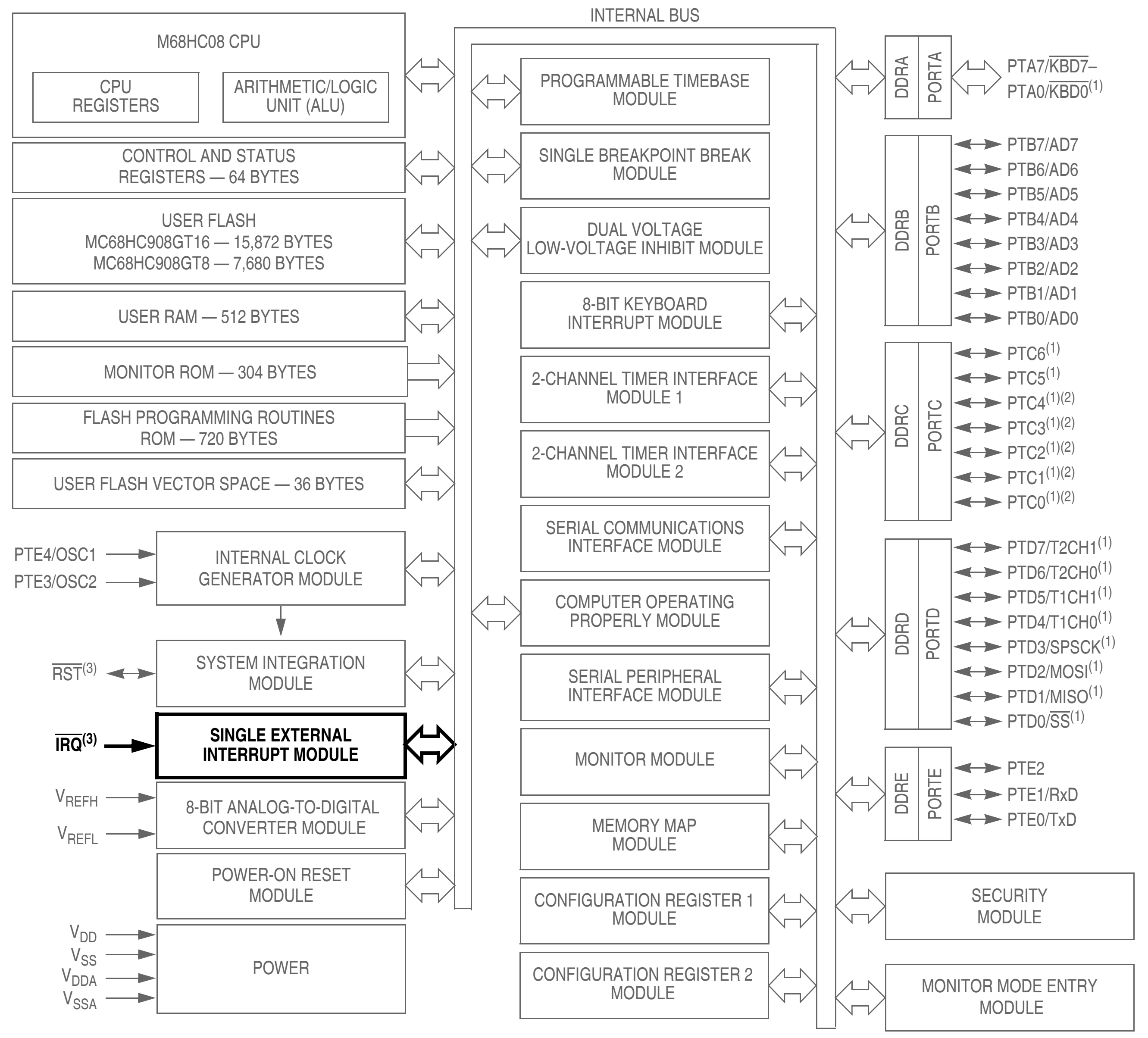
7.5 Low-Power Modes

The WAIT and STOP instructions put the MCU in low power- consumption standby modes.

7.5.1 Wait Mode

The ICG remains active in wait mode. If enabled, the ICG interrupt to the CPU can bring the MCU out of wait mode.

In some applications, low power-consumption is desired in wait mode and a high-frequency clock is not needed. In these applications, reduce power consumption by either selecting a low-frequency external clock and turn the internal clock generator off or reduce the bus frequency by minimizing the ICG multiplier factor (N) before executing the WAIT instruction.


INTERNAL BUS
M68HC08 CPU
CPU REGISTERS
ARITHMETIC/LOGIC UNIT (ALU)
CONTROL AND STATUS REGISTERS — 64 BYTES
USER FLASH MC68HC908GT16 — 15,872 BYTES MC68HC908GT8 — 7,680 BYTES
USER RAM — 512 BYTES
MONITOR ROM — 304 BYTES
FLASH PROGRAMMING ROUTINES ROM — 720 BYTES
USER FLASH VECTOR SPACE — 36 BYTES
PTE4/OSC1
PTE3/OSC2
INTERNAL CLOCK GENERATOR MODULE
RST(3)
SYSTEM INTEGRATION MODULE
IRQ(3)
SINGLE EXTERNAL INTERRUPT MODULE
VREFH
VREFL
8-BIT ANALOG-TO-DIGITAL CONVERTER MODULE
POWER-ON RESET MODULE
VDD
VSS
VDDA
VSSA
POWER
PROGRAMMABLE TIMEBASE MODULE
SINGLE BREAKPOINT BREAK MODULE
DUAL VOLTAGE LOW-VOLTAGE INHIBIT MODULE
8-BIT KEYBOARD INTERRUPT MODULE
2-CHANNEL TIMER INTERFACE MODULE 1
2-CHANNEL TIMER INTERFACE MODULE 2
SERIAL COMMUNICATIONS INTERFACE MODULE
COMPUTER OPERATING PROPERLY MODULE
SERIAL PERIPHERAL INTERFACE MODULE
MONITOR MODULE
MEMORY MAP MODULE
CONFIGURATION REGISTER 1 MODULE
CONFIGURATION REGISTER 2 MODULE
DDRA
PORTA
PTA7/KBD7–PTA0/KBD0(1)
DDRB
PORTB
PTB7/AD7
PTB6/AD6
PTB5/AD5
PTB4/AD4
PTB3/AD3
PTB2/AD2
PTB1/AD1
PTB0/AD0
DDRC
PORTC
PTC6(1)
PTC5(1)
PTC4(1)(2)
PTC3(1)(2)
PTC2(1)(2)
PTC1(1)(2)
PTC0(1)(2)
DDRD
PORTD
PTD7/T2CH1(1)
PTD6/T2CH0(1)
PTD5/T1CH1(1)
PTD4/T1CH0(1)
PTD3/SPSCK(1)
PTD2/MOSI(1)
PTD1/MISO(1)
PTD0/SS(1)
DDRE
PORTE
PTE2
PTE1/RxD
PTE0/TxD
SECURITY MODULE
MONITOR MODE ENTRY MODULE

1. Ports are software configurable with pullup device if input port.
2. Higher current drive port pins
3. Pin contains integrated pullup device

Figure 8-1. Block Diagram Highlighting IRQ Block and Pins

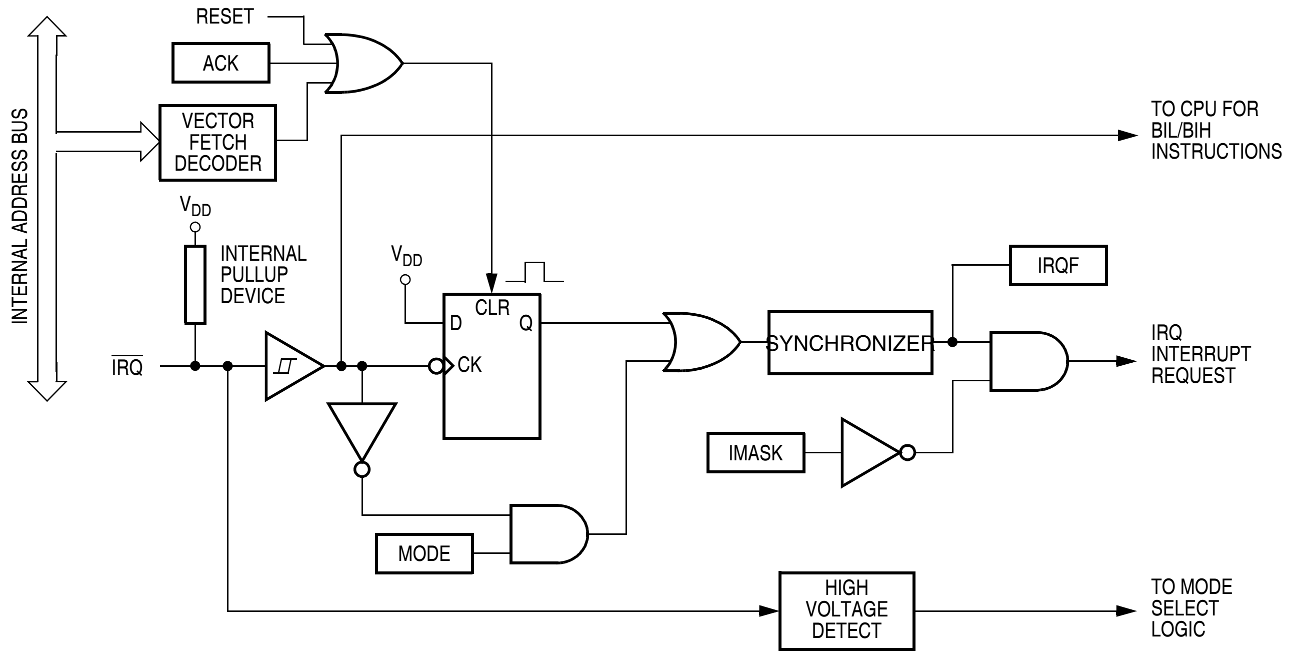


Figure 8-2. IRQ Module Block Diagram

The vector fetch or software clear may occur before or after the interrupt pin returns to logic 1. As long as the pin is low, the interrupt request remains pending. A reset will clear the latch and the MODE control bit, thereby clearing the interrupt even if the pin stays low.

When set, the IMASK bit in the INTSCR mask all external interrupt requests. A latched interrupt request is not presented to the interrupt priority logic unless the IMASK bit is clear.

NOTE

The interrupt mask (I) in the condition code register (CCR) masks all interrupt requests, including external interrupt requests.

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$001D	IRQ Status and Control Register (INTSCR) See page 104.	Read:	0	0	0	0	IRQF	0	IMASK	MODE
		Write:	▨	▨	▨	▨	▨	ACK		
		Reset:	0	0	0	0	0	0	0	0

▨ = Unimplemented

Figure 8-3. IRQ I/O Register Summary

8.4 $\overline{\text{IRQ}}$ Pin

A logic 0 on the $\overline{\text{IRQ}}$ pin can latch an interrupt request into the IRQ latch. A vector fetch, software clear, or reset clears the IRQ latch.

If the MODE bit is set, the $\overline{\text{IRQ}}$ pin is both falling-edge-sensitive and low-level-sensitive. With MODE set, both of the following actions must occur to clear IRQ:

- Vector fetch or software clear — A vector fetch generates an interrupt acknowledge signal to clear the latch. Software may generate the interrupt acknowledge signal by writing a 1 to the ACK bit in the interrupt status and control register (INTSCR). The ACK bit is useful in applications that poll the

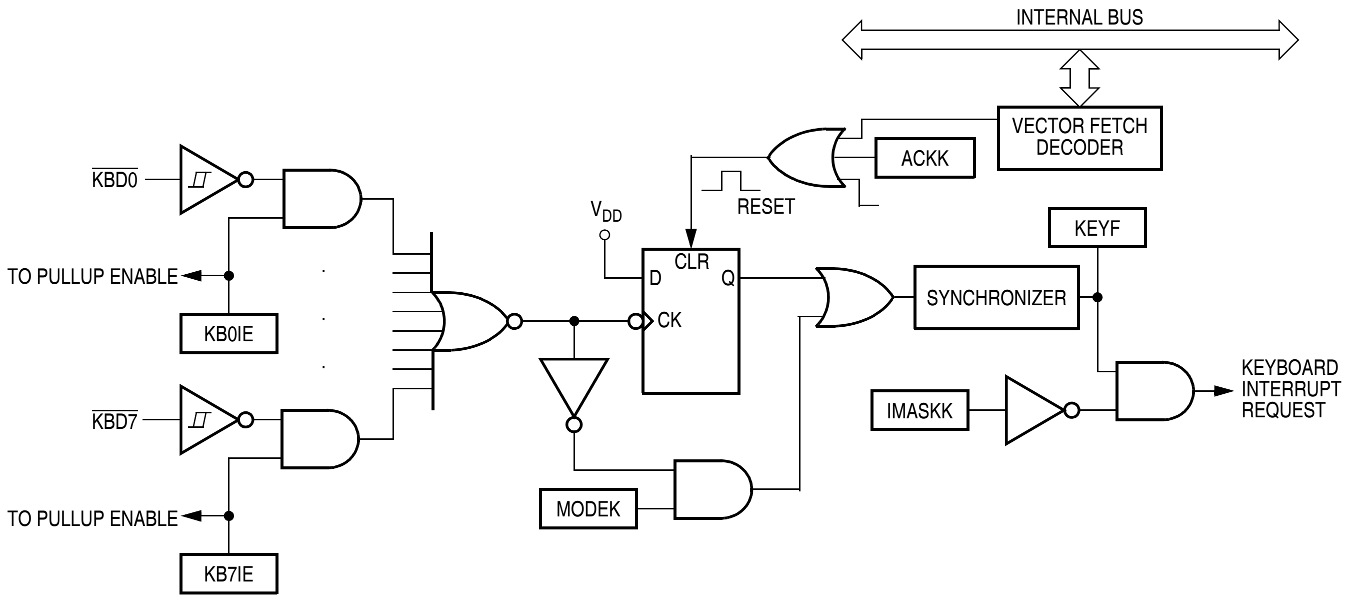


Figure 9-2. Keyboard Module Block Diagram

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$001A	Keyboard Status and Control Register (INTKBSCR) See page 111.	Read:	0	0	0	0	KEYF	0	IMASKK	MODEK
		Write:	▨	▨	▨	▨	▨	ACKK		
		Reset:	0	0	0	0	0	0	0	0
$001B	Keyboard Interrupt Enable Register (INTKBIER) See page 112.	Read:	KBIE7	KBIE6	KBIE5	KBIE4	KBIE3	KBIE2	KBIE1	KBIE0
		Write:								
		Reset:	0	0	0	0	0	0	0	0

▨ = Unimplemented

Figure 9-3. I/O Register Summary

If the MODEK bit is set, the keyboard interrupt pins are both falling edge- and low-level sensitive, and both of the following actions must occur to clear a keyboard interrupt request:

- Vector fetch or software clear — A vector fetch generates an interrupt acknowledge signal to clear the interrupt request. Software may generate the interrupt acknowledge signal by writing a 1 to the ACKK bit in the keyboard status and control register (INTKBSCR). The ACKK bit is useful in applications that poll the keyboard interrupt pins and require software to clear the keyboard interrupt request. Writing to the ACKK bit prior to leaving an interrupt service routine can also prevent spurious interrupts due to noise. Setting ACKK does not affect subsequent transitions on the keyboard interrupt pins. A falling edge that occurs after writing to the ACKK bit latches another interrupt request. If the keyboard interrupt mask bit, IMASKK, is clear, the CPU loads the program counter with the vector address at locations $FFE0 and $FFE1.
- Return of all enabled keyboard interrupt pins to logic 1 — As long as any enabled keyboard interrupt pin is at logic 0, the keyboard interrupt remains set.

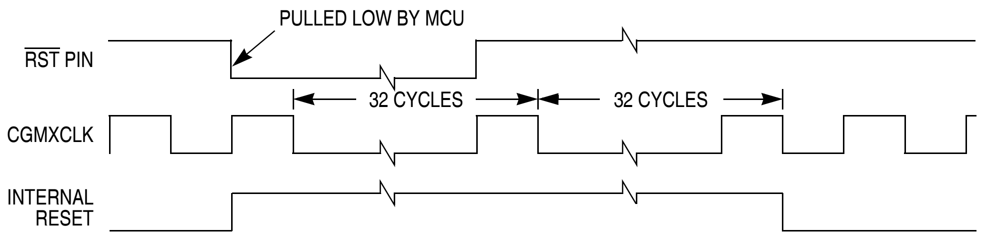


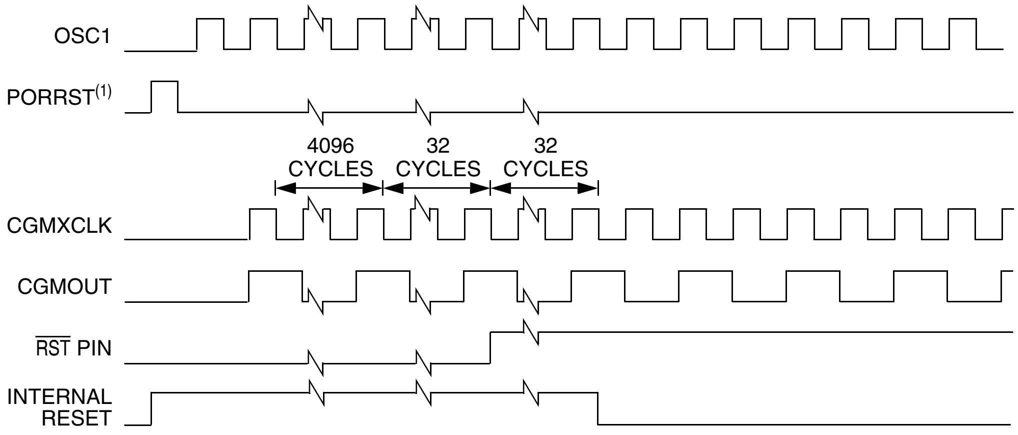
Figure 13-1. Internal Reset Timing

13.2.3.1 Power-On Reset (POR)

A power-on reset (POR) is an internal reset caused by a positive transition on the V_{DD} pin. V_{DD} at the POR must go completely to 0 V to reset the MCU. This distinguishes between a reset and a POR. The POR is not a brown-out detector, low-voltage detector, or glitch detector.

A power-on reset:

- Holds the clocks to the CPU and modules inactive for an oscillator stabilization delay of 4096 CGMXCLK cycles
- Drives the $\overline{\text{RST}}$ pin low during the oscillator stabilization delay
- Releases the RST pin 32 CGMXCLK cycles after the oscillator stabilization delay
- Releases the CPU to begin the reset vector sequence 64 CGMXCLK cycles after the oscillator stabilization delay
- Sets the POR bit in the SIM reset status register and clears all other bits in the register



1. PORRST is an internally generated power-on reset pulse.

Figure 13-2. Power-On Reset Recovery

13.2.3.2 Computer Operating Properly (COP) Reset

A COP reset is an internal reset caused by an overflow of the COP counter. A COP reset sets the COP bit in the system integration module (SIM) reset status register.

To clear the COP counter and prevent a COP reset, write any value to the COP control register at location $FFFF.

Chapter 15
System Integration Module (SIM)

15.1 Introduction

This section describes the system integration module (SIM). Together with the central processor unit (CPU), the SIM controls all microconroller unit (MCU) activities. A block diagram of the SIM is shown in Figure 15-1. Table 15-1 is a summary of the SIM input/output (I/O) registers. The SIM is a system state controller that coordinates CPU and exception timing.

The SIM is responsible for:

- Bus clock generation and control for CPU and peripherals:
  - Stop/wait/reset/break entry and recovery
  - Internal clock control
- Master reset control, including power-on reset (POR) and computer operating properly (COP) timeout
- Interrupt arbitration

Table 15-1 shows the internal signal names used in this section.

Table 15-1. Signal Name Conventions

Signal Name	Description
CGMXCLK	Selected clock source from internal clock generator module (ICG)
CGMOUT	Clock output from ICG module (Bus clock = CGMOUT divided by two)
IAB	Internal address bus
IDB	Internal data bus
PORRST	Signal from the power-on reset module to the SIM
IRST	Internal reset signal
R/$\overline{\text{W}}$	Read/write signal

is pending upon exit from the original interrupt service routine, the pending interrupt is serviced before the LDA instruction is executed.

The LDA opcode is prefetched by both the INT1 and INT2 RTI instructions. However, in the case of the INT1 RTI prefetch, this is a redundant operation.

NOTE

To maintain compatibility with the M6805 Family, the H register is not pushed on the stack during interrupt entry. If the interrupt service routine modifies the H register or uses the indexed addressing mode, software should save the H register and then restore it prior to exiting the routine.

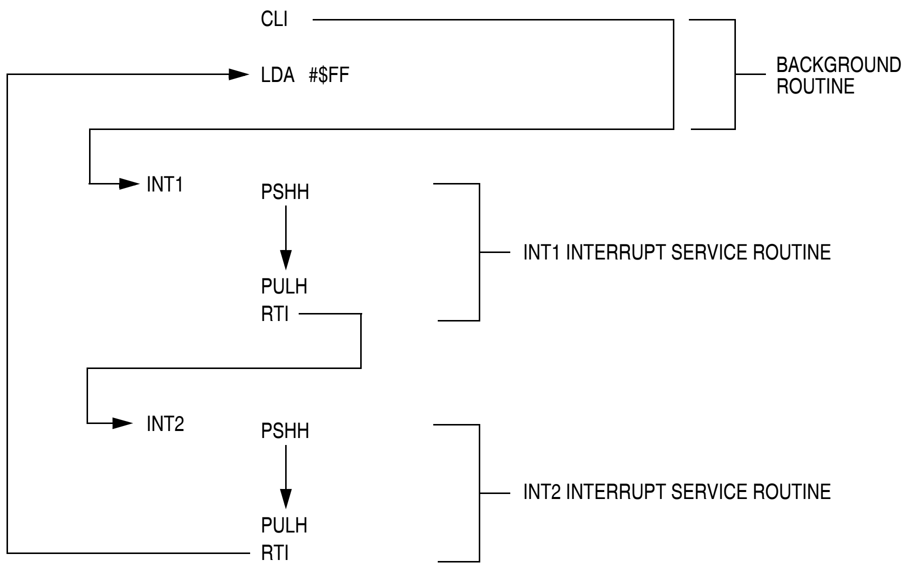

CLI
LDA #$FF
BACKGROUND ROUTINE
INT1
PSHH
PULH
RTI
INT1 INTERRUPT SERVICE ROUTINE
INT2
PSHH
PULH
RTI
INT2 INTERRUPT SERVICE ROUTINE

Figure 15-11. Interrupt Recognition Example

15.5.1.2 SWI Instruction

The SWI instruction is a non-maskable instruction that causes an interrupt regardless of the state of the interrupt mask (I bit) in the condition code register.

NOTE

A software interrupt pushes PC onto the stack. A software interrupt does not push PC – 1, as a hardware interrupt does.

15.5.1.3 Interrupt Status Registers

The flags in the interrupt status registers identify maskable interrupt sources. Table 15-3 summarizes the interrupt sources and the interrupt status register flags that they set. The interrupt status registers can be useful for debugging.

When the internal address bus matches the value written in the break address registers or when software writes a 1 to the BRKA bit in the break status and control register, the CPU starts a break interrupt by:

- Loading the instruction register with the SWI instruction
- Loading the program counter with \$FFFC and \$FFFD (\$FEFC and \$FEFD in monitor mode)

The break interrupt timing is:

- When a break address is placed at the address of the instruction opcode, the instruction is not executed until after completion of the break interrupt routine.
- When a break address is placed at an address of an instruction operand, the instruction is executed before the break interrupt.
- When software writes a 1 to the BRKA bit, the break interrupt occurs just before the next instruction is executed.

By updating a break address and clearing the BRKA bit in a break interrupt routine, a break interrupt can be generated continuously.

CAUTION

A break address should be placed at the address of the instruction opcode. When software does not change the break address and clears the BRKA bit in the first break interrupt routine, the next break interrupt will not be generated after exiting the interrupt routine even when the internal address bus matches the value written in the break address registers.

19.2.1.1 Flag Protection During Break Interrupts

The system integration module (SIM) controls whether or not module status bits can be cleared during the break state. The BCFE bit in the break flag control register (BFCR) enables software to clear status bits during the break state. See 15.7.3 SIM Break Flag Control Register and the **Break Interrupts** subsection for each module.

19.2.1.2 TIM1 and TIM2 During Break Interrupts

A break interrupt stops the timer counters.

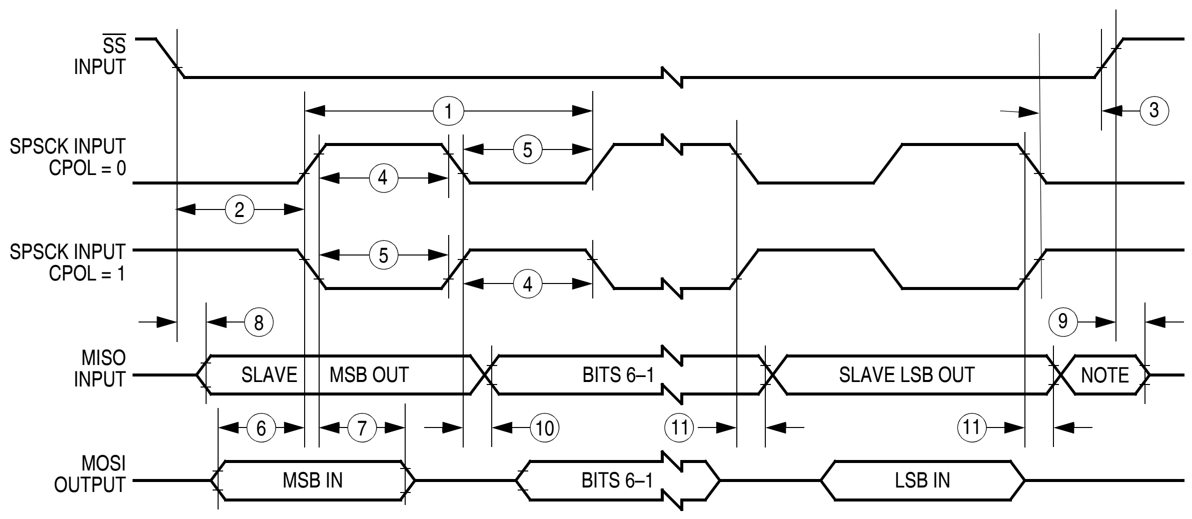
19.2.1.3 COP During Break Interrupts

The COP is disabled during a break interrupt when V_{TST} is present on the $\overline{RST}$ pin.

19.2.2 Break Module Registers

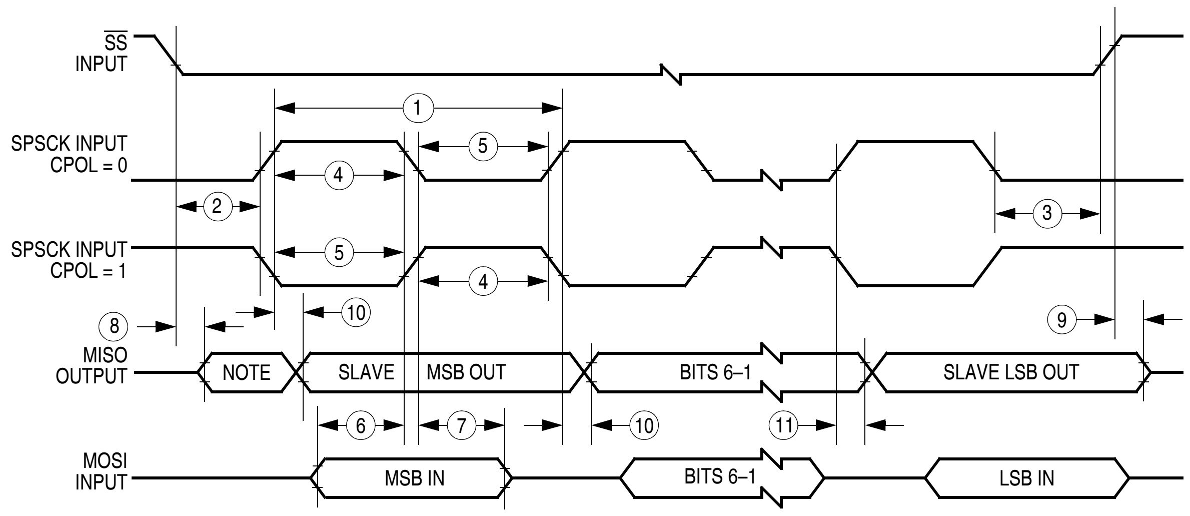
These registers control and monitor operation of the break module:

- Break status and control register (BRKSCR)
- Break address register high (BRKH)
- Break address register low (BRKL)
- SIM break status register (SBSR)
- SIM break flag control register (SBFCR)



Note: Not defined but normally MSB of character just received

a) SPI Slave Timing (CPHA = 0)



Note: Not defined but normally LSB of character previously transmitted

b) SPI Slave Timing (CPHA = 1)

Figure 20-18. SPI Slave Timing

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.

2. ALL DIMENSIONS IN MILLIMETERS.

3. DIMENSION TO CENTER OF LEAD WHEN FORMED PARALLEL.

4. DIMENSION DOES NOT INCLUDE MOLD FLASH. MAXIMUM MOLD FLASH 0.25.

	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: 42 LD PDIP	DOCUMENT NO: 98ASB42767B	REV: A
	CASE NUMBER: 858-01	24 OCT 2005
	STANDARD: NON JEDEC	

A.9.1 Internal Oscillator Characteristics

Characteristic[1]	Symbol	Min	Typ	Max	Unit
Internal oscillator base frequency[2], [3]	f_{INTOSC}	183.75	245	306.25	kHz
Internal oscillator tolerance	f_{OSC_TOL}	–25	—	+25	%
Internal oscillator multiplier[4]	N	1	—	127	—

1. V_{DD} = 5.5 Vdc to 2.7 Vdc, V_{SS} = 0 Vdc, $T_A = T_A$ (min) to T_A (max), unless otherwise noted
2. Internal oscillator is selectable through software for a maximum frequency.
   Actual frequency will be multiplier (N) x base frequency.
3. $f_{Bus} = (f_{INTOSC} / 4) \times N$ when internal clock source selected
4. Multiplier must be chosen to limit the maximum bus frequency of 4 MHz for 2.7-V operation and 8 MHz for 4.5-V operation.

A.9.2 Memory Characteristics

Characteristic	Symbol	Min	Max	Unit
RAM data retention voltage	V_{RDR}	1.3	—	V

Note: Since MC68HC08GT16 is a ROM device, Flash memory electrical characteristics do not apply.

A.10 Order Numbers

These part numbers are generic numbers only. To place an order, ROM code must be submitted to the ROM Processing Center (RPC).

MC Order Number	Package	Operating Temperature Range	RoHS Compliant
MC08GT16CBE	42-pin SDIP	–40 to +85°C	Yes
MC08GT16CFBE	44-pin QFP	–40 to +85°C	Yes