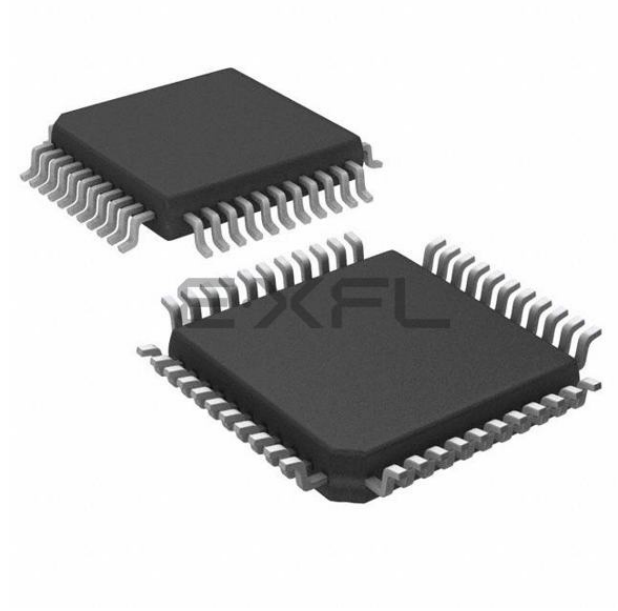

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	HC08
Core Size	8-Bit
Speed	8MHz
Connectivity	SCI, SPI
Peripherals	LVD, POR, PWM
Number of I/O	36
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 8x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-QFP
Supplier Device Package	44-QFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc908gt16cfbe

Revision History (Sheet 2 of 2)

Date	Revision Level	Description	Page Number(s)
September, 2004	3.0 (Continued from previous page)	Chapter 15 System Integration Module (SIM) — Clarified SIM features and functionality	179, 182, 183, 184
		15.7.2 SIM Reset Status Register — Clarified SRSR operation	194
		Table 19-1. Monitor Mode Signal Requirements and Options — Reworked	247
		19.2.1 Functional Description — Corrected Break description	237, 240
		19.3 Monitor Module (MON) — Reworked	243
		Chapter 20 Electrical Specifications — Revised/added tables: 20.5 5.0-V DC Electrical Characteristics 20.6 3.0-V DC Electrical Characteristics 20.7 Supply Current Characteristics 20.8 5-V Control Timing 20.9 3-V Control Timing	 257 258 259 260 260
		20.20 Memory Characteristics — Updated memory table	273
		Chapter 20 Electrical Specifications — Added figures: Figure 20-1. RST and IRQ Timing Figure 20-2. RST and IRQ Timing	 260 260
March, 2006	4.0	Appendix A MC68HC08GT16 — Introduces the MC68HC08GT16, the ROM part equivalent to the MC68HC908GT16.	281
April, 2007	5.0	4.2 Functional Description — In the description of the COP Rate Select Bit corrected the values for COP timeout period	57
		Figure 5-1. COP Block Diagram — Replaced BUSCLKX4 with COPCLK	61
		14.9.1 ESCI Arbiter Control Register — Replaced one half with one quarter in definition for ACLK = 0	176
		14.9.3 Bit Time Measurement — Replaced one half with one quarter in definition for ACLK = 0	177
		Revised the following diagrams: Figure 19-10. Forced Monitor Mode (Low) Figure 19-11. Forced Monitor Mode (High) Figure 19-12. Standard Monitor Mode	 245 245 246

Chapter 3
Analog-to-Digital Converter (ADC)

Chapter 4
Configuration Register (CONFIG)

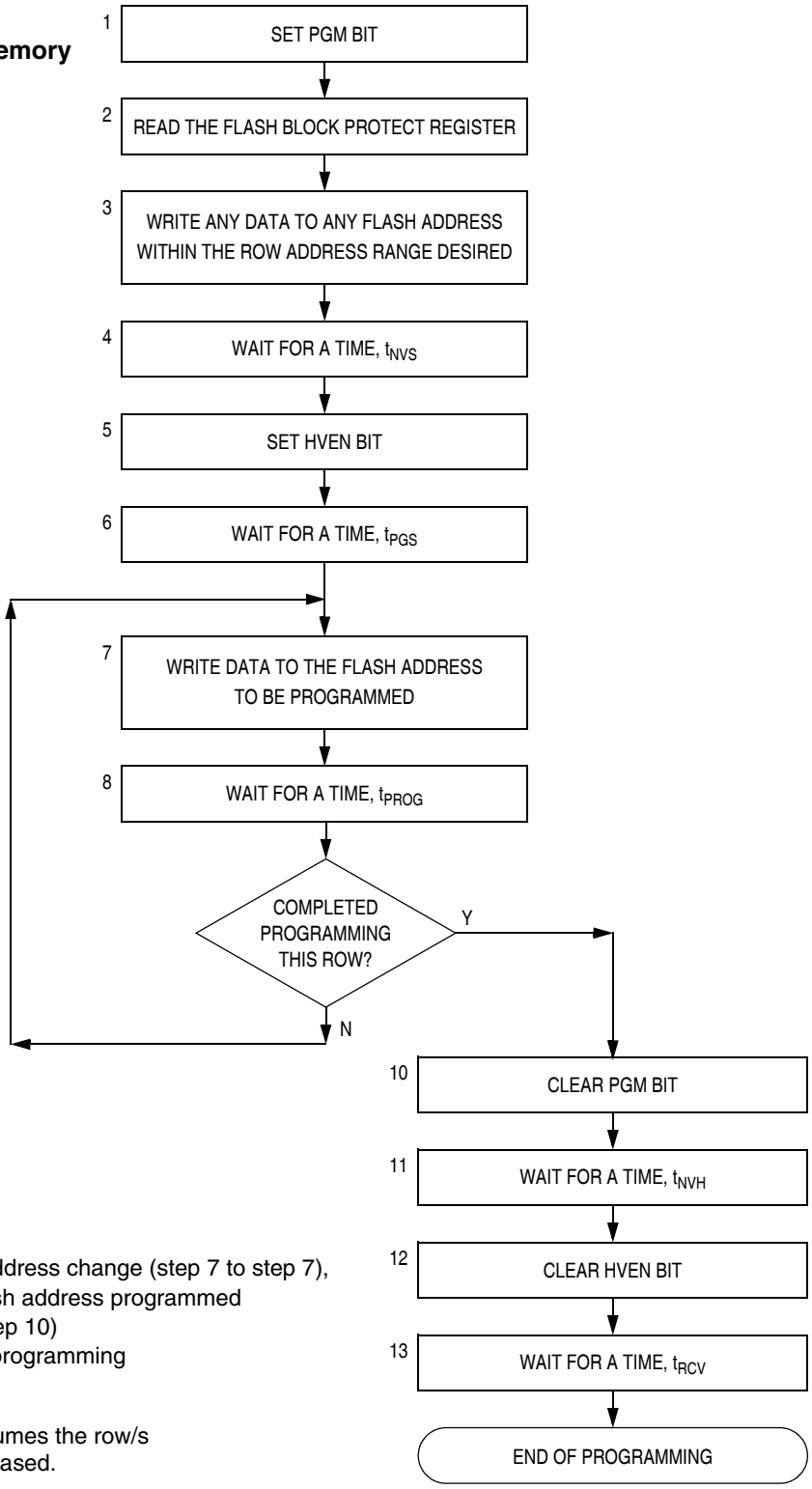
Chapter 5
Computer Operating Properly (COP) Module

$FE0C	LVI STATUS REGISTER (LVISR)
$FE0D ↓ $FE0F	UNIMPLEMENTED 3 BYTES
$FE10 ↓ $FE1F	UNIMPLEMENTED 16 BYTES RESERVED FOR COMPATIBILITY WITH MONITOR CODE FOR A-FAMILY PART
$FE20 ↓ $FF4F	MONITOR ROM 304 BYTES
$FF50 ↓ $FF7D	UNIMPLEMENTED 46 BYTES
$FF7E	FLASH BLOCK PROTECT REGISTER (FLBPR)
$FF7F	UNIMPLEMENTED 1 BYTE
$FF80	ICG USER TRIM REGISTER 5V (ICGTR5)
$FF81	ICG USER TRIM REGISTER 3V (ICGTR3)
$FF82 ↓ $FFDB	UNIMPLEMENTED 90 BYTES
$FFDC ↓ $FFFF[2]	FLASH VECTORS 36 BYTES

2. $FFF6–$FFFD reserved for eight security bytes

Figure 2-1. Memory Map (Continued)

Algorithm for programming a row (32 bytes) of FLASH memory



Note:

The time between each Flash address change (step 7 to step 7), or the time between the last Flash address programmed to clearing PGM bit (step 7 to step 10) must not exceed the maximum programming time, t_{PROG} max.

This row program algorithm assumes the row/s to be programmed are initially erased.

Figure 2-4. Flash Programming Flowchart

3.5.2 Stop Mode

The ADC module is inactive after the execution of a STOP instruction. Any pending conversion is aborted. ADC conversions resume when the MCU exits stop mode after an external interrupt. Allow one conversion cycle to stabilize the analog circuitry.

3.6 I/O Signals

The ADC module has eight pins shared with port B, PTB7/AD7–PTB0/AD0.

3.6.1 ADC Analog Power Pin (V_{DDA})

The ADC analog portion uses V_{DDA} as its power pin. Connect the V_{DDA} pin to the same voltage potential as V_{DD}. External filtering may be necessary to ensure clean V_{DDA} for good results.

NOTE

For maximum noise immunity, route V_{DDA} carefully and place bypass capacitors as close as possible to the package.

3.6.2 ADC Analog Ground Pin (V_{SSA})

The ADC analog portion uses V_{SSA} as its ground pin. Connect the V_{SSA} pin to the same voltage potential as V_{SS}.

NOTE

Route V_{SSA} cleanly to avoid any offset errors.

3.6.3 ADC Voltage Reference High Pin (V_{REFH})

The ADC analog portion uses V_{REFH} as its upper voltage reference pin. The V_{REFH} pin must be connected to the same voltage potential as V_{DDA}. External filtering is often necessary to ensure a clean V_{REFH} for good results. Any noise present on this pin will be reflected and possibly magnified in A/D conversion values.

NOTE

For maximum noise immunity, route V_{REFH} carefully and place bypass capacitors as close as possible to the package. Routing V_{REFH} close and parallel to V_{REFL} may improve common mode noise rejection.

3.6.4 ADC Voltage Reference Low Pin (V_{REFL})

The ADC analog portion uses V_{REFL} as its lower voltage reference pin. The V_{REFL} pin must be connected to the same voltage potential as V_{SSA}. External filtering is often necessary to ensure a clean V_{REFL} for good results. Any noise present on this pin will be reflected and possibly magnified in A/D conversion values.

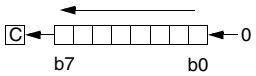
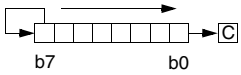
NOTE

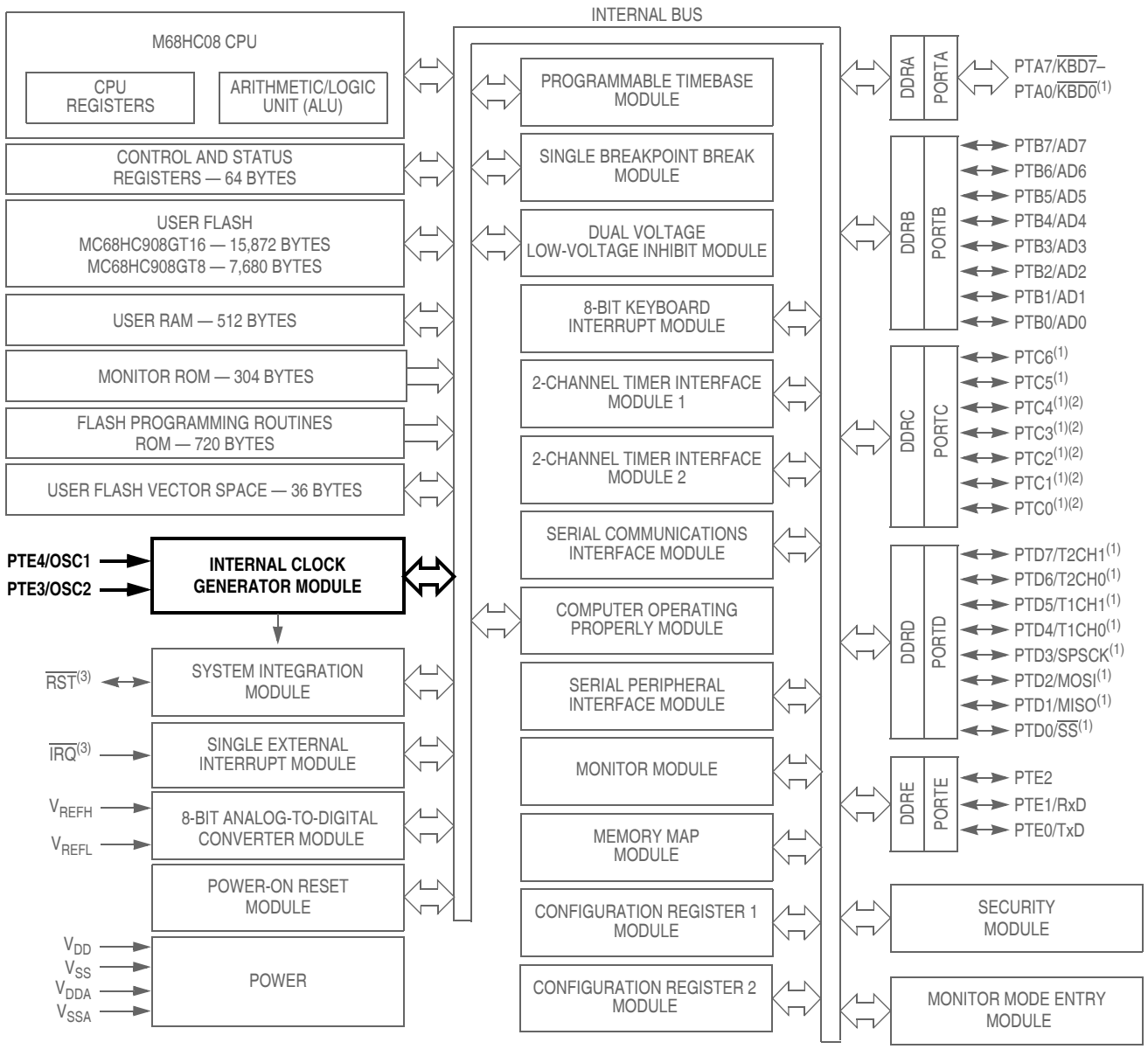
For maximum noise immunity, route V_{REFL} carefully and, if not connected to V_{SS}, place bypass capacitors as close as possible to the package. Routing V_{REFH} close and parallel to V_{REFL} may improve common mode noise rejection.

6.7 Instruction Set Summary

Table 6-1 provides a summary of the M68HC08 instruction set.

Table 6-1. Instruction Set Summary (Sheet 1 of 6)

Source Form	Operation	Description	Effect on CCR						Address Mode	Opcode	Operand	Cycles
			V	H	I	N	Z	C				
ADC #*opr* ADC *opr* ADC *opr* ADC *opr*,X ADC *opr*,X ADC ,X ADC *opr*,SP ADC *opr*,SP	Add with Carry	A ← (A) + (M) + (C)	↕	↕	–	↕	↕	↕	IMM DIR EXT IX2 IX1 IX SP1 SP2	A9 B9 C9 D9 E9 F9 9EE9 9ED9	ii dd hh ll ee ff ff ff ee ff	2 3 4 4 3 2 4 5
ADD #*opr* ADD *opr* ADD *opr* ADD *opr*,X ADD *opr*,X ADD ,X ADD *opr*,SP ADD *opr*,SP	Add without Carry	A ← (A) + (M)	↕	↕	–	↕	↕	↕	IMM DIR EXT IX2 IX1 IX SP1 SP2	AB BB CB DB EB FB 9EEB 9EDB	ii dd hh ll ee ff ff ff ee ff	2 3 4 4 3 2 4 5
AIS #*opr*	Add Immediate Value (Signed) to SP	SP ← (SP) + (16 « M)	–	–	–	–	–	–	IMM	A7	ii	2
AIX #*opr*	Add Immediate Value (Signed) to H:X	H:X ← (H:X) + (16 « M)	–	–	–	–	–	–	IMM	AF	ii	2
AND #*opr* AND *opr* AND *opr* AND *opr*,X AND *opr*,X AND ,X AND *opr*,SP AND *opr*,SP	Logical AND	A ← (A) & (M)	0	–	–	↕	↕	–	IMM DIR EXT IX2 IX1 IX SP1 SP2	A4 B4 C4 D4 E4 F4 9EE4 9ED4	ii dd hh ll ee ff ff ff ee ff	2 3 4 4 3 2 4 5
ASL *opr* ASLA ASLX ASL *opr*,X ASL ,X ASL *opr*,SP	Arithmetic Shift Left (Same as LSL)		↕	–	–	↕	↕	↕	DIR INH INH IX1 IX SP1	38 48 58 68 78 9E68	dd ff ff	4 1 1 4 3 5
ASR *opr* ASRA ASRX ASR *opr*,X ASR *opr*,X ASR *opr*,SP	Arithmetic Shift Right		↕	–	–	↕	↕	↕	DIR INH INH IX1 IX SP1	37 47 57 67 77 9E67	dd ff ff	4 1 1 4 3 5
BCC *rel*	Branch if Carry Bit Clear	PC ← (PC) + 2 + rel ? (C) = 0	–	–	–	–	–	–	REL	24	rr	3
BCLR *n*, *opr*	Clear Bit n in M	Mn ← 0	–	–	–	–	–	–	DIR (b0) DIR (b1) DIR (b2) DIR (b3) DIR (b4) DIR (b5) DIR (b6) DIR (b7)	11 13 15 17 19 1B 1D 1F	dd dd dd dd dd dd dd dd	4 4 4 4 4 4 4 4
BCS *rel*	Branch if Carry Bit Set (Same as BLO)	PC ← (PC) + 2 + *rel* ? (C) = 1	–	–	–	–	–	–	REL	25	rr	3
BEQ *rel*	Branch if Equal	PC ← (PC) + 2 + *rel* ? (Z) = 1	–	–	–	–	–	–	REL	27	rr	3
BGE *opr*	Branch if Greater Than or Equal To (Signed Operands)	PC ← (PC) + 2 + *rel* ? (N ⊕ V) = 0	–	–	–	–	–	–	REL	90	rr	3
BGT *opr*	Branch if Greater Than (Signed Operands)	PC ← (PC) + 2 + *rel* ? (Z) ǀ (N ⊕ V) = 0	–	–	–	–	–	–	REL	92	rr	3
BHCC *rel*	Branch if Half Carry Bit Clear	PC ← (PC) + 2 + *rel* ? (H) = 0	–	–	–	–	–	–	REL	28	rr	3
BHCS *rel*	Branch if Half Carry Bit Set	PC ← (PC) + 2 + *rel* ? (H) = 1	–	–	–	–	–	–	REL	29	rr	3
BHI *rel*	Branch if Higher	PC ← (PC) + 2 + *rel* ? (C) ǀ (Z) = 0	–	–	–	–	–	–	REL	22	rr	3



1. Ports are software configurable with pullup device if input port.
2. Higher current drive port pins
3. Pin contains integrated pullup device

Figure 7-1. Block Diagram Highlighting ICG Module and Pins

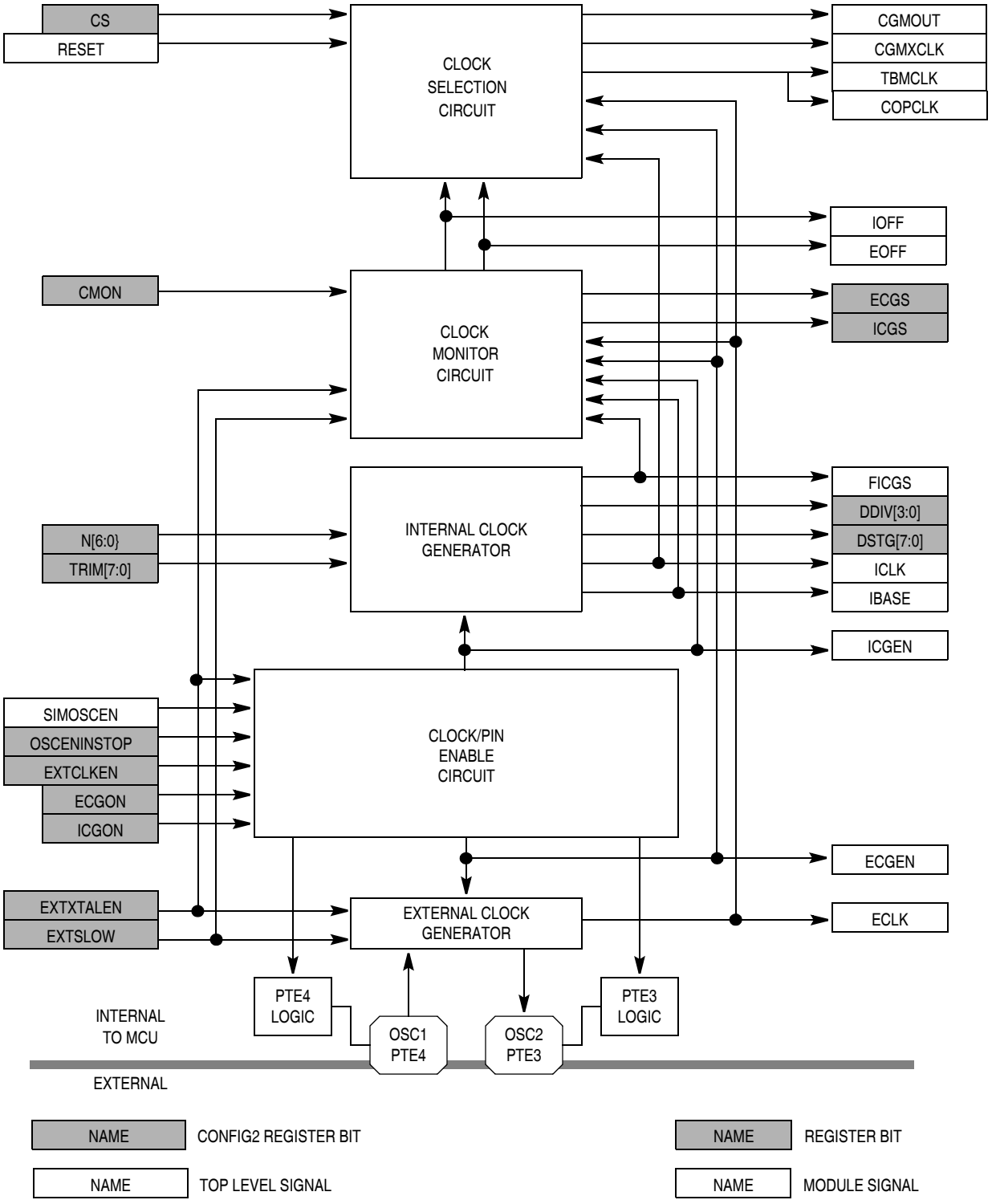


Figure 7-2. ICG Module Block Diagram

clock period tolerance plus 10 percent) must be added. This adjustment can be reduced with trimming. Table 7-3 shows some typical values for settling time.

Table 7-3. Typical Settling Time Examples

τ_1	τ_2	N	τ_{15}	τ_5	τ_{tot}
1/ (6.45 MHz)	1/ (25.8 MHz)	84	430 µs	535 µs	850 µs
1/ (25.8 MHz)	1/ (6.45 MHz)	21	107 µs	212 µs	525 µs
1/ (25.8 MHz)	1/ (307.2 kHz)	1	141 µs	246 µs	560 µs
1/ (307.2 kHz)	1/ (25.8 MHz)	84	11.9 ms	12.0 ms	12.3 ms

7.4.7 Trimming Frequency on the Internal Clock Generator

The unadjusted frequency of the low-frequency base clock (IBASE), when the comparators in the frequency comparator indicate zero error, will vary as much as ±25 percent due to process, temperature, and voltage dependencies. These dependencies are in the voltage and current references, the offset of the comparators, and the internal capacitor.

The method of changing the unadjusted operating point is by changing the size of the capacitor. This capacitor is designed with 639 equally sized units. Of that number, 384 of these units are always connected. The remaining 255 units are put in by adjusting the ICG trim factor (TRIM). The default value for TRIM is $80, or 128 units, making the default capacitor size 512. Each unit added or removed will adjust the output frequency by about ±0.195 percent of the unadjusted frequency (adding to TRIM will decrease frequency). Therefore, the frequency of IBASE can be changed to ±25 percent of its unadjusted value, which is enough to cancel the process variability mentioned before.

The best way to trim the internal clock is to use the timer to measure the width of an input pulse on an input capture pin (this pulse must be supplied by the application and should be as long or wide as possible). Considering the prescale value of the timer and the theoretical (zero error) frequency of the bus (307.2 kHz *N/4), the error can be calculated. This error, expressed as a percentage, can be divided by 0.195 percent and the resultant factor added or subtracted from TRIM. This process should be repeated to eliminate any residual error.

7.5 Low-Power Modes

The WAIT and STOP instructions put the MCU in low power- consumption standby modes.

7.5.1 Wait Mode

The ICG remains active in wait mode. If enabled, the ICG interrupt to the CPU can bring the MCU out of wait mode.

In some applications, low power-consumption is desired in wait mode and a high-frequency clock is not needed. In these applications, reduce power consumption by either selecting a low-frequency external clock and turn the internal clock generator off or reduce the bus frequency by minimizing the ICG multiplier factor (N) before executing the WAIT instruction.

7.6.3 Slow External Clock (EXTSLOW)

Slow external clock (EXTSLOW), when set, will decrease the drive strength of the oscillator amplifier, enabling low-frequency crystal operation (30 kHz–100 kHz) if properly enabled with the external clock enable (EXTCLKEN) and external crystal enable (EXTXTALEN) bits. When clear, EXTSLOW enables high-frequency crystal operation (1 MHz to 8 MHz).

EXTSLOW, when set, also configures the clock monitor to expect an external clock source that is slower than the low-frequency base clock (60 Hz to 307.2 kHz). When EXTSLOW is clear, the clock monitor will expect an external clock faster than the low-frequency base clock (307.2 kHz to 32 MHz).

The default state for this option is clear.

7.6.4 Oscillator Enable In Stop (OSCENINSTOP)

Oscillator enable in stop (OSCENINSTOP), when set, will enable the ICG to continue to generate clocks (either CGMXCLK, CGMOUT, COPCLK, or TBMCLK) in stop mode. This function is used to keep the timebase and COP running while the rest of the microcontroller stops. The clock monitor and autoswitching functions remain operative.

When OSCENINSTOP is clear, all clock generation will cease and CGMXCLK, CGMOUT, COPCLK, and TBMCLK will be forced low during stop mode. The clock monitor and autoswitching functions become inoperative.

The default state for this option is clear.

7.7 Input/Output (I/O) Registers

The ICG contains five registers, summarized in Figure 7-11. These registers are:

1. ICG control register (ICGCR)
2. ICG multiplier register (ICGMR)
3. ICG trim register (ICGTR)
4. ICG DCO divider control register (ICGDVR)
5. ICG DCO stage control register (ICGDSR)

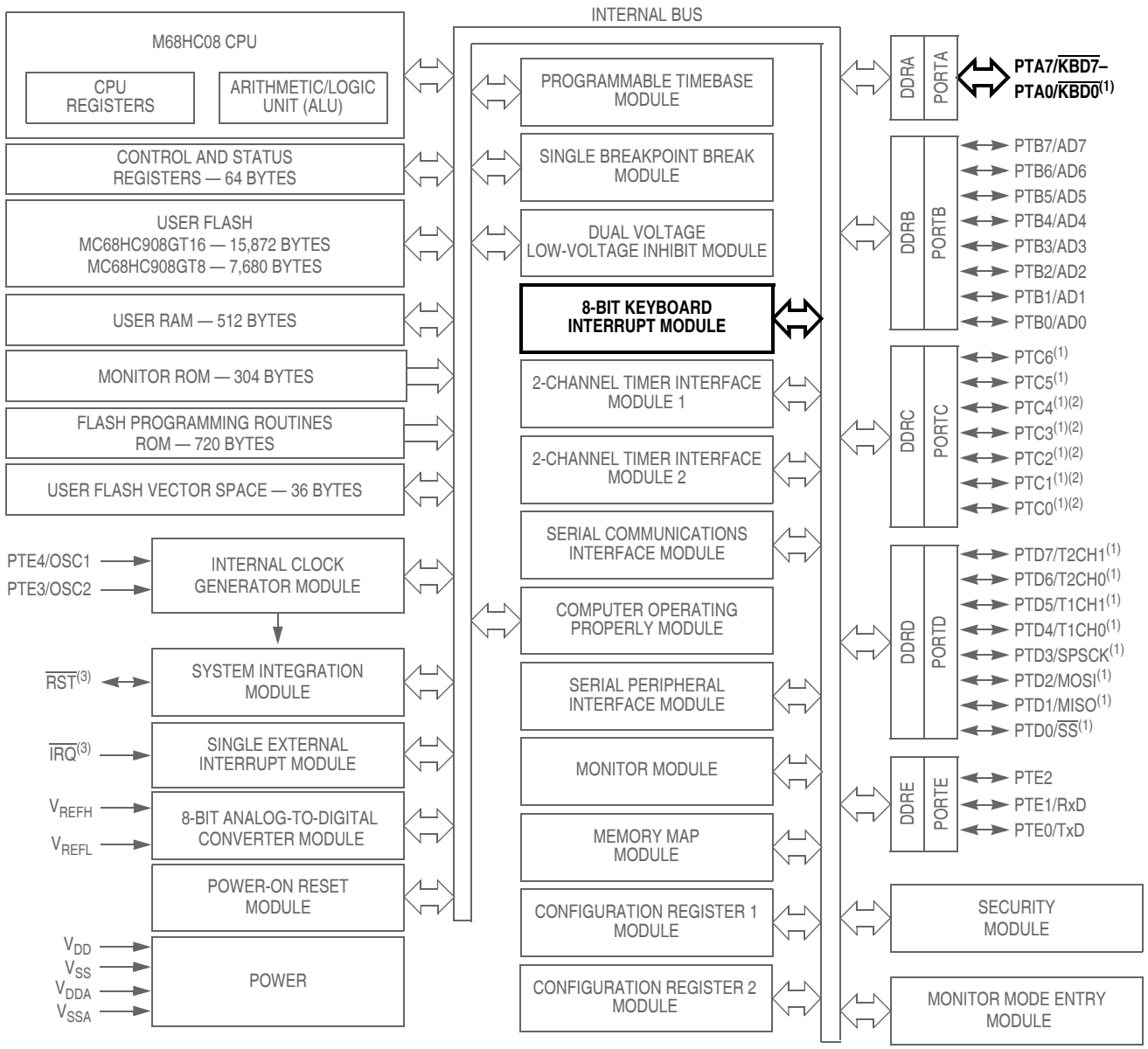
Several of the bits in these registers have interaction where the state of one bit may force another bit to a particular state or prevent another bit from being set or cleared. A summary of this interaction is shown in Table 7-4.

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$0036	ICG Control Register (ICGCR) See page 98.	Read:	CMIE	CMF	CMON	CS	ICGON	ICGS	ECGON	ECGS
		Write:		0(1)						
		Reset:	0	0	0	0	1	0	0	0
$0037	ICG Multiply Register (ICGMR) See page 99.	Read:		N6	N5	N4	N3	N2	N1	N0
		Write:								
		Reset:	0	0	0	1	0	1	0	1

1. See 7.7.1 ICG Control Register for method of clearing the CMF bit.

= Unimplemented R = Reserved U = Unaffected

Figure 7-11. ICG Module I/O Register Summary



1. Ports are software configurable with pullup device if input port.
2. Higher current drive port pins
3. Pin contains integrated pullup device

Figure 9-1. Block Diagram Highlighting KBI Block and Pins

11.3.2 Stop Mode

The break module is inactive in stop mode. A break interrupt causes exit from stop mode and sets the SBSW bit in the break status register. The STOP instruction does not affect break module register states.

11.4 Central Processor Unit (CPU)

11.4.1 Wait Mode

The WAIT instruction:

- Clears the interrupt mask (I bit) in the condition code register, enabling interrupts. After exit from wait mode by interrupt, the I bit remains clear. After exit by reset, the I bit is set.
- Disables the CPU clock

11.4.2 Stop Mode

The STOP instruction:

- Clears the interrupt mask (I bit) in the condition code register, enabling external interrupts. After exit from stop mode by external interrupt, the I bit remains clear. After exit by reset, the I bit is set.
- Disables the CPU clock

After exiting stop mode, the CPU clock begins running after the oscillator stabilization delay.

11.5 Internal Clock Generator Module (ICG)

11.5.1 Wait Mode

The internal clock generator (ICG) module remains active in wait mode. If enabled, the ICG interrupt to the CPU can bring the MCU out of wait mode.

In some applications, low power-consumption is desired in wait mode and a high-frequency clock is not needed. In these applications, reduce power consumption by either selecting a low-frequency external clock and turn the internal clock generator off or reduce the bus frequency by minimizing the ICG multiplier factor (N) before executing the WAIT instruction.

11.5.2 Stop Mode

The value of the oscillator enable in stop (OSCENINSTOP) bit in the CONFIG2 register determines the behavior of the ICG in stop mode. If OSCENINSTOP is low, the ICG is disabled in stop and, upon execution of the STOP instruction, all ICG activity will cease and the output clocks (CGMXCLK, CGMOUT, COPCLK, and TBMCLK) will be held low. Power consumption will be minimal.

If OSCENINSTOP is high, the ICG is enabled in stop and activity will continue. This is useful if the timebase module (TBM) is required to bring the MCU out of stop mode. ICG interrupts will not bring the MCU out of stop mode in this case.

During stop mode, if OSCENINSTOP is low, several functions in the ICG are affected. The stable bits (ECGS and ICGS) are cleared, which will enable the external clock stabilization divider upon recovery. The clock monitor is disabled (CMON = 0) which will also clear the clock monitor interrupt enable (CMIE) and clock monitor flag (CMF) bits. The CS, ICGON, ECGON, N, TRIM, DDIV, and DSTG bits are unaffected.

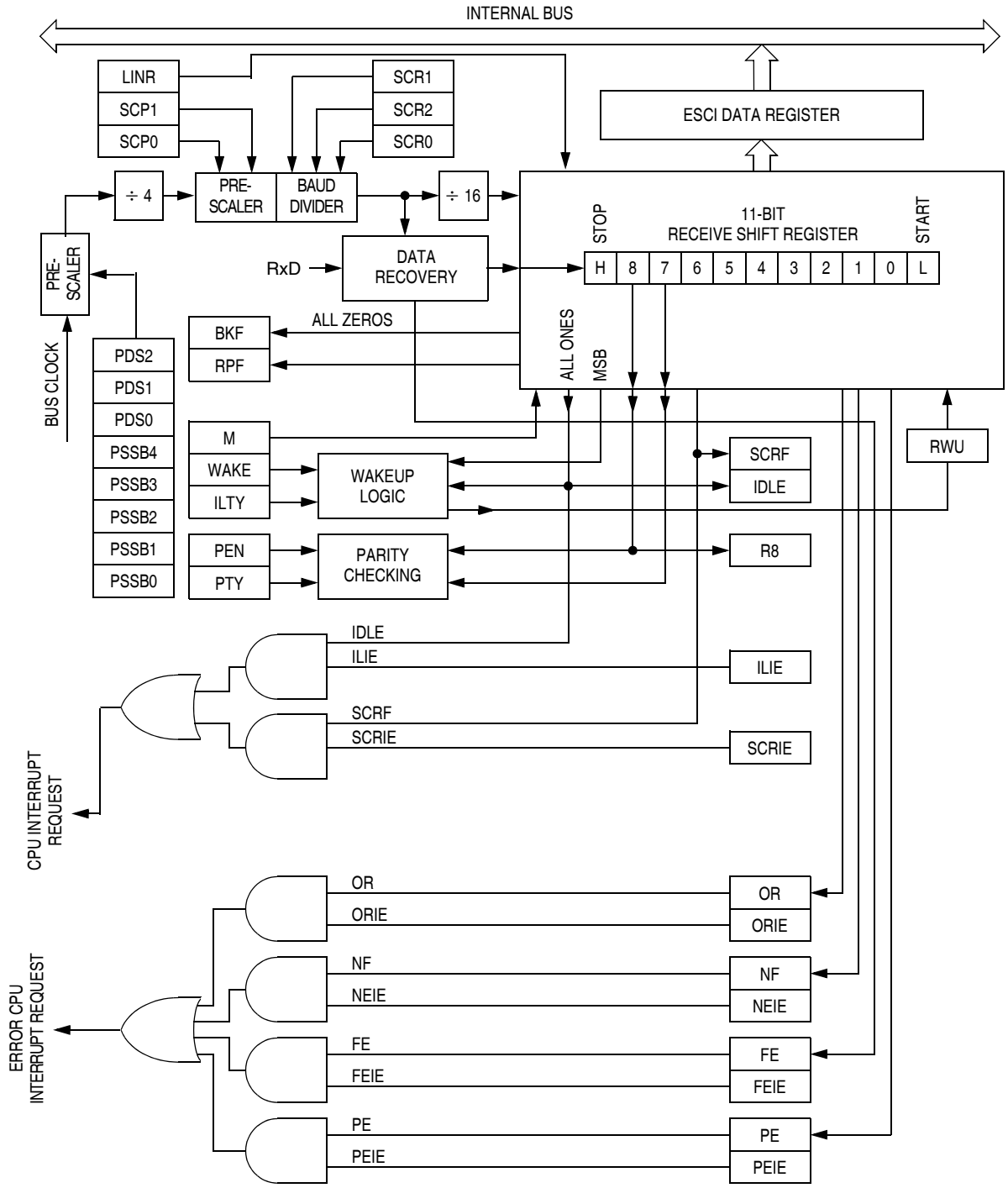


Figure 14-6. ESCI Receiver Block Diagram

Table 14-3. Data Bit Recovery

RT8, RT9, and RT10 Samples	Data Bit Determination	Noise Flag
000	0	0
001	0	1
010	0	1
011	1	1
100	0	1
101	1	1
110	1	1
111	1	0

NOTE

The RT8, RT9, and RT10 samples do not affect start bit verification. If any or all of the RT8, RT9, and RT10 start bit samples are 1s following a successful start bit verification, the noise flag (NF) is set and the receiver assumes that the bit is a start bit.

To verify a stop bit and to detect noise, recovery logic takes samples at RT8, RT9, and RT10. Table 14-4 summarizes the results of the stop bit samples.

Table 14-4. Stop Bit Recovery

RT8, RT9, and RT10 Samples	Framing Error Flag	Noise Flag
000	1	0
001	1	1
010	1	1
011	0	1
100	1	1
101	0	1
110	0	1
111	0	0

14.4.3.4 Framing Errors

If the data recovery logic does not detect a 1 where the stop bit should be in an incoming character, it sets the framing error bit, FE, in SCS1. A break character also sets the FE bit because a break character has no stop bit. The FE bit is set at the same time that the SCRF bit is set.

14.4.3.5 Baud Rate Tolerance

A transmitting device may be operating at a baud rate below or above the receiver baud rate. Accumulated bit time misalignment can cause one of the three stop bit data samples to fall outside the actual stop bit. Then a noise error occurs. If more than one of the samples is outside the stop bit, a framing error occurs. In most applications, the baud rate tolerance is much more than the degree of misalignment that is likely to occur.

As the receiver samples an incoming character, it resynchronizes the RT clock on any valid falling edge within the character. Resynchronization within characters corrects misalignments between transmitter bit times and receiver bit times.

14.9 ESCI Arbiter

The ESCI module comprises an arbiter module designed to support software for communication tasks as bus arbitration, baud rate recovery and break time detection. The arbiter module consists of an 9-bit counter with 1-bit overflow and control logic. The CPU can control operation mode via the ESCI arbiter control register (SCIACTL).

14.9.1 ESCI Arbiter Control Register

Address: $000A

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	AM1	ALOST	AM0	ACLK	AFIN	ARUN	AROVFL	ARD8
Write:								
Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 14-19. ESCI Arbiter Control Register (SCIACTL)

AM1 and AM0 — Arbiter Mode Select Bits

These read/write bits select the mode of the arbiter module as shown in Table 14-12. Reset clears AM1 and AM0.

Table 14-12. ESCI Arbiter Selectable Modes

AM[1:0]	ESCI Arbiter Mode
0 0	Idle / counter reset
0 1	Bit time measurement
1 0	Bus arbitration
1 1	Reserved / do not use

ALOST — Arbitration Lost Flag

This read-only bit indicates loss of arbitration. Clear ALOST by writing a 0 to AM1. Reset clears ALOST.

ACLK — Arbiter Counter Clock Select Bit

This read/write bit selects the arbiter counter clock source. Reset clears ACLK.

1 = Arbiter counter is clocked with one half of the ESCI input clock generated by the ESCI prescaler
0 = Arbiter counter is clocked with one quarter of the bus clock

AFIN— Arbiter Bit Time Measurement Finish Flag

This read-only bit indicates bit time measurement has finished. Clear AFIN by writing any value to SCIACTL. Reset clears AFIN.

1 = Bit time measurement has finished
0 = Bit time measurement not yet finished

ARUN— Arbiter Counter Running Flag

This read-only bit indicates the arbiter counter is running. Reset clears ARUN.

1 = Arbiter counter running
0 = Arbiter counter stopped

15.2.2 Clock Startup from POR or LVI Reset

When the power-on reset module or the low-voltage inhibit module generates a reset, the clocks to the CPU and peripherals are inactive and held in an inactive phase until after the 4096 CGMXCLK cycle POR timeout has completed. The $\overline{\text{RST}}$ pin is driven low by the SIM during this entire period. The IBUS clocks start upon completion of the timeout.

15.2.3 Clocks in Stop Mode and Wait Mode

Upon exit from stop mode by an interrupt, break, or reset, the SIM allows CGMXCLK to clock the SIM counter. The CPU and peripheral clocks do not become active until after the stop delay timeout. This timeout is selectable as 4096 or 32 CGMXCLK cycles. See 15.6.2 Stop Mode.

In wait mode, the CPU clocks are inactive. The SIM also produces two sets of clocks for other modules. Refer to the wait mode subsection of each module to see if the module is active or inactive in wait mode. Some modules can be programmed to be active in wait mode.

15.3 Reset and System Initialization

The MCU has these reset sources:

- Power-on reset module (POR)
- External reset pin ($\overline{\text{RST}}$)
- Computer operating properly module (COP)
- Low-voltage inhibit module (LVI)
- Illegal opcode
- Illegal address
- Forced monitor mode entry reset (MODRST)

All of these resets produce the vector $FFFE:$FFFF ($FEFE:$FEFF in monitor mode) and assert the internal reset signal (IRST). IRST causes all registers to be returned to their default values and all modules to be returned to their reset states.

An internal reset clears the SIM counter (see 15.4 SIM Counter), but an external reset does not. Each of the resets sets a corresponding bit in the SIM reset status register (SRSR). See 15.7 SIM Registers.

15.3.1 External Pin Reset

The $\overline{\text{RST}}$ pin circuit includes an internal pullup device. Pulling the asynchronous $\overline{\text{RST}}$ pin low halts all processing. The PIN bit of the SIM reset status register (SRSR) is set as long as $\overline{\text{RST}}$ is held low for a minimum of 67 CGMXCLK cycles, assuming that neither the POR nor the LVI was the source of the reset. See Table 15-2 for details. Figure 15-4 shows the relative timing.

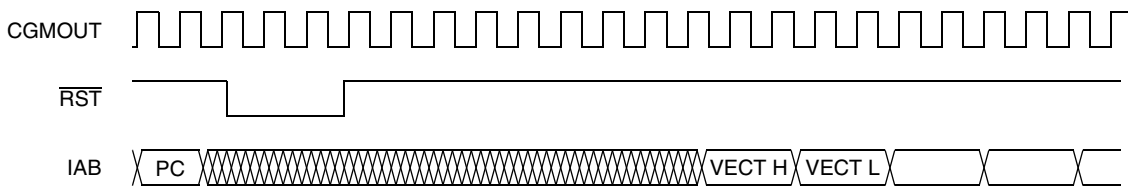


Figure 15-4. External Reset Timing

Chapter 16
Serial Peripheral Interface (SPI) Module

16.1 Introduction

This section describes the serial peripheral interface (SPI) module, which allows full-duplex, synchronous, serial communications with peripheral devices.

The text that follows describes the SPI. The SPI I/O pin names are $\overline{SS}$ (slave select), SPSCK (SPI serial clock), MOSI (master out slave in), and MISO (master in/slave out). The SPI shares four I/O pins with four parallel I/O ports.

16.2 Features

Features of the SPI module include:

- Full-duplex operation
- Master and slave modes
- Double-buffered operation with separate transmit and receive registers
- Four master mode frequencies (maximum = bus frequency ÷ 2)
- Maximum slave mode frequency = bus frequency
- Serial clock with programmable polarity and phase
- Two separately enabled interrupts:
  - SPRF (SPI receiver full)
  - SPTE (SPI transmitter empty)
- Mode fault error flag with CPU interrupt capability
- Overflow error flag with CPU interrupt capability
- Programmable wired-OR mode
- I/O (input/output) port bit(s) software configurable with pullup device(s) if configured as input port bit(s)

16.3 Functional Description

The SPI module allows full-duplex, synchronous, serial communication between the MCU and peripheral devices, including other MCUs. Software can poll the SPI status flags or SPI operation can be interrupt driven.

If a port bit is configured for input, then an internal pullup device may be enabled for that port bit.

The following paragraphs describe the operation of the SPI module. Refer to Figure 16-2 for a summary of the SPI I/O registers.

Upon power-on reset, if the received bytes of the security code do not match the data at locations $FFF6–$FFFD, the host fails to bypass the security feature. The MCU remains in monitor mode, but reading a Flash location returns an invalid value and trying to execute code from Flash causes an illegal address reset. After receiving the eight security bytes from the host, the MCU transmits a break character, signifying that it is ready to receive a command.

NOTE

The MCU does not transmit a break character until after the host sends the eight security bytes.

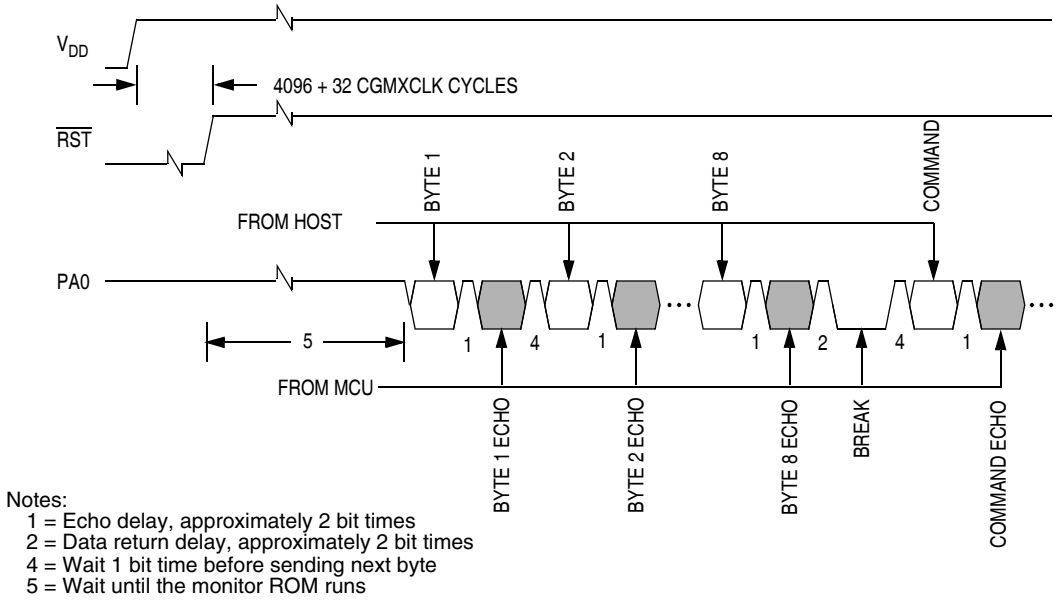


Figure 19-18. Monitor Mode Entry Timing

To determine whether the security code entered is correct, check to see if bit 6 of RAM address $40 is set. If it is, then the correct security code has been entered and Flash can be accessed.

If the security sequence fails, the device should be reset by a power-on reset and brought up in monitor mode to attempt another entry. After failing the security sequence, the Flash module can also be mass erased by executing an erase routine that was downloaded into internal RAM. The mass erase operation clears the security code locations so that all eight security bytes become $FF (blank).

A.8.1 5.0-V DC Electrical Characteristics

Characteristic[1]	Symbol	Min	Typ[2]	Max	Unit
Output high voltage (I_{Load} = –2.0 mA) all I/O pins (I_{Load} = –10.0 mA) all I/O pins (I_{Load} = –20.0 mA) pins PTC0–PTC4 only Maximum combined I_{OH} for port C, port E, port PTD0–PTD3 Maximum combined I_{OH} for port PTD4–PTD7, port A, port B Maximum total I_{OH} for all port pins	 V_{OH} V_{OH} V_{OH} I_{OH1} I_{OH2} I_{OHT}	 V_{DD} – 0.8 V_{DD} – 1.5 V_{DD} – 1.5 — — —	 — — — — — —	 — — — 50 50 100	 V V V mA mA mA
Output low voltage (I_{Load} = 1.6 mA) all I/O pins (I_{Load} = 10 mA) all I/O pins (I_{Load} = 20mA) pins PTC0–PTC4 only Maximum combined I_{OL} for port C, port E, port PTD0–PTD3 Maximum combined I_{OL} for port PTD4–PTD7, port A, port B Maximum total I_{OL} for all port pins	 V_{OL} V_{OL} V_{OL} I_{OL1} I_{OL2} I_{OLT}	 — — — — — —	 — — — — — —	 0.4 1.5 1.5 50 50 100	 V V V mA mA mA
Input high voltage All ports, $\overline{IRQ}$, $\overline{RST}$, OSC1	V_{IH}	0.7 × V_{DD}	—	V_{DD}	V
Input low voltage All ports, $\overline{IRQ}$, $\overline{RST}$, OSC1	V_{IL}	V_{SS}	—	0.2 × V_{DD}	V
DC injection current, all ports[3]	I_{INJ}	– 2.0	—	+ 2.0	mA
Total DC current injection (sum of all I/O)[3]	I_{INJTOT}	– 25	—	+25	mA
I/O ports Hi-Z leakage current[4]	I_{IL}	—	—	±10	µA
Input current	I_{In}	—	—	±1	µA
Pullup resistors (as input only) Ports PTA7/$\overline{KBD7}$–PTA0/$\overline{KBD0}$, PTC6–PTC0, PTD7/T2CH1–PTD0/$\overline{SS}$	R_{PU}	20	30	65	kΩ
Capacitance Ports (as input or output)	C_{Out} C_{In}	— —	— —	12 8	pF
Monitor mode entry voltage	V_{TST}	V_{DD} + 2.5	—	V_{DD} + 4.0	V
Low-voltage inhibit, trip falling voltage	V_{TRIPF}	3.90	4.25	4.50	V
Low-voltage inhibit, trip rising voltage	V_{TRIPR}	4.00	4.35	4.60	V
Low-voltage inhibit reset/recover hysteresis (V_{TRIPF} + V_{HYS} = V_{TRIPR})	V_{HYS}	—	100	—	mV
POR rearm voltage[5]	V_{POR}	0	—	100	mV
POR reset voltage[6]	V_{PORRST}	0	700	—	mV
POR rise time ramp rate[7]	R_{POR}	0.035	—	—	V/ms

1. V_{DD} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, T_A = T_A (min) to T_A (max), unless otherwise noted
2. Typical values reflect average measurements at midpoint of voltage range, 25°C only.
3. Some disturbance of the ADC accuracy is possible during any injection event and is dependent on board layout and power supply decoupling. This parameter is guaranteed by characterization.
4. Pullups and pulldowns are disabled. Port B leakage is specified in 20.16 ADC Characteristics.
5. Maximum is highest voltage that POR is guaranteed.
6. Maximum is highest voltage that POR is possible.
7. If minimum V_{DD} is not reached before the internal POR reset is released, $\overline{RST}$ must be driven low externally until minimum V_{DD} is reached.

A.9 ADC Characteristics

Characteristic[1]	Symbol	Min	Max	Unit	Comments
Supply voltage	V_{DDA}	2.7 (V_{DD} min)	5.5 (V_{DD} max)	V	V_{DDA} should be tied to the same potential as V_{DD} via separate traces.
Input voltages	V_{ADIN}	0	V_{DDA}	V	
Resolution	B_{AD}	8	8	Bits	
Absolute accuracy ($V_{REFL} = V_{SSA}$, $V_{REFH} = V_{DDA}$)	A_{AD}	—	± 1.5	LSB	Includes quantization
ADC internal clock	f_{ADIC}	0.5	1.048	MHz	$t_{AIC} = 1/f_{ADIC}$, tested only at 1 MHz
Conversion range	R_{AD}	V_{REFL}	V_{REFH}	V	$V_{SSA} \le V_{ADIN} \le V_{DDA}$
Power-up time	t_{ADPU}	16		t_{AIC} cycles	
ADC voltage reference high	V_{REFH}	$V_{SSA} - 0.1$	$V_{DDA} + 0.1$	V	$V_{REFL} \le V_{REFH}$
ADC voltage reference low	V_{REFL}	$V_{SSA} - 0.1$	$V_{DDA} + 0.1$	V	$V_{REFL} \le V_{REFH}$
Conversion time	t_{ADC}	16	17	t_{AIC} cycles	
Sample time[2]	t_{ADS}	5	—	t_{AIC} cycles	
Zero input reading[3]	Z_{ADI}	00	01	Hex	$V_{IN} = V_{REFL}$
Full-scale reading[3]	F_{ADI}	FE	FF	Hex	$V_{IN} = V_{REFH}$
Input capacitance	C_{ADI}	—	8	pF	Not tested
Input leakage[4] Port B	—	—	± 1	μA	

1. V_{DD} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, V_{DDA} = 5.0 Vdc ± 10%, V_{SSA} = 0 Vdc, V_{REFH} = 5.0 Vdc ± 10%, V_{REFL} = 0
2. Source impedances greater than 10 kΩ adversely affect internal RC charging time during input sampling.
3. Zero-input/full-scale reading requires sufficient decoupling measures for accurate conversions.
4. The external system error caused by input leakage current is approximately equal to the product of R source and input current.