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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	ARM7®
Core Size	16/32-Bit
Speed	72MHz
Connectivity	CANbus, I²C, Microwire, SPI, SSI, SSP, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	70
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	34K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 6x10b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc2361fbd100-551

- Serial interfaces:
  - Ethernet MAC with associated DMA controller (LPC2362 only). These functions reside on an independent AHB.
  - USB 2.0 device/host/OTG with on-chip PHY and associated DMA controller.
  - Four UARTs with fractional baud rate generation, one with modem control I/O, one with IrDA support, all with FIFO.
  - CAN controller with two channels.
  - SPI controller.
  - Two SSP controllers, with FIFO and multi-protocol capabilities. One is an alternate for the SPI port, sharing its interrupt and pins. These can be used with the GPDMA controller.
  - Three I^2C-bus interfaces (one with open-drain and two with standard port pins).
  - I^2S (Inter-IC Sound) interface for digital audio input or output. It can be used with the GPDMA.
- Other peripherals:
  - 70 general purpose I/O pins with configurable pull-up/down resistors.
  - 10-bit ADC with input multiplexing among 6 pins.
  - 10-bit DAC.
  - Four general purpose timers/counters with a total of 8 capture inputs and 10 compare outputs. Each timer block has an external count input.
  - One PWM/timer block with support for three-phase motor control. The PWM has two external count inputs.
  - Real-Time Clock (RTC) with separate power pin, clock source can be the RTC oscillator or the APB clock.
  - 2 kB SRAM powered from the RTC power pin, allowing data to be stored when the rest of the chip is powered off.
  - WatchDog Timer (WDT). The WDT can be clocked from the internal RC oscillator, the RTC oscillator, or the APB clock.
- Standard ARM test/debug interface for compatibility with existing tools.
- Emulation trace module supports real-time trace.
- Single 3.3 V power supply (3.0 V to 3.6 V).
- Four reduced power modes: idle, sleep, power-down, and deep power-down.
- Four external interrupt inputs configurable as edge/level sensitive. All pins on PORT0 and PORT2 can be used as edge sensitive interrupt sources.
- Processor wake-up from Power-down mode via any interrupt able to operate during Power-down mode (includes external interrupts, RTC interrupt, USB activity, Ethernet wake-up interrupt).
- Two independent power domains allow fine tuning of power consumption based on needed features.
- Each peripheral has its own clock divider for further power saving.
- Brownout detect with separate thresholds for interrupt and forced reset.
- On-chip power-on reset.
- On-chip crystal oscillator with an operating range of 1 MHz to 25 MHz.
- 4 MHz internal RC oscillator trimmed to 1 % accuracy that can optionally be used as the system clock. When used as the CPU clock, does not allow CAN and USB to run.

Table 3. Pin description *…continued*

Symbol	Pin	Type	Description
P0[5]/I2SRX_WS/ TD2/CAP2[1]	80[1]	I/O	**P0[5] —** General purpose digital input/output pin.
		I/O	**I2SRX_WS —** Receive Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I²S-bus specification*.
		O	**TD2 —** CAN2 transmitter output.
		I	**CAP2[1] —** Capture input for Timer 2, channel 1.
P0[6]/I2SRX_SDA/ SSEL1/MAT2[0]	79[1]	I/O	**P0[6] —** General purpose digital input/output pin.
		I/O	**I2SRX_SDA —** Receive data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I²S-bus specification*.
		I/O	**SSEL1 —** Slave Select for SSP1.
		O	**MAT2[0] —** Match output for Timer 2, channel 0.
P0[7]/I2STX_CLK/ SCK1/MAT2[1]	78[1]	I/O	**P0[7] —** General purpose digital input/output pin.
		I/O	**I2STX_CLK —** Transmit Clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the *I²S-bus specification*.
		I/O	**SCK1 —** Serial Clock for SSP1.
		O	**MAT2[1] —** Match output for Timer 2, channel 1.
P0[8]/I2STX_WS/ MISO1/MAT2[2]	77[1]	I/O	**P0[8] —** General purpose digital input/output pin.
		I/O	**I2STX_WS —** Transmit Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I²S-bus specification*.
		I/O	**MISO1 —** Master In Slave Out for SSP1.
		O	**MAT2[2] —** Match output for Timer 2, channel 2.
P0[9]/I2STX_SDA/ MOSI1/MAT2[3]	76[1]	I/O	**P0[9] —** General purpose digital input/output pin.
		I/O	**I2STX_SDA —** Transmit data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I²S-bus specification*.
		I/O	**MOSI1 —** Master Out Slave In for SSP1.
		O	**MAT2[3] —** Match output for Timer 2, channel 3.
P0[10]/TXD2/ SDA2/MAT3[0]	48[1]	I/O	**P0[10] —** General purpose digital input/output pin.
		O	**TXD2 —** Transmitter output for UART2.
		I/O	**SDA2 —** I²C2 data input/output (this is not an open-drain pin).
		O	**MAT3[0] —** Match output for Timer 3, channel 0.
P0[11]/RXD2/ SCL2/MAT3[1]	49[1]	I/O	**P0[11] —** General purpose digital input/output pin.
		I	**RXD2 —** Receiver input for UART2.
		I/O	**SCL2 —** I²C2 clock input/output (this is not an open-drain pin).
		O	**MAT3[1] —** Match output for Timer 3, channel 1.
P0[15]/TXD1/ SCK0/SCK	62[1]	I/O	**P0[15] —** General purpose digital input/output pin.
		O	**TXD1 —** Transmitter output for UART1.
		I/O	**SCK0 —** Serial clock for SSP0.
		I/O	**SCK —** Serial clock for SPI.
P0[16]/RXD1/ SSEL0/SSEL	63[1]	I/O	**P0[16] —** General purpose digital input/output pin.
		I	**RXD1 —** Receiver input for UART1.
		I/O	**SSEL0 —** Slave Select for SSP0.
		I/O	**SSEL —** Slave Select for SPI.

Table 3. Pin description *…continued*

Symbol	Pin	Type	Description
P1[20]/ USB_TX_DP1/ PWM1[2]/SCK0	34[1]	I/O	**P1[20] —** General purpose digital input/output pin.
		O	**USB_TX_DP1 —** D+ transmit data for USB port 1 (OTG transceiver).
		O	**PWM1[2] —** Pulse Width Modulator 1, channel 2 output.
		I/O	**SCK0 —** Serial clock for SSP0.
P1[21]/ USB_TX_DM1/ PWM1[3]/SSEL0	35[1]	I/O	**P1[21] —** General purpose digital input/output pin.
		O	**USB_TX_DM1 —** D− transmit data for USB port 1 (OTG transceiver).
		O	**PWM1[3] —** Pulse Width Modulator 1, channel 3 output.
		I/O	**SSEL0 —** Slave Select for SSP0.
P1[22]/ USB_RCV1/ USB_PWRD1/ MAT1[0]	36[1]	I/O	**P1[22] —** General purpose digital input/output pin.
		I	**USB_RCV1 —** Differential receive data for USB port 1 (OTG transceiver).
		I	**USB_PWRD1 —** Power Status for USB port 1 (host power switch).
		O	**MAT1[0] —** Match output for Timer 1, channel 0.
P1[23]/ USB_RX_DP1/ PWM1[4]/MISO0	37[1]	I/O	**P1[23] —** General purpose digital input/output pin.
		I	**USB_RX_DP1 —** D+ receive data for USB port 1 (OTG transceiver).
		O	**PWM1[4] —** Pulse Width Modulator 1, channel 4 output.
		I/O	**MISO0 —** Master In Slave Out for SSP0.
P1[24]/ USB_RX_DM1/ PWM1[5]/MOSI0	38[1]	I/O	**P1[24] —** General purpose digital input/output pin.
		I	**USB_RX_DM1 —** D− receive data for USB port 1 (OTG transceiver).
		O	**PWM1[5] —** Pulse Width Modulator 1, channel 5 output.
		I/O	**MOSI0 —** Master Out Slave in for SSP0.
P1[25]/ $\overline{\text{USB\_LS1}}$/ $\overline{\text{USB\_HSTEN1}}$/ MAT1[1]	39[1]	I/O	**P1[25] —** General purpose digital input/output pin.
		O	**$\overline{\text{USB\_LS1}}$ —** Low-speed status for USB port 1 (OTG transceiver).
		O	**$\overline{\text{USB\_HSTEN1}}$ —** Host Enabled status for USB port 1.
		O	**MAT1[1] —** Match output for Timer 1, channel 1.
P1[26]/ $\overline{\text{USB\_SSPND1}}$/ PWM1[6]/ CAP0[0]	40[1]	I/O	**P1[26] —** General purpose digital input/output pin.
		O	**$\overline{\text{USB\_SSPND1}}$ —** USB port 1 bus suspend status (OTG transceiver).
		O	**PWM1[6] —** Pulse Width Modulator 1, channel 6 output.
		I	**CAP0[0] —** Capture input for Timer 0, channel 0.
P1[27]/ $\overline{\text{USB\_INT1}}$/ USB_OVRCR1/ CAP0[1]	43[1]	I/O	**P1[27] —** General purpose digital input/output pin.
		I	**$\overline{\text{USB\_INT1}}$ —** USB port 1 OTG transceiver interrupt (OTG transceiver).
		I	**USB_OVRCR1 —** USB port 1 Over-Current status.
		I	**CAP0[1] —** Capture input for Timer 0, channel 1.
P1[28]/USB_SCL1/ PCAP1[0]/MAT0[0]	44[1]	I/O	**P1[28] —** General purpose digital input/output pin.
		I/O	**USB_SCL1 —** USB port 1 I^2C-bus serial clock (OTG transceiver).
		I	**PCAP1[0] —** Capture input for PWM1, channel 0.
		O	**MAT0[0] —** Match output for Timer 0, channel 0.
P1[29]/USB_SDA1/ PCAP1[1]/MAT0[1]	45[1]	I/O	**P1[29] —** General purpose digital input/output pin.
		I/O	**USB_SDA1 —** USB port 1 I^2C-bus serial data (OTG transceiver).
		I	**PCAP1[1] —** Capture input for PWM1, channel 1.
		O	**MAT0[1] —** Match output for Timer 0, channel 0.

Table 3. Pin description *…continued*

Symbol	Pin	Type	Description
P2[7]/RD2/RTS1/ TRACEPKT2	66[1]	I/O	**P2[7] —** General purpose digital input/output pin.
		I	**RD2 —** CAN2 receiver input.
		O	**RTS1 —** Request to Send output for UART1.
		O	**TRACEPKT2 —** Trace Packet, bit 2.
P2[8]/TD2/TXD2/ TRACEPKT3	65[1]	I/O	**P2[8] —** General purpose digital input/output pin.
		O	**TD2 —** CAN2 transmitter output.
		O	**TXD2 —** Transmitter output for UART2.
		O	**TRACEPKT3 —** Trace Packet, bit 3.
P2[9]/ USB_CONNECT/ RXD2/EXTIN0	64[1]	I/O	**P2[9] —** General purpose digital input/output pin.
		O	**USB_CONNECT —** Signal used to switch an external 1.5 kΩ resistor under software control. Used with the SoftConnect USB feature.
		I	**RXD2 —** Receiver input for UART2.
		I	**EXTIN0 —** External Trigger Input.
P2[10]/$\overline{\text{EINT0}}$	53[6]	I/O	**P2[10] —** General purpose digital input/output pin. **Note:** LOW on this pin while $\overline{\text{RESET}}$ is LOW forces on-chip bootloader to take over control of the part after a reset.
		I	**$\overline{\text{EINT0}}$ —** External interrupt 0 input.
P2[11]/$\overline{\text{EINT1}}$/ I2STX_CLK	52[6]	I/O	**P2[11] —** General purpose digital input/output pin.
		I	**$\overline{\text{EINT1}}$ —** External interrupt 1 input.
		I/O	**I2STX_CLK —** Transmit Clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the *I^2S-bus specification*.
P2[12]/$\overline{\text{EINT2}}$/ I2STX_WS	51[6]	I/O	**P2[12] —** General purpose digital input/output pin.
		I	**$\overline{\text{EINT2}}$ —** External interrupt 2 input.
		I/O	**I2STX_WS —** Transmit Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I^2S-bus specification*.
P2[13]/$\overline{\text{EINT3}}$/ I2STX_SDA	50[6]	I/O	**P2[13] —** General purpose digital input/output pin.
		I	**$\overline{\text{EINT3}}$ —** External interrupt 3 input.
		I/O	**I2STX_SDA —** Transmit data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I^2S-bus specification*.
P3[0] to P3[31]		I/O	**Port 3:** Port 3 is a 32-bit I/O port with individual direction controls for each bit. The operation of port 3 pins depends upon the pin function selected via the pin connect block. Pins 0 through 24, and 27 through 31 of this port are not available.
P3[25]/MAT0[0]/ PWM1[2]	27[1]	I/O	**P3[25] —** General purpose digital input/output pin.
		O	**MAT0[0] —** Match output for Timer 0, channel 0.
		O	**PWM1[2] —** Pulse Width Modulator 1, output 2.
P3[26]/MAT0[1]/ PWM1[3]	26[1]	I/O	**P3[26] —** General purpose digital input/output pin.
		O	**MAT0[1] —** Match output for Timer 0, channel 1.
		O	**PWM1[3] —** Pulse Width Modulator 1, output 3.
P4[0] to P4[31]		I/O	**Port 4:** Port 4 is a 32-bit I/O port with individual direction controls for each bit. The operation of port 4 pins depends upon the pin function selected via the pin connect block. Pins 0 through 27, 30, and 31 of this port are not available.

[3] 5 V tolerant pad providing digital I/O with TTL levels and hysteresis and analog output function. When configured as the DAC output, digital section of the pad is disabled.

[4] Open-drain 5 V tolerant digital I/O pad, compatible with I^2C-bus 400 kHz specification. This pad requires an external pull-up to provide output functionality. When power is switched off, this pin connected to the I^2C-bus is floating and does not disturb the I^2C lines. Open-drain configuration applies to all functions on this pin.

[5] Pad provides digital I/O and USB functions. It is designed in accordance with the *USB specification, revision 2.0* (Full-speed and Low-speed mode only).

[6] 5 V tolerant pad with 10 ns glitch filter providing digital I/O functions with TTL levels and hysteresis.

[7] This pin has no built-in pull-up and no built-in pull-down resistor.

[8] This pin has a built-in pull-up resistor.

[9] 5 V tolerant pad with 20 ns glitch filter providing digital I/O function with TTL levels and hysteresis.

[10] Pad provides special analog functionality.

[11] When the main oscillator is not used, connect XTAL1 and XTAL2 as follows: XTAL1 can be left floating or can be grounded (grounding is preferred to reduce susceptibility to noise). XTAL2 should be left floating.

[12] If the RTC is not used, these pins can be left floating.

[13] Pad provides special analog functionality.

[14] Pad provides special analog functionality.

[15] Pad provides special analog functionality.

[16] Pad provides special analog functionality.

[17] Pad provides special analog functionality.

7. Functional description

7.1 Architectural overview

The LPC2361/2362 microcontroller consists of an ARM7TDMI-S CPU with emulation support, the ARM7 local bus for closely coupled, high-speed access to the majority of on-chip memory, the AMBA AHB interfacing to high-speed on-chip peripherals, and the AMBA APB for connection to other on-chip peripheral functions. The microcontroller permanently configures the ARM7TDMI-S processor for little-endian byte order.

The LPC2362 implements two AHBs in order to allow the Ethernet block to operate without interference caused by other system activity. The primary AHB, referred to as AHB1, includes the VIC and GPDMA controller.

The second AHB, referred to as AHB2, includes only the Ethernet block and an associated 16 kB SRAM. In addition, a bus bridge is provided that allows the secondary AHB to be a bus master on AHB1, allowing expansion of Ethernet buffer space into off-chip memory or unused space in memory residing on AHB1.

In summary, bus masters with access to AHB1 are the ARM7 itself, the GPDMA function, and the Ethernet block (via the bus bridge from AHB2). Bus masters with access to AHB2 are the ARM7 and the Ethernet block.

AHB peripherals are allocated a 2 MB range of addresses at the very top of the 4 GB ARM memory space. Each AHB peripheral is allocated a 16 kB address space within the AHB address space. Lower speed peripheral functions are connected to the APB. The AHB to APB bridge interfaces the APB to the AHB. APB peripherals are also allocated a 2 MB range of addresses, beginning at the 3.5 GB address point. Each APB peripheral is allocated a 16 kB address space within the APB address space.

7.14 UARTs

The LPC2361/2362 each contain four UARTs. In addition to standard transmit and receive data lines, UART1 also provides a full modem control handshake interface.

The UARTs include a fractional baud rate generator. Standard baud rates such as 115200 Bd can be achieved with any crystal frequency above 2 MHz.

7.14.1 Features

- 16 B Receive and Transmit FIFOs.
- Register locations conform to 16C550 industry standard.
- Receiver FIFO trigger points at 1 B, 4 B, 8 B, and 14 B.
- Built-in fractional baud rate generator covering wide range of baud rates without a need for external crystals of particular values.
- Fractional divider for baud rate control, auto baud capabilities and FIFO control mechanism that enables software flow control implementation.
- UART1 equipped with standard modem interface signals. This module also provides full support for hardware flow control (auto-CTS/RTS).
- UART3 includes an IrDA mode to support infrared communication.

7.15 SPI serial I/O controller

The LPC2361/2362 each contain one SPI controller. SPI is a full duplex serial interface designed to handle multiple masters and slaves connected to a given bus. Only a single master and a single slave can communicate on the interface during a given data transfer. During a data transfer the master always sends 8 bits to 16 bits of data to the slave, and the slave always sends 8 bits to 16 bits of data to the master.

7.15.1 Features

- Compliant with SPI specification
- Synchronous, serial, full duplex communication
- Combined SPI master and slave
- Maximum data bit rate of one eighth of the input clock rate
- 8 bits to 16 bits per transfer

7.16 SSP serial I/O controller

The LPC2361/2362 each contain two SSP controllers. The SSP controller is capable of operation on a SPI, 4-wire SSI, or Microwire bus. It can interact with multiple masters and slaves on the bus. Only a single master and a single slave can communicate on the bus during a given data transfer. The SSP supports full duplex transfers, with frames of 4 bits to 16 bits of data flowing from the master to the slave and from the slave to the master. In practice, often only one of these data flows carries meaningful data.

7.16.1 Features

- Compatible with Motorola SPI, 4-wire Texas Instruments SSI, and National Semiconductor Microwire buses

- Match register updates are synchronized with pulse outputs to prevent generation of erroneous pulses. Software must ‘release’ new match values before they can become effective.
- May be used as a standard timer if the PWM mode is not enabled.
- A 32-bit Timer/Counter with a programmable 32-bit Prescaler.

7.21 Watchdog timer

The purpose of the watchdog is to reset the microcontroller within a reasonable amount of time if it enters an erroneous state. When enabled, the watchdog will generate a system reset if the user program fails to ‘feed’ (or reload) the watchdog within a predetermined amount of time.

7.21.1 Features

- Internally resets chip if not periodically reloaded.
- Debug mode.
- Enabled by software but requires a hardware reset or a watchdog reset/interrupt to be disabled.
- Incorrect/Incomplete feed sequence causes reset/interrupt if enabled.
- Flag to indicate watchdog reset.
- Programmable 32-bit timer with internal prescaler.
- Selectable time period from ($T_{cy(WDCLK)} \times 256 \times 4$) to ($T_{cy(WDCLK)} \times 2^{32} \times 4$) in multiples of $T_{cy(WDCLK)} \times 4$.
- The Watchdog Clock (WDCLK) source can be selected from the RTC clock, the Internal RC oscillator (IRC), or the APB peripheral clock. This gives a wide range of potential timing choices of watchdog operation under different power reduction conditions. It also provides the ability to run the WDT from an entirely internal source that is not dependent on an external crystal and its associated components and wiring, for increased reliability.

7.22 RTC and battery RAM

The RTC is a set of counters for measuring time when system power is on, and optionally when it is off. It uses little power in Power-down and Deep power-down modes. On the LPC2361/2362, the RTC can be clocked by a separate 32.768 kHz oscillator, or by a programmable prescale divider based on the APB clock. Also, the RTC is powered by its own power supply pin, VBAT, which can be connected to a battery or to the same 3.3 V supply used by the rest of the device.

The VBAT pin supplies power only to the RTC and the battery RAM. These two functions require a minimum of power to operate, which can be supplied by an external battery.

7.22.1 Features

- Measures the passage of time to maintain a calendar and clock.
- Ultra low power design to support battery powered systems.
- Provides Seconds, Minutes, Hours, Day of Month, Month, Year, Day of Week, and Day of Year.

- Dedicated 32 kHz oscillator or programmable prescaler from APB clock.
- Dedicated power supply pin can be connected to a battery or to the main 3.3 V.
- Periodic interrupts can be generated from increments of any field of the time registers, and selected fractional second values.
- 2 kB data SRAM powered by VBAT.
- RTC and battery RAM power supply is isolated from the rest of the chip.

7.23 Clocking and power control

7.23.1 Crystal oscillators

The LPC2361/2362 includes three independent oscillators. These are the Main Oscillator, the Internal RC oscillator, and the RTC oscillator. Each oscillator can be used for more than one purpose as required in a particular application. Any of the three clock sources can be chosen by software to drive the PLL and ultimately the CPU.

Following reset, the LPC2361/2362 will operate from the Internal RC oscillator until switched by software. This allows systems to operate without any external crystal and the bootloader code to operate at a known frequency.

7.23.1.1 Internal RC oscillator

The IRC may be used as the clock source for the WDT, and/or as the clock that drives the PLL and subsequently the CPU. The nominal IRC frequency is 4 MHz. The IRC is trimmed to 1 % accuracy.

Upon power-up or any chip reset, the LPC2361/2362 uses the IRC as the clock source. Software may later switch to one of the other available clock sources.

7.23.1.2 Main oscillator

The main oscillator can be used as the clock source for the CPU, with or without using the PLL. The main oscillator operates at frequencies of 1 MHz to 25 MHz. This frequency can be boosted to a higher frequency, up to the maximum CPU operating frequency, by the PLL. The clock selected as the PLL input is PLLCLKIN. The ARM processor clock frequency is referred to as CCLK elsewhere in this document. The frequencies of PLLCLKIN and CCLK are the same value unless the PLL is active and connected. The clock frequency for each peripheral can be selected individually and is referred to as PCLK. Refer to Section 7.23.2 for additional information.

7.23.1.3 RTC oscillator

The RTC oscillator can be used as the clock source for the RTC and/or the WDT. Also, the RTC oscillator can be used to drive the PLL and the CPU.

7.23.2 PLL

The PLL accepts an input clock frequency in the range of 32 kHz to 25 MHz. The input frequency is multiplied up to a high frequency, then divided down to provide the actual clock used by the CPU and the USB block.

The PLL input, in the range of 32 kHz to 25 MHz, may initially be divided down by a value ‘N’, which may be in the range of 1 to 256. This input division provides a wide range of output frequencies from the same input frequency.

Following the PLL input divider is the PLL multiplier. This can multiply the input divider output through the use of a Current Controlled Oscillator (CCO) by a value 'M', in the range of 1 through 32768. The resulting frequency must be in the range of 275 MHz to 550 MHz. The multiplier works by dividing the CCO output by the value of M, then using a phase-frequency detector to compare the divided CCO output to the multiplier input. The error value is used to adjust the CCO frequency.

The PLL is turned off and bypassed following a chip Reset and by entering Power-down mode. PLL is enabled by software only. The program must configure and activate the PLL, wait for the PLL to Lock, then connect to the PLL as a clock source.

7.23.3 Wake-up timer

The LPC2361/2362 begins operation at power-up and when awakened from Power-down and Deep power-down modes by using the 4 MHz IRC oscillator as the clock source. This allows chip operation to resume quickly. If the main oscillator or the PLL is needed by the application, software will need to enable these features and wait for them to stabilize before they are used as a clock source.

When the main oscillator is initially activated, the wake-up timer allows software to ensure that the main oscillator is fully functional before the processor uses it as a clock source and starts to execute instructions. This is important at power-on, all types of Reset, and whenever any of the aforementioned functions are turned off for any reason. Since the oscillator and other functions are turned off during Power-down and Deep power-down modes, any wake-up of the processor from Power-down modes makes use of the wake-up timer.

The wake-up timer monitors the crystal oscillator to check whether it is safe to begin code execution. When power is applied to the chip, or when some event caused the chip to exit Power-down mode, some time is required for the oscillator to produce a signal of sufficient amplitude to drive the clock logic. The amount of time depends on many factors, including the rate of $V_{DD(3V3)}$ ramp (in the case of power-on), the type of crystal and its electrical characteristics (if a quartz crystal is used), as well as any other external circuitry (e.g., capacitors), and the characteristics of the oscillator itself under the existing ambient conditions.

7.23.4 Power control

The LPC2361/2362 supports a variety of power control features. There are four special modes of processor power reduction: Idle mode, Sleep mode, Power-down mode, and Deep power-down mode. The CPU clock rate may also be controlled as needed by changing clock sources, reconfiguring PLL values, and/or altering the CPU clock divider value. This allows a trade-off of power versus processing speed based on application requirements. In addition, Peripheral Power Control allows shutting down the clocks to individual on-chip peripherals, allowing fine tuning of power consumption by eliminating all dynamic power use in any peripherals that are not required for the application. Each of the peripherals has its own clock divider which provides even better power control.

The LPC2361/2362 also implements a separate power domain in order to allow turning off power to the bulk of the device while maintaining operation of the RTC and a small SRAM, referred to as the battery RAM.

While in Deep power-down mode, external device power may be removed. In this case, the LPC2361/2362 will start up when external power is restored.

Essential data may be retained through Deep power-down mode (or through complete powering off of the chip) by storing data in the Battery RAM, as long as the external power to the VBAT pin is maintained.

7.23.4.5 Power domains

The LPC2361/2362 provides two independent power domains that allow the bulk of the device to have power removed while maintaining operation of the RTC and the battery RAM.

On the LPC2361/2362, I/O pads are powered by the 3.3 V ($V_{DD(3V3)}$) pins, while the $V_{DD(DCDC)(3V3)}$ pin powers the on-chip DC-to-DC converter which in turn provides power to the CPU and most of the peripherals.

Depending on the LPC2361/2362 application, a design can use two power options to manage power consumption.

The first option assumes that power consumption is not a concern and the design ties the $V_{DD(3V3)}$ and $V_{DD(DCDC)(3V3)}$ pins together. This approach requires only one 3.3 V power supply for both pads, the CPU, and peripherals. While this solution is simple, it does not support powering down the I/O pad ring “on the fly” while keeping the CPU and peripherals alive.

The second option uses two power supplies; a 3.3 V supply for the I/O pads ($V_{DD(3V3)}$) and a dedicated 3.3 V supply for the CPU ($V_{DD(DCDC)(3V3)}$). Having the on-chip DC-to-DC converter powered independently from the I/O pad ring enables shutting down of the I/O pad power supply “on the fly”, while the CPU and peripherals stay active.

The VBAT pin supplies power only to the RTC and the battery RAM. These two functions require a minimum of power to operate, which can be supplied by an external battery. When the CPU and the rest of chip functions are stopped and power removed, the RTC can supply an alarm output that may be used by external hardware to restore chip power and resume operation.

7.24 System control

7.24.1 Reset

Reset has four sources on the LPC2361/2362: the $\overline{\text{RESET}}$ pin, the watchdog reset, power-on reset, and the BrownOut Detection (BOD) circuit. The $\overline{\text{RESET}}$ pin is a Schmitt trigger input pin. Assertion of chip Reset by any source, once the operating voltage attains a usable level, starts the wake-up timer (see description in Section 7.23.3 “Wake-up timer”), causing reset to remain asserted until the external Reset is de-asserted, the oscillator is running, a fixed number of clocks have passed, and the flash controller has completed its initialization.

When the internal Reset is removed, the processor begins executing at address 0, which is initially the Reset vector mapped from the Boot Block. At that point, all of the processor and peripheral registers have been initialized to predetermined values.

outputs information about processor execution to a trace port. A software debugger allows configuration of the ETM using a JTAG interface and displays the trace information that has been captured.

The ETM is connected directly to the ARM core and not to the main AMBA system bus. It compresses the trace information and exports it through a narrow trace port. An external Trace Port Analyzer captures the trace information under software debugger control. The trace port can broadcast the Instruction trace information. Instruction trace (or PC trace) shows the flow of execution of the processor and provides a list of all the instructions that were executed. Instruction trace is significantly compressed by only broadcasting branch addresses as well as a set of status signals that indicate the pipeline status on a cycle by cycle basis. Trace information generation can be controlled by selecting the trigger resource. Trigger resources include address comparators, counters and sequencers. Since trace information is compressed the software debugger requires a static image of the code being executed. Self-modifying code can not be traced because of this restriction.

7.25.3 RealMonitor

RealMonitor is a configurable software module, developed by ARM Inc., which enables real-time debug. It is a lightweight debug monitor that runs in the background while users debug their foreground application. It communicates with the host using the DCC, which is present in the EmbeddedICE logic. The LPC2361/2362 contain a specific configuration of RealMonitor software programmed into the on-chip ROM memory.

Table 7. Static characteristics *…continued*

T_{amb} = −40 °C to +85 °C for commercial applications, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
I_{latch}	I/O latch-up current	$-(0.5V_{DD(3V3)}) < V_I < (1.5V_{DD(3V3)})$; $T_j < 125$ °C		-	-	100	mA
V_I	input voltage	pin configured to provide a digital function	[5][6] [7][8]	0	-	5.5	V
V_O	output voltage	output active		0	-	$V_{DD(3V3)}$	V
V_{IH}	HIGH-level input voltage			2.0	-	-	V
V_{IL}	LOW-level input voltage			-	-	0.8	V
V_{hys}	hysteresis voltage			0.4	-	-	V
V_{OH}	HIGH-level output voltage	I_{OH} = −4 mA	[9]	$V_{DD(3V3)} - 0.4$	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = −4 mA	[9]	-	-	0.4	V
I_{OH}	HIGH-level output current	$V_{OH} = V_{DD(3V3)} - 0.4$ V	[9]	−4	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V	[9]	4	-	-	mA
I_{OHS}	HIGH-level short-circuit output current	V_{OH} = 0 V	[10]	-	-	−45	mA
I_{OLS}	LOW-level short-circuit output current	$V_{OL} = V_{DDA}$	[10]	-	-	50	mA
I_{pd}	pull-down current	V_I = 5 V	[11]	10	50	150	μA
I_{pu}	pull-up current	V_I = 0 V		−15	−50	−85	μA
		$V_{DD(3V3)} < V_I < 5$ V	[11]	0	0	0	μA
I^2C-bus pins (P0[27] and P0[28])							
V_{IH}	HIGH-level input voltage			$0.7V_{DD(3V3)}$	-	-	V
V_{IL}	LOW-level input voltage			-	-	$0.3V_{DD(3V3)}$	V
V_{hys}	hysteresis voltage			-	$0.05V_{DD(3V3)}$	-	V
V_{OL}	LOW-level output voltage	I_{OLS} = 3 mA	[9]	-	-	0.4	V
I_{LI}	input leakage current	$V_I = V_{DD(3V3)}$	[12]	-	2	4	μA
		V_I = 5 V		-	10	22	μA
Oscillator pins							
$V_{i(XTAL1)}$	input voltage on pin XTAL1			−0.5	1.8	1.95	V
$V_{o(XTAL2)}$	output voltage on pin XTAL2			−0.5	1.8	1.95	V
$V_{i(RTCX1)}$	input voltage on pin RTCX1			−0.5	1.8	1.95	V
$V_{o(RTCX2)}$	output voltage on pin RTCX2			−0.5	1.8	1.95	V

Table 7. Static characteristics *…continued*

T_{amb} = −40 °C to +85 °C for commercial applications, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
USB pins							
I_{OZ}	OFF-state output current	0 V < V_I < 3.3 V		-	-	±10	μA
V_{BUS}	bus supply voltage			-	-	5.25	V
V_{DI}	differential input sensitivity voltage	|(D+) − (D−)|		0.2	-	-	V
V_{CM}	differential common mode voltage range	includes V_{DI} range		0.8	-	2.5	V
$V_{th(rs)se}$	single-ended receiver switching threshold voltage			0.8	-	2.0	V
V_{OL}	LOW-level output voltage for low-/full-speed	R_L of 1.5 kΩ to 3.6 V		-	-	0.18	V
V_{OH}	HIGH-level output voltage (driven) for low-/full-speed	R_L of 15 kΩ to GND		2.8	-	3.5	V
C_{trans}	transceiver capacitance	pin to GND		-	-	20	pF
Z_{DRV}	driver output impedance for driver which is not high-speed capable	with 33 Ω series resistor; steady state drive	[13]	36	-	44.1	Ω

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[2] The RTC typically fails when $V_{i(VBAT)}$ drops below 1.6 V.

[3] $V_{DD(DCDC)(3V3)}$ = 3.3 V; $V_{DD(3V3)}$ = 3.3 V; $V_{i(VBAT)}$ = 3.3 V; T_{amb} = 25 °C.

[4] On pin VBAT.

[5] Including voltage on outputs in 3-state mode.

[6] $V_{DD(3V3)}$ supply voltages must be present.

[7] 3-state outputs go into 3-state mode when $V_{DD(3V3)}$ is grounded.

[8] Please also see the errata note mentioned in errata sheet.

[9] Accounts for 100 mV voltage drop in all supply lines.

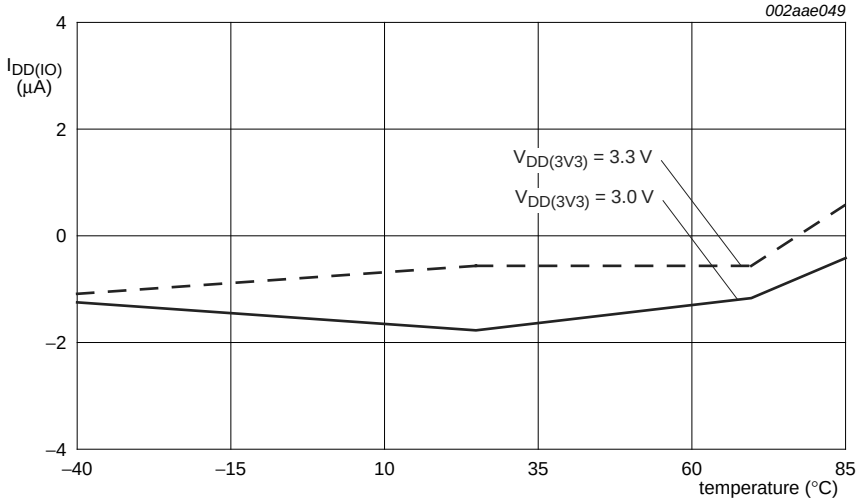
[10] Allowed as long as the current limit does not exceed the maximum current allowed by the device.

[11] Minimum condition for V_I = 4.5 V, maximum condition for V_I = 5.5 V.

[12] To V_{SS}.

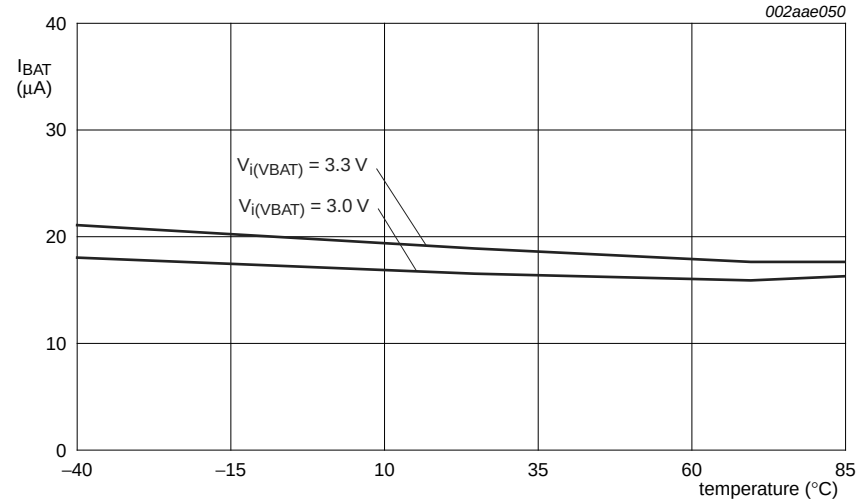
[13] Includes external resistors of 33 Ω ± 1 % on D+ and D−.

10.1 Power-down mode



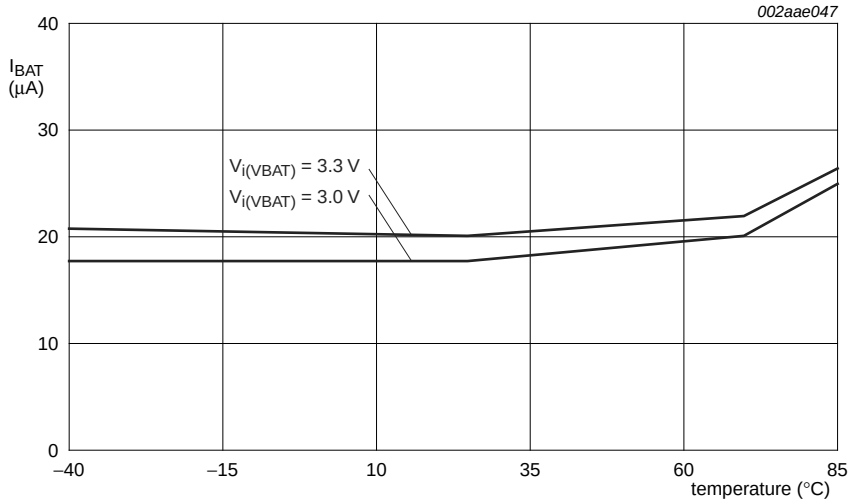
$V_{i(VBAT)} = V_{DD(DCDC)(3V3)} = 3.3$ V; $T_{amb} = 25$ °C.

Fig 4. I/O maximum supply current $I_{DD(IO)}$ versus temperature in Power-down mode



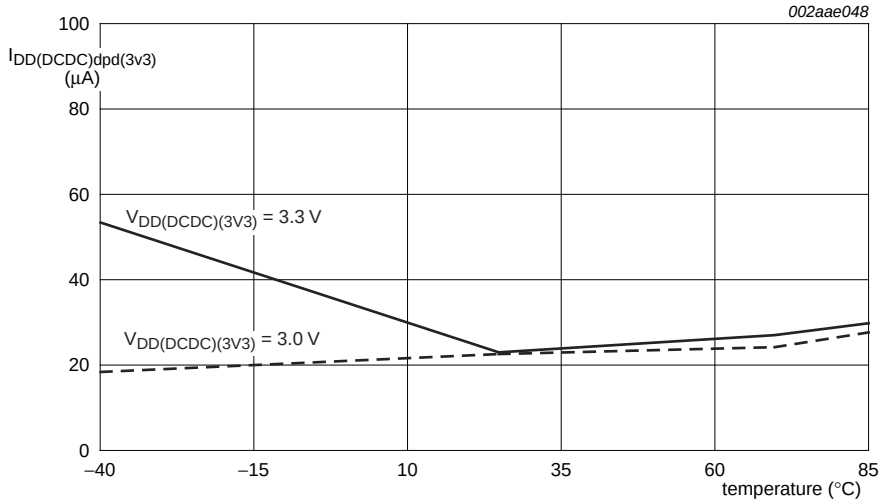
$V_{DD(3V3)} = V_{DD(DCDC)(3V3)} = 3.3$ V; $T_{amb} = 25$ °C.

Fig 5. RTC battery maximum supply current I_{BAT} versus temperature in Power-down mode



$V_{DD(3V3)} = V_{DD(DCDC)(3V3)} = 3.3$ V; $T_{amb} = 25$ °C

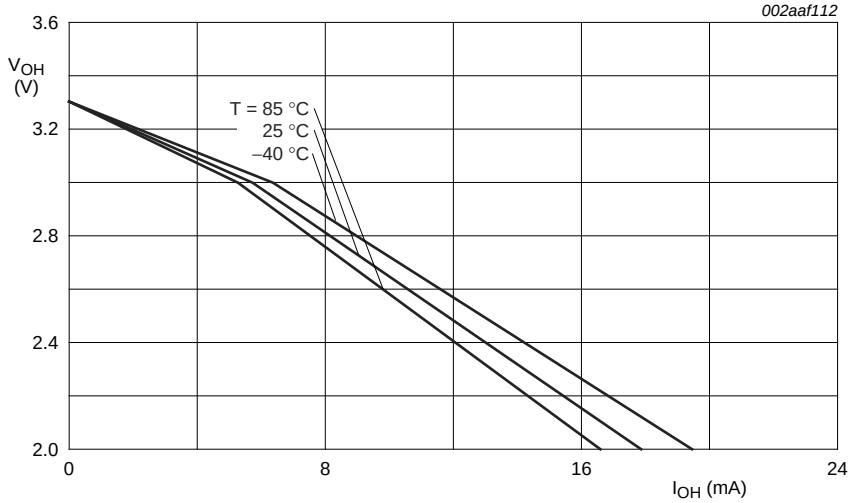
Fig 8. RTC battery maximum supply current I_{BAT} versus temperature in Deep power-down mode



$V_{DD(3V3)} = V_{i(VBAT)} = 3.3$ V; $T_{amb} = 25$ °C.

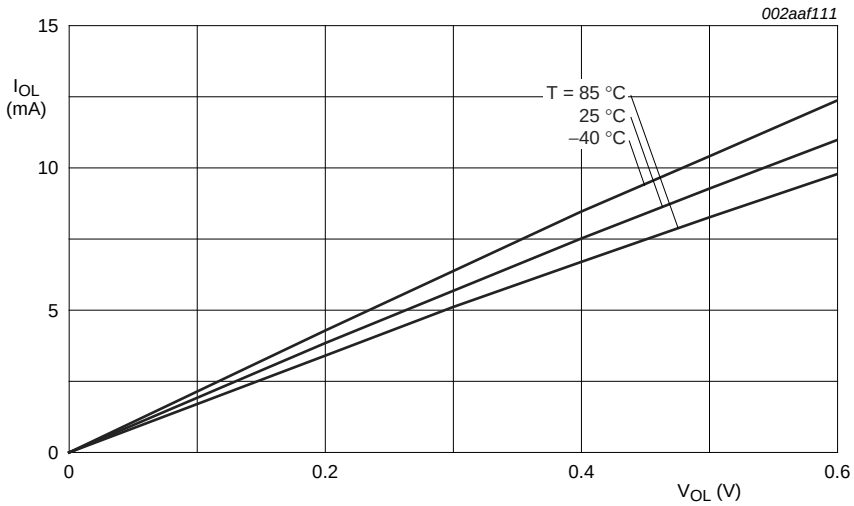
Fig 9. Total DC-to-DC converter maximum supply current $I_{DD(DCDC)dpd(3V3)}$ versus temperature in Deep power-down mode

10.3 Electrical pin characteristics



Conditions: $V_{DD(3V3)}$ = 3.3 V; standard port pins.

Fig 10. Typical HIGH-level output voltage V_{OH} versus HIGH-level output source current I_{OH}



Conditions: $V_{DD(3V3)}$ = 3.3 V; standard port pins.

Fig 11. Typical LOW-level output current I_{OL} versus LOW-level output voltage V_{OL}

11. Dynamic characteristics

Table 8. Dynamic characteristics

T_{amb} = −40 °C to +85 °C for commercial applications; $V_{DD(3V3)}$ over specified ranges.[1]

Symbol	Parameter	Conditions	Min	Typ[2]	Max	Unit
ARM processor clock frequency						
f_{oper}	operating frequency	CCLK; −40 °C to +85 °C	1	-	72	MHz
		IRC; −40 °C to +85 °C	3.96	4	4.04	MHz
External clock						
f_{osc}	oscillator frequency		1	-	25	MHz
$T_{cy(clk)}$	clock cycle time		40	-	1000	ns
t_{CHCX}	clock HIGH time		$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCX}	clock LOW time		$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCH}	clock rise time		-	-	5	ns
t_{CHCL}	clock fall time		-	-	5	ns
I^2C-bus pins (P0[27] and P0[28])						
$t_{f(o)}$	output fall time	V_{IH} to V_{IL}	$20 + 0.1 \times C_b$[3]	-	-	ns
SSP interface						
$t_{su(SPI\_MISO)}$	SPI_MISO set-up time	T_{amb} = 25 °C; measured in SPI Master mode; see Figure 14	-	11	-	ns

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[3] Bus capacitance C_b in pF, from 10 pF to 400 pF.

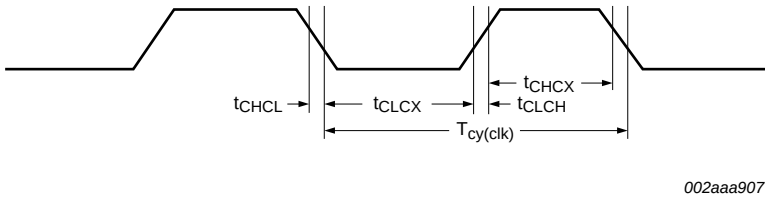


Fig 12. External clock timing (with an amplitude of at least $V_{i(RMS)}$ = 200 mV)

11.4 Flash memory

Table 12. Dynamic characteristics of flash

T_{amb} = −40 °C to +85 °C, unless otherwise specified; $V_{DD(3V3)}$ = 3.0 V to 3.6 V; all voltages are measured with respect to ground.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
N_{endu}	endurance		[1]	10000	100000	-	cycles
t_{ret}	retention time	powered; < 100 cycles	[2]	10	-	-	years
		unpowered; < 100 cycles		20	-	-	years
t_{er}	erase time	sector or multiple consecutive sectors		95	100	105	ms
t_{prog}	programming time		[2]	0.95	1	1.05	ms

[1] Number of program/erase cycles.

[2] Programming times are given for writing 256 bytes from RAM to the flash. Data must be written to the flash in blocks of 256 bytes.

11.5 Timing

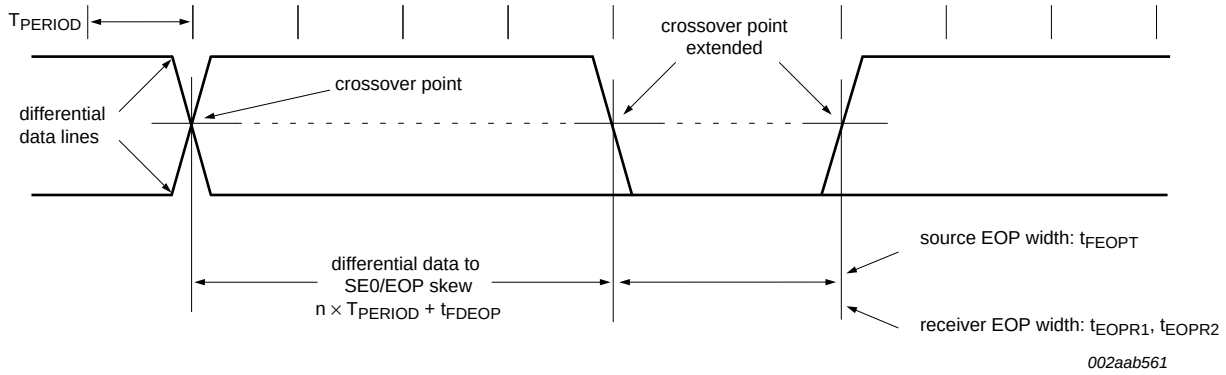


Fig 13. Differential data-to-EOP transition skew and EOP width

17. Revision history

Table 19. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC2361_62 v.5.1	20131015	Product data sheet	-	LPC2361_62 v.5
Modifications:	• Table 3 “Pin description”, Table note 6: Changed glitch filter spec from 5 ns to 10 ns. • Table 8 “Dynamic characteristics”: Changed min clock cycle time from 42 to 40.			
LPC2361_62 v.5	20111025	Product data sheet	-	LPC2361_62 v.4
Modifications:	• Table 3: – Updated description for USB_UP_LED. – Added Table note 7 for TCK and TDO pins. – Added Table note 8 for TMS, TDI, $\overline{\text{TRST}}$, and RTCK pins. – Added Table note 12 for RTCX1 and RTCX2 pins. • Table 4: – Added “non-operating” to conditions column of T_{stg}. – Updated storage temperature minimum/maximum to −65/+150. – Updated Table note 5. • Table 7: Changed V_{hys} typical value from $0.5V_{DD(3V3)}$ to $0.05V_{DD(3V3)}$. • Table 12: Updated table. • Section 14.2: Changed section title and updated contents. • Section 14.4: Changed section title. • Added: – Section 9 “Thermal characteristics”. – Section 10.3 “Electrical pin characteristics”. – Section 11.1 “Internal oscillators”. – Section 11.2 “I/O pins”. – Section 14.3 “RTC 32 kHz oscillator component selection” – Section 14.5 “Standard I/O pin configuration” – Section 14.6 “Reset pin configuration”.			
LPC2361_62 v.4	20100304	Product data sheet	-	LPC2361_62 v.3

Table 19. Revision history *…continued*

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC2361_62 v.3	20081111	Product data sheet	-	LPC2361_62 v.2
Modifications:	• Figure 3: corrected memory map.			
LPC2361_62 v.2	20081016	Product data sheet	-	LPC2361_62 v.1
Modifications:	• Clarify Ethernet availability between devices throughout data sheet. • Section 2 and Section 7.3: clarify SRAM size difference between devices. • Table 2: add table note to clarify Ethernet SRAM usage, changed orientation from landscape to portrait. • Table 5: removed table note “Includes external resistors...”. • Table 5: removed row R_{pu}. • Table 5: V_I, added Table note 6. • Table 5: V_{hys}, moved 0.4 from Typ to Min column. • Table 5: I_{OHS}, I_{OLS}, updated Table note 8. • Figure 6: removed figure note row “V_{DD} = 1.8 V”.			
LPC2361_62 v.1	20080804	Product data sheet	-	-