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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Not For New Designs |
| Core Processor | ARM7® |
| Core Size | 16/32-Bit |
| Speed | 72MHz |
| Connectivity | CANbus, Ethernet, I²C, Microwire, SPI, SSI, SSP, UART/USART, USB OTG |
| Peripherals | Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT |
| Number of I/O | 70 |
| Program Memory Size | 128KB (128K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 58K x 8 |
| Voltage - Supply (Vcc/Vdd) | 3V ~ 3.6V |
| Data Converters | A/D 6x10b; D/A 1x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 100-LQFP |
| Supplier Device Package | 100-LQFP (14x14) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc2362fbd100-551 |

- Serial interfaces:
  - Ethernet MAC with associated DMA controller (LPC2362 only). These functions reside on an independent AHB.
  - USB 2.0 device/host/OTG with on-chip PHY and associated DMA controller.
  - Four UARTs with fractional baud rate generation, one with modem control I/O, one with IrDA support, all with FIFO.
  - CAN controller with two channels.
  - SPI controller.
  - Two SSP controllers, with FIFO and multi-protocol capabilities. One is an alternate for the SPI port, sharing its interrupt and pins. These can be used with the GPDMA controller.
  - Three $I^2C$-bus interfaces (one with open-drain and two with standard port pins).
  - $I^2S$ (Inter-IC Sound) interface for digital audio input or output. It can be used with the GPDMA.
- Other peripherals:
  - 70 general purpose I/O pins with configurable pull-up/down resistors.
  - 10-bit ADC with input multiplexing among 6 pins.
  - 10-bit DAC.
  - Four general purpose timers/counters with a total of 8 capture inputs and 10 compare outputs. Each timer block has an external count input.
  - One PWM/timer block with support for three-phase motor control. The PWM has two external count inputs.
  - Real-Time Clock (RTC) with separate power pin, clock source can be the RTC oscillator or the APB clock.
  - 2 kB SRAM powered from the RTC power pin, allowing data to be stored when the rest of the chip is powered off.
  - WatchDog Timer (WDT). The WDT can be clocked from the internal RC oscillator, the RTC oscillator, or the APB clock.
- Standard ARM test/debug interface for compatibility with existing tools.
- Emulation trace module supports real-time trace.
- Single 3.3 V power supply (3.0 V to 3.6 V).
- Four reduced power modes: idle, sleep, power-down, and deep power-down.
- Four external interrupt inputs configurable as edge/level sensitive. All pins on PORT0 and PORT2 can be used as edge sensitive interrupt sources.
- Processor wake-up from Power-down mode via any interrupt able to operate during Power-down mode (includes external interrupts, RTC interrupt, USB activity, Ethernet wake-up interrupt).
- Two independent power domains allow fine tuning of power consumption based on needed features.
- Each peripheral has its own clock divider for further power saving.
- Brownout detect with separate thresholds for interrupt and forced reset.
- On-chip power-on reset.
- On-chip crystal oscillator with an operating range of 1 MHz to 25 MHz.
- 4 MHz internal RC oscillator trimmed to 1 % accuracy that can optionally be used as the system clock. When used as the CPU clock, does not allow CAN and USB to run.

- On-chip PLL allows CPU operation up to the maximum CPU rate without the need for a high frequency crystal. May be run from the main oscillator, the internal RC oscillator, or the RTC oscillator.
- Versatile pin function selections allow more possibilities for using on-chip peripheral functions.

# 3. Applications

- Industrial control
- Medical systems
- Protocol converter
- Communications

# 4. Ordering information

**Table 1. Ordering information**

| Type number | Package | | |
|---|---|---|---|
| | Name | Description | Version |
| LPC2361FBD100 | LQFP100 | plastic low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm | SOT407-1 |
| LPC2362FBD100 | LQFP100 | plastic low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm | SOT407-1 |

## 4.1 Ordering options

**Table 2. Ordering options**

| Type number | Flash (kB) | SRAM (kB) | | | | | Ethernet | USB device + 4 kB FIFO | GP DMA | Channels | | | Temp range |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Local bus | Ethernet buffer | GP/USB | RTC | Total | | | | CAN | ADC | DAC | |
| LPC2361FBD100 | 64 | 8 | 16[1] | 8 | 2 | 34 | - | yes | yes | 2 | 6 | 1 | −40 °C to +85 °C |
| LPC2362FBD100 | 128 | 32 | 16 | 8 | 2 | 58 | RMII | yes | yes | 2 | 6 | 1 | −40 °C to +85 °C |

[1] Available as general purpose SRAM for the LPC2361.

# 6. Pinning information

## 6.1 Pinning

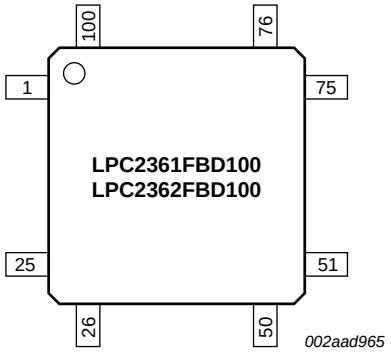



**Fig 2. LPC2361/2362 pinning**

## 6.2 Pin description

**Table 3. Pin description**

| Symbol | Pin | Type | Description |
|---|---|---|---|
| P0[0] to P0[31] | | I/O | **Port 0:** Port 0 is a 32-bit I/O port with individual direction controls for each bit. The operation of port 0 pins depends upon the pin function selected via the pin connect block. Pins 12, 13, 14, and 31 of this port are not available. |
| P0[0]/RD1/TXD3/ SDA1 | 46[1] | I/O | **P0[0] —** General purpose digital input/output pin. |
| | | I | **RD1 —** CAN1 receiver input. |
| | | O | **TXD3 —** Transmitter output for UART3. |
| | | I/O | **SDA1 —** $I^2C1$ data input/output (this is not an open-drain pin). |
| P0[1]/TD1/RXD3/ SCL1 | 47[1] | I/O | **P0[1] —** General purpose digital input/output pin. |
| | | O | **TD1 —** CAN1 transmitter output. |
| | | I | **RXD3 —** Receiver input for UART3. |
| | | I/O | **SCL1 —** $I^2C1$ clock input/output (this is not an open-drain pin). |
| P0[2]/TXD0 | 98[1] | I/O | **P0[2] —** General purpose digital input/output pin. |
| | | O | **TXD0 —** Transmitter output for UART0. |
| P0[3]/RXD0 | 99[1] | I/O | **P0[3] —** General purpose digital input/output pin. |
| | | I | **RXD0 —** Receiver input for UART0. |
| P0[4]/I2SRX_CLK/ RD2/CAP2[0] | 81[1] | I/O | **P0[4] —** General purpose digital input/output pin. |
| | | I/O | **I2SRX_CLK —** Receive Clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the *$I^2S$-bus specification*. |
| | | I | **RD2 —** CAN2 receiver input. |
| | | I | **CAP2[0] —** Capture input for Timer 2, channel 0. |

**Table 3. Pin description** *…continued*

| Symbol | Pin | Type | Description |
|---|---|---|---|
| P0[17]/CTS1/ MISO0/MISO | 61[1] | I/O | **P0[17] —** General purpose digital input/output pin. |
| | | I | **CTS1 —** Clear to Send input for UART1. |
| | | I/O | **MISO0 —** Master In Slave Out for SSP0. |
| | | I/O | **MISO —** Master In Slave Out for SPI. |
| P0[18]/DCD1/ MOSI0/MOSI | 60[1] | I/O | **P0[18] —** General purpose digital input/output pin. |
| | | I | **DCD1 —** Data Carrier Detect input for UART1. |
| | | I/O | **MOSI0 —** Master Out Slave In for SSP0. |
| | | I/O | **MOSI —** Master Out Slave In for SPI. |
| P0[19]/DSR1/SDA1 | 59[1] | I/O | **P0[19] —** General purpose digital input/output pin. |
| | | I | **DSR1 —** Data Set Ready input for UART1. |
| | | I/O | **SDA1 —** $I^2C$1 data input/output (this is not an open-drain pin). |
| P0[20]/DTR1/SCL1 | 58[1] | I/O | **P0[20] —** General purpose digital input/output pin. |
| | | O | **DTR1 —** Data Terminal Ready output for UART1. |
| | | I/O | **SCL1 —** $I^2C$1 clock input/output (this is not an open-drain pin). |
| P0[21]/RI1/RD1 | 57[1] | I/O | **P0[21] —** General purpose digital input/output pin. |
| | | I | **RI1 —** Ring Indicator input for UART1. |
| | | I | **RD1 —** CAN1 receiver input. |
| P0[22]/RTS1/TD1 | 56[1] | I/O | **P0[22] —** General purpose digital input/output pin. |
| | | O | **RTS1 —** Request to Send output for UART1. |
| | | O | **TD1 —** CAN1 transmitter output. |
| P0[23]/AD0[0]/ I2SRX_CLK/ CAP3[0] | 9[2] | I/O | **P0[23] —** General purpose digital input/output pin. |
| | | I | **AD0[0] —** A/D converter 0, input 0. |
| | | I/O | **I2SRX_CLK —** Receive Clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the *$I^2S$-bus specification*. |
| | | I | **CAP3[0] —** Capture input for Timer 3, channel 0. |
| P0[24]/AD0[1]/ I2SRX_WS/ CAP3[1] | 8[2] | I/O | **P0[24] —** General purpose digital input/output pin. |
| | | I | **AD0[1] —** A/D converter 0, input 1. |
| | | I/O | **I2SRX_WS —** Receive Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *$I^2S$-bus specification*. |
| | | I | **CAP3[1] —** Capture input for Timer 3, channel 1. |
| P0[25]/AD0[2]/ I2SRX_SDA/ TXD3 | 7[2] | I/O | **P0[25] —** General purpose digital input/output pin. |
| | | I | **AD0[2] —** A/D converter 0, input 2. |
| | | I/O | **I2SRX_SDA —** Receive data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *$I^2S$-bus specification*. |
| | | O | **TXD3 —** Transmitter output for UART3. |
| P0[26]/AD0[3]/ AOUT/RXD3 | 6[3] | I/O | **P0[26] —** General purpose digital input/output pin. |
| | | I | **AD0[3] —** A/D converter 0, input 3. |
| | | O | **AOUT —** D/A converter output. |
| | | I | **RXD3 —** Receiver input for UART3. |
| P0[27]/SDA0 | 25[4] | I/O | **P0[27] —** General purpose digital input/output pin. Output is open-drain. |
| | | I/O | **SDA0 —** $I^2C$0 data input/output. Open-drain output (for $I^2C$-bus compliance). |

## 7.4 Memory map

The LPC2361/2362 memory map incorporates several distinct regions as shown in Figure 3.

In addition, the CPU interrupt vectors may be remapped to allow them to reside in either flash memory (default), boot ROM, or SRAM (see Section 7.24.6).

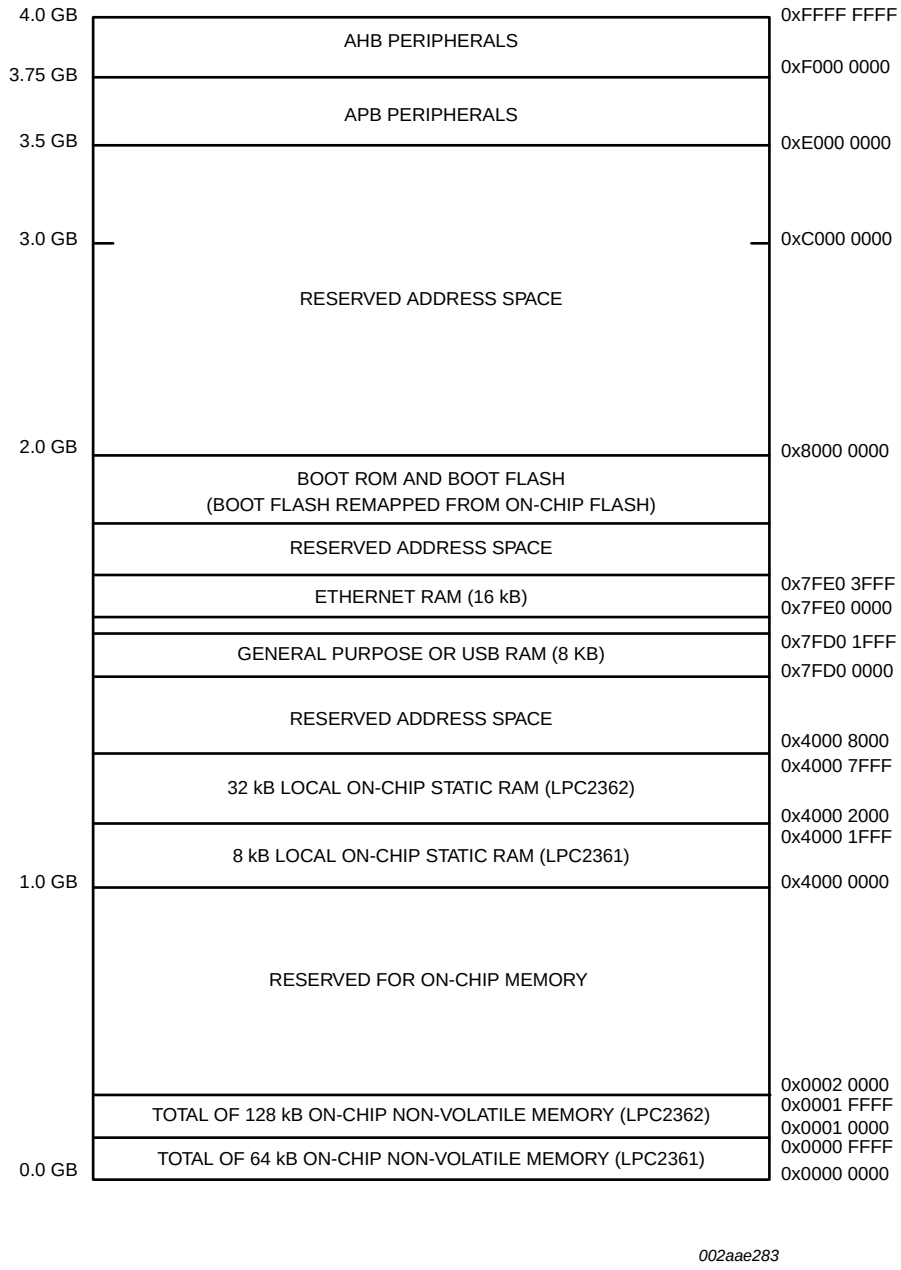



**Fig 3. LPC2361/2362 memory map**

Each CAN controller has a register structure similar to the NXP SJA1000 and the PeliCAN Library block, but the 8-bit registers of those devices have been combined in 32-bit words to allow simultaneous access in the ARM environment. The main operational difference is that the recognition of received Identifiers, known in CAN terminology as Acceptance Filtering, has been removed from the CAN controllers and centralized in a global Acceptance Filter.

### 7.11.1 Features

- Two CAN controllers and buses.
- Data rates to 1 Mbit/s on each bus.
- 32-bit register and RAM access.
- Compatible with *CAN specification 2.0B, ISO 11898-1*.
- Global Acceptance Filter recognizes 11-bit and 29-bit receive identifiers for all CAN buses.
- Acceptance Filter can provide FullCAN-style automatic reception for selected Standard Identifiers.
- FullCAN messages can generate interrupts.

## 7.12 10-bit ADC

The LPC2361/2362 contain one ADC. It is a single 10-bit successive approximation ADC with six channels.

### 7.12.1 Features

- 10-bit successive approximation ADC.
- Input multiplexing among 6 pins.
- Power-down mode.
- Measurement range 0 V to $V_{i(VREF)}$.
- 10-bit conversion time $\geq$ 2.44 $\mu$s.
- Burst conversion mode for single or multiple inputs.
- Optional conversion on transition of input pin or Timer Match signal.
- Individual result registers for each ADC channel to reduce interrupt overhead.

## 7.13 10-bit DAC

The DAC allows the LPC2361/2362 to generate a variable analog output. The maximum output value of the DAC is $V_{i(VREF)}$.

### 7.13.1 Features

- 10-bit DAC
- Resistor string architecture
- Buffered output
- Power-down mode
- Selectable output drive

- Dedicated 32 kHz oscillator or programmable prescaler from APB clock.
- Dedicated power supply pin can be connected to a battery or to the main 3.3 V.
- Periodic interrupts can be generated from increments of any field of the time registers, and selected fractional second values.
- 2 kB data SRAM powered by VBAT.
- RTC and battery RAM power supply is isolated from the rest of the chip.

## 7.23 Clocking and power control

### 7.23.1 Crystal oscillators

The LPC2361/2362 includes three independent oscillators. These are the Main Oscillator, the Internal RC oscillator, and the RTC oscillator. Each oscillator can be used for more than one purpose as required in a particular application. Any of the three clock sources can be chosen by software to drive the PLL and ultimately the CPU.

Following reset, the LPC2361/2362 will operate from the Internal RC oscillator until switched by software. This allows systems to operate without any external crystal and the bootloader code to operate at a known frequency.

#### 7.23.1.1 Internal RC oscillator

The IRC may be used as the clock source for the WDT, and/or as the clock that drives the PLL and subsequently the CPU. The nominal IRC frequency is 4 MHz. The IRC is trimmed to 1 % accuracy.

Upon power-up or any chip reset, the LPC2361/2362 uses the IRC as the clock source. Software may later switch to one of the other available clock sources.

#### 7.23.1.2 Main oscillator

The main oscillator can be used as the clock source for the CPU, with or without using the PLL. The main oscillator operates at frequencies of 1 MHz to 25 MHz. This frequency can be boosted to a higher frequency, up to the maximum CPU operating frequency, by the PLL. The clock selected as the PLL input is PLLCLKIN. The ARM processor clock frequency is referred to as CCLK elsewhere in this document. The frequencies of PLLCLKIN and CCLK are the same value unless the PLL is active and connected. The clock frequency for each peripheral can be selected individually and is referred to as PCLK. Refer to Section 7.23.2 for additional information.

#### 7.23.1.3 RTC oscillator

The RTC oscillator can be used as the clock source for the RTC and/or the WDT. Also, the RTC oscillator can be used to drive the PLL and the CPU.

### 7.23.2 PLL

The PLL accepts an input clock frequency in the range of 32 kHz to 25 MHz. The input frequency is multiplied up to a high frequency, then divided down to provide the actual clock used by the CPU and the USB block.

The PLL input, in the range of 32 kHz to 25 MHz, may initially be divided down by a value ‘N’, which may be in the range of 1 to 256. This input division provides a wide range of output frequencies from the same input frequency.

Following the PLL input divider is the PLL multiplier. This can multiply the input divider output through the use of a Current Controlled Oscillator (CCO) by a value 'M', in the range of 1 through 32768. The resulting frequency must be in the range of 275 MHz to 550 MHz. The multiplier works by dividing the CCO output by the value of M, then using a phase-frequency detector to compare the divided CCO output to the multiplier input. The error value is used to adjust the CCO frequency.

The PLL is turned off and bypassed following a chip Reset and by entering Power-down mode. PLL is enabled by software only. The program must configure and activate the PLL, wait for the PLL to Lock, then connect to the PLL as a clock source.

### 7.23.3 Wake-up timer

The LPC2361/2362 begins operation at power-up and when awakened from Power-down and Deep power-down modes by using the 4 MHz IRC oscillator as the clock source. This allows chip operation to resume quickly. If the main oscillator or the PLL is needed by the application, software will need to enable these features and wait for them to stabilize before they are used as a clock source.

When the main oscillator is initially activated, the wake-up timer allows software to ensure that the main oscillator is fully functional before the processor uses it as a clock source and starts to execute instructions. This is important at power-on, all types of Reset, and whenever any of the aforementioned functions are turned off for any reason. Since the oscillator and other functions are turned off during Power-down and Deep power-down modes, any wake-up of the processor from Power-down modes makes use of the wake-up timer.

The wake-up timer monitors the crystal oscillator to check whether it is safe to begin code execution. When power is applied to the chip, or when some event caused the chip to exit Power-down mode, some time is required for the oscillator to produce a signal of sufficient amplitude to drive the clock logic. The amount of time depends on many factors, including the rate of $V_{DD(3V3)}$ ramp (in the case of power-on), the type of crystal and its electrical characteristics (if a quartz crystal is used), as well as any other external circuitry (e.g., capacitors), and the characteristics of the oscillator itself under the existing ambient conditions.

### 7.23.4 Power control

The LPC2361/2362 supports a variety of power control features. There are four special modes of processor power reduction: Idle mode, Sleep mode, Power-down mode, and Deep power-down mode. The CPU clock rate may also be controlled as needed by changing clock sources, reconfiguring PLL values, and/or altering the CPU clock divider value. This allows a trade-off of power versus processing speed based on application requirements. In addition, Peripheral Power Control allows shutting down the clocks to individual on-chip peripherals, allowing fine tuning of power consumption by eliminating all dynamic power use in any peripherals that are not required for the application. Each of the peripherals has its own clock divider which provides even better power control.

The LPC2361/2362 also implements a separate power domain in order to allow turning off power to the bulk of the device while maintaining operation of the RTC and a small SRAM, referred to as the battery RAM.

#### 7.23.4.1 Idle mode

In Idle mode, execution of instructions is suspended until either a Reset or interrupt occurs. Peripheral functions continue operation during Idle mode and may generate interrupts to cause the processor to resume execution. Idle mode eliminates dynamic power used by the processor itself, memory systems and related controllers, and internal buses.

#### 7.23.4.2 Sleep mode

In Sleep mode, the oscillator is shut down and the chip receives no internal clocks. The processor state and registers, peripheral registers, and internal SRAM values are preserved throughout Sleep mode and the logic levels of chip pins remain static. The output of the IRC is disabled but the IRC is not powered down for a fast wake-up later. The 32 kHz RTC oscillator is not stopped because the RTC interrupts may be used as the wake-up source. The PLL is automatically turned off and disconnected. The CCLK and USB clock dividers automatically get reset to zero.

The Sleep mode can be terminated and normal operation resumed by either a Reset or certain specific interrupts that are able to function without clocks. Since all dynamic operation of the chip is suspended, Sleep mode reduces chip power consumption to a very low value. The flash memory is left on in Sleep mode, allowing a very quick wake-up.

On the wake-up of Sleep mode, if the IRC was used before entering Sleep mode, the code execution and peripherals activities will resume after 4 cycles expire. If the main external oscillator was used, the code execution will resume when 4096 cycles expire.

The customers need to reconfigure the PLL and clock dividers accordingly.

#### 7.23.4.3 Power-down mode

Power-down mode does everything that Sleep mode does, but also turns off the IRC oscillator and the flash memory. This saves more power, but requires waiting for resumption of flash operation before execution of code or data access in the flash memory can be accomplished.

On the wake-up of Power-down mode, if the IRC was used before entering Power-down mode, it will take IRC 60 μs to start-up. After this 4 IRC cycles will expire before the code execution can then be resumed if the code was running from SRAM. In the meantime, the flash wake-up timer then counts 4 MHz IRC clock cycles to make the 100 μs flash start-up time. When it times out, access to the flash will be allowed. The customers need to reconfigure the PLL and clock dividers accordingly.

#### 7.23.4.4 Deep power-down mode

Deep power-down mode is similar to the Power-down mode, but now the on-chip regulator that supplies power to the internal logic is also shut off. This produces the lowest possible power consumption without removing power from the entire chip. Since the Deep power-down mode shuts down the on-chip logic power supply, there is no register or memory retention, and resumption of operation involves the same activities as a full chip reset.

If power is supplied to the LPC2361/2362 during Deep power-down mode, wake-up can be caused by the RTC Alarm interrupt or by external Reset.

While in Deep power-down mode, external device power may be removed. In this case, the LPC2361/2362 will start up when external power is restored.

Essential data may be retained through Deep power-down mode (or through complete powering off of the chip) by storing data in the Battery RAM, as long as the external power to the VBAT pin is maintained.

#### 7.23.4.5 Power domains

The LPC2361/2362 provides two independent power domains that allow the bulk of the device to have power removed while maintaining operation of the RTC and the battery RAM.

On the LPC2361/2362, I/O pads are powered by the 3.3 V ($V_{DD(3V3)}$) pins, while the $V_{DD(DCDC)(3V3)}$ pin powers the on-chip DC-to-DC converter which in turn provides power to the CPU and most of the peripherals.

Depending on the LPC2361/2362 application, a design can use two power options to manage power consumption.

The first option assumes that power consumption is not a concern and the design ties the $V_{DD(3V3)}$ and $V_{DD(DCDC)(3V3)}$ pins together. This approach requires only one 3.3 V power supply for both pads, the CPU, and peripherals. While this solution is simple, it does not support powering down the I/O pad ring “on the fly” while keeping the CPU and peripherals alive.

The second option uses two power supplies; a 3.3 V supply for the I/O pads ($V_{DD(3V3)}$) and a dedicated 3.3 V supply for the CPU ($V_{DD(DCDC)(3V3)}$). Having the on-chip DC-to-DC converter powered independently from the I/O pad ring enables shutting down of the I/O pad power supply “on the fly”, while the CPU and peripherals stay active.

The VBAT pin supplies power only to the RTC and the battery RAM. These two functions require a minimum of power to operate, which can be supplied by an external battery. When the CPU and the rest of chip functions are stopped and power removed, the RTC can supply an alarm output that may be used by external hardware to restore chip power and resume operation.

## 7.24 System control

### 7.24.1 Reset

Reset has four sources on the LPC2361/2362: the $\overline{\text{RESET}}$ pin, the watchdog reset, power-on reset, and the BrownOut Detection (BOD) circuit. The $\overline{\text{RESET}}$ pin is a Schmitt trigger input pin. Assertion of chip Reset by any source, once the operating voltage attains a usable level, starts the wake-up timer (see description in Section 7.23.3 “Wake-up timer”), causing reset to remain asserted until the external Reset is de-asserted, the oscillator is running, a fixed number of clocks have passed, and the flash controller has completed its initialization.

When the internal Reset is removed, the processor begins executing at address 0, which is initially the Reset vector mapped from the Boot Block. At that point, all of the processor and peripheral registers have been initialized to predetermined values.

outputs information about processor execution to a trace port. A software debugger allows configuration of the ETM using a JTAG interface and displays the trace information that has been captured.

The ETM is connected directly to the ARM core and not to the main AMBA system bus. It compresses the trace information and exports it through a narrow trace port. An external Trace Port Analyzer captures the trace information under software debugger control. The trace port can broadcast the Instruction trace information. Instruction trace (or PC trace) shows the flow of execution of the processor and provides a list of all the instructions that were executed. Instruction trace is significantly compressed by only broadcasting branch addresses as well as a set of status signals that indicate the pipeline status on a cycle by cycle basis. Trace information generation can be controlled by selecting the trigger resource. Trigger resources include address comparators, counters and sequencers. Since trace information is compressed the software debugger requires a static image of the code being executed. Self-modifying code can not be traced because of this restriction.

### 7.25.3 RealMonitor

RealMonitor is a configurable software module, developed by ARM Inc., which enables real-time debug. It is a lightweight debug monitor that runs in the background while users debug their foreground application. It communicates with the host using the DCC, which is present in the EmbeddedICE logic. The LPC2361/2362 contain a specific configuration of RealMonitor software programmed into the on-chip ROM memory.

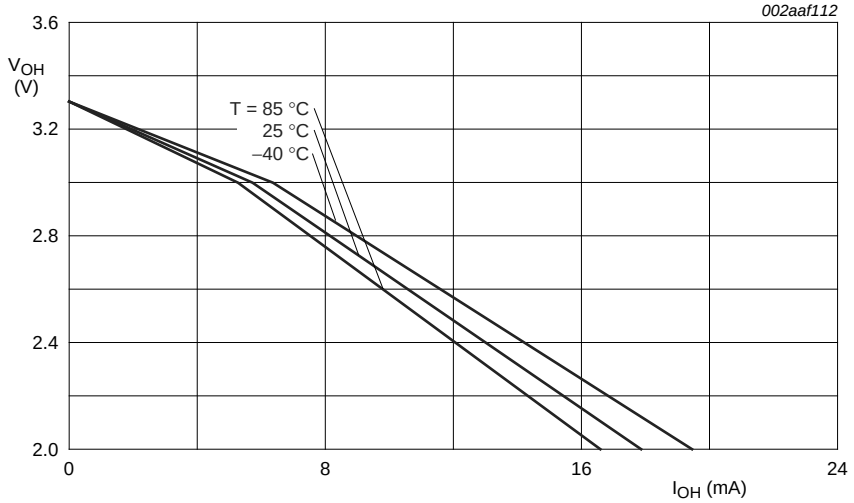
# 10. Static characteristics

**Table 7. Static characteristics**

*$T_{amb}$ = −40 °C to +85 °C for commercial applications, unless otherwise specified.*

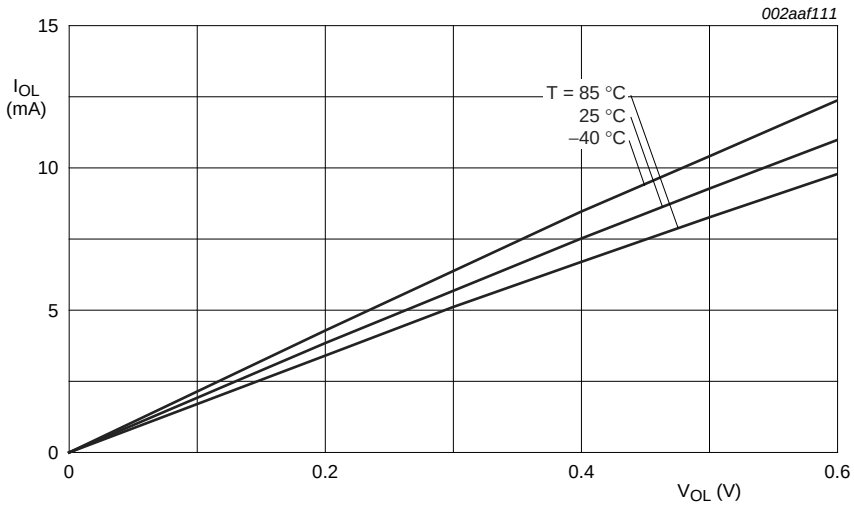
| Symbol | Parameter | Conditions | | Min | Typ[1] | Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_{DD(3V3)}$ | supply voltage (3.3 V) | core and external rail | | 3.0 | 3.3 | 3.6 | V |
| $V_{DD(DCDC)(3V3)}$ | DC-to-DC converter supply voltage (3.3 V) | | | 3.0 | 3.3 | 3.6 | V |
| $V_{DDA}$ | analog 3.3 V pad supply voltage | | | 3.0 | 3.3 | 3.6 | V |
| $V_{i(VBAT)}$ | input voltage on pin VBAT | | [2] | 2.0 | 3.3 | 3.6 | V |
| $V_{i(VREF)}$ | input voltage on pin VREF | | | 2.5 | 3.3 | $V_{DDA}$ | V |
| $I_{DD(DCDC)act(3V3)}$ | active mode DC-to-DC converter supply current (3.3 V) | $V_{DD(DCDC)(3V3)}$ = 3.3 V; $T_{amb}$ = 25 °C; code `while(1){}` executed from flash; no peripherals enabled; PCLK = CCLK | | | | | |
| | | CCLK = 10 MHz | | - | 15 | - | mA |
| | | CCLK = 72 MHz | | - | 63 | - | mA |
| | | all peripherals enabled; PCLK = CCLK / 8 | | | | | |
| | | CCLK = 10 MHz | | - | 21 | - | mA |
| | | CCLK = 72 MHz | | - | 92 | - | mA |
| | | all peripherals enabled; PCLK = CCLK | | | | | |
| | | CCLK = 10 MHz | | - | 27 | - | mA |
| | | CCLK = 72 MHz | | - | 125 | - | mA |
| $I_{DD(DCDC)pd(3V3)}$ | Power-down mode DC-to-DC converter supply current (3.3 V) | $V_{DD(DCDC)(3V3)}$ = 3.3 V; $T_{amb}$ = 25 °C | [3] | - | 113 | - | µA |
| $I_{DD(DCDC)dpd(3V3)}$ | Deep power-down mode DC-to-DC converter supply current (3.3 V) | | [3] | - | 20 | - | µA |
| $I_{BATact}$ | active mode battery supply current | | [4] | - | 20 | - | µA |
| $I_{BAT}$ | battery supply current | Deep power-down mode | [3] | - | 20 | - | µA |
| **Standard port pins, $\overline{\text{RESET}}$, RTCK** | | | | | | | |
| $I_{IL}$ | LOW-level input current | $V_I$ = 0 V; no pull-up | | - | - | 3 | µA |
| $I_{IH}$ | HIGH-level input current | $V_I = V_{DD(3V3)}$; no pull-down | | - | - | 3 | µA |
| $I_{OZ}$ | OFF-state output current | $V_O$ = 0 V; $V_O = V_{DD(3V3)}$; no pull-up/down | | - | - | 3 | µA |

## 10.3 Electrical pin characteristics




Conditions: $V_{DD(3V3)}$ = 3.3 V; standard port pins.

**Fig 10. Typical HIGH-level output voltage $V_{OH}$ versus HIGH-level output source current $I_{OH}$**




Conditions: $V_{DD(3V3)}$ = 3.3 V; standard port pins.

**Fig 11. Typical LOW-level output current $I_{OL}$ versus LOW-level output voltage $V_{OL}$**

## 14.3 RTC 32 kHz oscillator component selection

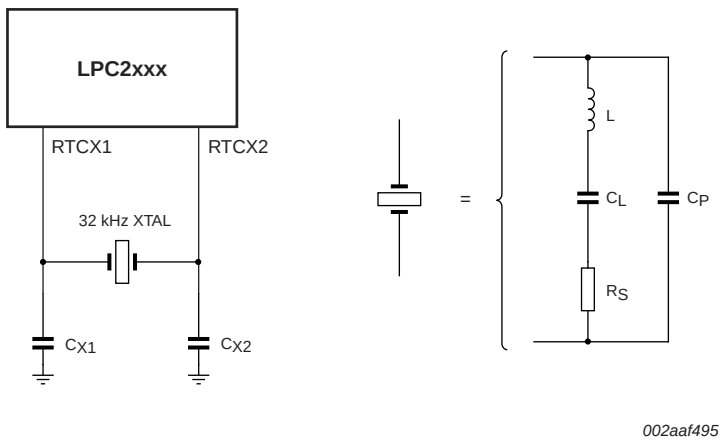



**Fig 24. RTC oscillator modes and models: oscillation mode of operation and external crystal model used for $C_{X1}/C_{X2}$ evaluation**

The RTC external oscillator circuit is shown in Figure 24. Since the feedback resistance is integrated on chip, only a crystal, the capacitances $C_{X1}$ and $C_{X2}$ need to be connected externally to the microcontroller.

Table 17 gives the crystal parameters that should be used. $C_L$ is the typical load capacitance of the crystal and is usually specified by the crystal manufacturer. The actual $C_L$ influences oscillation frequency. When using a crystal that is manufactured for a different load capacitance, the circuit will oscillate at a slightly different frequency (depending on the quality of the crystal) compared to the specified one. Therefore for an accurate time reference it is advised to use the load capacitors as specified in Table 17 that belong to a specific $C_L$. The value of external capacitances $C_{X1}$ and $C_{X2}$ specified in this table are calculated from the internal parasitic capacitances and the $C_L$. Parasitics from PCB and package are not taken into account.

**Table 17. Recommended values for the RTC external 32 kHz oscillator $C_{X1}/C_{X2}$ components**

| Crystal load capacitance $C_L$ | Maximum crystal series resistance $R_S$ | External load capacitors $C_{X1}/C_{X2}$ |
|---|---|---|
| 11 pF | < 100 kΩ | 18 pF, 18 pF |
| 13 pF | < 100 kΩ | 22 pF, 22 pF |
| 15 pF | < 100 kΩ | 27 pF, 27 pF |

## 14.4 XTAL and RTCX Printed Circuit Board (PCB) layout guidelines

The crystal should be connected on the PCB as close as possible to the oscillator input and output pins of the chip. Take care that the load capacitors $C_{x1}$, $C_{x2}$, and $C_{x3}$ in case of third overtone crystal usage have a common ground plane. The external components must also be connected to the ground plane. Loops must be made as small as possible in order to keep the noise coupled in via the PCB as small as possible. Also parasitics should stay as small as possible. Values of $C_{x1}$ and $C_{x2}$ should be chosen smaller accordingly to the increase in parasitics of the PCB layout.

# 17. Revision history

**Table 19. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| LPC2361_62 v.5.1 | 20131015 | Product data sheet | - | LPC2361_62 v.5 |
| Modifications: | • Table 3 “Pin description”, Table note 6: Changed glitch filter spec from 5 ns to 10 ns.<br>• Table 8 “Dynamic characteristics”: Changed min clock cycle time from 42 to 40. | | | |
| LPC2361_62 v.5 | 20111025 | Product data sheet | - | LPC2361_62 v.4 |
| Modifications: | • Table 3:<br>– Updated description for USB_UP_LED.<br>– Added Table note 7 for TCK and TDO pins.<br>– Added Table note 8 for TMS, TDI, $\overline{\text{TRST}}$, and RTCK pins.<br>– Added Table note 12 for RTCX1 and RTCX2 pins.<br>• Table 4:<br>– Added “non-operating” to conditions column of $T_{stg}$.<br>– Updated storage temperature minimum/maximum to −65/+150.<br>– Updated Table note 5.<br>• Table 7: Changed $V_{hys}$ typical value from $0.5V_{DD(3V3)}$ to $0.05V_{DD(3V3)}$.<br>• Table 12: Updated table.<br>• Section 14.2: Changed section title and updated contents.<br>• Section 14.4: Changed section title.<br>• Added:<br>– Section 9 “Thermal characteristics”.<br>– Section 10.3 “Electrical pin characteristics”.<br>– Section 11.1 “Internal oscillators”.<br>– Section 11.2 “I/O pins”.<br>– Section 14.3 “RTC 32 kHz oscillator component selection”<br>– Section 14.5 “Standard I/O pin configuration”<br>– Section 14.6 “Reset pin configuration”. | | | |
| LPC2361_62 v.4 | 20100304 | Product data sheet | - | LPC2361_62 v.3 |

**Table 19. Revision history** *…continued*

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| Modifications: | • Table 3 “Pin description”: Added table note for XTAL1 and XTAL2 pins.<br>• Table 4 “Limiting values”: Changed $V_{ESD}$ min/max to −2500/+2500.<br>• Table 5 “Static characteristics”: Updated min, typical and max values for oscillator pins.<br>• Table 5 “Static characteristics”: Added table note for $Z_{DRV}$.<br>• Table 5 “Static characteristics”: Updated conditions and typical values for $I_{DD(DCDC)dpd(3V3)}$, $I_{BATact}$, and $I_{BAT}$.<br>• Table 6 “Dynamic characteristics”: Added ARM processor clock frequency information.<br>• Added Table 8 “Dynamic characteristics of flash”.<br>• Added Table 10 “DAC electrical characteristics”.<br>• Section 7.2 “On-chip flash programming memory”: Removed text regarding flash endurance minimum specs.<br>• Added Section 7.23.4.4 “Deep power-down mode”.<br>• Section 7.24.2 “Brownout detection”: Changed $V_{DD(3V3)}$ to $V_{DD(DCDC)(3V3)}$.<br>• Added Section 9.1 “Power-down mode”.<br>• Added Section 9.2 “Deep power-down mode”.<br>• Added Section 13.2 “XTAL1 input”.<br>• Added Section 13.3 “XTAL and RTC Printed Circuit Board (PCB) layout guidelines”.<br>• Figure 13 “ADC characteristics”: Changed $V_{DDA}$ to $V_{i(VREF)}$. | | | |

**Table 19. Revision history** *…continued*

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| LPC2361_62 v.3 | 20081111 | Product data sheet | - | LPC2361_62 v.2 |
| Modifications: | • Figure 3: corrected memory map. | | | |
| LPC2361_62 v.2 | 20081016 | Product data sheet | - | LPC2361_62 v.1 |
| Modifications: | • Clarify Ethernet availability between devices throughout data sheet.<br>• Section 2 and Section 7.3: clarify SRAM size difference between devices.<br>• Table 2: add table note to clarify Ethernet SRAM usage, changed orientation from landscape to portrait.<br>• Table 5: removed table note “Includes external resistors...”.<br>• Table 5: removed row $R_{pu}$.<br>• Table 5: $V_I$, added Table note 6.<br>• Table 5: $V_{hys}$, moved 0.4 from Typ to Min column.<br>• Table 5: $I_{OHS}$, $I_{OLS}$, updated Table note 8.<br>• Figure 6: removed figure note row “$V_{DD}$ = 1.8 V”. | | | |
| LPC2361_62 v.1 | 20080804 | Product data sheet | - | - |

# 18. Legal information

## 18.1 Data sheet status

| Document status[1][2] | Product status[3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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