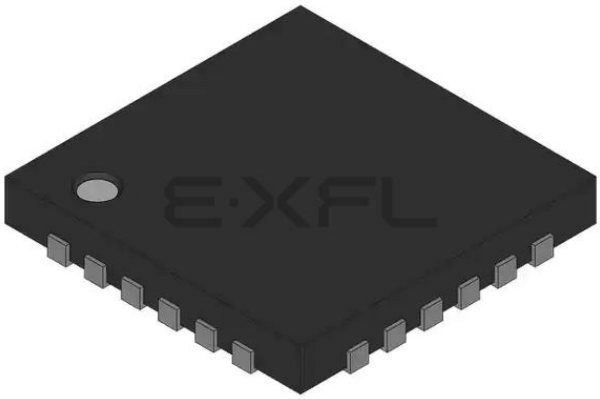

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

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Details	
Product Status	Active
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Program Memory Type	-
EEPROM Size	-
RAM Size	-
Voltage - Supply (Vcc/Vdd)	-
Data Converters	-
Oscillator Type	-
Operating Temperature	-
Mounting Type	-
Package / Case	-
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mc9s08su16vfk

Ordering information

Part Number	Memory		Maximum number of I\O's
	Flash (KB)	SRAM (Byte)	
MC9S08SU16VFK	16	768	17
MC9S08SU8VFK	8	768	17

Related resources

Type	Description	Resource
Selector Guide	The NXP Solution Advisor is a web-based tool that features interactive application wizards and a dynamic product selector.	Solution Advisor
Reference Manual	The Reference Manual contains a comprehensive description of the structure and function (operation) of a device. [1]	MC9S08SU16RM
Data Sheet	The Data Sheet includes electrical characteristics and signal connections.	MC9S08SU16[1]
Chip Errata	The chip mask set Errata provides additional or corrective information for a particular device mask set.	xN88M[2]
Package drawing	Package dimensions are provided in package drawings.	QFN 24-pin: 98ASA00602D

1. To find the associated resource, go to nxp.com and perform a search using this term.
2. To find the associated resource, go to nxp.com and perform a search using this term with the “x” replaced by the revision of the device you are using.

Figure 1 shows the functional modules in the chip.

Table of Contents

1 Ratings

1.1 Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T_{STG}	Storage temperature	–55	150	°C	1
T_{SDR}	Solder temperature, lead-free	—	260	°C	2

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

1.2 Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

1.3 ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V_{HBM}	Electrostatic discharge voltage, human body model	-2000	+2000	V	1
V_{CDM}	Electrostatic discharge voltage, charged-device model	-500	+500	V	2
I_{LAT}	Latch-up current at ambient temperature of 105°C	-100	+100	mA	

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.

2 General

2.1 Nonswitching electrical specifications

2.1.1 DC characteristics

This section includes information about power supply requirements and I/O pin characteristics.

Table 1. DC characteristics

Symbol	C	Descriptions			Min	Typical[1]	Max	Unit
—	—	Operating voltage		—	4.5	—	18	V
V_{OH}	P	Output high voltage	All I/O pins, standard-drive strength	5 V, I_{load} = -5 mA	V_{DDX} - 0.8	—	—	V
	P		High current drive pins, high-drive strength[2]	5 V, I_{load} = -20 mA	V_{DDX} - 0.8	—	—	V
I_{OHT}	D	Output high current	Max total I_{OH} for all ports	5 V	—	—	-100	mA
V_{OL}	P	Output low voltage	All I/O pins, standard-drive strength	5 V, I_{load} = 5 mA	—	—	0.8	V
	P		High current drive pins, high-drive strength[2]	5 V, I_{load} =20 mA	—	—	0.8	V
I_{OLT}	D	Output low current	Max total I_{OL} for all ports	5 V	—	—	100	mA
V_{IH}	P	Input high voltage	All digital inputs	V_{DDX}>4.5V	0.70 × V_{DDX}	—	—	V
	C			V_{DDX}>2.7V	0.75 × V_{DDX}	—	—	
V_{IL}	P	Input low voltage	All digital inputs	V_{DDX}>4.5V	—	—	0.30 × V_{DDX}	V
	C			V_{DDX}>2.7V	—	—	0.35 × V_{DDX}	
V_{hys}	C	Input hysteresis	All digital inputs	—	0.06 × V_{DDX}	—	—	mV
$\lvert I_{In} \rvert$	P	Input leakage current	All input only pins (per pin)	V_{IN} = V_{DDX} or V_{SS}	—	0.1	1	µA
$\lvert I_{OZTOT} \rvert$	C	Total leakage combined for all inputs and Hi-Z pins	All input only and I/O	V_{IN} = V_{DDX} or V_{SS}	—	—	2	µA

Table continues on the next page...

Table 1. DC characteristics (continued)

Symbol	C	Descriptions			Min	Typical[1]	Max	Unit
R_{PU}	P	Pullup resistors	All digital inputs, when enabled (all I/O pins other than PTA4 and PTA5)	—	30.0	—	50.0	kΩ
R_{PU}[3]	P	Pullup resistors	PTA4 and PTA5 pin	—	30.0	—	60.0	kΩ
R_{PD}[4]	P	Pulldown resistors	PTB3, PTB4 and PTB5 pin	—	30	40	50	kΩ
I_{IC}	D	DC injection current[5, 6, 7]	Single pin limit	$V_{IN} < V_{SS}$, $V_{IN} > V_{DDX}$	-2	—	2	mA
			Total MCU limit, includes sum of all stressed pins		-5	—	25	
C_{In}	C	Input capacitance, all pins		—	—	—	7	pF
V_{RAM}	C	RAM retention voltage		—	2.0	—	—	V

1. Typical values are measured at 25 °C. Characterized, not tested.
2. Only PTB3, PTB4, PTB5, and PTB7 are high drive pins, and support ultra-high current output.
3. The specified resistor value is the actual value internal to the device. The pullup value may appear higher when measured externally on the pin.
4. The specified resistor value is the actual value internal to the device. The pulldown value may appear higher when measured externally on the pin.
5. All functional non-supply pins, except PTA4 and PTA5, are internally clamped to V_{SS} and V_{DDX}.
6. Input must be current-limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the large one.
7. Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If the positive injection current ($V_{In} > V_{DD}$) is higher than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure that external V_{DD} load will shunt current higher than maximum injection current when the MCU is not consuming power, such as no system clock is present, or clock rate is very low (which would reduce overall power consumption).

Table 2. Power supply electrical characteristics

Symbol	Description		Min.	Typical[1]	Max.	Unit
V_{DDX}	Output voltage V_{DDX}	Run mode 4.5 V≤ V_{DD}<5.3 V	4.20	—	5.25	V
		Run mode V_{DD}≥5.3 V	4.75	4.99	5.25	V
		Stop mode[2]	2.5	—	5.75	V
I_{DDX}	Load current V_{DDX}	Run mode 4.5V ≤ V_{DD}<5.3 V	0	—	28	mA
		Run mode V_{DD}≥5.3 V	0	—	50	mA
		Stop mode[2]	0	—	5	mA
V_{REFH}	Output voltage V_{REFH}	V_{DD} ≥ 4.5 V	4.166	4.2[3]	4.234	V
—	V_{REFH} accuracy	V_{DD}≥V_{REFH} + 0.3, 0—70 °C	—	—	0.8	%
		V_{DD}≥V_{REFH} + 0.3, -40—105 °C	—	—	1.0	%
I_{REFH}	Output current V_{REFH}	V_{DD}≥V_{REFH} + 0.3	0	—	5	mA

Table continues on the next page...

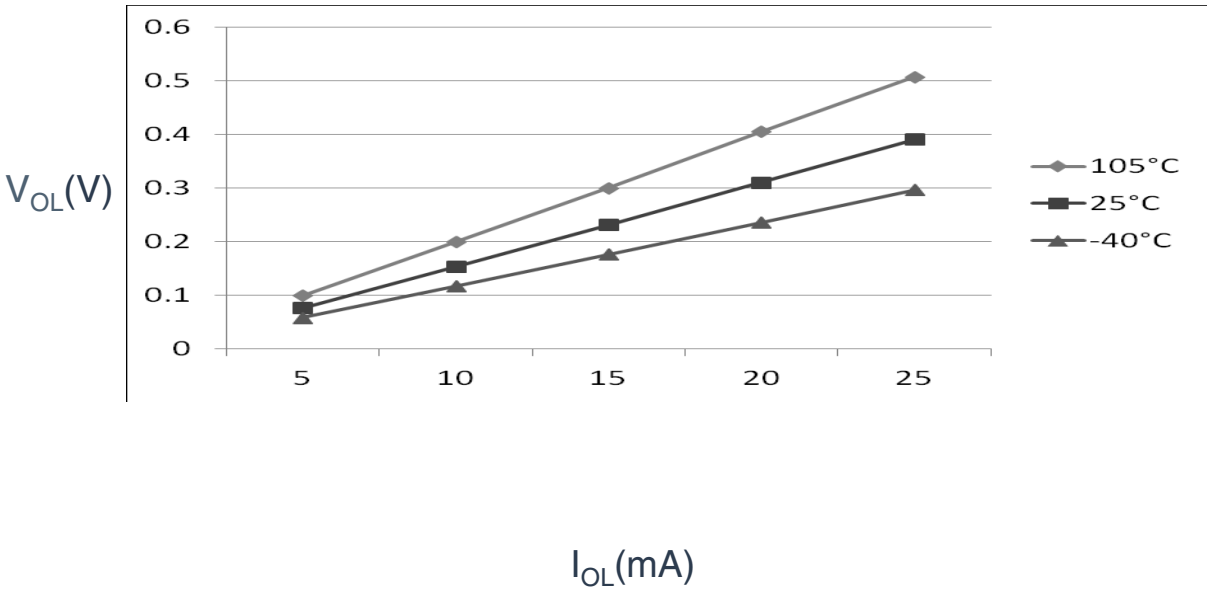


Figure 6. Typical I_{OL} Vs. V_{OL} (high drive strength) (V_{DDX} = 5 V)

2.1.2 Supply current characteristics

This section includes information about power supply current in various operating modes.

Table 3. Supply current characteristics

C	Parameter	Symbol	Core/Bus Freq	V_{DD} (V)	Typical[1]	Max	Unit	Temp
C	Run supply current, FEI mode, all clock gate is off, code run from flash	RI_{DD}	40/20 MHz	18	11.00	—	mA	-40 to 105 °C
C			20/10 MHz		7.50	—		
			20/1 MHz		6.00	—		
C			20/20 MHz	12	9.15	—		
C			20/10 MHz		7.50	—		
			20/1 MHz		5.95	—		
			20/20 MHz	5.3	9.10	—		
			20/10 MHz		7.45	—		
			20/1 MHz		5.90	—		
			20/20 MHz	4.5	9.35	—		
			20/10 MHz		7.65	—		
			20/1 MHz		6.15	—		

Table continues on the next page...

Table 3. Supply current characteristics (continued)

C	Parameter	Symbol	Core/Bus Freq	V_{DD} (V)	Typical[1]	Max	Unit	Temp
C			20/10 MHz		6.05	—		
			20/1 MHz		4.40	—		
C			20/20 MHz	12	7.70	—		
			20/10 MHz		6.00	—		
			20/1 MHz		4.40	—		
			20/20 MHz	5.3	7.65	—		
			20/10 MHz		5.95	—		
			20/1 MHz		4.35	—		
			20/20 MHz	4.5	7.85	—		
			20/10 MHz		6.20	—		
			20/1 MHz		4.60	—		
C	Stop mode supply current, no clocks active (except 20 kHz LPO clock)	SI_{DD}	—	18	19.85	—	µA	-40 to 105 °C
C				12	19.05	—		
C				5.3	18.25	—		
C				4.5	17.65	—		
C	ADC adder to Stop	—	—	18	88.80	—	µA	-40 to 105 °C
C	ADLPC = 1			12	87.95	—		
C	ADLSMP = 1			5.3	86.70	—		
C	ADCO = 1			4.5	85.40	—		

1. Data in Typical column was characterized at 25 °C or is typical recommended value.

2.1.3 EMC performance

Electromagnetic compatibility (EMC) performance is highly dependant on the environment in which the MCU resides. Board design and layout, circuit topology choices, location and characteristics of external components as well as MCU software operation all play a significant role in EMC performance. The system designer should consult Freescale applications notes such as AN2321, AN1050, AN1263, AN2764, and AN1259 for advice and guidance specifically targeted at optimizing EMC performance.

2.1.3.1 EMC radiated emissions operating behaviors

NOTE

If using external reset switch to design hardware board, connect two 0.1 µF decoupling capacitors on $\overline{\text{RESET}}$ pin for

Table 10. Flash characteristics (continued)

C	Characteristic	Symbol	Min[1]	Typical[2]	Max[3]	Unit[4]
D	Program Flash (2 word)	t_{PGM2}	0.12	0.13	0.31	ms
D	Program Flash (4 word)	t_{PGM4}	0.21	0.21	0.49	ms
D	Program Once	$t_{PGMONCE}$	0.20	0.21	0.21	ms
D	Erase All Blocks	t_{ERSALL}	95.42	100.18	100.30	ms
D	Erase Flash Block	t_{ERSBLK}	95.42	100.18	100.30	ms
D	Erase Flash Sector	t_{ERSPG}	19.10	20.05	20.09	ms
D	Unsecure Flash	t_{UNSECU}	95.42	100.19	100.31	ms
D	Verify Backdoor Access Key	t_{VFYKEY}	—	—	482	t_{cyc}
D	Set User Margin Level	t_{MLOADU}	—	—	415	t_{cyc}
C	FLASH Program/erase endurance T_L to T_H = -40 °C to 105 °C	n_{FLPE}	10 k	100 k	—	Cycles
C	Data retention at an average junction temperature of T_{Javg} = 85°C after up to 10,000 program/erase cycles	t_{D_ret}	15	100	—	years

1. Minimum times are based on maximum f_{NVMOP} and maximum f_{NVMBUS}
2. Typical times are based on typical f_{NVMOP} and maximum f_{NVMBUS}
3. Maximum times are based on typical f_{NVMOP} and typical f_{NVMBUS} plus aging
4. $t_{cyc} = 1 / f_{NVMBUS}$

Program and erase operations do not require any special power sources other than the normal V_{DDX} supply. For more detailed information about program/erase operations, see the Flash Memory Module section in the reference manual.

3.3 Analog

3.3.1 ADC characteristics

Table 11. 5 V 12-bit ADC operating conditions

Characteristic	Conditions	Symb	Min	Typ[1]	Max	Unit	Comment
Input voltage		V_{ADIN}	V_{REFL}	—	V_{REFH}	V	
Input capacitance		C_{ADIN}	—	4.5	5.5	pF	
Input resistance		R_{ADIN}	—	3	5	kΩ	—

Table continues on the next page...

Table 11. 5 V 12-bit ADC operating conditions (continued)

Characteristic	Conditions	Symb	Min	Typ[1]	Max	Unit	Comment
Analog source resistance	12-bit mode • f_{ADCK} > 4 MHz • f_{ADCK} < 4 MHz	R_{AS}	— —	— —	2 5	kΩ	External to MCU
	10-bit mode • f_{ADCK} > 4 MHz • f_{ADCK} < 4 MHz		— —	— —	5 10		
	8-bit mode (all valid f_{ADCK})		—	—	10		
ADC conversion clock frequency	High speed (ADLPC=0)	f_{ADCK}	0.4	—	8.0	MHz	—
	Low power (ADLPC=1)		0.4	—	4.0		

1. Typical values assume V_{DDA} = 5.0 V, Temp = 25°C, f_{ADCK}=1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

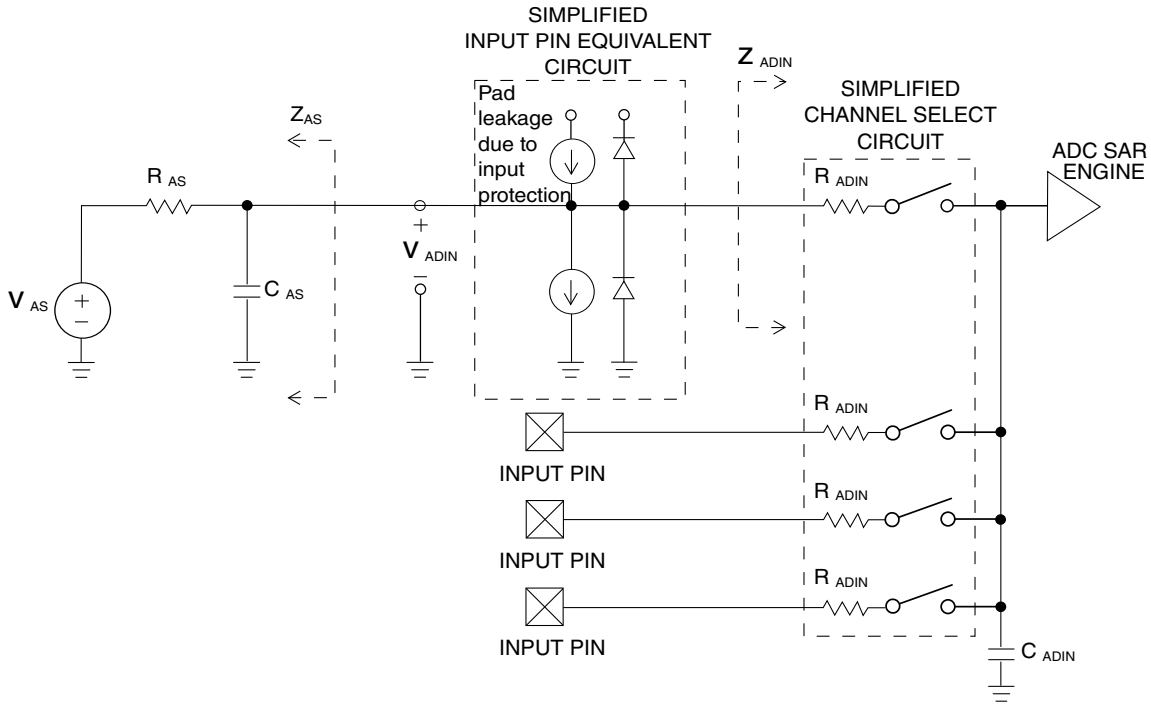


Figure 11. ADC input impedance equivalency diagram

Table 12. 12-bit ADC Characteristics (V_{REFH} = V_{DDA}, V_{REFL} = V_{SSA})

Characteristic	Conditions	C	Symb	Min	Typ[1]	Max	Unit
Supply current ADLPC = 1 ADLSMP = 1		T	I_{DDA}	—	133	—	µA

Table continues on the next page...

Table 12. 12-bit ADC Characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$) (continued)

Characteristic	Conditions	C	Symb	Min	Typ[1]	Max	Unit
ADCO = 1							
Supply current ADLPC = 1 ADLSMP = 0 ADCO = 1		T	I_{DDA}	—	218	—	µA
Supply current ADLPC = 0 ADLSMP = 1 ADCO = 1		T	I_{DDA}	—	327	—	µA
Supply current ADLPC = 0 ADLSMP = 0 ADCO = 1		T	I_{DDAD}	—	582	990	µA
Supply current	Stop, reset, module off	T	I_{DDA}	—	0.011	1	µA
ADC asynchronous clock source	High speed (ADLPC = 0)	T	f_{ADACK}	2	3.3	5	MHz
	Low power (ADLPC = 1)			1.25	2	3.3	
Conversion time (including sample time)	Short sample (ADLSMP = 0)	T	t_{ADC}	—	20	—	ADCK cycles
	Long sample (ADLSMP = 1)			—	40	—	
Sample time	Short sample (ADLSMP = 0)	T	t_{ADS}	—	3.5	—	ADCK cycles
	Long sample (ADLSMP = 1)			—	23.5	—	
Total unadjusted Error[2, 3]	12-bit mode	T	E_{TUE}	—	±5.5	—	LSB[4]
	10-bit mode	T		—	±1.7	±2.0	
	8-bit mode	T		—	±0.9	±1.0	
Differential Non-Linearity[3]	12-bit mode	T	DNL	—	1.4	—	LSB[4]
	10-bit mode[5]	P		—	0.5	—	
	8-bit mode[5]	T		—	0.15	—	
Integral Non-Linearity[3]	12-bit mode	T	INL	—	1.4	—	LSB[4]
	10-bit mode	T		—	0.5	—	
	8-bit mode	T		—	0.15	—	
Zero-scale error[6]	12-bit mode	C	E_{ZS}	—	±2.0	—	LSB[4]
	10-bit mode	T		—	±0.25	±1.0	
	8-bit mode	T		—	±0.65	±1.0	
Full-scale error[7]	12-bit mode	T	E_{FS}	—	±2.5	—	LSB[4]

Table continues on the next page...

Table 12. 12-bit ADC Characteristics (V_{REFH} = V_{DDA}, V_{REFL} = V_{SSA}) (continued)

Characteristic	Conditions	C	Symb	Min	Typ[1]	Max	Unit
	10-bit mode	T		—	±0.5	±1.0	
	8-bit mode	T		—	±0.5	±1.0	
Quantization error	≤12 bit modes	D	E_Q	—	—	±0.5	LSB[4]
Input leakage error[8]	all modes	D	E_{IL}	I_{In} * R_{AS}			mV
Temp sensor slope	-40°C– 25°C	D	m	—	3.266	—	mV/°C
	25°C– 125°C			—	3.638	—	
Temp sensor voltage	25°C	D	V_{TEMP25}	—	1.36	—	V

1. Typical values assume V_{DDX} = 5.0 V, V_{DD} ≥ 5.3 V, Temp = 25°C, f_{ADCK}=1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
2. Includes quantization.
3. To get better ADC performance: For the application case of V_{DD}<5.3 V, suggest to select V_{REFH} as ADC reference. For the application case VDD≥5.3 V, suggest to select V_{DDX} as ADC reference.
4. 1 LSB = (V_{REFH} - V_{REFL})/2^N
5. Monotonicity and no-missing-codes guaranteed in 10-bit and 8-bit modes
6. V_{ADIN} = V_{SSA}
7. V_{ADIN} = V_{DDA}
8. I_{In} = leakage current (refer to DC characteristics)

3.3.2 CMP and 6-bit DAC electrical specifications

Table 13. Comparator and 6-bit DAC electrical specifications

Symbol	Description		Min.	Typ.	Max.	Unit
V_{DDX}	Supply voltage		4.20	5.0	5.25	V
I_{DDHS}	Supply current, high-speed mode (EN=1, PMODE=1)		—	100	—	µA
I_{DDLS}	Supply current, low-speed mode (EN=1, PMODE=0)		—	18	20	µA
V_{AIN}	Analog input voltage		V_{SS} – 0.3	—	V_{DDX}	V
V_{AIO}	Analog input offset voltage		—	—	40	mV
V_H	Analog comparator hysteresis	CR0[HYSTCTR] = 0	—	15	20	mV
		CR0[HYSTCTR] = 1	—	20	30	mV
V_{CMPOh}	Output high		V_{DDX} – 0.5	—	—	V
V_{CMPOl}	Output low		—	—	0.5	V
I_{ALKG}	Analog input leakage current		—	—	20	nA
t_{DHS}	Propagation delay, high-speed mode (EN=1, PMODE=1)	200 mV delta voltage	—	70	120	ns
		100 mV delta voltage	—	100	150	ns
		50 mV delta voltage	—	200	250	ns
t_{DLS}	Propagation delay, low-speed mode (EN=1, PMODE=0)	200 mV delta voltage	—	400	600	ns
		100 mV delta voltage	—	600	800	ns

Table continues on the next page...

Table 14. GDU electrical specifications (continued)

Symbol	Description		Min.	Typ.	Max.	Unit	Note
		I_{Load}=15 mA	—	317	590	mV	
		I_{Load}=20 mA	—	330	600	mV	
	DC VOL for LS, V_{DDX}=5 V, V_{DD}=12 V	I_{Load}=5 mA	—	290	570	mV	
		I_{Load}=15 mA	—	320	580	mV	
		I_{Load}=20 mA	—	335	600	mV	
I_{OH}	V_{DDX}=5 V, V_{DD}=12 V, V_{Out}= V_{DD}-0.4V	DC IOH at lowest strength for HS	—	7.45	—	mA	
	V_{DDX}=5 V, V_{DD}=12 V, V_{Out}= V_{DDX}-0.4V	DC IOH at lowest strength for LS	—	7.45	—	mA	
I_{OL}	V_{DDX}=5 V, V_{DD}=12 V V_{Out}=V_{clamp}+0.4V	DC IOL at lowest strength for HS	—	6.45	—	mA	
	V_{DDX}=5 V, V_{DD}=12 V V_{Out}=V_{SS}+0.4V	DC IOL at lowest strength for LS	—	6.45	—	mA	
R_{pullup}	Pullup resistor of HS predriver, gate to source of PFET		192	226	260	kΩ	
$R_{pulldown}$	Pulldown resistor of LS predriver, gate to source of NFET		30	40	50	kΩ	
V_{clamp1}	V_{DD}-Vo_clamp in regulation mode with 5.5 V ≤ V_{DD} ≤ 18 V, loading current is less than 10 mA		4.5	5	5.5	V	
V_{clamp2}	V_{DD}-Vo_clamp in open loop mode with 4.5 V ≤ V_{DD} < 5.5 V, loading current is less than 10 mA		4.0	—	5	V	
I_{Load}	The sink current capability		—	—	10	mA	
	Line regulation, ΔV_{clamp} over ΔV_{DD}	4.5 V ≤ V_{DD}< 5.5 V[3]	—	1000	—	mV/V	
		5.5 V ≤ V_{DD}≤ 18 V	—	10	—	mV/V	
	Load regulation, ΔV_{clamp} over ΔI_{Load}	4.5 V ≤ V_{DD}< 5.5 V[3]	—	25	—	Ω	
		5.5 V ≤ V_{DD}≤ 18 V	—	1	—	Ω	
OVP_22V_a	22V over-voltage asserting threshold		21	22	23	V	
OVP_22V_d	22V over-voltage de-asserting threshold		19	20	21	V	
OVP_22V_h	22V over-voltage hysteresis		1.9	2	2.1	V	
OVP_24V_a	24V over-voltage asserting threshold		23	24	25	V	
OVP_24V_d	24V over-voltage de-asserting threshold		22	23	24	V	
OVP_24V_h	24V over-voltage hysteresis		0.9	1	1.1	V	

1. Customer need to add external resistor Rext1 for voltage divider. For example ,if Rext1=85 kΩ ,1/6 voltage divider; if Rext1=105 kΩ ,1/7 voltage divider.
2. PGA gain is default to 20X. User can cascade one external series resistor (Rext2) to reduce the PGA gain. To keep the current sensor PGA output without saturation distortion, the selected Rext2 must meet PGA output=V_{REF}+(R1/(R2+R_{ext2}))xV_{shunt}, V_{REF}=0.5xV_{DDX}, see reference manual for the R1 and R2.
3. This 5.5 V is a rough value, each part might has different value but around 5.5 V.

Table 15. GDU phase detector ACMP electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
V_{DDX}	Supply voltage	4.20	5.0	5.25	V
I_{DDHS}	Supply current, high-speed mode (EN=1, PMODE=1)	—	100	—	µA
I_{DDLS}	Supply current, low-speed mode (EN=1, PMODE=0)	—	18	20	µA
V_{AIN}	Analog input voltage	0	—	V_{DDX}-1	V
V_{AIO}	Analog input offset voltage	—	—	40	mV
V_H	Analog comparator hysteresis • CR0[HYSTCTR] = 0 • CR0[HYSTCTR] = 1	 — —	 15 20	 20 30	 mV mV
V_{CMPOh}	Output high	V_{DDX} – 0.5	—	—	V
V_{CMPOl}	Output low	—	—	0.5	V
I_{ALKG}	Analog input leakage current	—	—	20	nA
t_{DHS}	Propagation delay, high-speed mode (EN=1, PMODE=1), 200mV delta voltage	—	70	120	ns
t_{DLS}	Propagation delay, low-speed mode (EN=1, PMODE=0), 200mV delta voltage	—	400	600	ns
	Analog comparator initialization delay[1]	—	—	40	µs

1. Comparator initialization delay is defined as the time between software writes to change control inputs (Writes to DACEN, VRSEL, PSEL, MSEL, VOSEL) and the comparator output settling to a stable level.

Table 16. GDU over current protect ACMP electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
V_{DDX}	Supply voltage	4.20	5.0	5.25	V
I_{DDHS}	Supply current, high-speed mode (EN=1, PMODE=1)	—	100	—	µA
I_{DDLS}	Supply current, low-speed mode (EN=1, PMODE=0)	—	18	20	µA
V_{AIN}	Analog input voltage	V_{SS} – 0.3	—	V_{DDX}	V
V_{AIO}	Analog input offset voltage	—	20	40	mV
V_H	Analog comparator hysteresis • CR0[HYSTCTR] = 0 • CR0[HYSTCTR] = 1	 — —	 15 20	 20 30	 mV mV
V_{CMPOh}	Output high	V_{DDX} – 0.5	—	—	V
V_{CMPOl}	Output low	—	—	0.5	V
I_{ALKG}	Analog input leakage current	—	—	20	nA
t_{DHS}	Propagation delay, high-speed mode (EN=1, PMODE=1), 200mV delta voltage	—	70	120	ns
t_{DLS}	Propagation delay, low-speed mode (EN=1, PMODE=0), 200mV delta voltage[1]	—	400	600	ns
	Analog comparator initialization delay[2]	—	—	40	µs
INL	6-bit DAC integral non-linearity	–0.5	—	0.5	LSB[3]

Table continues on the next page...

Table 16. GDU over current protect ACMP electrical specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit
DNL	6-bit DAC differential non-linearity	–0.3	—	0.3	LSB

1. This ACMP is used for over-current protection, customer can use low power mode to avoid sparkles. Digital filter can produce max of 12.8 µs filter window.
2. Comparator initialization delay is defined as the time between software writes to change control inputs (Writes to DACEN, VRSEL, PSEL, MSEL, VOSEL) and the comparator output settling to a stable level.
3. 1 LSB = $V_{reference}/64$

3.4 Communication interfaces

3.4.1 Inter-Integrated Circuit Interface (I2C) timing

Table 17. I2C timing

Characteristic	Symbol	Standard Mode		Fast Mode		Unit
		Minimum	Maximum	Minimum	Maximum	
SCL Clock Frequency	f_{SCL}	0	100	0	400[1]	kHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated.	t_{HD}; STA	4	—	0.6	—	µs
LOW period of the SCL clock	t_{LOW}	4.7	—	1.3	—	µs
HIGH period of the SCL clock	t_{HIGH}	4	—	0.6	—	µs
Set-up time for a repeated START condition	t_{SU}; STA	4.7	—	0.6	—	µs
Data hold time for I^2C bus devices	t_{HD}; DAT	0[2]	3.45[3]	0[4]	0.9[2]	µs
Data set-up time	t_{SU}; DAT	250[5]	—	100[3, 6]	—	ns
Rise time of SDA and SCL signals	t_r	—	1000	20 +0.1C_b[7]	300	ns
Fall time of SDA and SCL signals	t_f	—	300	20 +0.1C_b[6]	300	ns
Set-up time for STOP condition	t_{SU}; STO	4	—	0.6	—	µs
Bus free time between STOP and START condition	t_{BUF}	4.7	—	1.3	—	µs
Pulse width of spikes that must be suppressed by the input filter	t_{SP}	N/A	N/A	0	50	ns

1. The maximum SCL Clock Frequency in Fast mode with maximum bus loading can only achieved when using the High drive pins (see DC characteristics) or when using the Normal drive pins and $V_{DDX} \geq 2.7$ V
2. The master mode I^2C deasserts ACK of an address byte simultaneously with the falling edge of SCL. If no slaves acknowledge this address byte, then a negative hold time can result, depending on the edge rates of the SDA and SCL lines.
3. The maximum tHD; DAT must be met only if the device does not stretch the LOW period (tLOW) of the SCL signal.
4. Input signal Slew = 10 ns and Output Load = 50 pF
5. Set-up time in slave-transmitter mode is 1 IPBus clock period, if the TX FIFO is empty.

6. A Fast mode I^2C bus device can be used in a Standard mode I2C bus system, but the requirement $t_{SU;\ DAT} \geq 250$ ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, then it must output the next data bit to the SDA line $t_{rmax} + t_{SU;\ DAT} = 1000 + 250 = 1250$ ns (according to the Standard mode I^2C bus specification) before the SCL line is released.
7. C_b = total capacitance of the one bus line in pF.

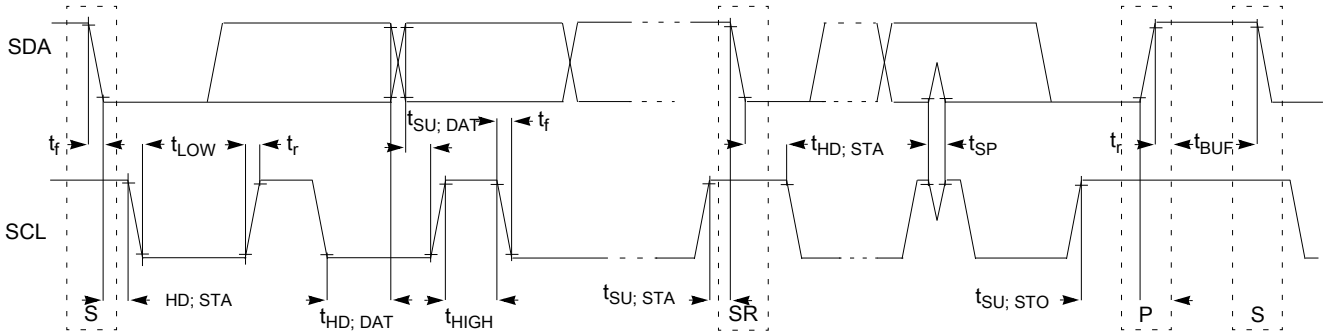


Figure 16. Timing definition for fast and standard mode devices on the I^2C bus

4 Dimensions

4.1 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to nxp.com and perform a keyword search for the drawing's document number:

If you want the drawing for this package	Then use this document number
24-pin QFN	98ASA00602D

5 Pinout

5.1 Signal multiplexing and pin assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The Port Control Module is responsible for selecting which ALT functionality is available on each pin.

24 QFN	Pin Name	Default/ALT0	ALT1	ALT2	ALT3
1	PTB5	PWM_WL			PTB5

24 QFN	Pin Name	Default/ALT0	ALT1	ALT2	ALT3
2	PWM_UH	PWM_UH			
3	PWM_VH	PWM_VH			
4	PWM_WH	PWM_WH			
5	VCLAMP	VCLAMP			
6	VDD	VDD			
7	VDDX	VDDX			
8	VSS	VSS			
9	PTB6/ RESET_b	RESET_b		TCLK	PTB6
10	PTC0	CMP_REF/ VREFH	PWM_FAULT0	CLK_IN	PTC0
11	PTB7/ BKGD/ MS	BKGD/ MS		CLKOUT	PTB7
12	PTA7	PWT1	TX	XB_OUT1	PTA7/ KBI7
13	PTA6	PWT0	RX	XB_IN1	PTA6/ KBI6
14	PTA5	TX	SDA	XB_OUT0	PTA5/ KBI5
15	PTA4	RX	SCL	XB_IN0	PTA4/ KBI4
16	PTA3	AMP1_M/ ADC1AD1	CLKOUT	XB_OUT1	PTA3/ KBI3
17	PTA2	AMP1_P/ CMP2/ ADC1AD0	XB_IN1	XB_OUT0	PTA2/ KBI2
18	PTA1	AMP0_M/ CMP1/ ADC0AD1	XB_OUT0	XB_IN1	PTA1/ KBI1
19	PTA0	AMP0_P/ CMP0/ ADC0AD0	CLK_IN	XB_IN0	PTA0/ KBI0
20	PTB0	GDU_CMP0/ ADC0AD2/ ADC1AD2			PTB0
21	PTB1	GDU_CMP1/ ADC0AD3/ ADC1AD3			PTB1
22	PTB2	GDU_CMP2/ ADC0AD4/ ADC1AD4			PTB2
23	PTB3	PWM_UL			PTB3
24	PTB4	PWM_VL			PTB4

5.2 Pinout

The following figures show the pinout diagrams for the devices supported by this document. Many signals may be multiplexed onto a single pin. To determine what signals can be used on which pin, see Signal multiplexing and pin assignments.

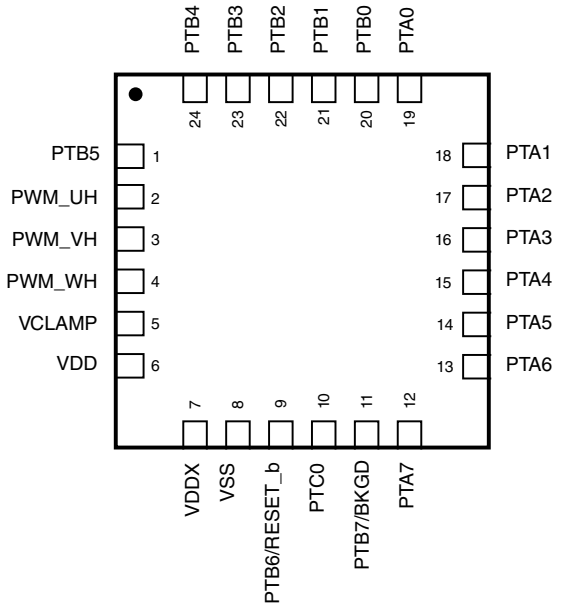


Figure 17. 24-pin QFN pinout diagram

6 Part identification

6.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

7.1.1 Example

This is an example of an operating requirement:

Symbol	Description	Min.	Max.	Unit
V_{DD}	1.0 V core supply voltage	0.9	1.1	V

7.2 Definition: Operating behavior

Unless otherwise specified, an *operating behavior* is a specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions.

7.2.1 Example

This is an example of an operating behavior:

Symbol	Description	Min.	Max.	Unit
I_{WP}	Digital I/O weak pullup/ pulldown current	10	130	µA

7.3 Definition: Attribute

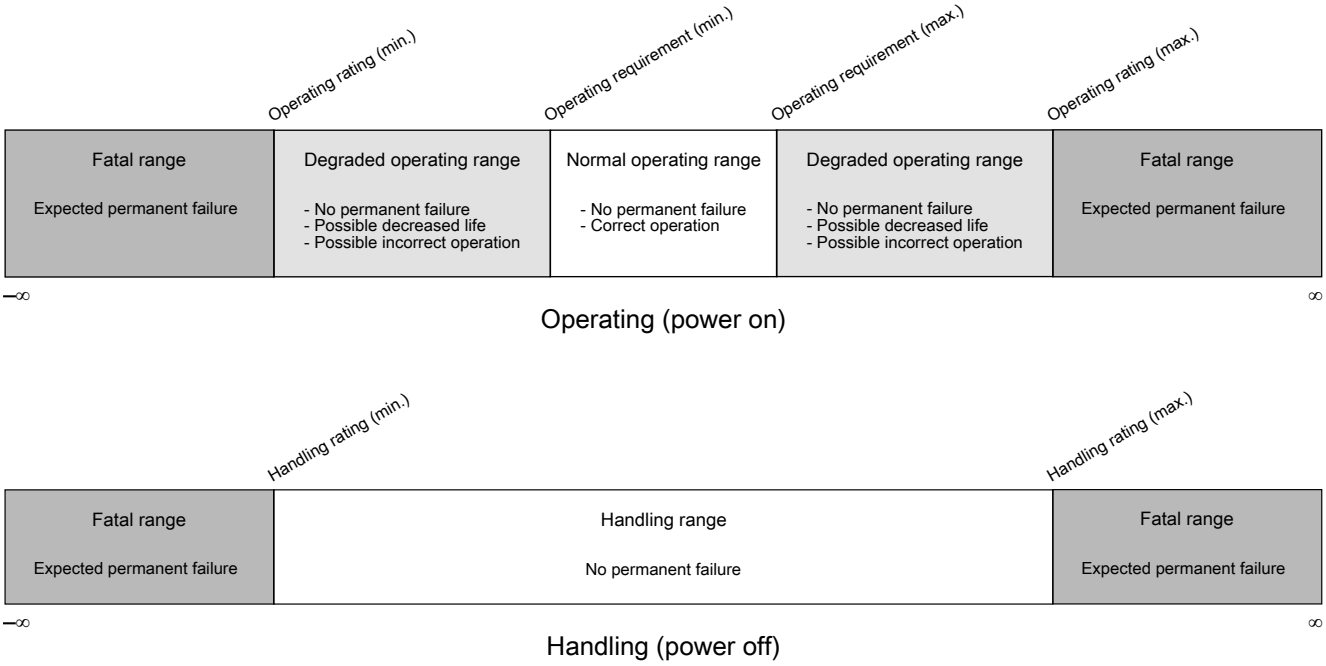
An *attribute* is a specified value or range of values for a technical characteristic that are guaranteed, regardless of whether you meet the operating requirements.

7.3.1 Example

This is an example of an attribute:

Symbol	Description	Min.	Max.	Unit
CIN_D	Input capacitance: digital pins	—	7	pF

7.6 Relationship between ratings and operating requirements



7.7 Guidelines for ratings and operating requirements

Follow these guidelines for ratings and operating requirements:

- Never exceed any of the chip's ratings.
- During normal operation, don't exceed any of the chip's operating requirements.
- If you must exceed an operating requirement at times other than during normal operation (for example, during power sequencing), limit the duration as much as possible.

7.8 Definition: Typical value

A *typical value* is a specified value for a technical characteristic that:

- Lies within the range of values specified by the operating behavior
- Given the typical manufacturing process, is representative of that characteristic during operation when you meet the typical-value conditions or other specified conditions

Typical values are provided as design guidelines and are neither tested nor guaranteed.

Table 18. Typical value conditions

Symbol	Description	Value	Unit
T_A	Ambient temperature	25	°C
V_{DD}	3.3 V supply voltage	3.3	V

7.10 Parameter Classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding, the following classification is used and the parameters are tagged accordingly in the tables where appropriate:

Table 19. Parameter Classifications

P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

NOTE

The classification is shown in the column labeled “C” in the parameter tables where appropriate.

8 Revision history

The following table provides a revision history for this document.

Table 20. Revision history

Rev. No.	Date	Substantial Changes
1	09/2016	• Initial public release.
2	11/2016	• Added MC9S08SU8VFK part.