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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	S08
Core Size	8-Bit
Speed	40MHz
Connectivity	I²C, SCI
Peripherals	PWM, WDT
Number of I/O	17
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 18V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	24-UFQFN Exposed Pad
Supplier Device Package	24-QFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc9s08su8vfk

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1.4 Voltage and current operating ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maximum is not guaranteed. Stress beyond the limits specified in below table may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this document.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, either V_{SS} or V_{DDX}) or the programmable pullup resistor associated with the pin is enabled.

Symbol	Description	Min.	Max.	Unit
V_{DD}	Supply voltage	4.5	18	V
V_{DDX}	Supply voltage to digital I/O drivers[1]	4.20	5.25	V
I_{DDX}	Maximum current into V_{DDX}	—	50	mA
V_{DIO}	Digital input voltage (except $\overline{\text{RESET}}$ or true open drain pin PTA4 and PTA5)	-0.3	V_{DDX}+0.3	V
	Digital input voltage (true open drain pin PTA4 and PTA5)	-0.3	V_{DDX}+0.3	V
V_{AIO}	Analog[2], $\overline{\text{RESET}}$ input voltage	-0.3	V_{DDX}+0.3	V
I_D	Instantaneous maximum current single pin limit (applies to all port pins)	-25	25	mA

1. See Table 2 for detail.
2. All digital I/O pins, except open-drain pin PTA4 and PTA5, are internally clamped to V_{SS} and V_{DDX}. PTA4 and PTA5 is only clamped to V_{SS}.

Table 2. Power supply electrical characteristics (continued)

Symbol	Description		Min.	Typical [1]	Max.	Unit
V_{LVWA}	V_{DDX} Low voltage warning assert level	PMC_LVCTLSTAT1[SLVWSEL] = 1b	3.43	3.63	3.83	V
		PMC_LVCTLSTAT1[SLVWSEL] = 0b	3.94	4.14	4.34	
V_{LVWD}	V_{DDX} Low voltage warning deassert level	PMC_LVCTLSTAT1[SLVWSEL] = 1b	3.54	3.74	3.94	V
		PMC_LVCTLSTAT1[SLVWSEL] = 0b	4.08	4.28	4.48	
V_{LVRA}	V_{DDX} low voltage reset assert		2.97	3.02	—	V
V_{LVRD}	V_{DDX} low voltage reset deassertl		—	—	3.13	V
$V_{LVWREFHA}$	Low voltage warning for V_{REFH} assert level[4]	PMC_VREFHLVW[LVWCFG]=00b	3.34	3.54	3.74	V
		PMC_VREFHLVW[LVWCFG]=01b	3.43	3.63	3.83	V
		PMC_VREFHLVW[LVWCFG]=10b	3.86	4.06	4.26	V
		PMC_VREFHLVW[LVWCFG]=11b	4.11	4.31	4.51	V
$V_{LVWREFHA}$	Low voltage warning for V_{REFH} deassert level[4]	PMC_VREFHLVW[LVWCFG]=00b	3.45	3.65	3.85	V
		PMC_VREFHLVW[LVWCFG]=01b	3.55	3.75	3.95	V
		PMC_VREFHLVW[LVWCFG]=10b	4.00	4.20	4.40	V
		PMC_VREFHLVW[LVWCFG]=11b	4.27	4.47	4.67	V
f_{LPOCLK}	Trimmed LPOCLK output frequency		—	20	—	kHz
df_{LPOCLK}	Trimmed LPOCLK internal clock Δf / $f_{NOMINAL}$[5]		-5	—	5	%
t_{SDEL}	LPOCLK start up delay		—	25	50	µs
dV_{HT}	Temperature sensor slope		—	5.07	—	mV/°C
V_{HT}	Temperature sensor output voltage		—	1.73	—	V
T_{HTIA}	High temperature interrupt assert[6]		110	130	150	°C
T_{HTID}	High temperature interrupt deassert[6]		100	120	140	°C
V_{BG}	Bandgap output voltage		1.13	1.2	1.32	V
V_{HCBG}	HC Bandgap output voltage		1.14	1.15	1.16	V
t_{STP_REC}	Recovery time from Stop	not including V_{REFH}	—	15	—	µs
		including V_{REFH}	—	1	—	ms

1. Typical values are measured at 25 °C.
2. Power supply enters reduced power mode when MCU is in Stop mode.
3. This typical value is configurable based on V_{REC}.
4. PMC_VREFHLVW[LVWCFG]=01b is recommended for the configuration.
5. User need to trim the LPOCLK in order to get ±5% LPOCLK
6. This is junction temperature.

Figure 2 illustrates the power distribution of this chip.

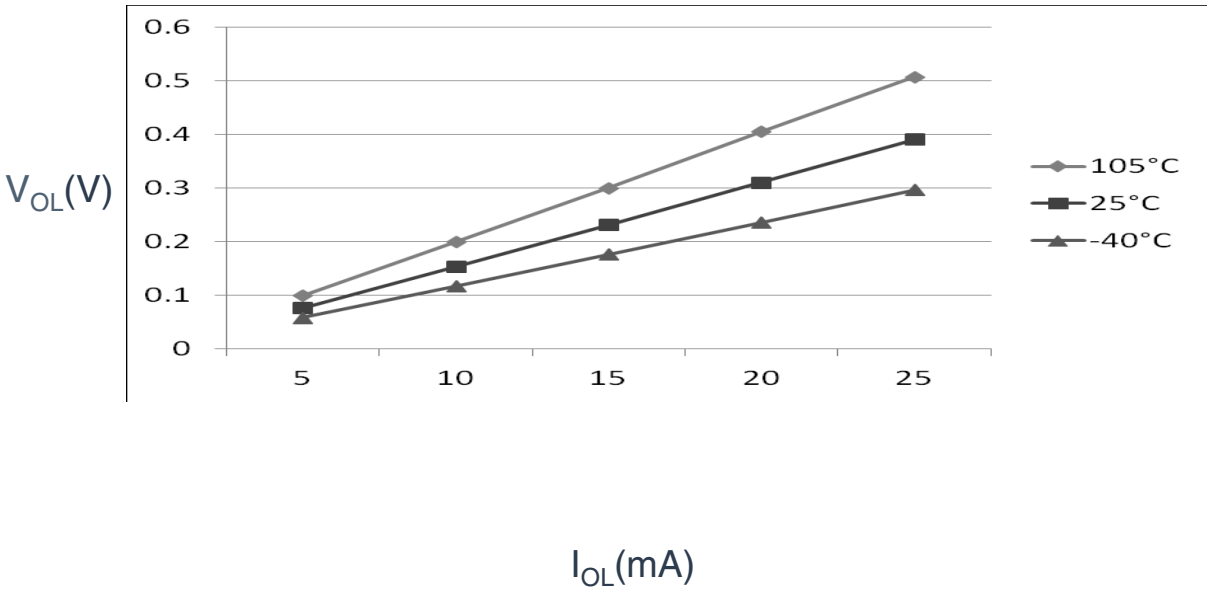


Figure 6. Typical I_{OL} Vs. V_{OL} (high drive strength) (V_{DDX} = 5 V)

2.1.2 Supply current characteristics

This section includes information about power supply current in various operating modes.

Table 3. Supply current characteristics

C	Parameter	Symbol	Core/Bus Freq	V_{DD} (V)	Typical[1]	Max	Unit	Temp
C	Run supply current, FEI mode, all clock gate is off, code run from flash	RI_{DD}	40/20 MHz	18	11.00	—	mA	-40 to 105 °C
C			20/10 MHz		7.50	—		
			20/1 MHz		6.00	—		
C			20/20 MHz	12	9.15	—		
C			20/10 MHz		7.50	—		
			20/1 MHz		5.95	—		
			20/20 MHz	5.3	9.10	—		
			20/10 MHz		7.45	—		
			20/1 MHz		5.90	—		
			20/20 MHz	4.5	9.35	—		
			20/10 MHz		7.65	—		
			20/1 MHz		6.15	—		

Table continues on the next page...

Table 3. Supply current characteristics (continued)

C	Parameter	Symbol	Core/Bus Freq	V_{DD} (V)	Typical[1]	Max	Unit	Temp
C	Run supply current, FEI mode, all clock gate is on, code run from flash	RI_{DD}	40/20 MHz	18	13.05	—	mA	-40 to 105 °C
C			20/10 MHz		8.45	—		
			20/1 MHz		6.05	—		
C			20/20 MHz	12	11.00	—		
C			20/10 MHz		8.40	—		
			20/1 MHz		6.00	—		
			20/20 MHz	5.3	10.95	—		
			20/10 MHz		8.35	—		
			20/1 MHz		6.00	—		
			20/20 MHz	4.5	11.20	—		
			20/10 MHz		8.60	—		
			20/1 MHz		6.20	—		
C	Run supply current, FBE mode, all clock gate is off, code run from SRAM	RI_{DD}	40/20 MHz	18	9.60	—	mA	-40 to 105 °C
C			20/10 MHz		6.05	—		
			20/1 MHz		4.50	—		
C			20/20 MHz	12	7.80	—		
C			20/10 MHz		6.05	—		
			20/1 MHz		4.45	—		
			20/20 MHz	5.3	7.75	—		
			20/10 MHz		6.00	—		
			20/1 MHz		4.40	—		
			20/20 MHz	4.5	7.90	—		
			20/10 MHz		6.20	—		
			20/1 MHz		4.60	—		
C	Run supply current, FBE mode, all clock gate is on, code run from SRAM	RI_{DD}	40/20 MHz	18	11.65	—	mA	-40 to 105 °C
C			20/10 MHz		7.00	—		
			20/1 MHz		4.60	—		
C			20/20 MHz	12	9.60	—		
C			20/10 MHz		6.95	—		
			20/1 MHz		4.55	—		
			20/20 MHz	5.3	9.60	—		
			20/10 MHz		6.90	—		
			20/1 MHz		4.50	—		
			20/20 MHz	4.5	9.75	—		
			20/10 MHz		7.10	—		
			20/1 MHz		4.70	—		
C	Wait mode current, FEI mode, all clock gate is on	WI_{DD}	40/20 MHz	18	7.80	—	mA	-40 to 105 °C

Table continues on the next page...

Table 3. Supply current characteristics (continued)

C	Parameter	Symbol	Core/Bus Freq	V_{DD} (V)	Typical[1]	Max	Unit	Temp
C			20/10 MHz		6.05	—		
			20/1 MHz		4.40	—		
C			20/20 MHz	12	7.70	—		
			20/10 MHz		6.00	—		
			20/1 MHz		4.40	—		
			20/20 MHz	5.3	7.65	—		
			20/10 MHz		5.95	—		
			20/1 MHz		4.35	—		
			20/20 MHz	4.5	7.85	—		
			20/10 MHz		6.20	—		
			20/1 MHz		4.60	—		
C	Stop mode supply current, no clocks active (except 20 kHz LPO clock)	SI_{DD}	—	18	19.85	—	µA	-40 to 105 °C
C				12	19.05	—		
C				5.3	18.25	—		
C				4.5	17.65	—		
C	ADC adder to Stop	—	—	18	88.80	—	µA	-40 to 105 °C
C	ADLPC = 1			12	87.95	—		
C	ADLSMP = 1			5.3	86.70	—		
C	ADCO = 1			4.5	85.40	—		

1. Data in Typical column was characterized at 25 °C or is typical recommended value.

2.1.3 EMC performance

Electromagnetic compatibility (EMC) performance is highly dependant on the environment in which the MCU resides. Board design and layout, circuit topology choices, location and characteristics of external components as well as MCU software operation all play a significant role in EMC performance. The system designer should consult Freescale applications notes such as AN2321, AN1050, AN1263, AN2764, and AN1259 for advice and guidance specifically targeted at optimizing EMC performance.

2.1.3.1 EMC radiated emissions operating behaviors

NOTE

If using external reset switch to design hardware board, connect two 0.1 µF decoupling capacitors on $\overline{\text{RESET}}$ pin for

Table 5. Control timing (continued)

C	Rating		Symbol	Min	Typical[1]	Max	Unit
C	Port rise and fall time - Normal drive strength (HDRVE_PTXx = 0) (load = 50 pF)[5]	—	t_{Rise}	—	10.2	—	ns
C			t_{Fall}	—	9.5	—	ns
C	Port rise and fall time - Extreme high drive strength (HDRVE_PTXx = 1) (load = 50 pF)[5]	—	t_{Rise}	—	5.4	—	ns
C			t_{Fall}	—	4.6	—	ns

1. Typical values are based on characterization data at V_{DDX} = 5.0 V, 25 °C unless otherwise stated.
2. This is the shortest pulse that is guaranteed to be recognized as a reset pin request.
3. To enter BDM mode following a POR, BKGD/MS must be held low during the powerup and for a hold time of t_{MSH} after V_{DDX} rises above V_{LVD}.
4. This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In stop mode, the synchronizer is bypassed so shorter pulses can be recognized.
5. Timing is shown with respect to 20% V_{DDX} and 80% V_{DDX} levels. Temperature range -40 °C to 105 °C.

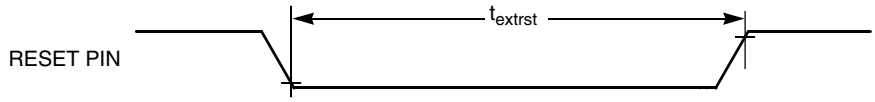


Figure 7. Reset timing

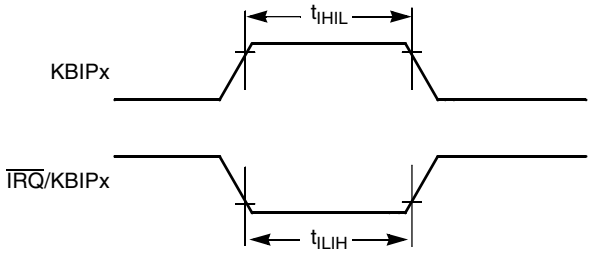


Figure 8. IRQ/KBIPx timing

2.2.2 FTM module timing

Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the timer counter. These synchronizers operate from the current bus rate clock.

Table 6. FTM input timing

No.	C	Function	Symbol	Min	Max	Unit
1	D	External clock frequency	f_{TCLK}	0	$f_{Bus}/4$	Hz
2	D	External clock period	t_{TCLK}	4	—	t_{cyc}

Table continues on the next page...

2.3.2 Thermal characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and voltage regulator circuits, and it is user-determined rather than being controlled by the MCU design. To take $P_{I/O}$ into account in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DDX} and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and V_{SS} or V_{DDX} will be very small.

Table 8. Thermal attributes

Board type	Symbol	Description	24-pin QFN	Unit	Notes
Single-layer (1S)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	114	°C/W	1, 2
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	42	°C/W	1, 3
Single-layer (1S)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	96	°C/W	1, 3
Four-layer (2s2p)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	36	°C/W	1, 3
—	$R_{\theta JB}$	Thermal resistance, junction to board	19	°C/W	4
—	$R_{\theta JC}$	Thermal resistance, junction to case	3.4	°C/W	5
—	Ψ_{JT}	Thermal characterization parameter, junction to package top outside center (natural convection)	15	°C/W	6

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-2 with the single layer board (JESD51-3) horizontal.
3. Per JEDEC JESD51-6 with the board (JESD51-7) horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the solder pad on the bottom of the package. Interface resistance is ignored.
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization.

3 Peripheral operating requirements and behaviors

3.1 ICS characteristics

Table 9. ICS specifications (temperature range = -40 to 105 °C ambient)

C	Characteristic		Symbol	Min	Typical[1]	Max	Unit
T	Internal reference start-up time		t_{IRST}	—	20	50	µs
D	Square wave input clock frequency	FEE or FBE mode[2]	f_{extal}	0.03125	—	5	MHz
D		FBELP mode		0	—	40	MHz
P	Average internal reference frequency - trimmed		f_{int_t}	—	39.0625	—	kHz
P	DCO output frequency range - trimmed		f_{dco_t}	16	—	40	MHz
P	Total deviation of DCO output from trimmed frequency[3]	Over full voltage and temperature range	Δf_{dco_t}	—	—	±2.0	$\%f_{dco}$
C		Over fixed voltage and temperature range of 0 to 70 °C				±1.0	
C	FLL acquisition time[3, 4]		$t_{Acquire}$	—	—	2	ms
C	Long term jitter of DCO output clock (averaged over 2 ms interval)[5]		C_{Jitter}	—	0.02	0.2	$\%f_{dco}$

1. Data in Typical column was characterized at V_{DDX} = 5.0 V, 25 °C or is typical recommended value.
2. When ICS is configured for FEE or FBE mode, input clock source must be divisible using RDIV to within the range of 31.25 kHz to 39.0625 kHz.
3. This parameter is characterized and not tested on each device.
4. This specification applies to any time the FLL reference source or reference divider is changed, trim value changed, DMX32 bit is changed, DRS bit is changed, or changing from FLL disabled (FBELP, FBILP) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.
5. Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{Bus}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FLL circuitry via V_{DDX} and V_{SS} and variation in crystal oscillator frequency increase the C_{Jitter} percentage for a given interval.

3.2 NVM specifications

This section provides details about program/erase times and program/erase endurance for the flash memories.

Table 10. Flash characteristics

C	Characteristic	Symbol	Min[1]	Typical[2]	Max[3]	Unit[4]
D	NVM Bus frequency	f_{NVMBUS}	1	—	20	MHz
D	NVM Operating frequency	f_{NVMOP}	0.8	1	1.05	MHz
D	Erase Verify All Blocks	t_{VFYALL}	—	—	2605	t_{cyc}
D	Erase Verify Flash Block	t_{RD1BLK}	—	—	2579	t_{cyc}
D	Erase Verify Flash Section	t_{RD1SEC}	—	—	485	t_{cyc}
D	Read Once	t_{RDONCE}	—	—	464	t_{cyc}

Table continues on the next page...

Table 11. 5 V 12-bit ADC operating conditions (continued)

Characteristic	Conditions	Symb	Min	Typ[1]	Max	Unit	Comment
Analog source resistance	12-bit mode • f_{ADCK} > 4 MHz • f_{ADCK} < 4 MHz	R_{AS}	— —	— —	2 5	kΩ	External to MCU
	10-bit mode • f_{ADCK} > 4 MHz • f_{ADCK} < 4 MHz		— —	— —	5 10		
	8-bit mode (all valid f_{ADCK})		—	—	10		
ADC conversion clock frequency	High speed (ADLPC=0)	f_{ADCK}	0.4	—	8.0	MHz	—
	Low power (ADLPC=1)		0.4	—	4.0		

1. Typical values assume V_{DDA} = 5.0 V, Temp = 25°C, f_{ADCK}=1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

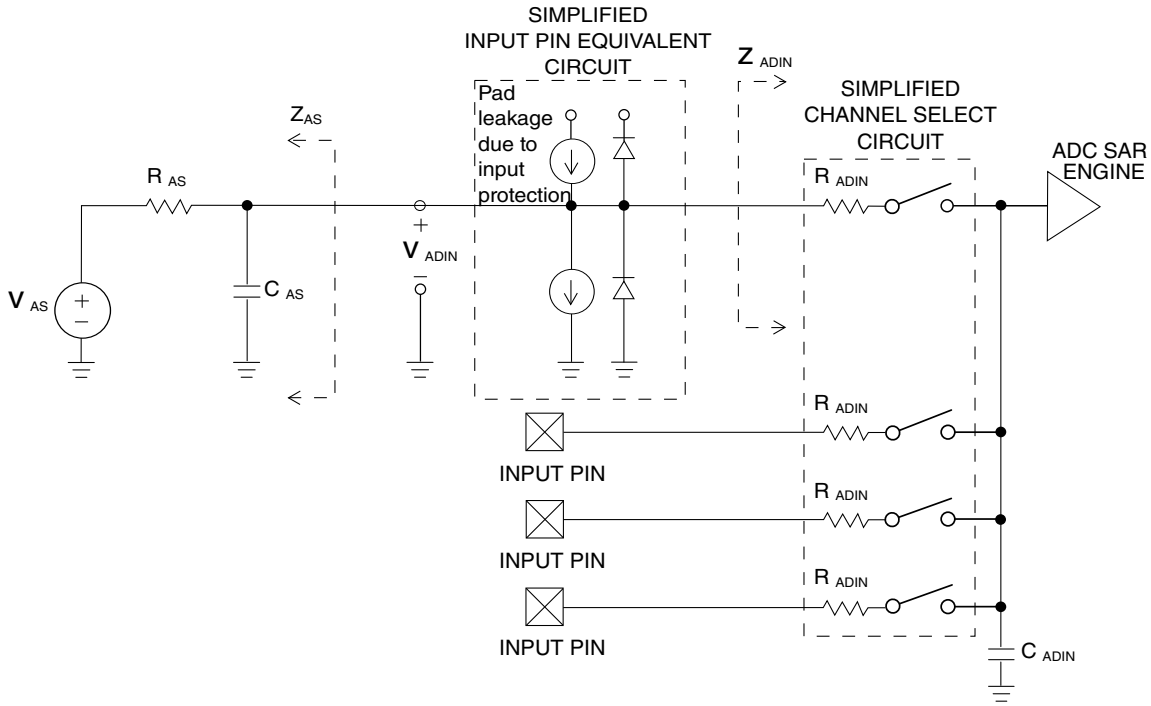


Figure 11. ADC input impedance equivalency diagram

Table 12. 12-bit ADC Characteristics (V_{REFH} = V_{DDA}, V_{REFL} = V_{SSA})

Characteristic	Conditions	C	Symb	Min	Typ[1]	Max	Unit
Supply current ADLPC = 1 ADLSMP = 1		T	I_{DDA}	—	133	—	µA

Table continues on the next page...

Table 12. 12-bit ADC Characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$) (continued)

Characteristic	Conditions	C	Symb	Min	Typ[1]	Max	Unit
ADCO = 1							
Supply current ADLPC = 1 ADLSMP = 0 ADCO = 1		T	I_{DDA}	—	218	—	µA
Supply current ADLPC = 0 ADLSMP = 1 ADCO = 1		T	I_{DDA}	—	327	—	µA
Supply current ADLPC = 0 ADLSMP = 0 ADCO = 1		T	I_{DDAD}	—	582	990	µA
Supply current	Stop, reset, module off	T	I_{DDA}	—	0.011	1	µA
ADC asynchronous clock source	High speed (ADLPC = 0)	T	f_{ADACK}	2	3.3	5	MHz
	Low power (ADLPC = 1)			1.25	2	3.3	
Conversion time (including sample time)	Short sample (ADLSMP = 0)	T	t_{ADC}	—	20	—	ADCK cycles
	Long sample (ADLSMP = 1)			—	40	—	
Sample time	Short sample (ADLSMP = 0)	T	t_{ADS}	—	3.5	—	ADCK cycles
	Long sample (ADLSMP = 1)			—	23.5	—	
Total unadjusted Error[2, 3]	12-bit mode	T	E_{TUE}	—	±5.5	—	LSB[4]
	10-bit mode	T		—	±1.7	±2.0	
	8-bit mode	T		—	±0.9	±1.0	
Differential Non-Linearity[3]	12-bit mode	T	DNL	—	1.4	—	LSB[4]
	10-bit mode[5]	P		—	0.5	—	
	8-bit mode[5]	T		—	0.15	—	
Integral Non-Linearity[3]	12-bit mode	T	INL	—	1.4	—	LSB[4]
	10-bit mode	T		—	0.5	—	
	8-bit mode	T		—	0.15	—	
Zero-scale error[6]	12-bit mode	C	E_{ZS}	—	±2.0	—	LSB[4]
	10-bit mode	T		—	±0.25	±1.0	
	8-bit mode	T		—	±0.65	±1.0	
Full-scale error[7]	12-bit mode	T	E_{FS}	—	±2.5	—	LSB[4]

Table continues on the next page...

Table 12. 12-bit ADC Characteristics (V_{REFH} = V_{DDA}, V_{REFL} = V_{SSA}) (continued)

Characteristic	Conditions	C	Symb	Min	Typ[1]	Max	Unit
	10-bit mode	T		—	±0.5	±1.0	
	8-bit mode	T		—	±0.5	±1.0	
Quantization error	≤12 bit modes	D	E_Q	—	—	±0.5	LSB[4]
Input leakage error[8]	all modes	D	E_{IL}	I_{In} * R_{AS}			mV
Temp sensor slope	-40°C– 25°C	D	m	—	3.266	—	mV/°C
	25°C– 125°C			—	3.638	—	
Temp sensor voltage	25°C	D	V_{TEMP25}	—	1.36	—	V

1. Typical values assume V_{DDX} = 5.0 V, V_{DD} ≥ 5.3 V, Temp = 25°C, f_{ADCK}=1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
2. Includes quantization.
3. To get better ADC performance: For the application case of V_{DD}<5.3 V, suggest to select V_{REFH} as ADC reference. For the application case VDD≥5.3 V, suggest to select V_{DDX} as ADC reference.
4. 1 LSB = (V_{REFH} - V_{REFL})/2^N
5. Monotonicity and no-missing-codes guaranteed in 10-bit and 8-bit modes
6. V_{ADIN} = V_{SSA}
7. V_{ADIN} = V_{DDA}
8. I_{In} = leakage current (refer to DC characteristics)

3.3.2 CMP and 6-bit DAC electrical specifications

Table 13. Comparator and 6-bit DAC electrical specifications

Symbol	Description		Min.	Typ.	Max.	Unit
V_{DDX}	Supply voltage		4.20	5.0	5.25	V
I_{DDHS}	Supply current, high-speed mode (EN=1, PMODE=1)		—	100	—	µA
I_{DDLS}	Supply current, low-speed mode (EN=1, PMODE=0)		—	18	20	µA
V_{AIN}	Analog input voltage		V_{SS} – 0.3	—	V_{DDX}	V
V_{AIO}	Analog input offset voltage		—	—	40	mV
V_H	Analog comparator hysteresis	CR0[HYSTCTR] = 0	—	15	20	mV
		CR0[HYSTCTR] = 1	—	20	30	mV
V_{CMPOh}	Output high		V_{DDX} – 0.5	—	—	V
V_{CMPOl}	Output low		—	—	0.5	V
I_{ALKG}	Analog input leakage current		—	—	20	nA
t_{DHS}	Propagation delay, high-speed mode (EN=1, PMODE=1)	200 mV delta voltage	—	70	120	ns
		100 mV delta voltage	—	100	150	ns
		50 mV delta voltage	—	200	250	ns
t_{DLS}	Propagation delay, low-speed mode (EN=1, PMODE=0)	200 mV delta voltage	—	400	600	ns
		100 mV delta voltage	—	600	800	ns

Table continues on the next page...

Table 13. Comparator and 6-bit DAC electrical specifications (continued)

Symbol	Description		Min.	Typ.	Max.	Unit
		50 mV delta voltage	—	1000	1500	ns
	Analog comparator initialization delay[1]		—	—	40	µs
I_{DAC6b}	6-bit DAC current adder (enabled)		—	7	—	µA
INL	6-bit DAC integral non-linearity		–0.5	—	0.5	LSB[2]
DNL	6-bit DAC differential non-linearity		–0.3	—	0.3	LSB

1. Comparator initialization delay is defined as the time between software writes to change control inputs (Writes to DACEN, VRSEL, PSEL, MSEL, VOSEL) and the comparator output settling to a stable level.
2. 1 LSB = $V_{reference}/64$

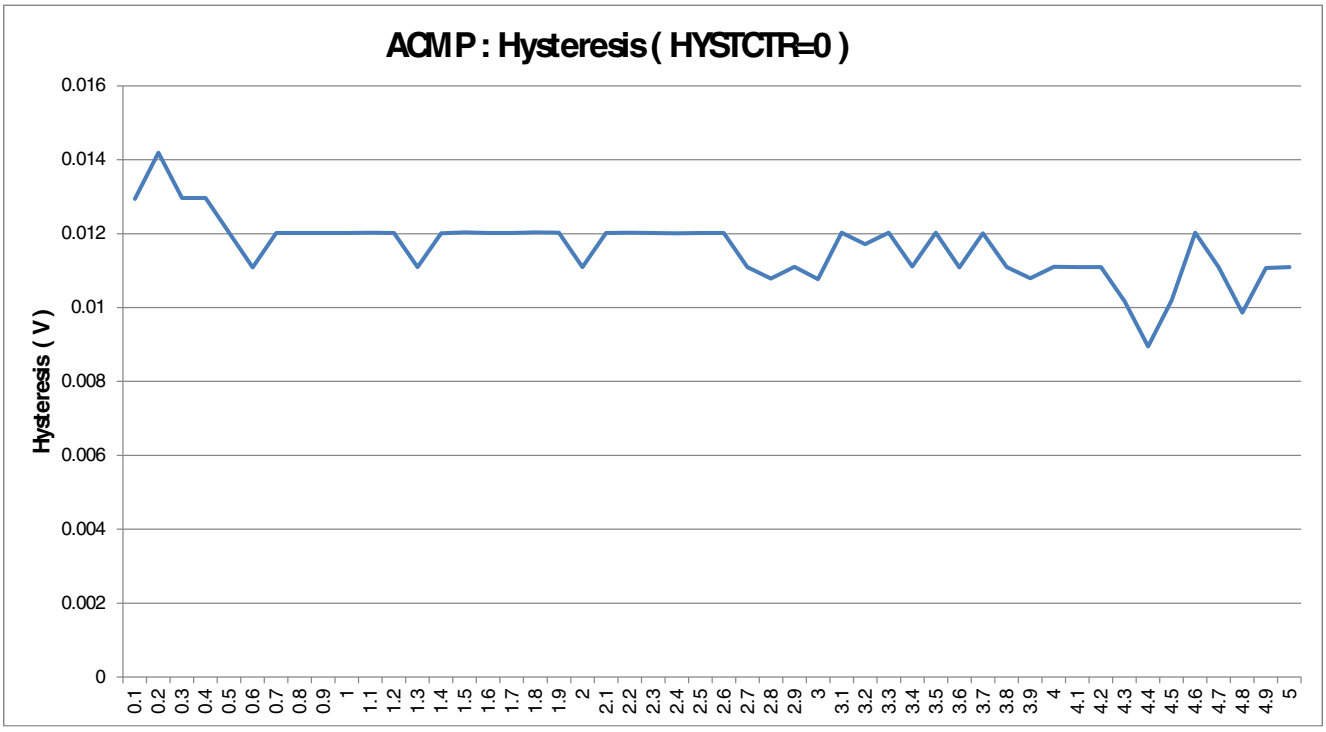


Figure 12. Typical hysteresis vs. Vin level (V_{DDX} = 5.0 V, PMODE = 0)

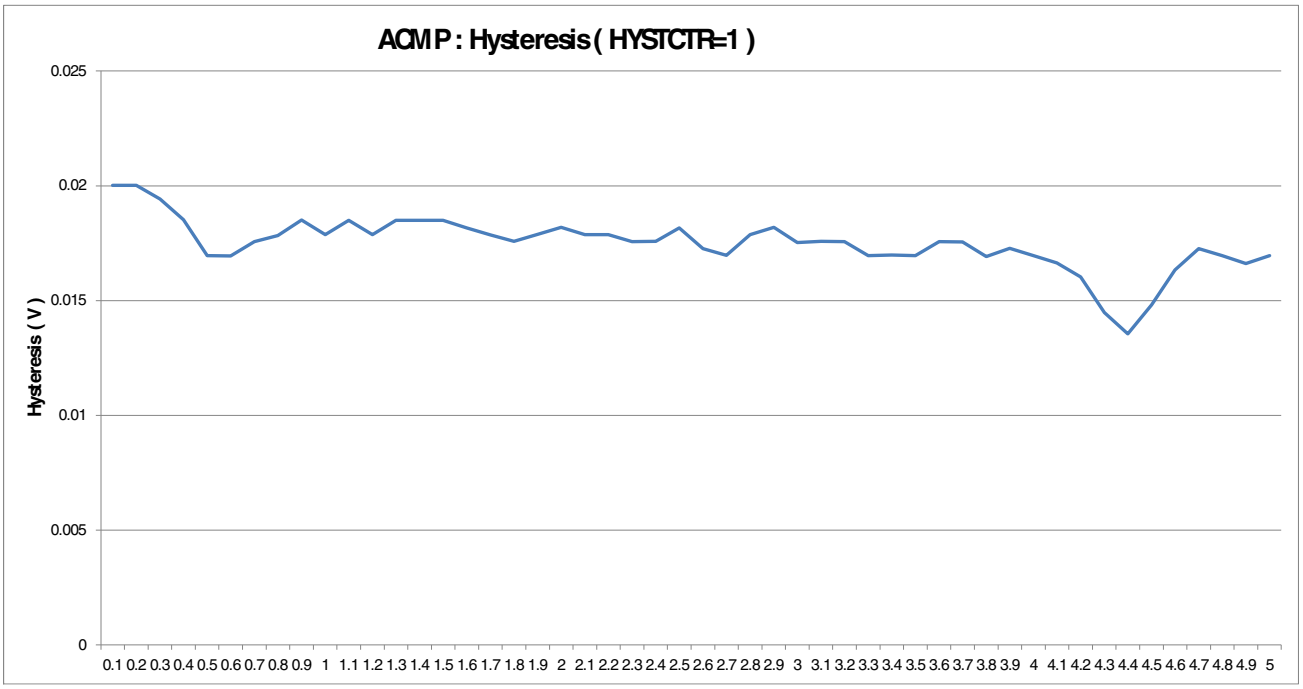


Figure 13. Typical hysteresis vs. Vin level (V_{DDX} = 5.0 V, PMODE = 1)

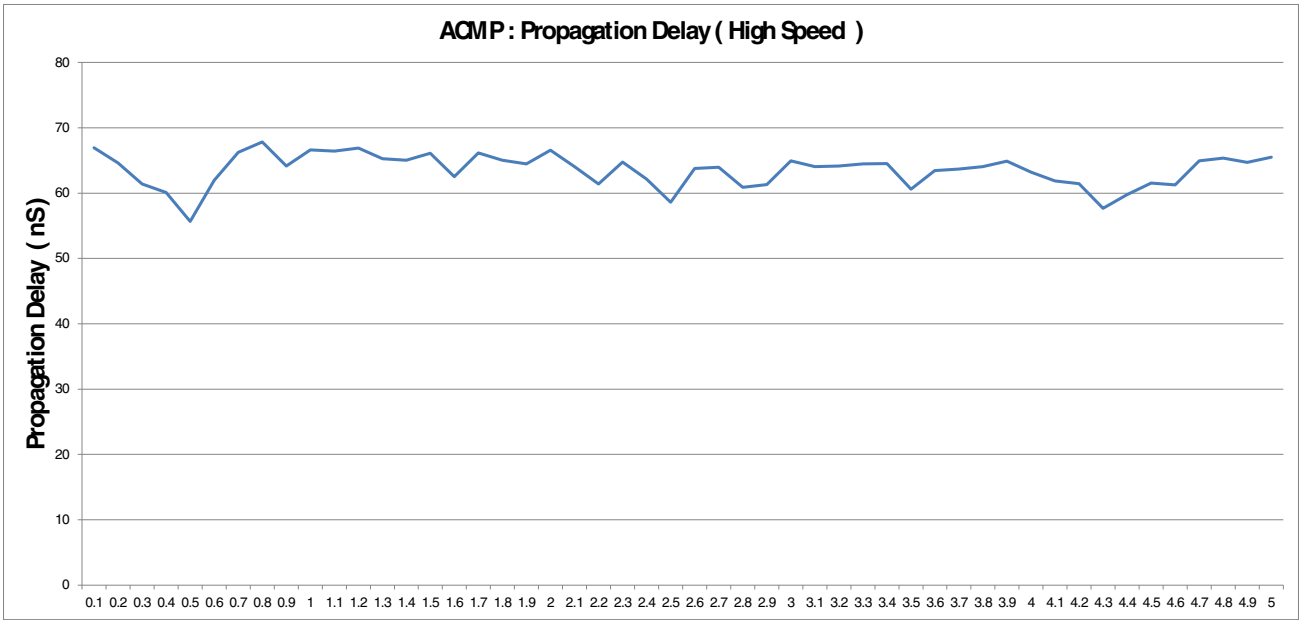


Figure 14. Typical propagation delay vs. Vin level (V_{DDX} = 5.0 V, high speed mode))

Table 14. GDU electrical specifications (continued)

Symbol	Description		Min.	Typ.	Max.	Unit	Note
		I_{Load}=15 mA	—	317	590	mV	
		I_{Load}=20 mA	—	330	600	mV	
	DC VOL for LS, V_{DDX}=5 V, V_{DD}=12 V	I_{Load}=5 mA	—	290	570	mV	
		I_{Load}=15 mA	—	320	580	mV	
		I_{Load}=20 mA	—	335	600	mV	
I_{OH}	V_{DDX}=5 V, V_{DD}=12 V, V_{Out}= V_{DD}-0.4V	DC IOH at lowest strength for HS	—	7.45	—	mA	
	V_{DDX}=5 V, V_{DD}=12 V, V_{Out}= V_{DDX}-0.4V	DC IOH at lowest strength for LS	—	7.45	—	mA	
I_{OL}	V_{DDX}=5 V, V_{DD}=12 V V_{Out}=V_{clamp}+0.4V	DC IOL at lowest strength for HS	—	6.45	—	mA	
	V_{DDX}=5 V, V_{DD}=12 V V_{Out}=V_{SS}+0.4V	DC IOL at lowest strength for LS	—	6.45	—	mA	
R_{pullup}	Pullup resistor of HS predriver, gate to source of PFET		192	226	260	kΩ	
$R_{pulldown}$	Pulldown resistor of LS predriver, gate to source of NFET		30	40	50	kΩ	
V_{clamp1}	V_{DD}-Vo_clamp in regulation mode with 5.5 V ≤ V_{DD} ≤ 18 V, loading current is less than 10 mA		4.5	5	5.5	V	
V_{clamp2}	V_{DD}-Vo_clamp in open loop mode with 4.5 V ≤ V_{DD} < 5.5 V, loading current is less than 10 mA		4.0	—	5	V	
I_{Load}	The sink current capability		—	—	10	mA	
	Line regulation, ΔV_{clamp} over ΔV_{DD}	4.5 V ≤ V_{DD}< 5.5 V[3]	—	1000	—	mV/V	
		5.5 V ≤ V_{DD}≤ 18 V	—	10	—	mV/V	
	Load regulation, ΔV_{clamp} over ΔI_{Load}	4.5 V ≤ V_{DD}< 5.5 V[3]	—	25	—	Ω	
		5.5 V ≤ V_{DD}≤ 18 V	—	1	—	Ω	
OVP_22V_a	22V over-voltage asserting threshold		21	22	23	V	
OVP_22V_d	22V over-voltage de-asserting threshold		19	20	21	V	
OVP_22V_h	22V over-voltage hysteresis		1.9	2	2.1	V	
OVP_24V_a	24V over-voltage asserting threshold		23	24	25	V	
OVP_24V_d	24V over-voltage de-asserting threshold		22	23	24	V	
OVP_24V_h	24V over-voltage hysteresis		0.9	1	1.1	V	

1. Customer need to add external resistor Rext1 for voltage divider. For example ,if Rext1=85 kΩ ,1/6 voltage divider; if Rext1=105 kΩ ,1/7 voltage divider.
2. PGA gain is default to 20X. User can cascade one external series resistor (Rext2) to reduce the PGA gain. To keep the current sensor PGA output without saturation distortion, the selected Rext2 must meet PGA output=V_{REF}+(R1/(R2+R_{ext2}))xV_{shunt}, V_{REF}=0.5xV_{DDX}, see reference manual for the R1 and R2.
3. This 5.5 V is a rough value, each part might has different value but around 5.5 V.

Table 16. GDU over current protect ACMP electrical specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit
DNL	6-bit DAC differential non-linearity	–0.3	—	0.3	LSB

1. This ACMP is used for over-current protection, customer can use low power mode to avoid sparkles. Digital filter can produce max of 12.8 µs filter window.
2. Comparator initialization delay is defined as the time between software writes to change control inputs (Writes to DACEN, VRSEL, PSEL, MSEL, VOSEL) and the comparator output settling to a stable level.
3. 1 LSB = $V_{reference}/64$

3.4 Communication interfaces

3.4.1 Inter-Integrated Circuit Interface (I2C) timing

Table 17. I2C timing

Characteristic	Symbol	Standard Mode		Fast Mode		Unit
		Minimum	Maximum	Minimum	Maximum	
SCL Clock Frequency	f_{SCL}	0	100	0	400[1]	kHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated.	t_{HD}; STA	4	—	0.6	—	µs
LOW period of the SCL clock	t_{LOW}	4.7	—	1.3	—	µs
HIGH period of the SCL clock	t_{HIGH}	4	—	0.6	—	µs
Set-up time for a repeated START condition	t_{SU}; STA	4.7	—	0.6	—	µs
Data hold time for I^2C bus devices	t_{HD}; DAT	0[2]	3.45[3]	0[4]	0.9[2]	µs
Data set-up time	t_{SU}; DAT	250[5]	—	100[3, 6]	—	ns
Rise time of SDA and SCL signals	t_r	—	1000	20 +0.1C_b[7]	300	ns
Fall time of SDA and SCL signals	t_f	—	300	20 +0.1C_b[6]	300	ns
Set-up time for STOP condition	t_{SU}; STO	4	—	0.6	—	µs
Bus free time between STOP and START condition	t_{BUF}	4.7	—	1.3	—	µs
Pulse width of spikes that must be suppressed by the input filter	t_{SP}	N/A	N/A	0	50	ns

1. The maximum SCL Clock Frequency in Fast mode with maximum bus loading can only achieved when using the High drive pins (see DC characteristics) or when using the Normal drive pins and $V_{DDX} \geq 2.7$ V
2. The master mode I^2C deasserts ACK of an address byte simultaneously with the falling edge of SCL. If no slaves acknowledge this address byte, then a negative hold time can result, depending on the edge rates of the SDA and SCL lines.
3. The maximum tHD; DAT must be met only if the device does not stretch the LOW period (tLOW) of the SCL signal.
4. Input signal Slew = 10 ns and Output Load = 50 pF
5. Set-up time in slave-transmitter mode is 1 IPBus clock period, if the TX FIFO is empty.

24 QFN	Pin Name	Default/ALT0	ALT1	ALT2	ALT3
2	PWM_UH	PWM_UH			
3	PWM_VH	PWM_VH			
4	PWM_WH	PWM_WH			
5	VCLAMP	VCLAMP			
6	VDD	VDD			
7	VDDX	VDDX			
8	VSS	VSS			
9	PTB6/ RESET_b	RESET_b		TCLK	PTB6
10	PTC0	CMP_REF/ VREFH	PWM_FAULT0	CLK_IN	PTC0
11	PTB7/ BKGD/ MS	BKGD/ MS		CLKOUT	PTB7
12	PTA7	PWT1	TX	XB_OUT1	PTA7/ KBI7
13	PTA6	PWT0	RX	XB_IN1	PTA6/ KBI6
14	PTA5	TX	SDA	XB_OUT0	PTA5/ KBI5
15	PTA4	RX	SCL	XB_IN0	PTA4/ KBI4
16	PTA3	AMP1_M/ ADC1AD1	CLKOUT	XB_OUT1	PTA3/ KBI3
17	PTA2	AMP1_P/ CMP2/ ADC1AD0	XB_IN1	XB_OUT0	PTA2/ KBI2
18	PTA1	AMP0_M/ CMP1/ ADC0AD1	XB_OUT0	XB_IN1	PTA1/ KBI1
19	PTA0	AMP0_P/ CMP0/ ADC0AD0	CLK_IN	XB_IN0	PTA0/ KBI0
20	PTB0	GDU_CMP0/ ADC0AD2/ ADC1AD2			PTB0
21	PTB1	GDU_CMP1/ ADC0AD3/ ADC1AD3			PTB1
22	PTB2	GDU_CMP2/ ADC0AD4/ ADC1AD4			PTB2
23	PTB3	PWM_UL			PTB3
24	PTB4	PWM_VL			PTB4

7.1.1 Example

This is an example of an operating requirement:

Symbol	Description	Min.	Max.	Unit
V_{DD}	1.0 V core supply voltage	0.9	1.1	V

7.2 Definition: Operating behavior

Unless otherwise specified, an *operating behavior* is a specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions.

7.2.1 Example

This is an example of an operating behavior:

Symbol	Description	Min.	Max.	Unit
I_{WP}	Digital I/O weak pullup/ pulldown current	10	130	µA

7.3 Definition: Attribute

An *attribute* is a specified value or range of values for a technical characteristic that are guaranteed, regardless of whether you meet the operating requirements.

7.3.1 Example

This is an example of an attribute:

Symbol	Description	Min.	Max.	Unit
CIN_D	Input capacitance: digital pins	—	7	pF

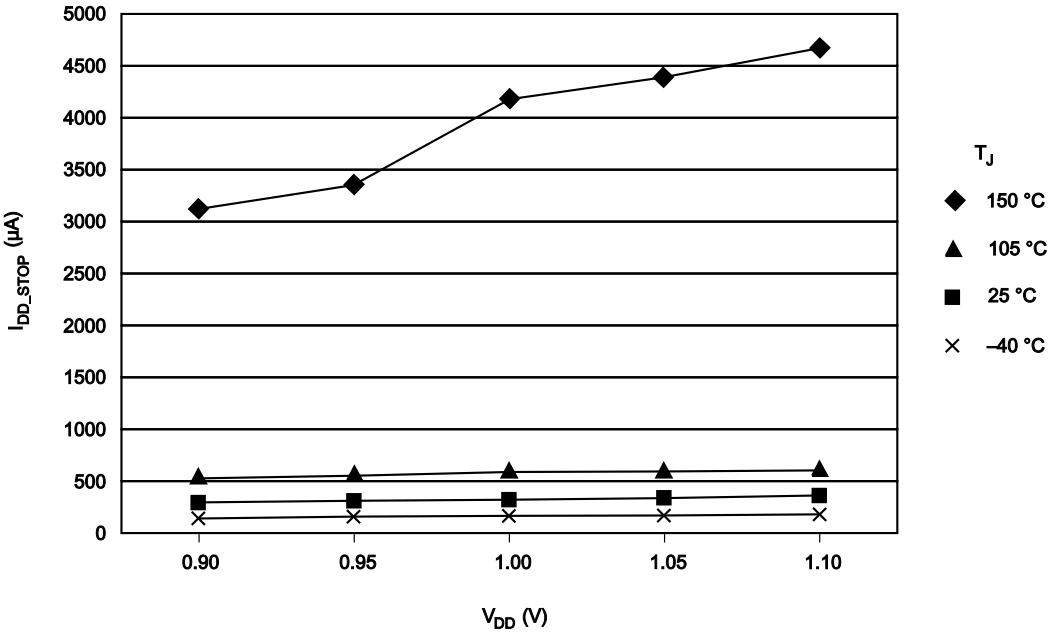
7.8.1 Example 1

This is an example of an operating behavior that includes a typical value:

Symbol	Description	Min.	Typ.	Max.	Unit
I_{WP}	Digital I/O weak pullup/pulldown current	10	70	130	µA

7.8.2 Example 2

This is an example of a chart that shows typical values for various voltage and temperature conditions:



7.9 Typical value conditions

Typical values assume you meet the following conditions (or other conditions as specified):

Table 18. Typical value conditions

Symbol	Description	Value	Unit
T_A	Ambient temperature	25	°C
V_{DD}	3.3 V supply voltage	3.3	V

7.10 Parameter Classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding, the following classification is used and the parameters are tagged accordingly in the tables where appropriate:

Table 19. Parameter Classifications

P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

NOTE

The classification is shown in the column labeled “C” in the parameter tables where appropriate.

8 Revision history

The following table provides a revision history for this document.

Table 20. Revision history

Rev. No.	Date	Substantial Changes
1	09/2016	• Initial public release.
2	11/2016	• Added MC9S08SU8VFK part.