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#### Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

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Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	40 MIPs
Connectivity	I <sup>2</sup> C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	53
Program Memory Size	128KB (43K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 18x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24hj128gp206a-i-pt

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	TABLE 4-5:	INTERRUPT CONTROLLER REGISTER MAP
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SFR Name	SFR Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
INTCON1	0800	NSTDIS	—	—		—	—	—	—	—	DIV0ERR	DMACERR	MATHERR	ADDRERR	STKERR	OSCFAIL	—	0000
INTCON2	0082	ALTIVT	DISI	—		—	—	—	—	—	—	_	INT4EP	INT3EP	INT2EP	INT1EP	INT0EP	0000
IFS0	0084	_	DMA1IF	AD1IF	U1TXIF	U1RXIF	SPI1IF	SPI1EIF	T3IF	T2IF	OC2IF	IC2IF	DMA0IF	T1IF	OC1IF	IC1IF	<b>INT0IF</b>	0000
IFS1	0086	U2TXIF	U2RXIF	INT2IF	T5IF	T4IF	OC4IF	OC3IF	DMA2IF	IC8IF	IC7IF	AD2IF	INT1IF	CNIF	—	MI2C1IF	SI2C1IF	0000
IFS2	0088	T6IF	DMA4IF	—	OC8IF	OC7IF	OC6IF	OC5IF	IC6IF	IC5IF	IC4IF	IC3IF	DMA3IF	C1IF	C1RXIF	SPI2IF	SPI2EIF	0000
IFS3	008A	—	—	DMA5IF	—	—	—	—	C2IF	C2RXIF	INT4IF	INT3IF	T9IF	T8IF	MI2C2IF	SI2C2IF	T7IF	0000
IFS4	008C	—	—	—	—	—	—	—	—	C2TXIF	C1TXIF	DMA7IF	DMA6IF	—	U2EIF	U1EIF	—	0000
IEC0	0094	—	DMA1IE	AD1IE	U1TXIE	U1RXIE	SPI1IE	SPI1EIE	T3IE	T2IE	OC2IE	IC2IE	DMA0IE	T1IE	OC1IE	IC1IE	INT0IE	0000
IEC1	0096	U2TXIE	U2RXIE	INT2IE	T5IE	T4IE	OC4IE	OC3IE	DMA2IE	IC8IE	IC7IE	AD2IE	INT1IE	CNIE	_	MI2C1IE	SI2C1IE	0000
IEC2	0098	T6IE	DMA4IE	—	OC8IE	OC7IE	OC6IE	OC5IE	IC6IE	IC5IE	IC4IE	IC3IE	DMA3IE	C1IE	C1RXIE	SPI2IE	SPI2EIE	0000
IEC3	009A	—	_	DMA5IE	_	—	_	—	C2IE	C2RXIE	INT4IE	INT3IE	T9IE	T8IE	MI2C2IE	SI2C2IE	T7IE	0000
IEC4	009C	—	—	—	—	_		—	—	C2TXIE	C1TXIE	DMA7IE	DMA6IE	—	U2EIE	U1EIE	—	0000
IPC0	00A4	—		T1IP<2:0>		—		OC1IP<2:(	)>	—		IC1IP<2:0>		—	11	NT0IP<2:0>	>	4444
IPC1	00A6	—		T2IP<2:0>		—		OC2IP<2:0	)>	—		IC2IP<2:0>		—	D	MA0IP<2:0	>	4444
IPC2	00A8	—	ι	J1RXIP<2:(	)>	—		SPI1IP<2:	)>	—		SPI1EIP<2:0	)>	—		T3IP<2:0>		4444
IPC3	00AA	—	—	—	—	—	0	MA1IP<2	:0>	—		AD1IP<2:03	>	—	U	1TXIP<2:0	>	0444
IPC4	00AC	—		CNIP<2:0>	>	—	—	—	—	—		MI2C1IP<2:0	)>	—	S	I2C1IP<2:0	>	4044
IPC5	00AE	—		IC8IP<2:0	>	—		IC7IP<2:0	>	—		AD2IP<2:0	>	—	II	NT1IP<2:0>	>	4444
IPC6	00B0	—		T4IP<2:0>		—		OC4IP<2:(	)>	—		OC3IP<2:0	>	—	D	MA2IP<2:0	>	4444
IPC7	00B2	—	l	J2TXIP<2:(	)>	—	ι	J2RXIP<2:	0>	—		INT2IP<2:0	>	—		T5IP<2:0>		4444
IPC8	00B4	—		C1IP<2:0>	•	—		C1RXIP<2:	0>	—		SPI2IP<2:0	>	-	SI	PI2EIP<2:0	>	4444
IPC9	00B6	_		IC5IP<2:0	>	_		IC4IP<2:0	>	_		IC3IP<2:0>		_	D	MA3IP<2:0	>	4444
IPC10	00B8	_		OC7IP<2:0	>	_		OC6IP<2:0	)>	_		OC5IP<2:0	>	_	I	IC6IP<2:0>		4444
IPC11	00BA	_		T6IP<2:0>		_	C	MA4IP<2	:0>	_	_	_	_	_	0	DC8IP<2:0>	<b>`</b>	4404
IPC12	00BC	_		T8IP<2:0>		_	N	112C2IP<2	:0>	_		SI2C2IP<2:0	)>	_		T7IP<2:0>		4444
IPC13	00BE	_	(	C2RXIP<2:0	)>	_	1	INT4IP<2:	)>	_		INT3IP<2:0	>	_		T9IP<2:0>		4444
IPC14	00C0	_		_	—	_	_	_	—	—	—	_	_	_		C2IP<2:0>		0004
IPC15	00C2	_	_	_	_	_	_	_	_	_		DMA5IP<2:0	)>	_	—	_	—	0040
IPC16	00C4	_	—	_	_	_		U2EIP<2:0	)>	_		U1EIP<2:0	>	_	_	_	_	0440
IPC17	00C6	_	(	C2TXIP<2:0	)>	_	(	C1TXIP<2:	0>	_		DMA7IP<2:0	)>	_	D	MA6IP<2:0	>	4444
INTTREG	00E0	_	—	—	—		ILR<	3:0>		—			VE	CNUM<6:0>				0000

Legend: x = unknown value on Reset, - = unimplemented, read as '0'. Reset values are shown in hexadecimal for PinHigh devices.

#### TABLE 4-24: PORTA REGISTER MAP<sup>(1)</sup>

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISA	02C0	TRISA15	TRISA14	TRISA13	TRISA12	—	TRISA10	TRISA9	—	TRISA7	TRISA6	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	F6FF
PORTA	02C2	RA15	RA14	RA13	RA12	_	RA10	RA9	_	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0	XXXX
LATA	02C4	LATA15	LATA14	LATA13	LATA12	_	LATA10	LATA9	_	LATA7	LATA6	LATA5	LATA4	LATA3	LATA2	LATA1	LATA0	XXXX
ODCA	06C0	ODCA15	ODCA14	_	_	_	_	_	_	_	_	ODCA5	ODCA4	ODCA3	ODCA2	ODCA1	ODCA0	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal for PinHigh devices.

Note 1: The actual set of I/O port pins varies from one device to another. Please refer to the corresponding pinout diagrams.

### TABLE 4-25: PORTB REGISTER MAP<sup>(1)</sup>

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISB	02C6	TRISB15	TRISB14	TRISB13	TRISB12	TRISB11	TRISB10	TRISB9	TRISB8	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	FFFF
PORTB	02C8	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx
LATB	02CA	LATB15	LATB14	LATB13	LATB12	LATB11	LATB10	LATB9	LATB8	LATB7	LATB6	LATB5	LATB4	LATB3	LATB2	LATB1	LATB0	XXXX

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal for PinHigh devices.

Note 1: The actual set of I/O port pins varies from one device to another. Please refer to the corresponding pinout diagrams.

# TABLE 4-26: PORTC REGISTER MAP<sup>(1)</sup>

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISC	02CC	TRISC15	TRISC14	TRISC13	TRISC12	-	—	—	—	—	—	—	TRISC4	TRISC3	TRISC2	TRISC1	-	F01E
PORTC	02CE	RC15	RC14	RC13	RC12	_	_	_	_	_	_	_	RC4	RC3	RC2	RC1	_	XXXX
LATC	02D0	LATC15	LATC14	LATC13	LATC12	_	_	_	_	_	_	_	LATC4	LATC3	LATC2	LATC1	_	xxxx

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal for PinHigh devices.

Note 1: The actual set of I/O port pins varies from one device to another. Please refer to the corresponding pinout diagrams.

# TABLE 4-27: PORTD REGISTER MAP<sup>(1)</sup>

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISD	02D2	TRISD15	TRISD14	TRISD13	TRISD12	TRISD11	TRISD10	TRISD9	TRISD8	TRISD7	TRISD6	TRISD5	TRISD4	TRISD3	TRISD2	TRISD1	TRISD0	FFFF
PORTD	02D4	RD15	RD14	RD13	RD12	RD11	RD10	RD9	RD8	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	xxxx
LATD	02D6	LATD15	LATD14	LATD13	LATD12	LATD11	LATD10	LATD9	LATD8	LATD7	LATD6	LATD5	LATD4	LATD3	LATD2	LATD1	LATD0	xxxx
ODCD	06D2	ODCD15	ODCD14	ODCD13	ODCD12	ODCD11	ODCD10	ODCD9	ODCD8	ODCD7	ODCD6	ODCD5	ODCD4	ODCD3	ODCD2	ODCD1	ODCD0	0000

Legend: x = unknown value on Reset, - = unimplemented, read as '0'. Reset values are shown in hexadecimal for PinHigh devices.

**Note** 1: The actual set of I/O port pins varies from one device to another. Please refer to the corresponding pinout diagrams.

### TABLE 4-31: SYSTEM CONTROL REGISTER MAP

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
RCON	0740	TRAPR	IOPUWR	-	—	—	—	—	VREGS	EXTR	SWR	SWDTEN	WDTO	SLEEP	IDLE	BOR	POR	xxxx(1)
OSCCON	0742	_	(	COSC<2:0	>	_	I	NOSC<2:0	WEEG         DATE         SWALLS         WEIG         SELECT         IDEL         DOK         FOX           10>         CLKLOCK         —         LOCK         —         CF         —         LPOSCEN         OSWEN					<sub>0300</sub> (2)				
CLKDIV	0744	ROI		DOZE<2:0	>	DOZEN	F	RCDIV<2:0	)>	PLLPOS	ST<1:0>				PLLPRE<4	:0>		3040
PLLFBD	0746	_	_	_	_	_	_	_					PLLDIV<8:	0>				0030
OSCTUN	0748	_	_	_	_	_	_	_	_	_	_			IDLE     BOR     POR       -     CF     -     LPOSCEN     OSWEN       -     PLLPRE<4:0>     V<8:0>     TUN<5:0>				

Legend: x = unknown value on Reset, - = unimplemented, read as '0'. Reset values are shown in hexadecimal for PinHigh devices.

Note 1: RCON register Reset values dependent on type of Reset.

2: OSCCON register Reset values dependent on the FOSC Configuration bits and by type of Reset.

#### TABLE 4-32: NVM REGISTER MAP

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
NVMCON	0760	WR	WREN	WRERR	—	-	—	_	—	_	ERASE	_	_	NVMOP<3:0>				0000(1)
NVMKEY	0766	_	_	_	—		—	_	—				NVMKE	Y<7:0>				0000

Legend: x = unknown value on Reset, - = unimplemented, read as '0'. Reset values are shown in hexadecimal for PinHigh devices.

Note 1: Reset value shown is for POR only. Value on other Reset states is dependent on the state of memory write or erase operations at the time of Reset.

#### TABLE 4-33: PMD REGISTER MAP

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PMD1	0770	T5MD	T4MD	T3MD	T2MD	T1MD	—	—	—	I2C1MD	U2MD	U1MD	SPI2MD	SPI1MD	C2MD	C1MD	AD1MD	0000
PMD2	0772	IC8MD	IC7MD	IC6MD	IC5MD	IC4MD	IC3MD	IC2MD	IC1MD	OC8MD	OC7MD	OC6MD	OC5MD	OC4MD	OC3MD	OC2MD	OC1MD	0000
PMD3	0774	T9MD	T8MD	T7MD	T6MD	_	_	_	_	_	_	_	_	_	_	I2C2MD	AD2MD	0000

Legend: x = unknown value on Reset, - = unimplemented, read as '0'. Reset values are shown in hexadecimal for PinHigh devices.

U-0	U-0	U-0	U-0	U-0	R/W-1	R/W-0	R/W-0
_	—	—	_	—		DMA1IP<2:0>	
bit 15		•					bit 8
U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
		AD1IP<2:0>				U1TXIP<2:0>	
bit 7	·						bit 0
Legend:							
R = Readat	ole bit	W = Writable	bit	U = Unimple	mented bit, rea	d as '0'	
-n = Value a	at POR	'1' = Bit is set		'0' = Bit is cle	eared	x = Bit is unkr	nown
bit 15-11	Unimplement	ted: Read as '	)'				
bit 10-8	DMA1IP<2:0>	>: DMA Channe	el 1 Data Tra	nsfer Complete	e Interrupt Prior	ity bits	
	111 = Interrup	ot is priority 7 (I	nighest priori	ty interrupt)			
	•						
	•						
	001 = Interrur	ot is priority 1					
	000 = Interrup	ot source is dis	abled				
bit 7	Unimplement	ted: Read as 'd	)'				
bit 6-4	AD1IP<2:0>:	ADC1 Convers	sion Complet	e Interrupt Prio	ority bits		
	111 = Interrup	ot is priority 7 (I	nighest priori	ty interrupt)			
	•						
	•						
	• 001 = Interrur	ot is priority 1					
	000 = Interrup	ot source is dis	abled				
bit 3	Unimplement	ted: Read as '	)'				
bit 2-0	U1TXIP<2:0>	: UART1 Trans	mitter Interru	upt Priority bits			
	111 = Interrup	ot is priority 7 (I	nighest priori	ty interrupt)			
	•		0				
	•						
	• 001 - Interrur	at is priority 1					
	000 = Interrupt	ot source is dis	abled				

### REGISTER 7-18: IPC3: INTERRUPT PRIORITY CONTROL REGISTER 3

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
_		T6IP<2:0>				DMA4IP<2:0>	
bit 15					·		bit 8
U-0	U-0	U-0	U-0	U-0	R/W-1	R/W-0	R/W-0
	—	—	_	—		OC8IP<2:0>	
bit 7							bit 0
Legend:							
R = Readab	le bit	W = Writable	bit	U = Unimple	mented bit, rea	d as '0'	
-n = Value a	t POR	'1' = Bit is set	t	'0' = Bit is cle	eared	x = Bit is unkr	nown
bit 15	Unimplemen	ted: Read as '	0'				
bit 14-12	<b>T6IP&lt;2:0&gt;:</b> ⊺	imer6 Interrupt	Priority bits				
	111 = Interru	pt is priority 7 (	highest priori	ty interrupt)			
	•						
	•						
	001 = Interru	pt is priority 1					
	000 = Interru	pt source is dis	sabled				
bit 11	Unimplemen	ted: Read as '	0'				
bit 10-8	DMA4IP<2:0	>: DMA Chann	iel 4 Data Tra	nsfer Complete	e Interrupt Prior	ity bits	
	111 = Interru	pt is priority 7 (	highest priori	ty interrupt)			
	•						
	•						
	001 = Interru	pt is priority 1					
		pt source is dis	sabled				
bit 7-3	Unimplemen	ted: Read as	0'				
bit 2-0	OC8IP<2:0>:	Output Compa	are Channel 8	3 Interrupt Prior	rity bits		
	111 = Interru	pt is priority 7 (	nignest priori	ty interrupt)			
	•						
	•						
	001 = Interru	pt is priority 1					
	000 = Interru	pt source is dis	sabled				

#### REGISTER 7-26: IPC11: INTERRUPT PRIORITY CONTROL REGISTER 11

### REGISTER 7-32: IPC17: INTERRUPT PRIORITY CONTROL REGISTER 17

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
_		C2TXIP<2:0>	10110	_		C1TXIP<2:0>	
bit 15	1				1		bit 8
U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
		DMA7IP<2:0>				DMA6IP<2:0>	
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable b	bit	U = Unimpler	mented bit, re	ad as '0'	
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown							wn
bit 15	Unimpleme	ented: Read as '0	,				
bit 14-12	C2TXIP<2:0	D>: ECAN2 Trans	mit Data Red	quest Interrupt	Priority bits		
	111 = Interr	rupt is priority 7 (h	ighest priorit	y interrupt)			
	•						
	•						
	001 = Interr	upt is priority 1					
	000 = Interr	rupt source is disa	bled				
bit 11	Unimpleme	ented: Read as '0	,				
bit 10-8	C1TXIP<2:0	<b>0&gt;:</b> ECAN1 Trans	mit Data Red	quest Interrupt	Priority bits		
	111 = Interr	rupt is priority 7 (h	ighest priorit	y interrupt)			
	•						
	•						
	001 = Interr	upt is priority 1					
	000 = Interr	upt source is disa	bled				
bit 7	Unimpleme	ented: Read as '0	,				
bit 6-4	DMA7IP<2:	0>: DMA Channe	l 7 Data Trai	nsfer Complete	Interrupt Price	ority bits	
	111 = Interr	rupt is priority 7 (h	ighest priorit	y interrupt)			
	•						
	•						
	001 = Interr	upt is priority 1					
	000 = Interr	upt source is disa	bled				
bit 3	Unimpleme	ented: Read as '0	,				
bit 2-0	DMA6IP<2:	0>: DMA Channe	l 6 Data Trai	nsfer Complete	Interrupt Price	ority bits	
	111 = Interr	upt is priority 7 (h	ighest priorit	y interrupt)			
	•						
	•						
	001 = Interr	upt is priority 1					
	000 = Interr	upt source is disa	bled				

U-0	U-0	U-0	U-0	R-0	R-0	R-0	R-0
—	—	—	—		ILR	<3:0>	
bit 15	·						bit 8
U-0	U-0	R-0	R-0	R-0	R-0	R-0	R-0
				VECNUM<6:0	>		
bit 7	•						bit 0
Legend:							
R = Readabl	le bit	W = Writable	bit	U = Unimplen	nented bit, rea	d as '0'	
-n = Value at	t POR	'1' = Bit is set		'0' = Bit is clea	ared	x = Bit is unkr	nown
<b>L</b>							
bit 15-12	Unimplement	ted: Read as '	0'				
bit 11-8	ILR<3:0>: Ne	w CPU Interrup	pt Priority Lev	el bits			
	1111 <b>= CPU I</b>	nterrupt Priorit	y Level is 15				
	•						
	•						
	0001 = CPU li	nterrupt Priority	y Level is 1				
	0000 <b>= CPU I</b>	nterrupt Priorit	y Level is 0				
bit 7	Unimplement	ted: Read as '	0'				
bit 6-0	VECNUM<6:0	>: Vector Num	ber of Pendir	ng Interrupt bits	i		
	1111111 = In	terrupt Vector	pending is nu	mber 135			
	•						
	•						
	0000001 = In	terrupt Vector	pending is nu	mber 9			
	0000000 = In	terrupt Vector	pending is nu	mber 8			

### REGISTER 7-33: INTTREG: INTERRUPT CONTROL AND STATUS REGISTER

# 9.1 CPU Clocking System

There are seven system clock options provided by the PIC24HJXXXGPX06A/X08A/X10A:

- FRC Oscillator
- FRC Oscillator with PLL
- Primary (XT, HS or EC) Oscillator
- Primary Oscillator with PLL
- Secondary (LP) Oscillator
- LPRC Oscillator
- FRC Oscillator with postscaler

#### 9.1.1 SYSTEM CLOCK SOURCES

The FRC (Fast RC) internal oscillator runs at a nominal frequency of 7.37 MHz. The user software can tune the FRC frequency. User software can optionally specify a factor (ranging from 1:2 to 1:256) by which the FRC clock frequency is divided. This factor is selected using the FRCDIV<2:0> (CLKDIV<10:8>) bits.

The primary oscillator can use one of the following as its clock source:

- XT (Crystal): Crystals and ceramic resonators in the range of 3 MHz to 10 MHz. The crystal is connected to the OSC1 and OSC2 pins.
- HS (High-Speed Crystal): Crystals in the range of 10 MHz to 40 MHz. The crystal is connected to the OSC1 and OSC2 pins.
- EC (External Clock): External clock signal is directly applied to the OSC1 pin.

The secondary (LP) oscillator is designed for low power and uses a 32.768 kHz crystal or ceramic resonator. The LP oscillator uses the SOSCI and SOSCO pins.

The LPRC (Low-Power RC) internal oscillator runs at a nominal frequency of 32.768 kHz. It is also used as a reference clock by the Watchdog Timer (WDT) and Fail-Safe Clock Monitor (FSCM).

The clock signals generated by the FRC and primary oscillators can be optionally applied to an on-chip Phase-Locked Loop (PLL) to provide a wide range of output frequencies for device operation. PLL configuration is described in **Section 9.1.3 "PLL Configuration**".

The FRC frequency depends on the FRC accuracy (see Table 24-19) and the value of the FRC Oscillator Tuning register (see Register 9-4).

### 9.1.2 SYSTEM CLOCK SELECTION

The oscillator source that is used at a device Power-on Reset event is selected using Configuration bit settings. The oscillator Configuration bit settings are located in the Configuration registers in the program memory. (Refer to **Section 21.1 "Configuration Bits"** for further details.) The Initial Oscillator Selection Configuration bits, FNOSC<2:0> (FOSCSEL<2:0>), and the Primary Oscillator Mode Select Configuration bits, POSCMD<1:0> (FOSC<1:0>), select the oscillator source that is used at a Power-on Reset. The FRC primary oscillator is the default (unprogrammed) selection.

The Configuration bits allow users to choose between twelve different clock modes, shown in Table 9-1.

The output of the oscillator (or the output of the PLL if a PLL mode has been selected) FOSC is divided by 2 to generate the device instruction clock (FCY) and the peripheral clock time base (FP). FCY defines the operating speed of the device, and speeds up to 40 MHz are supported by the PIC24HJXXXGPX06A/ X08A/X10A architecture.

Instruction execution speed or device operating frequency, FCY, is calculated, as shown in Equation 9-1:

#### EQUATION 9-1: DEVICE OPERATING FREQUENCY

$$FCY = \frac{FOSC}{2}$$

### 9.1.3 PLL CONFIGURATION

The primary oscillator and internal FRC oscillator can optionally use an on-chip PLL to obtain higher speeds of operation. The PLL provides a significant amount of flexibility in selecting the device operating speed. A block diagram of the PLL is shown in Figure 9-2.

The output of the primary oscillator or FRC, denoted as 'FIN', is divided down by a prescale factor (N1) of 2, 3, ... or 33 before being provided to the PLL's Voltage Controlled Oscillator (VCO). The input to the VCO must be selected to be in the range of 0.8 MHz to 8 MHz. Since the minimum prescale factor is 2, this implies that FIN must be chosen to be in the range of 1.6 MHz to 16 MHz. The prescale factor 'N1' is selected using the PLLPRE<4:0> bits (CLKDIV<4:0>).

The PLL Feedback Divisor, selected using the PLLDIV<8:0> bits (PLLFBD<8:0>), provides a factor 'M', by which the input to the VCO is multiplied. This factor must be selected such that the resulting VCO output frequency is in the range of 100 MHz to 200 MHz.

The VCO output is further divided by a postscale factor 'N2'. This factor is selected using the PLLPOST<1:0> bits (CLKDIV<7:6>). 'N2' can be either 2, 4 or 8, and must be selected such that the PLL output frequency (Fosc) is in the range of 12.5 MHz to 80 MHz, which generates device operating speeds of 6.25-40 MIPS.

For a primary oscillator or FRC oscillator, output 'FIN', the PLL output 'FOSC' is given by:

### EQUATION 9-2: Fosc CALCULATION

 $FOSC = FIN \cdot \left(\frac{M}{N1 \cdot N2}\right)$ 

## **REGISTER 9-1:** OSCCON: OSCILLATOR CONTROL REGISTER<sup>(1,3)</sup> (CONTINUED)

bit 1	LPOSCEN: Secondary (LP) Oscillator Enable bit
	1 = Enable secondary oscillator
	0 = Disable secondary oscillator
bit 0	<b>OSWEN:</b> Oscillator Switch Enable bit
	1 = Request oscillator switch to selection specified by NOSC<2:0> bits
	0 = Oscillator switch is complete

- Note 1: Writes to this register require an unlock sequence. Refer to Section 7. "Oscillator" (DS70186) in the "dsPIC33F/PIC24H Family Reference Manual" for details.
  - 2: Direct clock switches between any primary oscillator mode with PLL and FRCPLL mode are not permitted. This applies to clock switches in either direction. In these instances, the application must switch to FRC mode as a transition clock source between the two PLL modes.
  - 3: This register is reset only on a Power-on Reset (POR).

NOTES:

R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0		
TON		TSIDL	—		—	—	—		
bit 15							bit 8		
U-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	U-0		
	TGATE	TCKPS	S<1:0>		TSYNC	TCS			
bit 7	pit 7								
Legend:									
R = Readable	bit	W = Writable	bit	U = Unimpler	mented bit, read	as '0'			
-n = Value at F	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkn	nown		
bit 15	TON: Timer1	On bit							
	1 = Starts 16-	bit Timer1							
	0 = Stops 16-	bit Timer1							
bit 14	Unimplemen	ted: Read as '	)'						
bit 13	TSIDL: Stop i	n Idle Mode bit							
	1 = Discontinu 0 = Continue	ue module oper module operati	ration when d on in Idle mo	evice enters Id de	lle mode				
bit 12-7	Unimplemen	ted: Read as 'd	)'						
bit 6	TGATE: Time	r1 Gated Time	Accumulation	n Enable bit					
	When TCS = This bit is igno	<u>1:</u> ored.							
	When TCS =	0:							
	1 = Gated tim 0 = Gated tim	e accumulation	n enabled n disabled						
bit 5-4	TCKPS<1:0>: Timer1 Input Clock Prescale Select bits								
	11 <b>= 1:256</b>								
	10 <b>= 1:64</b>								
	01 = 1:8								
	00 = 1:1								
bit 3		ted: Read as 10	).						
DIT 2	When TCS -		ock input Syn	chronization Se	elect dit				
	$\frac{\text{when } 1\text{CS} =}{1 = \text{Synchroni}}$	<u>⊥:</u> ize external clo	ck input						
	0 = Do not sy	nchronize exter	rnal clock inp	ut					
	When TCS =	0:							
	This bit is igno	ored.							
bit 1	TCS: Timer1	Clock Source S	Select bit						
	1 = External c	clock from pin T	1CK (on the	rising edge)					
hit O		IUCK (FCY)	<b>,</b> '						
	Unimplemen	ieu: Reau as 1	J						

## 13.0 TIMER2/3, TIMER4/5, TIMER6/7 AND TIMER8/9

- Note 1: This data sheet summarizes the features of the PIC24HJXXXGPX06A/X08A/X10A family of devices. However, it is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 11. "Timers" (DS70205) of the "dsPIC33F/PIC24H Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
  - 2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

The Timer2/3, Timer4/5, Timer6/7 and Timer8/9 modules are 32-bit timers, which can also be configured as four independent 16-bit timers with selectable operating modes.

As a 32-bit timer, Timer2/3, Timer4/5, Timer6/7 and Timer8/9 operate in three modes:

- Two Independent 16-bit Timers (e.g., Timer2 and Timer3) with all 16-bit operating modes (except Asynchronous Counter mode)
- Single 32-bit Timer
- Single 32-bit Synchronous Counter

They also support these features:

- Timer Gate Operation
- Selectable Prescaler Settings
- Timer Operation during Idle and Sleep modes
- Interrupt on a 32-bit Period Register Match
- Time Base for Input Capture and Output Compare Modules (Timer2 and Timer3 only)
- ADC1 Event Trigger (Timer2/3 only)
- ADC2 Event Trigger (Timer4/5 only)

Individually, all eight of the 16-bit timers can function as synchronous timers or counters. They also offer the features listed above, except for the event trigger; this is implemented only with Timer2/3. The operating modes and enabled features are determined by setting the appropriate bit(s) in the T2CON, T3CON, T4CON, T5CON, T6CON, T7CON, T8CON and T9CON registers. T2CON, T4CON, T6CON and T8CON are shown in generic form in Register 13-1. T3CON, T5CON, T7CON and T9CON are shown in Register 13-2. For 32-bit timer/counter operation, Timer2, Timer4, Timer6 or Timer8 is the least significant word; Timer3, Timer5, Timer7 or Timer9 is the most significant word of the 32-bit timers.

Note:	For 32-bit operation, T3CON, T5CON,
	T7CON and T9CON control bits are
	ignored. Only T2CON, T4CON, T6CON
	and T8CON control bits are used for setup
	and control. Timer2, Timer4, Timer6 and
	Timer8 clock and gate inputs are utilized
	for the 32-bit timer modules, but an inter-
	rupt is generated with the Timer3, Timer5,
	Ttimer7 and Timer9 interrupt flags.

To configure Timer2/3, Timer4/5, Timer6/7 or Timer8/9 for 32-bit operation:

- 1. Set the corresponding T32 control bit.
- 2. Select the prescaler ratio for Timer2, Timer4, Timer6 or Timer8 using the TCKPS<1:0> bits.
- 3. Set the Clock and Gating modes using the corresponding TCS and TGATE bits.
- 4. Load the timer period value. PR3, PR5, PR7 or PR9 contains the most significant word of the value, while PR2, PR4, PR6 or PR8 contains the least significant word.
- 5. If interrupts are required, set the interrupt enable bit, T3IE, T5IE, T7IE or T9IE. Use the priority bits, T3IP<2:0>, T5IP<2:0>, T7IP<2:0> or T9IP<2:0>, to set the interrupt priority. While Timer2, Timer4, Timer6 or Timer8 control the timer, the interrupt appears as a Timer3, Timer5, Timer7 or Timer9 interrupt.
- 6. Set the corresponding TON bit.

The timer value at any point is stored in the register pair, TMR3:TMR2, TMR5:TMR4, TMR7:TMR6 or TMR9:TMR8. TMR3, TMR5, TMR7 or TMR9 always contains the most significant word of the count, while TMR2, TMR4, TMR6 or TMR8 contains the least significant word.

To configure any of the timers for individual 16-bit operation:

- 1. Clear the T32 bit corresponding to that timer.
- 2. Select the timer prescaler ratio using the TCKPS<1:0> bits.
- 3. Set the Clock and Gating modes using the TCS and TGATE bits.
- 4. Load the timer period value into the PRx register.
- 5. If interrupts are required, set the interrupt enable bit, TxIE. Use the priority bits, TxIP<2:0>, to set the interrupt priority.
- 6. Set the TON bit.



# 17.2 <sup>2</sup>C Resources

Many useful resources related to  $I^2C$  are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note:	In the event you are not able to access the product page using the link above, enter
	this URL in your browser:
	http://www.microchip.com/wwwproducts/
	Devices.aspx?dDocName=en546061

#### 17.2.1 KEY RESOURCES

- Section 11. "Inter-Integrated Circuit™ (I<sup>2</sup>C™)" (DS70195)
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All related dsPIC33F/PIC24H Family Reference Manuals Sections
- Development Tools

# 17.3 I<sup>2</sup>C Registers

I2CxCON and I2CxSTAT are control and status registers, respectively. The I2CxCON register is readable and writable. The lower six bits of I2CxSTAT are read-only. The remaining bits of the I2CSTAT are read/write.

I2CxRSR is the shift register used for shifting data, whereas I2CxRCV is the buffer register to which data bytes are written, or from which data bytes are read. I2CxRCV is the receive buffer. I2CxTRN is the transmit register to which bytes are written during a transmit operation.

The I2CxADD register holds the slave address. A status bit, ADD10, indicates 10-bit Address mode. The I2CxBRG acts as the Baud Rate Generator (BRG) reload value.

In receive operations, I2CxRSR and I2CxRCV together form a double-buffered receiver. When I2CxRSR receives a complete byte, it is transferred to I2CxRCV and an interrupt pulse is generated.

# 18.0 UNIVERSAL ASYNCHRONOUS RECEIVER TRANSMITTER (UART)

- Note 1: This data sheet summarizes the features of the PIC24HJXXXGPX06A/X08A/X10A family of devices. However, it is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 17. "UART" (DS70188) of the "dsPIC33F/PIC24H Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
  - 2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

The Universal Asynchronous Receiver Transmitter (UART) module is one of the serial I/O modules available in the PIC24HJXXXGPX06A/X08A/X10A device family. The UART is a full-duplex asynchronous system that can communicate with peripheral devices, such as personal computers, LIN, RS-232 and RS-485 interfaces. The module also supports a hardware flow control option with the UxCTS and UxRTS pins and also includes an IrDA<sup>®</sup> encoder and decoder.

The primary features of the UART module are:

- Full-Duplex, 8 or 9-bit Data Transmission through the UxTX and UxRX pins
- Even, Odd or No Parity Options (for 8-bit data)
- · One or Two Stop bits
- Hardware Flow Control Option with UxCTS and UxRTS pins
- Fully Integrated Baud Rate Generator with 16-bit Prescaler
- Baud rates ranging from 10 Mbps to 38 bps at 40 MIPS
- 4-deep First-In-First-Out (FIFO) Transmit Data Buffer
- 4-Deep FIFO Receive Data Buffer
- Parity, Framing and Buffer Overrun Error Detection
- Support for 9-bit mode with Address Detect (9th bit = 1)
- Transmit and Receive Interrupts
- A Separate Interrupt for all UART Error Conditions
- · Loopback mode for Diagnostic Support
- Support for Sync and Break Characters
- Supports Automatic Baud Rate Detection
- IrDA<sup>®</sup> Encoder and Decoder Logic
- 16x Baud Clock Output for IrDA<sup>®</sup> Support

A simplified block diagram of the UART is shown in Figure 18-1. The UART module consists of the key important hardware elements:

- Baud Rate Generator
- Asynchronous Transmitter
- · Asynchronous Receiver





- **Note 1:** Both UART1 and UART2 can trigger a DMA data transfer. If U1TX, U1RX, U2TX or U2RX is selected as a DMA IRQ source, a DMA transfer occurs when the U1TXIF, U1RXIF, U2TXIF or U2RXIF bit gets set as a result of a UART1 or UART2 transmission or reception.
  - 2: If DMA transfers are required, the UART TX/RX FIFO buffer must be set to a size of 1 byte/word (i.e., UTXISEL<1:0> = 00 and URXISEL<1:0> = 00).

### REGISTER 19-18: CiFMSKSEL1: ECAN™ MODULE FILTER 7-0 MASK SELECTION REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F7MS	K<1:0>	F6MSK	<1:0>	F5MS	SK<1:0>	F4MSK<	:1:0>
bit 15							bit 8
					=		
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F3MS	K<1:0>	F2MSK	<1:0>	FIMS	5K<1:0>	FUMSK<	:1:0> hit 0
							DILU
Legend:							
R = Readable	bit	W = Writable b	oit	U = Unimpler	mented bit, rea	d as '0'	
-n = Value at I	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unknow	wn
bit 15-14	F7MSK<1:0> 11 = Reserver 10 = Acceptar 01 = Acceptar 00 = Acceptar	: Mask Source d; do not use nce Mask 2 reg nce Mask 1 reg nce Mask 0 reg	for Filter 7 b sters contair sters contair sters contair	it 1 mask 1 mask 1 mask			
bit 13-12	F6MSK<1:0> 11 = Reserver 10 = Acceptar 01 = Acceptar 00 = Acceptar	Mask Source d; do not use nce Mask 2 reg nce Mask 1 reg nce Mask 0 reg	for Filter 6 bi isters contair isters contair isters contair	it n mask n mask n mask			
bit 11-10	F5MSK<1:0> 11 = Reserver 10 = Acceptar 01 = Acceptar 00 = Acceptar	: Mask Source d; do not use nce Mask 2 reg nce Mask 1 reg nce Mask 0 reg	for Filter 5 bi isters contair isters contair isters contair	it n mask n mask n mask			
bit 9-8	F4MSK<1:0> 11 = Reserver 10 = Acceptar 01 = Acceptar 00 = Acceptar	: Mask Source d; do not use nce Mask 2 reg nce Mask 1 reg nce Mask 0 reg	for Filter 4 bi isters contair isters contair isters contair	it n mask n mask n mask			
bit 7-6	F3MSK<1:0> 11 = Reserver 10 = Acceptar 01 = Acceptar 00 = Acceptar	: Mask Source d; do not use nce Mask 2 reg nce Mask 1 reg nce Mask 0 reg	for Filter 3 bi isters contair isters contair isters contair	it n mask n mask n mask			
bit 5-4	<b>F2MSK&lt;1:0&gt;</b> 11 = Reserver 10 = Acceptar 01 = Acceptar 00 = Acceptar	: Mask Source d; do not use nce Mask 2 reg nce Mask 1 reg nce Mask 0 reg	for Filter 2 bi isters contair isters contair isters contair	it n mask n mask n mask			
bit 3-2	F1MSK<1:0> 11 = Reserver 10 = Acceptar 01 = Acceptar 00 = Acceptar	: Mask Source d; do not use nce Mask 2 reg nce Mask 1 reg nce Mask 0 reg	for Filter 1 bi isters contair isters contair isters contair	it n mask n mask n mask			
bit 1-0	FOMSK<1:0> 11 = Reserver 10 = Acceptar 01 = Acceptar 00 = Acceptar	: Mask Source d; do not use nce Mask 2 reg nce Mask 1 reg nce Mask 0 reg	for Filter 0 b sters contair sters contair sters contair	it n mask n mask n mask			

# 20.0 10-BIT/12-BIT ANALOG-TO-DIGITAL CONVERTER (ADC)

- Note 1: This data sheet summarizes the features of the PIC24HJXXXGPX06A/X08A/X10A family of devices. However, it is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the "dsPIC33F/PIC24H Family Reference Manual", Section 16. "Analog-to-Digital Converter (ADC)" (DS70183), which is available from the Microchip web site (www.microchip.com).
  - Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

The PIC24HJXXXGPX06A/X08A/X10A devices have up to 32 Analog-to-Digital input channels. These devices also have up to 2 Analog-to-Digital converter modules (ADCx, where 'x' = 1 or 2), each with its own set of Special Function Registers.

The AD12B bit (ADxCON1<10>) allows each of the ADC modules to be configured by the user as either a 10-bit, 4-sample/hold ADC (default configuration) or a 12-bit, 1-sample/hold ADC.

Note: The ADC module needs to be disabled before modifying the AD12B bit.

## 20.1 Key Features

The 10-bit ADC configuration has the following key features:

- Successive Approximation (SAR) conversion
- Conversion speeds of up to 1.1 Msps
- · Up to 32 analog input pins
- External voltage reference input pins
- Simultaneous sampling of up to four analog input pins
- Automatic Channel Scan mode
- Selectable conversion trigger source
- Selectable Buffer Fill modes
- Two result alignment options (signed/unsigned)
- · Operation during CPU Sleep and Idle modes

The 12-bit ADC configuration supports all the above features, except:

- In the 12-bit configuration, conversion speeds of up to 500 ksps are supported
- There is only 1 sample/hold amplifier in the 12-bit configuration, so simultaneous sampling of multiple channels is not supported.

Depending on the particular device pinout, the Analog-to-Digital Converter can have up to 32 analog input pins, designated AN0 through AN31. In addition, there are two analog input pins for external voltage reference connections. These voltage reference inputs may be shared with other analog input pins. The actual number of analog input pins and external voltage reference input configuration will depend on the specific device.

A block diagram of the Analog-to-Digital Converter is shown in Figure 20-1.

### 20.2 Analog-to-Digital Initialization

The following configuration steps should be performed.

- 1. Configure the ADC module:
  - a) Select port pins as analog inputs (ADxPCFGH<15:0> or ADxPCFGL<15:0>)
  - b) Select voltage reference source to match expected range on analog inputs (ADxCON2<15:13>)
  - c) Select the analog conversion clock to match desired data rate with processor clock (ADxCON3<7:0>)
  - d) Determine how many S/H channels will be used (ADxCON2<9:8> and ADxPCFGH<15:0> or ADxPCFGL<15:0>)
  - e) Select the appropriate sample/conversion sequence (ADxCON1<7:5> and ADxCON3<12:8>)
  - f) Select how conversion results are presented in the buffer (ADxCON1<9:8>)
  - g) Turn on the ADC module (ADxCON1<15>)
  - Configure ADC interrupt (if required):
  - a) Clear the ADxIF bit

2.

b) Select ADC interrupt priority

## 20.3 ADC and DMA

If more than one conversion result needs to be buffered before triggering an interrupt, DMA data transfers can be used. Both ADC1 and ADC2 can trigger a DMA data transfer. If ADC1 or ADC2 is selected as the DMA IRQ source, a DMA transfer occurs when the AD1IF or AD2IF bit gets set as a result of an ADC1 or ADC2 sample conversion sequence.

The SMPI<3:0> bits (ADxCON2<5:2>) are used to select how often the DMA RAM buffer pointer is incremented.

The ADDMABM bit (ADxCON1<12>) determines how the conversion results are filled in the DMA RAM buffer area being used for ADC. If this bit is set, DMA buffers are written in the order of conversion. The module will provide an address to the DMA channel that is the same as the address used for the non-DMA stand-alone buffer. If the ADDMABM bit is cleared, the DMA buffers are written in Scatter/Gather mode. The module will provide a scatter/gather address to the DMA channel, based on the index of the analog input and the size of the DMA buffer.





TABLE 24-29:	SPIX MASTER MODE	(HALF-DUPLEX,	TRANSMIT ONLY	) TIMING REQUIREMENTS
--------------	------------------	---------------	---------------	-----------------------

AC CHARACTERISTICS			$\label{eq:constraint} \begin{array}{l} \mbox{Standard Operating Conditions: 3.0V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ & -40^{\circ}C \leq TA \leq +125^{\circ}C \mbox{ for Extended} \end{array}$				
Param No.	Symbol	Characteristic <sup>(1)</sup>	Min	Typ <sup>(2)</sup>	Max	Units	Conditions
SP10	TscP	Maximum SCK Frequency	—	_	15	MHz	See Note 3
SP20	TscF	SCKx Output Fall Time	—	—	_	ns	See parameter DO32 and <b>Note 4</b>
SP21	TscR	SCKx Output Rise Time	—	—	_	ns	See parameter DO31 and <b>Note 4</b>
SP30	TdoF	SDOx Data Output Fall Time	_	—	_	ns	See parameter DO32 and <b>Note 4</b>
SP31	TdoR	SDOx Data Output Rise Time	_	-		ns	See parameter DO31 and <b>Note 4</b>
SP35	TscH2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	_	6	20	ns	—
SP36	TdiV2scH, TdiV2scL	SDOx Data Output Setup to First SCKx Edge	30	—	—	ns	_

Note 1: These parameters are characterized, but are not tested in manufacturing.

2: Data in "Typ" column is at 3.3V, 25°C unless otherwise stated.

**3:** The minimum clock period for SCKx is 66.7 ns. Therefore, the clock generated in Master mode must not violate this specification.

4: Assumes 50 pF load on all SPIx pins.



# FIGURE 24-15: SPIX SLAVE MODE (FULL-DUPLEX CKE = 0, CKP = 1, SMP = 0) TIMING CHARACTERISTICS

# 64-Lead Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body [QFN] With 0.40 mm Contact Length

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	MILLIMETERS					
Dimension	MIN	NOM	MAX			
Contact Pitch	Contact Pitch E		0.50 BSC			
Optional Center Pad Width	W2			7.35		
Optional Center Pad Length	T2			7.35		
Contact Pad Spacing	C1		8.90			
Contact Pad Spacing	C2		8.90			
Contact Pad Width (X64)	X1			0.30		
Contact Pad Length (X64)	Y1			0.85		
Distance Between Pads	G	0.20				

#### Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2149A