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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

E·XEI

Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	40 MIPs
Connectivity	I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	85
Program Memory Size	128KB (43K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16К х 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 32x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24hj128gp310at-i-pt

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Pin Name	Pin Type	Buffer Type	Description
AN0-AN31	I	Analog	Analog input channels.
AVDD	Р	Р	Positive supply for analog modules. This pin must be connected at all times.
AVss	Р	Р	Ground reference for analog modules.
CLKI CLKO	I O	ST/CMOS	External clock source input. Always associated with OSC1 pin function. Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes. Always associated with OSC2 pin function.
CN0-CN23	I	ST	Input change notification inputs. Can be software programmed for internal weak pull-ups on all inputs.
C1RX C1TX C2RX	 0 	ST — ST	ECAN1 bus receive pin. ECAN1 bus transmit pin. ECAN2 bus receive pin.
C2TX	0	_	ECAN2 bus transmit pin.
PGED1 PGEC1 PGED2 PGEC2 PGED3 PGEC3	I/O I I/O I I/O I	ST ST ST ST ST ST	Data I/O pin for programming/debugging communication channel 1. Clock input pin for programming/debugging communication channel 1. Data I/O pin for programming/debugging communication channel 2. Clock input pin for programming/debugging communication channel 2. Data I/O pin for programming/debugging communication channel 3. Clock input pin for programming/debugging communication channel 3.
IC1-IC8	I	ST	Capture inputs 1 through 8.
INT0 INT1 INT2 INT3 INT4		ST ST ST ST ST	External interrupt 0. External interrupt 1. External interrupt 2. External interrupt 3. External interrupt 4.
MCLR	I/P	ST	Master Clear (Reset) input. This pin is an active-low Reset to the device
OCFA OCFB OC1-OC8	 0	ST ST —	Compare Fault A input (for Compare Channels 1, 2, 3 and 4). Compare Fault B input (for Compare Channels 5, 6, 7 and 8). Compare outputs 1 through 8.
OSC1 OSC2	 /O	ST/CMOS	Oscillator crystal input. ST buffer when configured in RC mode; CMOS otherwise. Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes.
RA0-RA7 RA9-RA10 RA12-RA15	I/O I/O I/O	ST ST ST	PORTA is a bidirectional I/O port.
RB0-RB15	I/O	ST	PORTB is a bidirectional I/O port.
RC1-RC4 RC12-RC15	I/O I/O	ST ST	PORTC is a bidirectional I/O port.
RD0-RD15	I/O	ST	PORTD is a bidirectional I/O port.
RE0-RE7	I/O	ST	PORTE is a bidirectional I/O port.
RF0-RF8 RF12-RF13	I/O	ST	PORTF is a bidirectional I/O port.
RG0-RG3 RG6-RG9 RG12-RG15	1/0 1/0 1/0	ST ST ST	PORTG is a bidirectional I/O port.

TABLE 1-1: PINOUT I/O DESCRIPTIONS

Legend: CMOS = CMOS compatible input or output ST = Schmitt Trigger input with CMOS levels Analog = Analog input P = Powe O = Output I = Input

2.0 GUIDELINES FOR GETTING STARTED WITH 16-BIT MICROCONTROLLERS

- Note 1: This data sheet summarizes the features of the PIC24HJXXXGPX06A/X08A/X10A family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the "dsPIC33F/PIC24H Family Reference Manual". Please see the Microchip web site (www.microchip.com) for the latest dsPIC33F/PIC24H Family Reference Manual sections.
 - 2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

2.1 Basic Connection Requirements

Getting started with the PIC24HJXXXGPX06A/X08A/X10A family of 16-bit Microcontrollers (MCUs) requires attention to a minimal set of device pin connections before proceeding with development. The following is a list of pin names, which must always be connected:

- All VDD and Vss pins (see Section 2.2 "Decoupling Capacitors")
- All AVDD and AVSS pins (regardless if ADC module is not used)
- (see Section 2.2 "Decoupling Capacitors") VCAP
- (see Section 2.3 "CPU Logic Filter Capacitor Connection (VCAP)")
- MCLR pin (see Section 2.4 "Master Clear (MCLR) Pin")
- PGECx/PGEDx pins used for In-Circuit Serial Programming[™] (ICSP[™]) and debugging purposes (see **Section 2.5 "ICSP Pins**")
- OSC1 and OSC2 pins when external oscillator source is used

(see Section 2.6 "External Oscillator Pins")

Additionally, the following pins may be required:

• VREF+/VREF- pins used when external voltage reference for ADC module is implemented

Note:	The	AVdd	and	AVss	pins	mus	st be
	connected		independent		of	the	ADC
	volta	ge refe	rence	source.			

2.2 Decoupling Capacitors

The use of decoupling capacitors on every pair of power supply pins, such as VDD, VSS, AVDD and AVSS is required.

Consider the following criteria when using decoupling capacitors:

- Value and type of capacitor: Recommendation of 0.1 μ F (100 nF), 10-20V. This capacitor should be a low-ESR and have resonance frequency in the range of 20 MHz and higher. It is recommended that ceramic capacitors be used.
- Placement on the printed circuit board: The decoupling capacitors should be placed as close to the pins as possible. It is recommended to place the capacitors on the same side of the board as the device. If space is constricted, the capacitor can be placed on another layer on the PCB using a via; however, ensure that the trace length from the pin to the capacitor is within one-quarter inch (6 mm) in length.
- Handling high frequency noise: If the board is experiencing high frequency noise, upward of tens of MHz, add a second ceramic-type capacitor in parallel to the above described decoupling capacitor. The value of the second capacitor can be in the range of 0.01 μ F to 0.001 μ F. Place this second capacitor next to the primary decoupling capacitor. In high-speed circuit designs, consider implementing a decade pair of capacitances as close to the power and ground pins as possible. For example, 0.1 μ F in parallel with 0.001 μ F.
- **Maximizing performance:** On the board layout from the power supply circuit, run the power and return traces to the decoupling capacitors first, and then to the device pins. This ensures that the decoupling capacitors are first in the power chain. Equally important is to keep the trace length between the capacitor and the power pins to a minimum thereby reducing PCB track inductance.

For remapping operations, the 8-bit Program Space Visibility register (PSVPAG) is used to define a 16K word page in the program space. When the Most Significant bit of the EA is '1', PSVPAG is concatenated with the lower 15 bits of the EA to form a 23-bit program space address. Unlike table operations, this limits remapping operations strictly to the user memory area. Table 4-35 and Figure 4-6 show how the program EA is created for table operations and remapping accesses from the data EA. Here, P<23:0> refers to a program space word, whereas D<15:0> refers to a data space word.

TABLE 4-35: PROGRAM SPACE ADDRESS CONSTRUCTION

	Access	Program Space Address						
Access Type	Space	<23>	<22:16>	<15>	<14:1>	<0>		
Instruction Access	User	0 PC<22:1>				0		
(Code Execution)		0xxx xxxx xxxx xxxx xxxx						
TBLRD/TBLWT (Byte/Word Read/Write)	User	TB	LPAG<7:0>	Data EA<15:0>				
		0xxx xxxx xxxx xxxx xxxx						
	Configuration	TBLPAG<7:0>		Data EA<15:0>				
		1xxx xxxx xxxx xxxx xxxx xxxx						
Program Space Visibility (Block Remap/Read)	User	0 PSVPAG<		7:0> Data EA<14:0> ⁽¹⁾		0> ⁽¹⁾		
		0	xxxx xxxx		xxx xxxx xxxx xxxx			

Note 1: Data EA<15> is always '1' in this case, but is not used in calculating the program space address. Bit 15 of the address is PSVPAG<0>.

5.0 FLASH PROGRAM MEMORY

- Note 1: This data sheet summarizes the features of the PIC24HJXXXGPX06A/X08A/X10A family of devices. However, it is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 5. "Flash Programming" (DS70191) of the "dsPIC33F/PIC24H Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
 - 2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

The PIC24HJXXXGPX06A/X08A/X10A devices contain internal Flash program memory for storing and executing application code. The memory is readable, writable and erasable during normal operation over the entire VDD range.

Flash memory can be programmed in two ways:

- In-Circuit Serial Programming[™] (ICSP[™]) programming capability
- 2. Run-Time Self-Programming (RTSP)

ICSP programming capability allows a PIC24HJXXXGPX06A/X08A/X10A device to be serially programmed while in the end application circuit. This is simply done with two lines for programming clock and programming data (one of the alternate programming pin pairs: PGECx/PGEDx, and three other lines for power (VDD), ground (VSS) and Master Clear (MCLR). This allows customers to manufacture boards with unprogrammed devices and then program the digital signal controller just before shipping the product. This also allows the most recent firmware or a custom firmware to be programmed.

RTSP is accomplished using TBLRD (table read) and TBLWT (table write) instructions. With RTSP, the user can write program memory data either in blocks or 'rows' of 64 instructions (192 bytes) at a time, or single instructions and erase program memory in blocks or 'pages' of 512 instructions (1536 bytes) at a time.

5.1 Table Instructions and Flash Programming

Regardless of the method used, all programming of Flash memory is done with the table read and table write instructions. These allow direct read and write access to the program memory space from the data memory while the device is in normal operating mode. The 24-bit target address in the program memory is formed using bits<7:0> of the TBLPAG register and the Effective Address (EA) from a W register specified in the table instruction, as shown in Figure 5-1.

The TBLRDL and the TBLWTL instructions are used to read or write to bits<15:0> of program memory. TBLRDL and TBLWTL can access program memory in both Word and Byte modes.

The TBLRDH and TBLWTH instructions are used to read or write to bits<23:16> of program memory. TBLRDH and TBLWTH can also access program memory in Word or Byte mode.

FIGURE 5-1: ADDRESSING FOR TABLE REGISTERS



5.4.1 PROGRAMMING ALGORITHM FOR FLASH PROGRAM MEMORY

The user can program one row of program Flash memory at a time. To do this, it is necessary to erase the 8-row erase page that contains the desired row. The general process is:

- 1. Read eight rows of program memory (512 instructions) and store in data RAM.
- 2. Update the program data in RAM with the desired new data.
- 3. Erase the page (see Example 5-1):
 - a) Set the NVMOP bits (NVMCON<3:0>) to '0010' to configure for block erase. Set the ERASE (NVMCON<6>) and WREN (NVMCON<14>) bits.
 - b) Write the starting address of the page to be erased into the TBLPAG and W registers.
 - Perform a dummy table write operation (TBLWTL) to any address within the page that needs to be erased.
 - d) Write 0x55 to NVMKEY.
 - e) Write 0xAA to NVMKEY.
 - f) Set the WR bit (NVMCON<15>). The erase cycle begins and the CPU stalls for the duration of the erase cycle. When the erase is done, the WR bit is cleared automatically.

- 4. Write the first 64 instructions from data RAM into the program memory buffers (see Example 5-2).
- 5. Write the program block to Flash memory:
 - a) Set the NVMOP bits to '0001' to configure for row programming. Clear the ERASE bit and set the WREN bit.
 - b) Write 0x55 to NVMKEY.
 - c) Write 0xAA to NVMKEY.
 - d) Set the WR bit. The programming cycle begins and the CPU stalls for the duration of the write cycle. When the write to Flash memory is done, the WR bit is cleared automatically.
- Repeat steps 4 and 5, using the next available 64 instructions from the block in data RAM by incrementing the value in TBLPAG, until all 512 instructions are written back to Flash memory.

For protection against accidental operations, the write initiate sequence for NVMKEY must be used to allow any erase or program operation to proceed. After the programming command has been executed, the user must wait for the programming time until programming is complete. The two instructions following the start of the programming sequence should be NOPS, as shown in Example 5-3.

EXAMPLE 5-1: ERASING A PROGRAM MEMORY PAGE

; Set up NVMCON for block erase opera	tion
MOV #0x4042, W0	;
MOV W0, NVMCON	; Initialize NVMCON
; Init pointer to row to be ERASED	
MOV #tblpage(PROG_ADDR), W	0 ;
MOV W0, TBLPAG	; Initialize PM Page Boundary SFR
MOV #tbloffset(PROG_ADDR),	W0 ; Initialize in-page EA<15:0> pointer
TBLWTL W0, [W0]	; Set base address of erase block
DISI #5	; Block all interrupts with priority <7
	; for next 5 instructions
MOV #0x55, W0	
MOV W0, NVMKEY	; Write the 55 key
MOV #0xAA, W1	;
MOV W1, NVMKEY	; Write the AA key
BSET NVMCON, #WR	; Start the erase sequence
NOP	; Insert two NOPs after the erase
NOP	; command is asserted

Note: A program memory page erase operation is set up by performing a dummy table write (TBLWTL) operation to any address within the page. This methodology is different from the page erase operation on dsPIC30F/33F devices in which the erase page was selected using a dedicated pair of registers (NVMADRU and NVMADR).

R/W-0	R-0	U-0	U-0	U-0	U-0	U-0	U-0		
ALTIVT	DISI		_	_	—	—	—		
bit 15	15 b								
U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
—	—		INT4EP	INT3EP	INT2EP	INT1EP	INT0EP		
bit 7							bit 0		
Legend:									
R = Readable	bit	W = Writable	bit	U = Unimplei	mented bit, read	as '0'			
-n = Value at I	POR	'1' = Bit is set		'0' = Bit is cle	eared	x = Bit is unkr	nown		
bit 15	ALTIVT: Enat	ole Alternate In	terrupt Vector	Table bit					
	1 = Use alterr	nate vector tab	le						
	0 = Use stand	lard (default) v	ector table						
bit 14	DISI: DISI In	struction Statu	s bit						
	1 = DISI Inst	ruction is activ	e Ictive						
bit 13-5		ted: Read as '	0'						
bit 4	INT4FP: Exte	rnal Interrunt 4	• 1 Edge Detect	Polarity Selec	t bit				
bit i	1 = Interrupt of	on negative ed	ae	r olarity coloo					
	0 = Interrupt o	on positive edg	le						
bit 3	INT3EP: Exte	ernal Interrupt 3	B Edge Detect	Polarity Selec	t bit				
	1 = Interrupt o	on negative ed	ge						
	0 = Interrupt o	on positive edg	е						
bit 2	INT2EP: Exte	ernal Interrupt 2	2 Edge Detect	Polarity Selec	t bit				
	1 = Interrupt o	on negative ed	ge						
hit 1		an positive edg	l Edgo Dotoct	Polarity Soloo	t hit				
DIL	1 = Interrupt	INITEP: External Interrupt 1 Edge Detect Polarity Select bit							
	0 = Interrupt of	on positive edg	le						
bit 0	INT0EP: Exte	ernal Interrupt () Edge Detect	Polarity Selec	t bit				
	1 = Interrupt o	on negative ed	ge	2					
	0 = Interrupt o	on positive edg	e						

REGISTER 7-4: INTCON2: INTERRUPT CONTROL REGISTER 2

REGISTER 7-17: IPC2: INTERRUPT PRIORITY CONTROL REGISTER 2

r							,
U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—		U1RXIP<2:0>		—		SPI1IP<2:0>	
bit 15							bit 8
U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
		SPI1EIP<2:0>				T3IP<2:0>	
bit 7							bit 0
Legend:							
R = Readable	e bit	W = Writable	bit	U = Unimplei	mented bit, rea	ad as '0'	
-n = Value at	POR	'1' = Bit is set		'0' = Bit is cle	eared	x = Bit is unkn	iown
							J
bit 15	Unimplem	ented: Read as ')'				
bit 14-12	U1RXIP<2	:0>: UART1 Rece	iver Interrupt	Priority bits			
	111 = Inter	rrupt is priority 7 (I	niahest priori	tv interrupt)			
	•	-FF2 (J	- J			
	•						
	• 001 - Intor	rupt is priority 1					
	001 = Inter	rrupt is priority i	abled				
bit 11	Unimplem	ented: Read as ')'				
bit 10-8	SPI1IP<2:0	0>: SPI1 Event Int	errupt Priorit	v bits			
	111 = Inter	rrupt is priority 7 (I	niahest priori	tv interrupt)			
	•			·) ······			
	•						
	• 001 - Intor	rupt is priority 1					
	001 - Inter	rrupt is priority i rrupt source is dis	abled				
bit 7	Unimplem	ented: Read as ')'				
bit 6-4	SPI1EIP<2	2:0>: SPI1 Frror Ir	Iterrupt Priori	tv bits			
	111 = Inter	rrupt is priority 7 (I	niahest priori	ty interrupt)			
	•		J	- J			
	•						
	• 001 - Intor	rupt is priority 1					
	001 = Inter	rrupt is priority i rrupt source is dis	abled				
bit 3	Unimplem	ented: Read as ')'				
bit 2-0	T3IP<2:0>	: Timer3 Interrupt	Priority bits				
5112 0	111 = Inter	rrupt is priority 7 (I	niahest priorit	tv interrupt)			
	•			·) ······			
	•						
	•	ruptic priority 4					
	001 = inter	rrupt is priority 1	abled				

NOTES:

NOTES:

FIGURE 17-1: $I^2 C^{TM}$ BLOCK DIAGRAM (x = 1 OR 2)



U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0		
—			_	_		_			
bit 15							bit 8		
R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0		
IVRIE	WAKIE	ERRIE		FIFOIE	RBOVIE	RBIE	TBIE		
bit 7							bit 0		
Legend:									
R = Readab	le bit	W = Writable	bit	U = Unimpler	nented bit, read	as '0'			
-n = Value a	t POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unk	nown		
bit 15-8	Unimplemen	ted: Read as '	0'						
bit 7	IVRIE: Invalio	d Message Inte	rrupt Enable b	bit					
	1 = Interrupt i	request enable	d bled						
bit 6	WAKIE: Bus	Wake-up Activi	tv Interrupt Fr	hable bit					
bit o	1 = Interrupt	request enable	d						
	0 = Interrupt	request not ena	abled						
bit 5	ERRIE: Error	Interrupt Enab	le bit						
	1 = Interrupt	request enable	d						
hit 4	Unimplemen	ited: Read as '							
bit 3	FIFOIF: FIFO) Almost Full In	∘ terrupt Enable	e bit					
Sit 0	1 = Interrupt	request enable	d						
	0 = Interrupt	request not ena	abled						
bit 2	RBOVIE: RX	Buffer Overflov	w Interrupt En	able bit					
	1 = Interrupt	request enable	d blod						
hit 1	BBIE: BX Bu	iffer Interrupt Fi	nable hit						
	1 = Interrupt	RBIE: RX Buffer Interrupt Enable bit 1 = Interrupt request enabled							
	0 = Interrupt	request not ena	abled						
bit 0	TBIE: TX Buf	ffer Interrupt Er	able bit						
	1 = Interrupt	request enable	d						
	0 = merrupt i	0 = Interrupt request not enabled							

REGISTER 19-7: CIINTE: ECAN™ MODULE INTERRUPT ENABLE REGISTER

REGISTER 20-9: AD1PCFGH: ADC1 PORT CONFIGURATION REGISTER HIGH^(1,2,3,4)

| R/W-0 |
|--------|--------|--------|--------|--------|--------|--------|---------|
| PCFG31 | PCFG30 | PCFG29 | PCFG28 | PCFG27 | PCFG26 | PCFG25 | PCFG24 |
| bit 15 | | | | | | | bit 8 |
| | | | | | | | |
| R/W-0 | R/\\/_0 |

| R/W-0 |
|--------|--------|--------|--------|--------|--------|--------|--------|
| PCFG23 | PCFG22 | PCFG21 | PCFG20 | PCFG19 | PCFG18 | PCFG17 | PCFG16 |
| bit 7 | | | | | | | bit 0 |

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	d as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 PCFG<31:16>: ADC Port Configuration Control bits

- 1 = Port pin in Digital mode, port read input enabled, ADC input multiplexer connected to AVss
- 0 = Port pin in Analog mode, port read input disabled, ADC samples pin voltage
- **Note 1:** On devices without 32 analog inputs, all PCFG bits are R/W by user. However, PCFG bits are ignored on ports without a corresponding input on device.
 - 2: ADC2 only supports analog inputs AN0-AN15; therefore, no ADC2 high port Configuration register exists.
 - **3:** PCFGx = ANx, where x = 16 through 31.
 - **4:** PCFGx bits will have no effect if ADC module is disabled by setting ADxMD bit in the PMDx register. In this case all port pins multiplexed with ANx will be in Digital mode.

Bit Field	Register	RTSP Effect	Description
BWRP	FBS	Immediate	Boot Segment Program Flash Write Protection 1 = Boot segment may be written 0 = Boot segment is write-protected
BSS<2:0>	FBS	Immediate	Boot Segment Program Flash Code Protection Size x11 = No Boot program Flash segment
			Boot space is 1K IW less VS 110 = Standard security; boot program Flash segment starts at End of VS, ends at 0x0007FE 010 = High security; boot program Flash segment starts at End of VS, ends at 0x0007FE
			Boot space is 4K IW less VS 101 = Standard security; boot program Flash segment starts at End of VS, ends at 0x001FFE 001 = High security; boot program Flash segment starts at End of VS, ends at 0x001FFE
			Boot space is 8K IW less VS 100 = Standard security; boot program Flash segment starts at End of VS, ends at 0x003FFE 000 = High security; boot program Flash segment starts at End of VS, ends at 0x003FFE
RBS<1:0>	FBS	Immediate	Boot Segment RAM Code Protection 11 = No Boot RAM defined 10 = Boot RAM is 128 Bytes 01 = Boot RAM is 256 Bytes 00 = Boot RAM is 1024 Bytes
SWRP	FSS	Immediate	Secure Segment Program Flash Write Protection 1 = Secure segment may be written 0 = Secure segment is write-protected

TABLE 21-2: CONFIGURATION BITS DESCRIPTION

23.7 MPLAB SIM Software Simulator

The MPLAB SIM Software Simulator allows code development in a PC-hosted environment by simulating the PIC MCUs and dsPIC[®] DSCs on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a comprehensive stimulus controller. Registers can be logged to files for further run-time analysis. The trace buffer and logic analyzer display extend the power of the simulator to record and track program execution, actions on I/O, most peripherals and internal registers.

The MPLAB SIM Software Simulator fully supports symbolic debugging using the MPLAB C Compilers, and the MPASM and MPLAB Assemblers. The software simulator offers the flexibility to develop and debug code outside of the hardware laboratory environment, making it an excellent, economical software development tool.

23.8 MPLAB REAL ICE In-Circuit Emulator System

MPLAB REAL ICE In-Circuit Emulator System is Microchip's next generation high-speed emulator for Microchip Flash DSC and MCU devices. It debugs and programs PIC[®] Flash MCUs and dsPIC[®] Flash DSCs with the easy-to-use, powerful graphical user interface of the MPLAB Integrated Development Environment (IDE), included with each kit.

The emulator is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with either a connector compatible with incircuit debugger systems (RJ11) or with the new high-speed, noise tolerant, Low-Voltage Differential Signal (LVDS) interconnection (CAT5).

The emulator is field upgradable through future firmware downloads in MPLAB IDE. In upcoming releases of MPLAB IDE, new devices will be supported, and new features will be added. MPLAB REAL ICE offers significant advantages over competitive emulators including low-cost, full-speed emulation, run-time variable watches, trace analysis, complex breakpoints, a ruggedized probe interface and long (up to three meters) interconnection cables.

23.9 MPLAB ICD 3 In-Circuit Debugger System

MPLAB ICD 3 In-Circuit Debugger System is Microchip's most cost effective high-speed hardware debugger/programmer for Microchip Flash Digital Signal Controller (DSC) and microcontroller (MCU) devices. It debugs and programs PIC[®] Flash microcontrollers and dsPIC[®] DSCs with the powerful, yet easyto-use graphical user interface of MPLAB Integrated Development Environment (IDE).

The MPLAB ICD 3 In-Circuit Debugger probe is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with a connector compatible with the MPLAB ICD 2 or MPLAB REAL ICE systems (RJ-11). MPLAB ICD 3 supports all MPLAB ICD 2 headers.

23.10 PICkit 3 In-Circuit Debugger/ Programmer and PICkit 3 Debug Express

The MPLAB PICkit 3 allows debugging and programming of PIC[®] and dsPIC[®] Flash microcontrollers at a most affordable price point using the powerful graphical user interface of the MPLAB Integrated Development Environment (IDE). The MPLAB PICkit 3 is connected to the design engineer's PC using a full speed USB interface and can be connected to the target via an Microchip debug (RJ-11) connector (compatible with MPLAB ICD 3 and MPLAB REAL ICE). The connector uses two device I/O pins and the reset line to implement in-circuit debugging and In-Circuit Serial Programming[™].

The PICkit 3 Debug Express include the PICkit 3, demo board and microcontroller, hookup cables and CDROM with user's guide, lessons, tutorial, compiler and MPLAB IDE software.

24.1 DC Characteristics

Characteristic	VDD Range	Temp Range	Max MIPS		
Characteristic	(in Volts)	(in °C)	PIC24HJXXXGPX06A/X08A/X10		
—	VBOR-3.6V ⁽¹⁾	-40°C to +85°C	40		
_	VBOR-3.6V ⁽¹⁾	-40°C to +125°C	40		

TABLE 24-1: OPERATING MIPS VS. VOLTAGE

Note 1: Device is functional at VBORMIN < VDD < VDDMIN. Analog modules such as the ADC will have degraded performance. Device functionality is tested but not characterized. Refer to parameter BO10 in Table 24-11 for the minimum and maximum BOR values.

TABLE 24-2: THERMAL OPERATING CONDITIONS

Rating	Symbol	Min	Тур	Max	Unit
Industrial Temperature Devices					
Operating Junction Temperature Range	TJ	-40	—	+125	°C
Operating Ambient Temperature Range	TA	-40	—	+85	°C
Extended Temperature Devices					
Operating Junction Temperature Range	TJ	-40	—	+150	°C
Operating Ambient Temperature Range	TA	-40	—	+125	°C
Power Dissipation: Internal chip power dissipation: $PINT = VDD x (IDD - \Sigma IOH)$ I/O Pin Power Dissipation:		Pint + Pi/o		W	
$I/O = \Sigma (\{VDD - VOH\} \times IOH) + \Sigma (VOL \times IOL)$					
Maximum Allowed Power Dissipation	PDMAX	(TJ — TA)/θJ	IA	W

TABLE 24-3: THERMAL PACKAGING CHARACTERISTICS

Characteristic	Symbol	Тур	Max	Unit	Notes
Package Thermal Resistance, 100-pin TQFP (14x14x1 mm)	θja	40	—	°C/W	1
Package Thermal Resistance, 100-pin TQFP (12x12x1 mm)	θja	40	—	°C/W	1
Package Thermal Resistance, 64-pin TQFP (10x10x1 mm)	θја	40	_	°C/W	1
Package Thermal Resistance, 64-pin QFN (9x9x0.9 mm)	θја	28	—	°C/W	1

Note 1: Junction to ambient thermal resistance, Theta-JA (θ JA) numbers are achieved by package simulations.

TABLE 24-7: DC CHARACTERISTICS: POWER-DOWN CURRENT (IPD)

DC CHARACT	ERISTICS		$\begin{array}{llllllllllllllllllllllllllllllllllll$						
Parameter No. ⁽³⁾	Typical ⁽²⁾	Мах	Units	Units Conditions					
Power-Down Current (IPD) ⁽¹⁾									
DC60d	50	200	μA	-40°C					
DC60a	50	200	μA	+25°C	2 2\/	Race Rower Down Current ⁽³⁾			
DC60b	200	500	μA	+85°C	3.3V	Base Fower-Down Current			
DC60c	600	1000	μA	+125°C					
DC61d	8	13	μΑ	-40°C					
DC61a	10	15	μA	+25°C	2 21/	Watchdog Timor Current: Alwot(3)			
DC61b	12	20	μA	+85°C	3.3V				
DC61c	13	25	μA	+125°C					

Note 1: IPD (Sleep) current is measured as follows:

- CPU core is off, oscillator is configured in EC mode and external clock active, OSC1 is driven with external square wave from rail-to-rail (EC clock overshoot/undershoot < 250 mV required)
- CLKO is configured as an I/O input pin in the Configuration word
- · All I/O pins are configured as inputs and pulled to Vss
- MCLR = VDD, WDT and FSCM are disabled, all peripheral modules except the ADC are disabled (PMDx bits are all '1's). The following ADC settings are enabled for each ADC module (ADCx) prior to executing the PWRSAV instruction: ADON = 1, VCFG = 1, AD12B = 1 and ADxMD = 0.
- VREGS bit (RCON<8>) = 0 (i.e., core regulator is set to stand-by while the device is in Sleep mode)
- RTCC is disabled.
- JTAG is disabled
- 2: Data in the "Typ" column is at 3.3V, +25°C unless otherwise stated.
- **3:** The Watchdog Timer Current is the additional current consumed when the WDT module is enabled. This current should be added to the base IPD current.
- 4: These currents are measured on the device containing the most memory in this family.
- 5: These parameters are characterized, but are not tested in manufacturing.

AC CHARACTERISTICS			$\begin{tabular}{lllllllllllllllllllllllllllllllllll$							
Param No.	Symbo I	Characteristic	Min.	Min. Typ Max. U			Conditions			
	Device Supply									
AD01	AVDD	Module VDD Supply	Greater of VDD – 0.3 or 3.0	_	Lesser of VDD + 0.3 or 3.6	V	_			
AD02	AVss	Module Vss Supply	Vss – 0.3	—	Vss + 0.3	V	_			
			Referen	ce Inpu	its					
AD05	VREFH	Reference Voltage High	AVss + 2.5	—	AVDD	V				
AD05a			3.0	—	3.6	V	Vrefh = AVdd Vrefl = AVss = 0			
AD06	Vrefl	Reference Voltage Low	AVss	-	AVDD – 2.5	V				
AD06a			0	_	0	V	Vrefh = AVdd Vrefl = AVss = 0			
AD07	Vref	Absolute Reference Voltage	2.5	—	3.6	V	VREF = VREFH - VREFL			
AD08	IREF	Current Drain	—	—	10	μA	ADC off			
AD08a	IAD	Operating Current	_	7.0 2.7	9.0 3.2	mA mA	10-bit ADC mode, See Note 1 12-bit ADC mode, See Note 1			
	-		Analo	g Input	-	_				
AD12	VINH	Input Voltage Range VINH	Vinl	_	VREFH	V	This voltage reflects Sample and Hold Channels 0, 1, 2, and 3 (CH0-CH3), positive input			
AD13	VINL	Input Voltage Range VINL	VREFL	_	AVss + 1V	V	This voltage reflects Sample and Hold Channels 0, 1, 2, and 3 (CH0-CH3), negative input			
AD17	Rin	Recommended Imped- ance of Analog Voltage Source			200 200	Ω Ω	10-bit ADC 12-bit ADC			

TABLE 24-39: ADC MODULE SPECIFICATIONS

Note 1: These parameters are not characterized or tested in manufacturing.

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V(unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for High					
			Temperature					
Param.	Symbol	Characteristic	Min.	Тур.	Max.	Units	Conditions	
		Output Low Voltage I/O Pins: 2x Sink Driver Pins - All pins not defined by 4x or 8x driver pins	_	_	0.4	V	IOL ≤ 1.8 mA, VDD = 3.3V See Note 1	
HDO10	Vol	Output Low Voltage I/O Pins: 4x Sink Driver Pins - RA2, RA3, RA9, RA10, RA14, RA15, RB0, RB1, RB11, RF4, RF5, RG2, RG3	_	_	0.4	V	IOL ≤ 3.6 mA, VDD = 3.3V See Note 1	
		Output Low Voltage I/O Pins: 8x Sink Driver Pins - OSC2, CLKO, RC15	_	_	0.4	V	Io∟ ≤ 6 mA, Voo = 3.3V See Note 1	
HDO20		Output High Voltage I/O Pins: 2x Source Driver Pins - All pins not defined by 4x or 8x driver pins	2.4	_	_	V	IoL ≥ -1.8 mA, VDD = 3.3V See Note 1	
	Vон	Output High Voltage I/O Pins: 4x Source Driver Pins - RA2, RA3, RA9, RA10, RA14, RA15, RB0, RB1, RB11, RF4, RF5, RG2, RG3	2.4	_	_	V	Io∟ ≥ -3 mA, VDD = 3.3V See Note 1	
		Output High Voltage I/O Pins: 8x Source Driver Pins - OSC2, CLKO, RC15	2.4	_	_	V	Io∟ ≥ -6 mA, VDD = 3.3V See Note 1	
		Output High Voltage I/O Pins:	1.5	—	—	V	IOH ≥ -1.9 mA, VDD = 3.3V See Note 1	
		2x Source Driver Pins - All pins not defined by 4x or 8x driver pins	2.0	_			IOH ≥ -1.85 mA, VDD = 3.3V See Note 1	
			3.0	_	_		$\label{eq:IOH} \begin{array}{l} \text{IOH} \geq -1.4 \text{ mA, VDD} = 3.3 \text{V} \\ \text{See Note 1} \end{array}$	
		Output High Voltage 4x Source Driver Pins - RA2, RA3,	1.5	_			IOH ≥ -3.9 mA, VDD = 3.3V See Note 1	
HDO20A	Voh1	RA9, RA10, RA14, RA15, RB0, RB1, RB11, RF4, RF5, RG2, RG3	2.0	—	_	V	IOH ≥ -3.7 mA, VDD = 3.3V See Note 1	
		Output High Voltage 8x Source Driver Pins - OSC2, CLKO, RC15	3.0	_	_		IOH ≥ -2 mA, VDD = 3.3V See Note 1	
			1.5	_		V	IOH ≥ -7.5 mA, VDD = 3.3V See Note 1	
			2.0	_			IOH ≥ -6.8 mA, VDD = 3.3V See Note 1	
			3.0	—	_		IOH ≥ -3 mA, VDD = 3.3V See Note 1	

TABLE 25-6: DC CHARACTERISTICS: I/O PIN OUTPUT SPECIFICATIONS

Note 1: Parameters are characterized, but not tested.

27.2 Package Details

64-Lead Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body with 5.40 x 5.40 Exposed Pad [QFN]



Microchip Technology Drawing C04-154A Sheet 1 of 2

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