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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

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Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	20 MIPS
Connectivity	CANbus, I <sup>2</sup> C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	85
Program Memory Size	128KB (43K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 32x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 150°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24hj128gp510a-h-pf

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# **PIC24H PRODUCT FAMILIES**

The PIC24H Family of devices is ideal for a wide variety of 16-bit MCU embedded applications. The device names, pin counts, memory sizes and peripheral availability of each device are listed below, followed by their pinout diagrams.

## **PIC24H Family Controllers**

Device	Pins	Program Flash Memory (KB)	RAM <sup>(1)</sup> (KB)	DMA Channels	Timer 16-bit	Input Capture	Output Compare Std. PWM	Codec Interface	ADC	UART	SPI	I²C™	CAN	I/O Pins (Max) <sup>(2)</sup>	Packages
PIC24HJ64GP206A	64	64	8	8	9	8	8	0	1 ADC, 18 ch	2	2	1	0	53	PT, MR
PIC24HJ64GP210A	100	64	8	8	9	8	8	0	1 ADC, 32 ch	2	2	2	0	85	PF, PT
PIC24HJ64GP506A	64	64	8	8	9	8	8	0	1 ADC, 18 ch	2	2	2	1	53	PT, MR
PIC24HJ64GP510A	100	64	8	8	9	8	8	0	1 ADC, 32 ch	2	2	2	1	85	PF, PT
PIC24HJ128GP206A	64	128	8	8	9	8	8	0	1 ADC, 18 ch	2	2	2	0	53	PT, MR
PIC24HJ128GP210A	100	128	8	8	9	8	8	0	1 ADC, 32 ch	2	2	2	0	85	PF, PT
PIC24HJ128GP506A	64	128	8	8	9	8	8	0	1 ADC, 18 ch	2	2	2	1	53	PT, MR
PIC24HJ128GP510A	100	128	8	8	9	8	8	0	1 ADC, 32 ch	2	2	2	1	85	PF, PT
PIC24HJ128GP306A	64	128	16	8	9	8	8	0	1 ADC, 18 ch	2	2	2	0	53	PT, MR
PIC24HJ128GP310A	100	128	16	8	9	8	8	0	1 ADC, 32 ch	2	2	2	0	85	PF, PT
PIC24HJ256GP206A	64	256	16	8	9	8	8	0	1 ADC, 18 ch	2	2	2	0	53	PT, MR
PIC24HJ256GP210A	100	256	16	8	9	8	8	0	1 ADC, 32 ch	2	2	2	0	85	PF, PT
PIC24HJ256GP610A	100	256	16	8	9	8	8	0	2 ADC, 32 ch	2	2	2	2	85	PF, PT

Note 1: RAM size is inclusive of 2 Kbytes DMA RAM.

2: Maximum I/O pin count includes pins shared by the peripheral functions.

## 3.0 CPU

- Note 1: This data sheet summarizes the features of the PIC24HJXXXGPX06A/X08A/X10A family of devices. However, it is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 2. "CPU" (DS70204) of the "dsPIC33F/PIC24H Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
  - 2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The PIC24HJXXXGPX06A/X08A/X10A CPU module has a 16-bit (data) modified Harvard architecture with an enhanced instruction set and addressing modes. The CPU has a 24-bit instruction word with a variable length opcode field. The Program Counter (PC) is 23 bits wide and addresses up to 4M x 24 bits of user program memory space. The actual amount of program memory implemented varies by device. A single-cycle instruction prefetch mechanism is used to help maintain throughput and provides predictable execution. All instructions execute in a single cycle, with the exception of instructions that change the program flow, the double word move (MOV.D) instruction and the table instructions. Overhead-free, single-cycle program loop constructs are supported using the REPEAT instruction, which is interruptible at any point.

The PIC24HJXXXGPX06A/X08A/X10A devices have sixteen, 16-bit working registers in the programmer's model. Each of the working registers can serve as a data, address or address offset register. The 16th working register (W15) operates as a software Stack Pointer (SP) for interrupts and calls.

The PIC24HJXXXGPX06A/X08A/X10A instruction set includes many addressing modes and is designed for optimum C compiler efficiency. For most instructions, the PIC24HJXXXGPX06A/X08A/X10A is capable of executing a data (or program data) memory read, a working register (data) read, a data memory write and a program (instruction) memory read per instruction cycle. As a result, three parameter instructions can be supported, allowing A + B = C operations to be executed in a single cycle.

A block diagram of the CPU is shown in Figure 3-1, and the programmer's model for the PIC24HJXXXGPX06A/X08A/X10A is shown in Figure 3-2.

### 3.1 Data Addressing Overview

The data space can be linearly addressed as 32K words or 64 Kbytes using an Address Generation Unit (AGU). The upper 32 Kbytes of the data space memory map can optionally be mapped into program space at any 16K program word boundary defined by the 8-bit Program Space Visibility Page (PSVPAG) register. The program to data space mapping feature lets any instruction access program space as if it were data space.

The data space also includes 2 Kbytes of DMA RAM, which is primarily used for DMA data transfers, but may be used as general purpose RAM.

## 3.2 Special MCU Features

The PIC24HJXXXGPX06A/X08A/X10A features a 17-bit by 17-bit, single-cycle multiplier. The multiplier can perform signed, unsigned and mixed-sign multiplication. Using a 17-bit by 17-bit multiplier for 16-bit by 16-bit multiplication makes mixed-sign multiplication possible.

The PIC24HJXXXGPX06A/X08A/X10A supports 16/16 and 32/16 integer divide operations. All divide instructions are iterative operations. They must be executed within a REPEAT loop, resulting in a total execution time of 19 instruction cycles. The divide operation can be interrupted during any of those 19 cycles without loss of data.

A multi-bit data shifter is used to perform up to a 16-bit, left or right shift in a single cycle.

### TABLE 4-17: DMA REGISTER MAP

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
DMA0CON	0380	CHEN	SIZE	DIR	HALF	NULLW	—	—	—	—	-	AMOD	E<1:0>	-	—	MODE	<1:0>	0000
DMA0REQ	0382	FORCE	_	—	—	—	—	_	_	—			I	RQSEL<6:0	>			0000
DMA0STA	0384								S	STA<15:0>								0000
DMA0STB	0386								S	STB<15:0>								0000
DMA0PAD	0388								F	PAD<15:0>								0000
DMA0CNT	038A	_	—	—	_	—						CN	<9:0>					0000
DMA1CON	038C	CHEN	SIZE	DIR	HALF	NULLW			—	—	_	AMOD	E<1:0>	—	—	MODE	<1:0>	0000
DMA1REQ	038E	FORCE	—	—	_	—			—	—			I	RQSEL<6:0	>			0000
DMA1STA	0390								S	STA<15:0>								0000
DMA1STB	0392								S	STB<15:0>								0000
DMA1PAD	0394								F	PAD<15:0>								0000
DMA1CNT	0396	_	—	—	_	—						CN	<9:0>					0000
DMA2CON	0398	CHEN	SIZE	DIR	HALF	NULLW			—	—	_	AMOD	E<1:0>	—	—	MODE	<1:0>	0000
DMA2REQ	039A	FORCE	—	—	_	—			—	—			I	RQSEL<6:0	>			0000
DMA2STA	039C								S	STA<15:0>								0000
DMA2STB	039E								S	STB<15:0>								0000
DMA2PAD	03A0								F	PAD<15:0>								0000
DMA2CNT	03A2	—	—	—	—	—	—					CN	<9:0>					0000
DMA3CON	03A4	CHEN	SIZE	DIR	HALF	NULLW	—	—	—	—	—	AMOD	E<1:0>	—	—	MODE	<1:0>	0000
DMA3REQ	03A6	FORCE	—	—	—	—	—	—	—	—			I	RQSEL<6:0	>			0000
DMA3STA	03A8								S	STA<15:0>								0000
DMA3STB	03AA								S	STB<15:0>								0000
DMA3PAD	03AC								F	PAD<15:0>								0000
DMA3CNT	03AE	—	_	—	_	—						CN	<9:0>					0000
DMA4CON	03B0	CHEN	SIZE	DIR	HALF	NULLW			—	—	_	AMOD	E<1:0>	—	—	MODE	<1:0>	0000
DMA4REQ	03B2	FORCE	—	—	_	—			—	—			I	RQSEL<6:0	>			0000
DMA4STA	03B4								S	STA<15:0>								0000
DMA4STB	03B6								S	STB<15:0>								0000
DMA4PAD	03B8								F	PAD<15:0>								0000
DMA4CNT	03BA	_	—	—	_	—						CN	<9:0>					0000
DMA5CON	03BC	CHEN	SIZE	DIR	HALF	NULLW	_	_	_	_	_	AMOD	E<1:0>	_	_	MODE	<1:0>	0000
DMA5REQ	03BE	FORCE	—	—	—	_	—	—	—	_				RQSEL<6:0	>			0000
DMA5STA	03C0	STA<15:0> 0000																
DMA5STB	03C2								S	STB<15:0>								0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal for PinHigh devices.

#### 4.4.3 READING DATA FROM PROGRAM MEMORY USING PROGRAM SPACE VISIBILITY

The upper 32 Kbytes of data space may optionally be mapped into any 16K word page of the program space. This option provides transparent access of stored constant data from the data space without the need to use special instructions (i.e., TBLRDL/H).

Program space access through the data space occurs if the Most Significant bit of the data space EA is '1' and program space visibility is enabled by setting the PSV bit in the Core Control register (CORCON<2>). The location of the program memory space to be mapped into the data space is determined by the Program Space Visibility Page register (PSVPAG). This 8-bit register defines any one of 256 possible pages of 16K words in program space. In effect, PSVPAG functions as the upper 8 bits of the program memory address, with the 15 bits of the EA functioning as the lower bits. Note that by incrementing the PC by 2 for each program memory word, the lower 15 bits of data space addresses directly map to the lower 15 bits in the corresponding program space addresses.

Data reads to this area add an additional cycle to the instruction being executed, since two program memory fetches are required.

Although each data space address, 0x8000 and higher, maps directly into a corresponding program memory address (see Figure 4-8), only the lower 16 bits of the 24-bit program word are used to contain the data. The upper 8 bits of any program space location used as data should be programmed with '1111 1111' or '0000 0000' to force a NOP. This prevents possible issues should the area of code ever be accidentally executed.

Note:	PSV access is temporarily disabled during
	table reads/writes.

For operations that use PSV and are executed outside a REPEAT loop, the MOV and MOV.D instructions require one instruction cycle in addition to the specified execution time. All other instructions require two instruction cycles in addition to the specified execution time.

For operations that use PSV, which are executed inside a REPEAT loop, there will be some instances that require two instruction cycles in addition to the specified execution time of the instruction:

- · Execution in the first iteration
- · Execution in the last iteration
- Execution prior to exiting the loop due to an interrupt
- Execution upon re-entering the loop after an interrupt is serviced

Any other iteration of the REPEAT loop will allow the instruction accessing data, using PSV, to execute in a single cycle.

#### When CORCON < 2 > = 1 and EA < 15 > = 1: **Program Space Data Space PSVPAG** 15 0 0x000000 0x0000 02 Data EA<14:0> 0x010000 0x018000 The data in the page designated by **PSVPAG** is mapped into the upper half of the data memory 0x8000 space... **PSV** Area ...while the lower 15 bits of the EA specify an exact address within 0xFFFF the PSV area. This corresponds exactly to the same lower 15 bits of the actual program space address. 0x800000

#### FIGURE 4-8: PROGRAM SPACE VISIBILITY OPERATION

U-0	U-0	U-0	U-0	U-0	R/W-1	R/W-0	R/W-0
—	—	—	—	—		U2EIP<2:0>	
bit 15							bit 8
U-0	R/W-1	R/W-0	R/W-0	U-0	U-0	U-0	U-0
_		U1EIP<2:0>			—	—	
bit 7							bit 0
Legend:							
R = Readable	e bit	W = Writable I	bit	U = Unimpler	mented bit, rea	d as '0'	
-n = Value at	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkn	own
bit 15-11	Unimplemen	ted: Read as 'd	)'				
bit 10-8	U2EIP<2:0>:	UART2 Error Ir	nterrupt Priori	ty bits			
	111 = Interru	pt is priority 7 (ł	nighest priorit	y interrupt)			
	•						
	•						
	001 = Interru	pt is priority 1					
	000 = Interru	pt source is disa	abled				
bit 7	Unimplemen	ted: Read as 'o	)'				
bit 6-4	U1EIP<2:0>:	UART1 Error Ir	nterrupt Priori	ty bits			
	111 = Interru	pt is priority 7 (ł	nighest priorit	y interrupt)			
	•						
	•						
	001 = Interru	pt is priority 1					
	000 = Interru	pt source is disa	abled				
bit 3-0	Unimplemen	ted: Read as 'o	)'				

#### REGISTER 7-31: IPC16: INTERRUPT PRIORITY CONTROL REGISTER 16

#### REGISTER 8-2: DMAxREQ: DMA CHANNEL x IRQ SELECT REGISTER

R/W-0	U-0						
FORCE <sup>(1)</sup>	—	—	—	—	—	—	—
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	IRQSEL6 <sup>(2)</sup>	IRQSEL5(2)	IRQSEL4(2)	IRQSEL3(2)	IRQSEL2 <sup>(2)</sup>	IRQSEL1(2)	IRQSEL0(2)
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **FORCE:** Force DMA Transfer bit<sup>(1)</sup>

1 = Force a single DMA transfer (Manual mode)

0 = Automatic DMA transfer initiation by DMA request

bit 14-7 Unimplemented: Read as '0'

- bit 6-0 IRQSEL<6:0>: DMA Peripheral IRQ Number Select bits<sup>(2)</sup> 0000000-1111111 = DMAIRQ0-DMAIRQ127 selected to be Channel DMAREQ
- **Note 1:** The FORCE bit cannot be cleared by the user. The FORCE bit is cleared by hardware when the forced DMA transfer is complete.

2: Please see Table 8-1 for a complete listing of IRQ numbers for all interrupt sources.

### REGISTER 9-3: PLLFBD: PLL FEEDBACK DIVISOR REGISTER<sup>(1)</sup>

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
	_				_	_	PLLDIV<8>
bit 15	÷						bit 8
R/W-0	R/W-0	R/W-1	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0
			PLLD	IV<7:0>			
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable I	oit	U = Unimpler	mented bit, read	1 as '0'	
-n = Value at F	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unl	known
							/
bit 15-9	Unimplemer	nted: Read as 'd	)'				
bit 8-0	PLLDIV<8:0	>: PLL Feedbac	k Divisor bits	(also denoted	as 'M', PLL mu	ltiplier)	
	111111111	= 513					
	•						
	•						
	•						
	000110000	= 50 (default)					
	•						
	•						
	•						
	00000010	= 4					
	000000001	= 3 - 2					
	000000000	- 2					

Note 1: This register is reset only on a Power-on Reset (POR).

### 10.2.2 IDLE MODE

Idle mode has these features:

- · The CPU stops executing instructions.
- The WDT is automatically cleared.
- The system clock source remains active. By default, all peripheral modules continue to operate normally from the system clock source, but can also be selectively disabled (see Section 10.4 "Peripheral Module Disable").
- If the WDT or FSCM is enabled, the LPRC also remains active.

The device will wake from Idle mode on any of these events:

- Any interrupt that is individually enabled.
- · Any device Reset.
- A WDT time-out.

On wake-up from Idle, the clock is reapplied to the CPU and instruction execution will begin (2-4 clock cycles later), starting with the instruction following the PWRSAV instruction, or the first instruction in the ISR.

#### 10.2.3 INTERRUPTS COINCIDENT WITH POWER SAVE INSTRUCTIONS

Any interrupt that coincides with the execution of a PWRSAV instruction is held off until entry into Sleep or Idle mode has completed. The device then wakes up from Sleep or Idle mode.

### 10.3 Doze Mode

Generally, changing clock speed and invoking one of the power-saving modes are the preferred strategies for reducing power consumption. There may be circumstances, however, where this is not practical. For example, it may be necessary for an application to maintain uninterrupted synchronous communication, even while it is doing nothing else. Reducing system clock speed may introduce communication errors, while using a power-saving mode may stop communications completely.

Doze mode is a simple and effective alternative method to reduce power consumption while the device is still executing code. In this mode, the system clock continues to operate from the same source and at the same speed. Peripheral modules continue to be clocked at the same speed, while the CPU clock speed is reduced. Synchronization between the two clock domains is maintained, allowing the peripherals to access the SFRs while the CPU executes code at a slower rate. Doze mode is enabled by setting the DOZEN bit (CLKDIV<11>). The ratio between peripheral and core clock speed is determined by the DOZE<2:0> bits (CLKDIV<14:12>). There are eight possible configurations, from 1:1 to 1:128, with 1:1 being the default setting.

It is also possible to use Doze mode to selectively reduce power consumption in event-driven applications. This allows clock-sensitive functions, such as synchronous communications, to continue without interruption while the CPU idles, waiting for something to invoke an interrupt routine. Enabling the automatic return to full-speed CPU operation on interrupts is enabled by setting the ROI bit (CLKDIV<15>). By default, interrupt events have no effect on Doze mode operation.

For example, suppose the device is operating at 20 MIPS and the CAN module has been configured for 500 kbps based on this device operating speed. If the device is now placed in Doze mode with a clock frequency ratio of 1:4, the CAN module continues to communicate at the required bit rate of 500 kbps, but the CPU now starts executing instructions at a frequency of 5 MIPS.

## 10.4 Peripheral Module Disable

The Peripheral Module Disable (PMD) registers provide a method to disable a peripheral module by stopping all clock sources supplied to that module. When a peripheral is disabled via the appropriate PMD control bit, the peripheral is in a minimum power consumption state. The control and status registers associated with the peripheral are also disabled, so writes to those registers will have no effect and read values will be invalid.

A peripheral module is only enabled if both the associated bit in the PMD register is cleared and the peripheral is supported by the specific dsPIC<sup>®</sup> DSC variant. If the peripheral is present in the device, it is enabled in the PMD register by default.

Note: If a PMD bit is set, the corresponding module is disabled after a delay of 1 instruction cycle. Similarly, if a PMD bit is cleared, the corresponding module is enabled after a delay of 1 instruction cycle (assuming the module control registers are already configured to enable module operation).

## 14.1 Input Capture Registers

#### REGISTER 14-1: ICxCON: INPUT CAPTURE x CONTROL REGISTER

U-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
		ICSIDL		_	_		
bit 15							bit 8
<b></b>							
R/W-0	R/W-0	R/W-0	R-0, HC	R-0, HC	R/W-0	R/W-0	R/W-0
ICTMR <sup>(1)</sup>	ICI<	1:0>	ICOV	ICBNE		ICM<2:0>	
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimpler	mented bit, read	d as '0'	
-n = Value at F	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	Iown
bit 15-14	Unimplement	ted: Read as '	כ'				
bit 13	ICSIDL: Input	Capture Modu	ile Stop in Idle	e Control bit			
	1 = Input capt	ure module wil	I halt in CPU	Idle mode	l Idla mada		
bit 12 9		ted: Road as '	' continue to c				
bit 7		Conture Timer	Soloct hite(1)				
	1 = TMR2 cor	tents are cant	ured on cantu	re event			
	0 = TMR3 cor	itents are capt	ured on captu	re event			
bit 6-5	ICI<1:0>: Sele	ect Number of	Captures per	Interrupt bits			
	11 = Interrupt	on every fourt	h capture eve	nt			
	10 = Interrupt	on every third	capture even	t vent			
	00 = Interrupt	on every capt	ure event	CIIL			
bit 4	ICOV: Input C	apture Overflo	w Status Flag	bit (read-only)	)		
	1 = Input capt	ure overflow o	ccurred				
	0 = No input c	apture overflow	w occurred				
bit 3	ICBNE: Input	Capture Buffe	Empty Status	s bit (read-only	') 		
	1 = Input capt 0 = Input capt	ure buffer is no ure buffer is er	ot empty, at le npty	ast one more o	capture value c	an be read	
bit 2-0	ICM<2:0>: Inp	out Capture Mo	de Select bits	6			
	111 = Input ca	apture function	s as interrupt	pin only when	device is in Sle	eep or Idle mode	e
	(Rising	edge detect o	nly, all other o	control bits are	not applicable.	)	
	101 = Capture	e mode, everv	16th risina ed	ae			
	100 = Capture	e mode, every	4th rising edg	e			
	011 = Capture	e mode, every	rising edge				
	010 = Capture 001 = Capture	e mode, every	edge (rising a	nd falling)			
	(ICI<1:	0> bits do not	control interru	pt generation f	for this mode.)		
	000 = Input ca	apture module	turned off				

## **REGISTER 15-1:** OCxCON: OUTPUT COMPARE x CONTROL REGISTER (x = 1, 2)

U-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
—	—	OCSIDL	—	—	_	—	_
bit 15							bit 8
U-0	U-0	U-0	R-0, HC	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	OCFLT	OCTSEL		OCM<2:0>	
bit 7							bit 0

Legend:	HC = Hardware Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14	Unimplemented: Read as '0'
bit 13	OCSIDL: Stop Output Compare in Idle Mode Control bit
	<ol> <li>1 = Output Compare x halts in CPU Idle mode</li> <li>0 = Output Compare x continues to operate in CPU Idle mode</li> </ol>
bit 12-5	Unimplemented: Read as '0'
bit 4	OCFLT: PWM Fault Condition Status bit
	<ul> <li>1 = PWM Fault condition has occurred (cleared in hardware only)</li> <li>0 = No PWM Fault condition has occurred (this bit is only used when OCM&lt;2:0&gt; = 111)</li> </ul>
bit 3	OCTSEL: Output Compare Timer Select bit
	<ul> <li>1 = Timer3 is the clock source for Compare x</li> <li>0 = Timer2 is the clock source for Compare x</li> </ul>
bit 2-0	OCM<2:0>: Output Compare Mode Select bits
	<ul> <li>111 = PWM mode on OCx, Fault pin enabled</li> <li>110 = PWM mode on OCx, Fault pin disabled</li> <li>101 = Initialize OCx pin low, generate continuous output pulses on OCx pin</li> <li>100 = Initialize OCx pin low, generate single output pulse on OCx pin</li> <li>011 = Compare event toggles OCx pin</li> <li>010 = Initialize OCx pin high, compare event forces OCx pin low</li> <li>001 = Initialize OCx pin low, compare event forces OCx pin high</li> <li>000 = Output compare channel is disabled</li> </ul>

REGISTER 16-3: SPIxCON2: SPIx CONTROL REGISTER 2

R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0	U-0	
FRMEN	SPIFSD	FRMPOL	—	—	—	—	—	
bit 15							bit 8	
U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	U-0	
		—	—			FRMDLY	—	
bit 7							bit 0	
Legend:								
R = Readable	e bit	W = Writable b	bit	U = Unimpler	mented bit, read	d as '0'		
-n = Value at	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkn	own	
bit 15 bit 14	FRMEN: Fran 1 = Framed S 0 = Framed S SPIFSD: Fran 1 = Frame sy 0 = Frame sy	med SPIx Suppor SPIx support ena SPIx support dis me Sync Pulse I nc pulse input (s nc pulse output	ort bit abled (SSx pi abled Direction Cor slave) (master)	n used as fran htrol bit	ne sync pulse ir	nput/output)		
bit 13	<b>FRMPOL:</b> Frame Sync Pulse Polarity bit 1 = Frame sync pulse is active-high 0 = Frame sync pulse is active-low							
bit 12-2	Unimplemen	ted: Read as '0	3					
bit 1	FRMDLY: Fra	ame Sync Pulse	Edge Select	bit				
	1 = Frame sy 0 = Frame sy	nc pulse coincion nc pulse preced	les with first l les first bit clo	oit clock ock				
bit 0	Unimplemen	ted: Read as '0	,					
	This bit must	not be set to '1'	by the user a	application				

#### REGISTER 19-26: CiTRmnCON: ECAN<sup>™</sup> MODULE TX/RX BUFFER m CONTROL REGISTER (m = 0.2.4.6: n = 1.3.5.7)

	(11 – 0,2	2, <del>4</del> ,0, 11 = 1,3,	5,1 )				
R/W-0	R-0	R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0
TXENn	TXABTn	TXLARBn	TXERRn	TXREQn	RTRENn	TXnPRI<1:0>	
bit 15							bit 8

R/W-0	R-0	R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0
TXENm	TXABTm <sup>(1)</sup>	TXLARBm <sup>(1)</sup>	TXERRm <sup>(1)</sup>	TXREQm	RTRENm	TXmPF	RI<1:0>
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8	See Definition for Bits 7-0, Controls Buffer n
bit 7	TXENm: TX/RX Buffer Selection bit
	<ul> <li>1 = Buffer TRBn is a transmit buffer</li> <li>0 = Buffer TRBn is a receive buffer</li> </ul>
bit 6	TXABTm: Message Aborted bit <sup>(1)</sup>
	<ul><li>1 = Message was aborted</li><li>0 = Message completed transmission successfully</li></ul>
bit 5	TXLARBm: Message Lost Arbitration bit <sup>(1)</sup>
	<ul> <li>1 = Message lost arbitration while being sent</li> <li>0 = Message did not lose arbitration while being sent</li> </ul>
bit 4	TXERRm: Error Detected During Transmission bit <sup>(1)</sup>
	<ul> <li>1 = A bus error occurred while the message was being sent</li> <li>0 = A bus error did not occur while the message was being sent</li> </ul>
bit 3	TXREQm: Message Send Request bit
	Setting this bit to '1' requests sending a message. The bit will automatically clear when the message is successfully sent. Clearing the bit to '0' while set will request a message abort.
bit 2	RTRENm: Auto-Remote Transmit Enable bit
	<ul> <li>1 = When a remote transmit is received, TXREQ will be set</li> <li>0 = When a remote transmit is received, TXREQ will be unaffected</li> </ul>
bit 1-0	TXmPRI<1:0>: Message Transmission Priority bits
	<ul> <li>11 = Highest message priority</li> <li>10 = High intermediate message priority</li> <li>01 = Low intermediate message priority</li> <li>00 = Lowest message priority</li> </ul>

Note 1: This bit is cleared when TXREQ is set.

# 22.0 INSTRUCTION SET SUMMARY

**Note:** This data sheet summarizes the features of the PIC24HJXXXGPX06A/X08A/X10A families of devices. However, it is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the related section in the *"dsPIC33F/PIC24H Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com).

The PIC24H instruction set is identical to that of the PIC24F, and is a subset of the dsPIC30F/33F instruction set.

Most instructions are a single program memory word (24 bits). Only three instructions require two program memory locations.

Each single-word instruction is a 24-bit word, divided into an 8-bit opcode, which specifies the instruction type and one or more operands, which further specify the operation of the instruction.

The instruction set is highly orthogonal and is grouped into five basic categories:

- · Word or byte-oriented operations
- · Bit-oriented operations
- · Literal operations
- DSP operations
- · Control operations

Table 22-1 shows the general symbols used in describing the instructions.

The PIC24H instruction set summary in Table 22-2 lists all the instructions, along with the status flags affected by each instruction.

Most word or byte-oriented W register instructions (including barrel shift instructions) have three operands:

- The first source operand which is typically a register 'Wb' without any address modifier
- The second source operand which is typically a register 'Ws' with or without an address modifier
- The destination of the result which is typically a register 'Wd' with or without an address modifier

However, word or byte-oriented file register instructions have two operands:

- · The file register specified by the value 'f'
- The destination, which could either be the file register 'f' or the W0 register, which is denoted as 'WREG'

Most bit-oriented instructions (including simple rotate/shift instructions) have two operands:

- The W register (with or without an address modifier) or file register (specified by the value of 'Ws' or 'f')
- The bit in the W register or file register (specified by a literal value or indirectly by the contents of register 'Wb')

The literal instructions that involve data movement may use some of the following operands:

- A literal value to be loaded into a W register or file register (specified by the value of 'k')
- The W register or file register where the literal value is to be loaded (specified by 'Wb' or 'f')

However, literal instructions that involve arithmetic or logical operations use some of the following operands:

- The first source operand which is a register 'Wb' without any address modifier
- The second source operand which is a literal value
- The destination of the result (only if not the same as the first source operand) which is typically a register 'Wd' with or without an address modifier

The control instructions may use some of the following operands:

- A program memory address
- The mode of the table read and table write instructions

All instructions are a single word, except for certain double word instructions, which were made double word instructions so that all the required information is available in these 48 bits. In the second word, the 8 MSbs are '0's. If this second word is executed as an instruction (by itself), it will execute as a NOP.

Most single-word instructions are executed in a single instruction cycle, unless a conditional test is true, or the program counter is changed as a result of the instruction. In these cases, the execution takes two instruction cycles with the additional instruction cycle(s) executed as a NOP. Notable exceptions are the BRA (unconditional/computed branch), indirect CALL/GOTO, all table reads and writes and RETURN/RETFIE instructions, which are single-word instructions but take two or three cycles. Certain instructions that involve skipping over the subsequent instruction require either two or three cycles if the skip is performed, depending on whether the instruction being skipped is a single-word or double word instruction. Moreover, double word moves require two cycles. The double word instructions execute in two instruction cycles.

Note: For more details on the instruction set, refer to the *"16-bit MCU and DSC Programmer's Reference Manual"* (DS70157).

### 24.1 DC Characteristics

Characteristic	VDD Range	Temp Range	Max MIPS
Characteristic	(in Volts)	(in °C)	PIC24HJXXXGPX06A/X08A/X10
—	VBOR-3.6V <sup>(1)</sup>	-40°C to +85°C	40
_	VBOR-3.6V <sup>(1)</sup>	-40°C to +125°C	40

#### TABLE 24-1: OPERATING MIPS VS. VOLTAGE

**Note 1:** Device is functional at VBORMIN < VDD < VDDMIN. Analog modules such as the ADC will have degraded performance. Device functionality is tested but not characterized. Refer to parameter BO10 in Table 24-11 for the minimum and maximum BOR values.

#### TABLE 24-2: THERMAL OPERATING CONDITIONS

Rating	Symbol	Min	Тур	Max	Unit
Industrial Temperature Devices					
Operating Junction Temperature Range	TJ	-40	—	+125	°C
Operating Ambient Temperature Range	TA	-40	—	+85	°C
Extended Temperature Devices					
Operating Junction Temperature Range	TJ	-40	—	+150	°C
Operating Ambient Temperature Range	TA	-40	—	+125	°C
Power Dissipation: Internal chip power dissipation: $PINT = VDD x (IDD - \Sigma IOH)$ I/O Pin Power Dissipation:	PD	PINT + PI/O			W
$I/O = \Sigma (\{VDD - VOH\} \times IOH) + \Sigma (VOL \times IOL)$					
Maximum Allowed Power Dissipation	PDMAX	(	TJ — TA)/θJ	IA	W

#### TABLE 24-3: THERMAL PACKAGING CHARACTERISTICS

Characteristic	Symbol	Тур	Max	Unit	Notes
Package Thermal Resistance, 100-pin TQFP (14x14x1 mm)	θja	40	—	°C/W	1
Package Thermal Resistance, 100-pin TQFP (12x12x1 mm)	θja	40	—	°C/W	1
Package Thermal Resistance, 64-pin TQFP (10x10x1 mm)	θја	40	_	°C/W	1
Package Thermal Resistance, 64-pin QFN (9x9x0.9 mm)	θја	28	—	°C/W	1

Note 1: Junction to ambient thermal resistance, Theta-JA ( $\theta$ JA) numbers are achieved by package simulations.

#### FIGURE 24-19: I2Cx BUS START/STOP BITS TIMING CHARACTERISTICS (SLAVE MODE)







AC CH	ARACTE	RISTICS	$\begin{array}{l} \mbox{Standard Operating Conditions: 3.0V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ -40^{\circ}C \leq TA \leq +125^{\circ}C \mbox{ for Extended} \end{array}$							
Param No.	Symbo I	Characteristic	Min.	Тур	Max.	Units	Conditions			
Device Supply										
AD01	AVDD	Module VDD Supply	Greater of VDD – 0.3 or 3.0	_	Lesser of VDD + 0.3 or 3.6	V	_			
AD02	AVss	Module Vss Supply	Vss – 0.3	—	Vss + 0.3	V	_			
			Referen	ce Inpu	Its					
AD05	Vrefh	Reference Voltage High	AVss + 2.5	_	AVDD	V				
AD05a			3.0	—	3.6	V	Vrefh = AVdd Vrefl = AVss = 0			
AD06	Vrefl	Reference Voltage Low	AVss	-	AVDD – 2.5	V				
AD06a			0	_	0	V	Vrefh = AVdd Vrefl = AVss = 0			
AD07	Vref	Absolute Reference Voltage	2.5	—	3.6	V	VREF = VREFH - VREFL			
AD08	IREF	Current Drain	—	—	10	μA	ADC off			
AD08a	IAD	Operating Current	_	7.0 2.7	9.0 3.2	mA mA	10-bit ADC mode, See <b>Note 1</b> 12-bit ADC mode, See <b>Note 1</b>			
			Analo	g Input						
AD12	VINH	Input Voltage Range VINH	VINL	_	Vrefh	V	This voltage reflects Sample and Hold Channels 0, 1, 2, and 3 (CH0-CH3), positive input			
AD13	VINL	Input Voltage Range VINL	VREFL		AVss + 1V	V	This voltage reflects Sample and Hold Channels 0, 1, 2, and 3 (CH0-CH3), negative input			
AD17	Rin	Recommended Imped- ance of Analog Voltage Source			200 200	Ω Ω	10-bit ADC 12-bit ADC			

#### TABLE 24-39: ADC MODULE SPECIFICATIONS

**Note 1:** These parameters are not characterized or tested in manufacturing.

AC CHARACTERISTICS			$\begin{tabular}{lllllllllllllllllllllllllllllllllll$							
Param No.	Symbol	Characteristic	Min.	Тур <sup>(2)</sup>	Max.	Units	Conditions			
		Clock	Paramete	ers <sup>(1)</sup>						
AD50	TAD	ADC Clock Period	117.6		_	ns	—			
AD51	tRC	ADC Internal RC Oscillator Period	—	250	—	ns	_			
	Conversion Rate									
AD55	tCONV	Conversion Time		14 Tad		ns	—			
AD56	FCNV	Throughput Rate			500	ksps	—			
AD57	TSAMP	Sample Time	3 Tad		_		—			
		Timin	ig Parame	eters						
AD60	tPCS	Conversion Start from Sample Trigger <sup>(2)</sup>	2.0 TAD	—	3.0 Tad		Auto convert trigger not selected			
AD61	tPSS	Sample Start from Setting Sample (SAMP) bit <sup>(2)</sup>	2.0 TAD	—	3.0 Tad		—			
AD62	tcss	Conversion Completion to Sample Start (ASAM = $1$ ) <sup>(2)</sup>		0.5 Tad	_		_			
AD63	tdpu	Time to Stabilize Analog Stage from ADC Off to ADC On <sup>(2,3)</sup>		_	20	μS	_			

## TABLE 24-42: ADC CONVERSION (12-BIT MODE) TIMING REQUIREMENTS

**Note 1:** Because the sample caps eventually loses charge, clock rates below 10 kHz may affect linearity performance, especially at elevated temperatures.

**2:** These parameters are characterized but not tested in manufacturing.

**3:** tDPU is the time required for the ADC module to stabilize when it is turned on (AD1CON1<ADON> = 1). During this time, the ADC result is indeterminate.

	A c Standard Operating Conditions: 3 0V to 3 6V (upless otherwise stated)								
CHARA	CTERISTICS	Operating temperature $-40^{\circ}C \le TA \le +150^{\circ}C$ for High Temperature							
Param No.	Symbol	Characteristic <sup>(1)</sup>	Min	Тур	Max	Units	Conditions		
HSP35	TscH2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	—	_	35	ns	_		
HSP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	25	—	-	ns	_		
HSP41	TscH2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	25	_	—	ns	_		
HSP51	TssH2doZ	SSx ↑ to SDOx Output High-Impedance	15	_	55	ns	See Note 2		

#### TABLE 25-12: SPIX MODULE SLAVE MODE (CKE = 0) TIMING REQUIREMENTS

Note 1: These parameters are characterized but not tested in manufacturing.

**2:** Assumes 50 pF load on all SPIx pins.

#### TABLE 25-13: SPIX MODULE SLAVE MODE (CKE = 1) TIMING REQUIREMENTS

AC CHARACTERISTICS		Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +150^{\circ}C$ for High Temperature						
Param No.	Symbol	Characteristic <sup>(1)</sup>	Min	Тур	Max	Units	Conditions	
HSP35	TscH2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge			35	ns	_	
HSP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	25			ns	_	
HSP41	TscH2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	25			ns	_	
HSP51	TssH2doZ	SSx ↑ to SDOx Output High-Impedance	15		55	ns	See Note 2	
HSP60	TssL2doV	SDOx Data Output Valid after SSx Edge	_	_	55	ns	—	

Note 1: These parameters are characterized but not tested in manufacturing.

**2:** Assumes 50 pF load on all SPIx pins.

# Revision D (June 2012)

This revision includes typographical and formatting changes throughout the data sheet text.

All other major changes are referenced by their respective section in the following table.

#### TABLE B-3: MAJOR SECTION UPDATES

Section Name	Update Description				
Section 2.0 "Guidelines for Getting Started with 16-Bit Microcontrollers"	Updated the Recommended Minimum Connection (see Figure 2-1).				
Section 9.0 "Oscillator Configuration"	Updated the COSC<2:0> and NOSC<2:0> bit value definitions for '001' (see Register 9-1).				
Section 20.0 "10-bit/12-bit Analog-to-Digital Converter (ADC)"	Updated the Analog-to-Digital Conversion Clock Period Block Diagram (see Figure 20-2).				
Section 21.0 "Special Features"	Added Note 3 to the On-chip Voltage Regulator Connections (see Figure 21-1).				
Section 24.0 "Electrical Characteristics"	Updated "Absolute Maximum Ratings".				
	Updated Operating MIPS vs. Voltage (see Table 24-1).				
	Removed parameter DC18 from the DC Temperature and Voltage Specifications (see Table 24-4).				
	Updated the notes in the following tables:				
	• Table 24-5				
	Table 24-6				
	• Table 24-7				
	Table 24-8				
	Updated the I/O Pin Output Specifications (see Table 24-10).				
	Updated the Conditions for parameter BO10 (see Table 24-11).				
	Updated the Conditions for parameters D136b, D137b, and D138b (TA = 150°C) (see Table 24-12).				
Section 25.0 "High Temperature Electrical	Updated "Absolute Maximum Ratings".				
Characteristics"	Updated the I/O Pin Output Specifications (see Table 25-6).				
	Removed Table 25-7: DC Characteristics: Program Memory.				

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