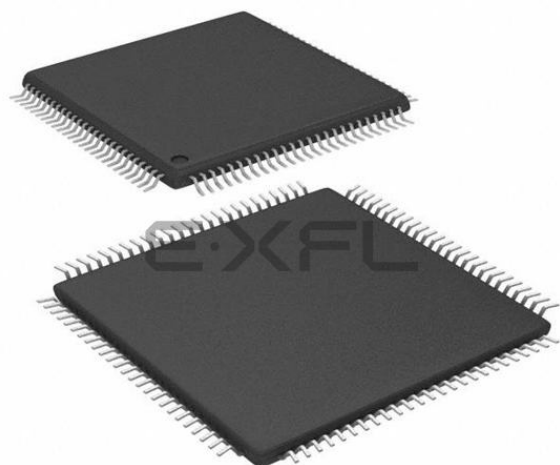




Welcome to [E-XFL.COM](https://www.e-xfl.com)

What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	PIC
Core Size	16-Bit
Speed	20 MIPS
Connectivity	CANbus, I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	85
Program Memory Size	128KB (43K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 32x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 150°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24hj128gp510a-h-pt

TO OUR VALUED CUSTOMERS

It is our intention to provide our valued customers with the best documentation possible to ensure successful use of your Microchip products. To this end, we will continue to improve our publications to better suit your needs. Our publications will be refined and enhanced as new volumes and updates are introduced.

If you have any questions or comments regarding this publication, please contact the Marketing Communications Department via E-mail at docerrors@microchip.com or fax the **Reader Response Form** in the back of this data sheet to (480) 792-4150. We welcome your feedback.

Most Current Data Sheet

To obtain the most up-to-date version of this data sheet, please register at our Worldwide Web site at:

<http://www.microchip.com>

You can determine the version of a data sheet by examining its literature number found on the bottom outside corner of any page. The last character of the literature number is the version number, (e.g., DS30000A is version A of document DS30000).

Errata

An errata sheet, describing minor operational differences from the data sheet and recommended workarounds, may exist for current devices. As device/documentation issues become known to us, we will publish an errata sheet. The errata will specify the revision of silicon and revision of document to which it applies.

To determine if an errata sheet exists for a particular device, please check with one of the following:

- Microchip's Worldwide Web site; <http://www.microchip.com>
- Your local Microchip sales office (see last page)

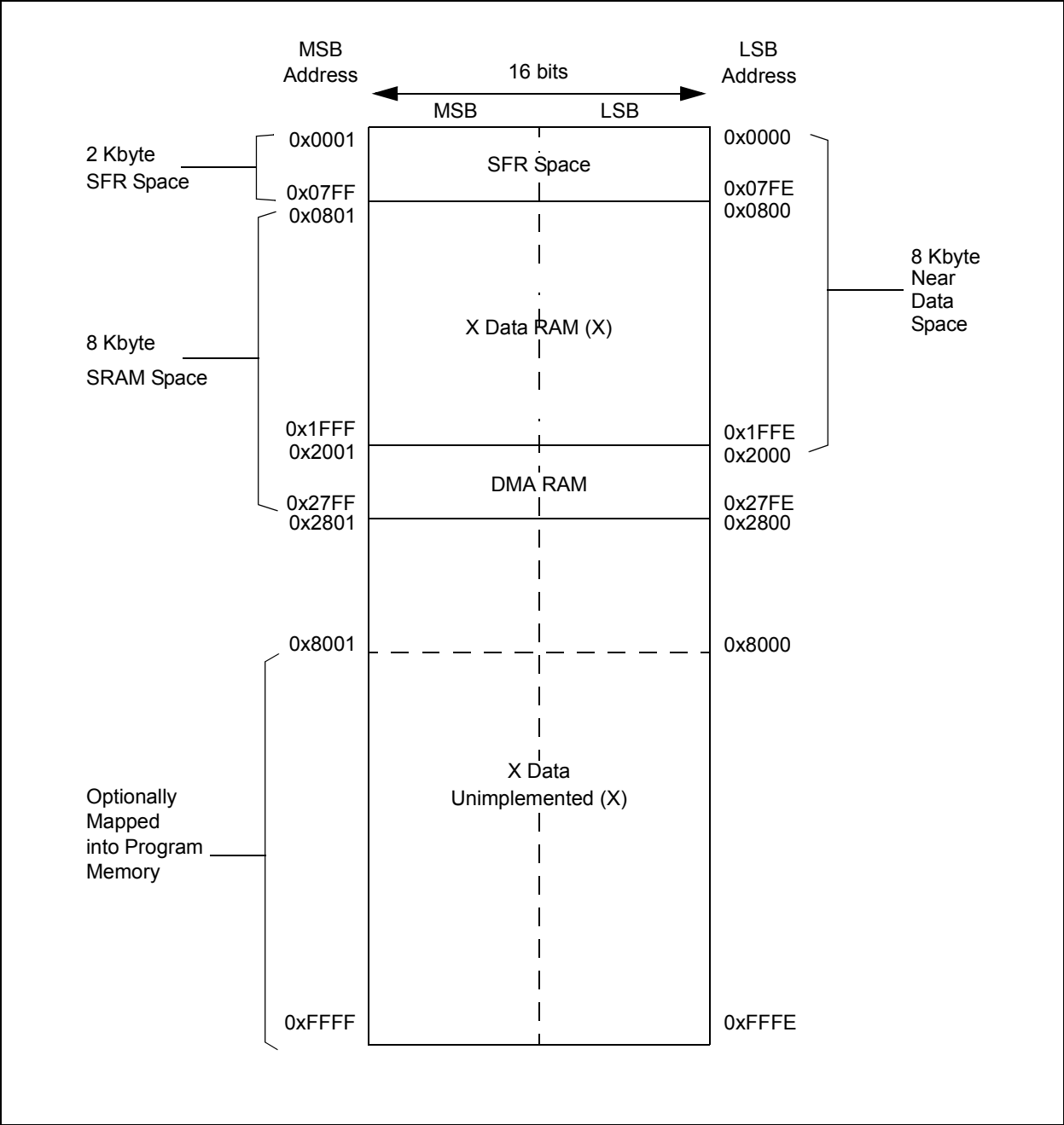
When contacting a sales office, please specify which device, revision of silicon and data sheet (include literature number) you are using.

Customer Notification System

Register on our web site at www.microchip.com to receive the most current information on all of our products.

PIC24HJXXXGPX06A/X08A/X10A

FIGURE 4-3: DATA MEMORY MAP FOR PIC24HJXXXGPX06A/X08A/X10A DEVICES WITH 8 KB RAM



PIC24HJXXXGPX06A/X08A/X10A

TABLE 7-1: INTERRUPT VECTORS

Vector Number	Interrupt Request (IRQ) Number	IVT Address	AIVT Address	Interrupt Source
8	0	0x000014	0x000114	INT0 – External Interrupt 0
9	1	0x000016	0x000116	IC1 – Input Capture 1
10	2	0x000018	0x000118	OC1 – Output Compare 1
11	3	0x00001A	0x00011A	T1 – Timer1
12	4	0x00001C	0x00011C	DMA0 – DMA Channel 0
13	5	0x00001E	0x00011E	IC2 – Input Capture 2
14	6	0x000020	0x000120	OC2 – Output Compare 2
15	7	0x000022	0x000122	T2 – Timer2
16	8	0x000024	0x000124	T3 – Timer3
17	9	0x000026	0x000126	SPI1E – SPI1 Error
18	10	0x000028	0x000128	SPI1 – SPI1 Transfer Done
19	11	0x00002A	0x00012A	U1RX – UART1 Receiver
20	12	0x00002C	0x00012C	U1TX – UART1 Transmitter
21	13	0x00002E	0x00012E	ADC1 – Analog-to-Digital Converter 1
22	14	0x000030	0x000130	DMA1 – DMA Channel 1
23	15	0x000032	0x000132	Reserved
24	16	0x000034	0x000134	SI2C1 – I2C1 Slave Events
25	17	0x000036	0x000136	MI2C1 – I2C1 Master Events
26	18	0x000038	0x000138	Reserved
27	19	0x00003A	0x00013A	CN - Change Notification Interrupt
28	20	0x00003C	0x00013C	INT1 – External Interrupt 1
29	21	0x00003E	0x00013E	ADC2 – Analog-to-Digital Converter 2
30	22	0x000040	0x000140	IC7 – Input Capture 7
31	23	0x000042	0x000142	IC8 – Input Capture 8
32	24	0x000044	0x000144	DMA2 – DMA Channel 2
33	25	0x000046	0x000146	OC3 – Output Compare 3
34	26	0x000048	0x000148	OC4 – Output Compare 4
35	27	0x00004A	0x00014A	T4 – Timer4
36	28	0x00004C	0x00014C	T5 – Timer5
37	29	0x00004E	0x00014E	INT2 – External Interrupt 2
38	30	0x000050	0x000150	U2RX – UART2 Receiver
39	31	0x000052	0x000152	U2TX – UART2 Transmitter
40	32	0x000054	0x000154	SPI2E – SPI2 Error
41	33	0x000056	0x000156	SPI1 – SPI1 Transfer Done
42	34	0x000058	0x000158	C1RX – ECAN1 Receive Data Ready
43	35	0x00005A	0x00015A	C1 – ECAN1 Event
44	36	0x00005C	0x00015C	DMA3 – DMA Channel 3
45	37	0x00005E	0x00015E	IC3 – Input Capture 3
46	38	0x000060	0x000160	IC4 – Input Capture 4
47	39	0x000062	0x000162	IC5 – Input Capture 5
48	40	0x000064	0x000164	IC6 – Input Capture 6
49	41	0x000066	0x000166	OC5 – Output Compare 5
50	42	0x000068	0x000168	OC6 – Output Compare 6
51	43	0x00006A	0x00016A	OC7 – Output Compare 7
52	44	0x00006C	0x00016C	OC8 – Output Compare 8
53	45	0x00006E	0x00016E	Reserved

PIC24HJXXXGPX06A/X08A/X10A

REGISTER 7-11: IEC1: INTERRUPT ENABLE CONTROL REGISTER 1

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
U2TXIE	U2RXIE	INT2IE	T5IE	T4IE	OC4IE	OC3IE	DMA2IE
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0
IC8IE	IC7IE	AD2IE	INT1IE	CNIE	—	MI2C1IE	SI2C1IE
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 15 **U2TXIE:** UART2 Transmitter Interrupt Enable bit
1 = Interrupt request enabled
0 = Interrupt request not enabled
- bit 14 **U2RXIE:** UART2 Receiver Interrupt Enable bit
1 = Interrupt request enabled
0 = Interrupt request not enabled
- bit 13 **INT2IE:** External Interrupt 2 Enable bit
1 = Interrupt request enabled
0 = Interrupt request not enabled
- bit 12 **T5IE:** Timer5 Interrupt Enable bit
1 = Interrupt request enabled
0 = Interrupt request not enabled
- bit 11 **T4IE:** Timer4 Interrupt Enable bit
1 = Interrupt request enabled
0 = Interrupt request not enabled
- bit 10 **OC4IE:** Output Compare Channel 4 Interrupt Enable bit
1 = Interrupt request enabled
0 = Interrupt request not enabled
- bit 9 **OC3IE:** Output Compare Channel 3 Interrupt Enable bit
1 = Interrupt request enabled
0 = Interrupt request not enabled
- bit 8 **DMA2IE:** DMA Channel 2 Data Transfer Complete Interrupt Enable bit
1 = Interrupt request enabled
0 = Interrupt request not enabled
- bit 7 **IC8IE:** Input Capture Channel 8 Interrupt Enable bit
1 = Interrupt request enabled
0 = Interrupt request not enabled
- bit 6 **IC7IE:** Input Capture Channel 7 Interrupt Enable bit
1 = Interrupt request enabled
0 = Interrupt request not enabled
- bit 5 **AD2IE:** ADC2 Conversion Complete Interrupt Enable bit
1 = Interrupt request enabled
0 = Interrupt request not enabled
- bit 4 **INT1IE:** External Interrupt 1 Enable bit
1 = Interrupt request enabled
0 = Interrupt request not enabled

PIC24HJXXXGPX06A/X08A/X10A

REGISTER 7-33: INTTREG: INTERRUPT CONTROL AND STATUS REGISTER

U-0	U-0	U-0	U-0	R-0	R-0	R-0	R-0
—	—	—	—	ILR<3:0>			
bit 15				bit 8			

U-0	U-0	R-0	R-0	R-0	R-0	R-0	R-0
—	VECNUM<6:0>						
bit 7				bit 0			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-12 **Unimplemented:** Read as '0'

bit 11-8 **ILR<3:0>:** New CPU Interrupt Priority Level bits

1111 = CPU Interrupt Priority Level is 15

•
•
•

0001 = CPU Interrupt Priority Level is 1

0000 = CPU Interrupt Priority Level is 0

bit 7 **Unimplemented:** Read as '0'

bit 6-0 **VECNUM<6:0>:** Vector Number of Pending Interrupt bits

1111111 = Interrupt Vector pending is number 135

•
•
•

0000001 = Interrupt Vector pending is number 9

0000000 = Interrupt Vector pending is number 8

PIC24HJXXXGPX06A/X08A/X10A

REGISTER 10-2: PMD2: PERIPHERAL MODULE DISABLE CONTROL REGISTER 2 (CONTINUED)

bit 3	OC4MD: Output Compare 4 Module Disable bit 1 = Output Compare 4 module is disabled 0 = Output Compare 4 module is enabled
bit 2	OC3MD: Output Compare 3 Module Disable bit 1 = Output Compare 3 module is disabled 0 = Output Compare 3 module is enabled
bit 1	OC2MD: Output Compare 2 Module Disable bit 1 = Output Compare 2 module is disabled 0 = Output Compare 2 module is enabled
bit 0	OC1MD: Output Compare 1 Module Disable bit 1 = Output Compare 1 module is disabled 0 = Output Compare 1 module is enabled

PIC24HJXXXGPX06A/X08A/X10A

14.1 Input Capture Registers

REGISTER 14-1: ICxCON: INPUT CAPTURE x CONTROL REGISTER

U-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
—	—	ICSIDL	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R-0, HC	R-0, HC	R/W-0	R/W-0	R/W-0
ICTMR ⁽¹⁾	ICI<1:0>	ICOV	ICBNE	ICM<2:0>			
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13 **ICSIDL:** Input Capture Module Stop in Idle Control bit
1 = Input capture module will halt in CPU Idle mode
0 = Input capture module will continue to operate in CPU Idle mode

bit 12-8 **Unimplemented:** Read as '0'

bit 7 **ICTMR:** Input Capture Timer Select bits⁽¹⁾
1 = TMR2 contents are captured on capture event
0 = TMR3 contents are captured on capture event

bit 6-5 **ICI<1:0>:** Select Number of Captures per Interrupt bits
11 = Interrupt on every fourth capture event
10 = Interrupt on every third capture event
01 = Interrupt on every second capture event
00 = Interrupt on every capture event

bit 4 **ICOV:** Input Capture Overflow Status Flag bit (read-only)
1 = Input capture overflow occurred
0 = No input capture overflow occurred

bit 3 **ICBNE:** Input Capture Buffer Empty Status bit (read-only)
1 = Input capture buffer is not empty, at least one more capture value can be read
0 = Input capture buffer is empty

bit 2-0 **ICM<2:0>:** Input Capture Mode Select bits
111 = Input capture functions as interrupt pin only when device is in Sleep or Idle mode
(Rising edge detect only, all other control bits are not applicable.)
110 = Unused (module disabled)
101 = Capture mode, every 16th rising edge
100 = Capture mode, every 4th rising edge
011 = Capture mode, every rising edge
010 = Capture mode, every falling edge
001 = Capture mode, every edge (rising and falling)
(ICI<1:0> bits do not control interrupt generation for this mode.)
000 = Input capture module turned off

PIC24HJXXXGPX06A/X08A/X10A

REGISTER 19-1: CiCTRL1: ECAN™ MODULE CONTROL REGISTER 1

U-0	U-0	R/W-0	R/W-0	r-0	R/W-1	R/W-0	R/W-0
—	—	CSIDL	ABAT	—	REQOP<2:0>		
bit 15					bit 8		

R-1	R-0	R-0	U-0	R/W-0	U-0	U-0	R/W-0
OPMODE<2:0>			—	CANCAP	—	—	WIN
bit 7							bit 0

Legend:	r = Bit is Reserved		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

- bit 15-14 **Unimplemented:** Read as '0'
- bit 13 **CSIDL:** Stop in Idle Mode bit
1 = Discontinue module operation when device enters Idle mode
0 = Continue module operation in Idle mode
- bit 12 **ABAT:** Abort All Pending Transmissions bit
1 = Signal all transmit buffers to abort transmission
0 = Module will clear this bit when all transmissions are aborted
- bit 11 **Reserved:** Do not use
- bit 10-8 **REQOP<2:0>:** Request Operation Mode bits
111 = Set Listen All Messages mode
110 = Reserved – do not use
101 = Reserved – do not use
100 = Set Configuration mode
011 = Set Listen Only Mode
010 = Set Loopback mode
001 = Set Disable mode
000 = Set Normal Operation mode
- bit 7-5 **OPMODE<2:0>:** Operation Mode bits
111 = Module is in Listen All Messages mode
110 = Reserved
101 = Reserved
100 = Module is in Configuration mode
011 = Module is in Listen Only mode
010 = Module is in Loopback mode
001 = Module is in Disable mode
000 = Module is in Normal Operation mode
- bit 4 **Unimplemented:** Read as '0'
- bit 3 **CANCAP:** CAN Message Receive Timer Capture Event Enable bit
1 = Enable input capture based on CAN message receive
0 = Disable CAN capture
- bit 2-1 **Unimplemented:** Read as '0'
- bit 0 **WIN:** SFR Map Window Select bit
1 = Use filter window
0 = Use buffer window

PIC24HJXXXGPX06A/X08A/X10A

REGISTER 19-11: CiFEN1: ECAN™ MODULE ACCEPTANCE FILTER ENABLE REGISTER

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
FLTEN15	FLTEN14	FLTEN13	FLTEN12	FLTEN11	FLTEN10	FLTEN9	FLTEN8
bit 15						bit 8	

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
FLTEN7	FLTEN6	FLTEN5	FLTEN4	FLTEN3	FLTEN2	FLTEN1	FLTEN0
bit 7						bit 0	

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-0

FLTENn: Enable Filter n (0-15) to Accept Messages bits

1 = Enable Filter n

0 = Disable Filter n

PIC24HJXXXGPX06A/X08A/X10A

REGISTER 19-31: CiTRBnSTAT: ECAN™ MODULE RECEIVE BUFFER n STATUS
(n = 0, 1, ..., 31)

U-0	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	—	—	FILHIT<4:0>				
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

- bit 15-13 **Unimplemented:** Read as '0'
- bit 12-8 **FILHIT<4:0>:** Filter Hit Code bits (only written by module for receive buffers, unused for transmit buffers)
Encodes number of filter that resulted in writing this buffer.
- bit 7-0 **Unimplemented:** Read as '0'

PIC24HJXXXGPX06A/X08A/X10A

FIGURE 24-3: CLKO AND I/O TIMING CHARACTERISTICS

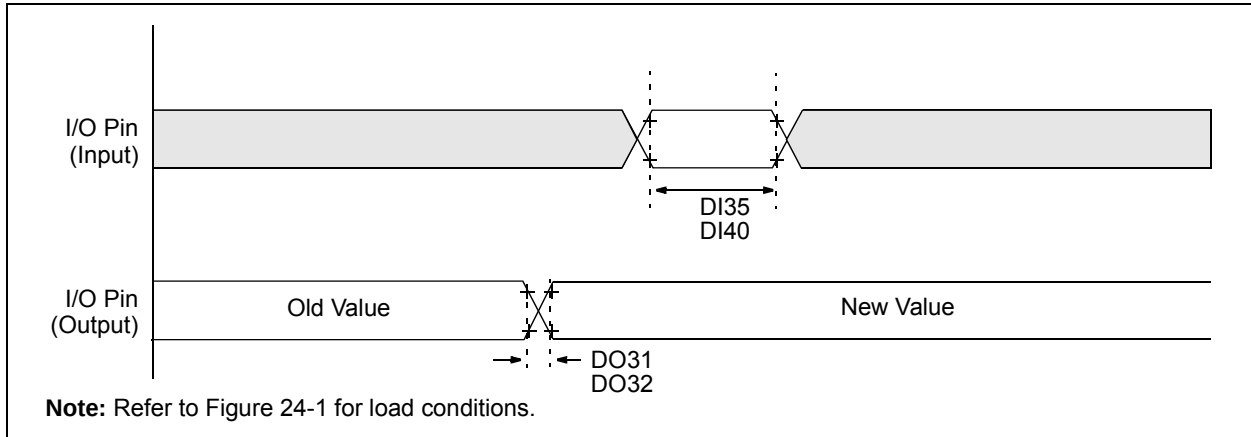


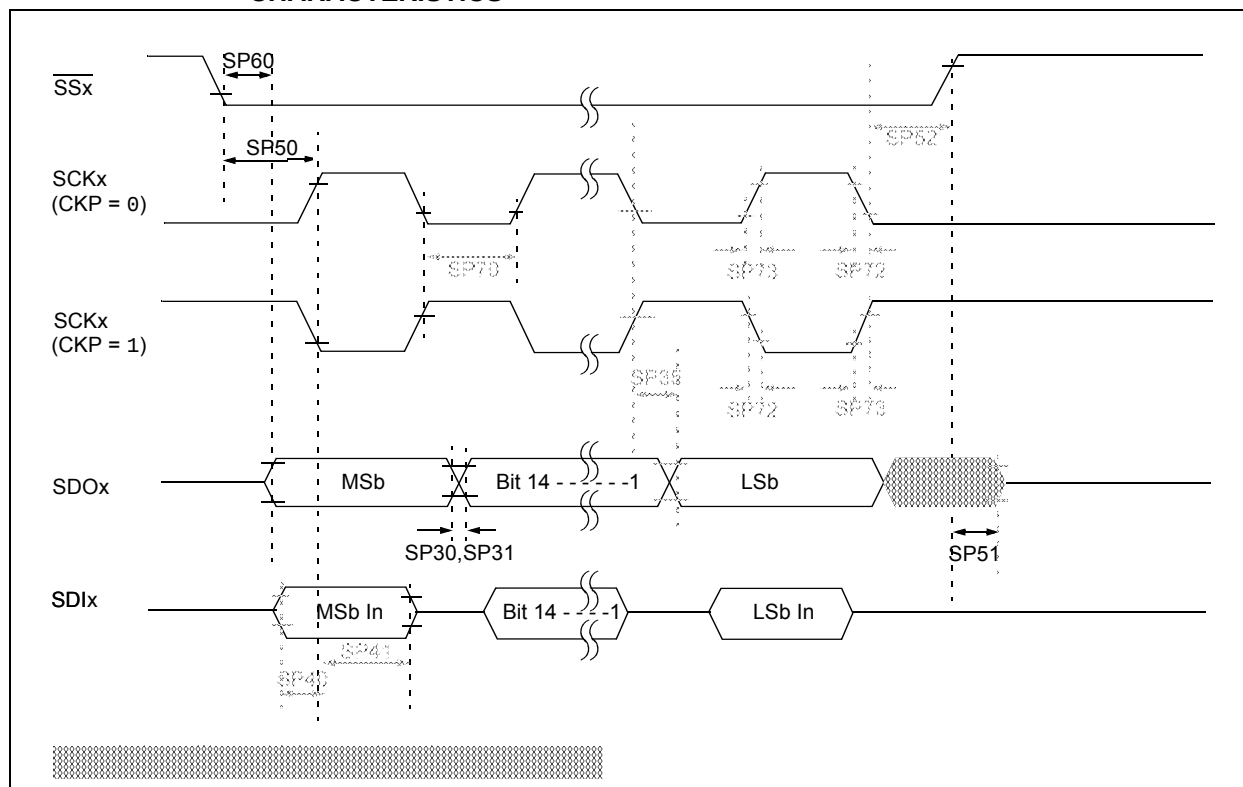
TABLE 24-20: I/O TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)				
			Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended				
Param No.	Symbol	Characteristic	Min	Typ ⁽¹⁾	Max	Units	Conditions
DO31	TioR	Port Output Rise Time	—	10	25	ns	—
DO32	TioF	Port Output Fall Time	—	10	25	ns	—
DI35	TINP	INTx Pin High or Low Time (input)	20	—	—	ns	—
DI40	TRBP	CNx High or Low Time (input)	2	—	—	Tcy	—

Note 1: Data in “Typ” column is at 3.3V, 25°C unless otherwise stated.

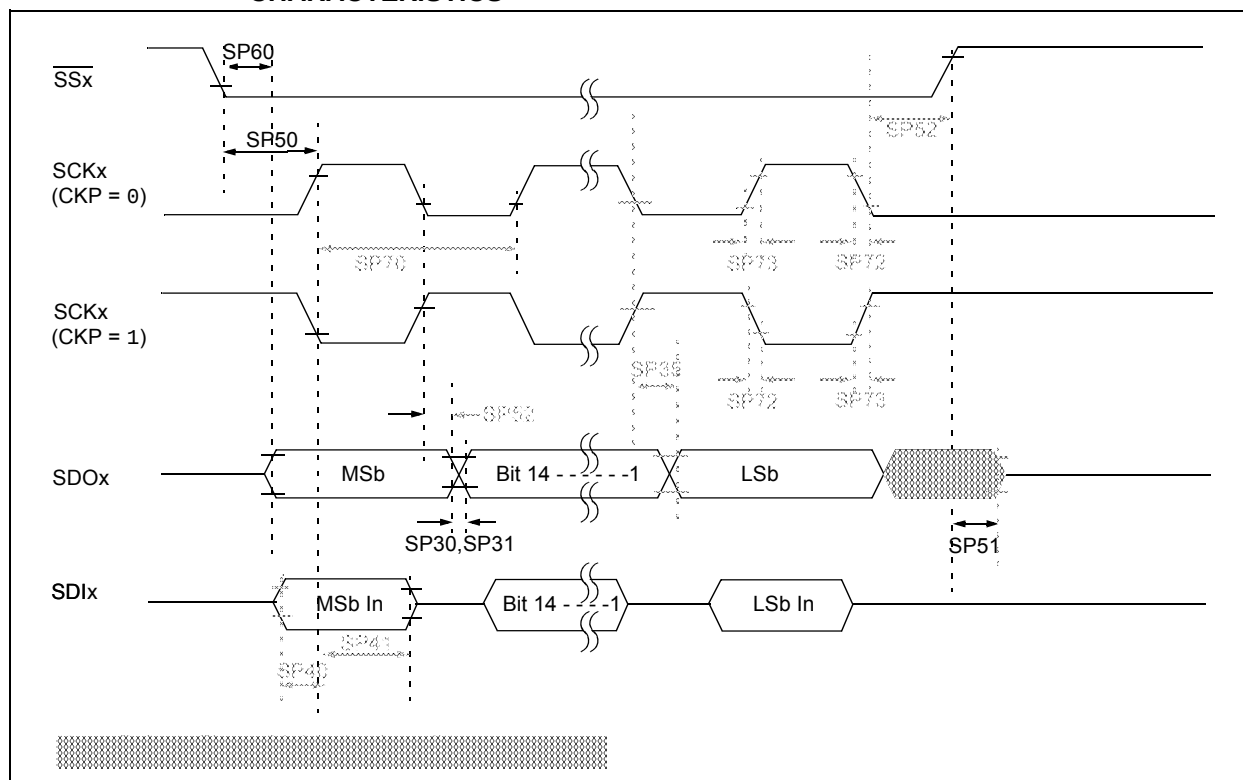
PIC24HJXXXGPX06A/X08A/X10A

FIGURE 24-13: SPIx SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 0, SMP = 0) TIMING CHARACTERISTICS



PIC24HJXXXGPX06A/X08A/X10A

FIGURE 24-14: SPIx SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 1, SMP = 0) TIMING CHARACTERISTICS



PIC24HJXXXGPX06A/X08A/X10A

FIGURE 24-21: ECAN™ MODULE I/O TIMING CHARACTERISTICS

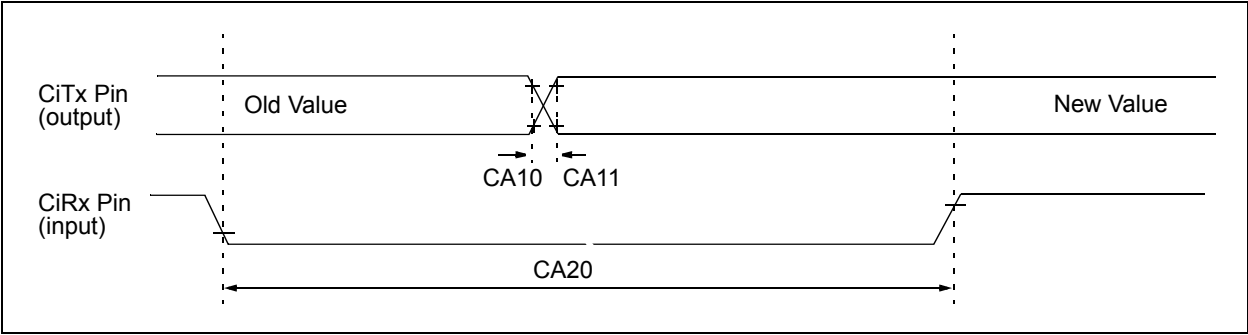


TABLE 24-38: ECAN™ MODULE I/O TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	Symbol	Characteristic ⁽¹⁾	Min	Typ ⁽²⁾	Max	Units	Conditions
CA10	TioF	Port Output Fall Time	—	—	—	ns	See parameter D032
CA11	TioR	Port Output Rise Time	—	—	—	ns	See parameter D031
CA20	Tcwf	Pulse-Width to Trigger CAN Wake-up Filter	120	—	—	ns	—

Note 1: These parameters are characterized but not tested in manufacturing.

2: Data in “Typ” column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

PIC24HJXXXGPX06A/X08A/X10A

TABLE 24-42: ADC CONVERSION (12-BIT MODE) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	Symbol	Characteristic	Min.	Typ ⁽²⁾	Max.	Units	Conditions
Clock Parameters⁽¹⁾							
AD50	TAD	ADC Clock Period	117.6	—	—	ns	—
AD51	tRC	ADC Internal RC Oscillator Period	—	250	—	ns	—
Conversion Rate							
AD55	tCONV	Conversion Time	—	14 TAD	—	ns	—
AD56	FCNV	Throughput Rate	—	—	500	ksps	—
AD57	TSAMP	Sample Time	3 TAD	—	—	—	—
Timing Parameters							
AD60	tPCS	Conversion Start from Sample Trigger ⁽²⁾	2.0 TAD	—	3.0 TAD	—	Auto convert trigger not selected
AD61	tPSS	Sample Start from Setting Sample (SAMP) bit ⁽²⁾	2.0 TAD	—	3.0 TAD	—	—
AD62	tCSS	Conversion Completion to Sample Start (ASAM = 1) ⁽²⁾	—	0.5 TAD	—	—	—
AD63	tDPU	Time to Stabilize Analog Stage from ADC Off to ADC On ^(2,3)	—	—	20	μs	—

- Note 1:** Because the sample caps eventually loses charge, clock rates below 10 kHz may affect linearity performance, especially at elevated temperatures.
- 2:** These parameters are characterized but not tested in manufacturing.
- 3:** tDPU is the time required for the ADC module to stabilize when it is turned on (AD1CON1<ADON> = 1). During this time, the ADC result is indeterminate.

FIGURE 26-9: TYPICAL FRC FREQUENCY @ VDD = 3.3V

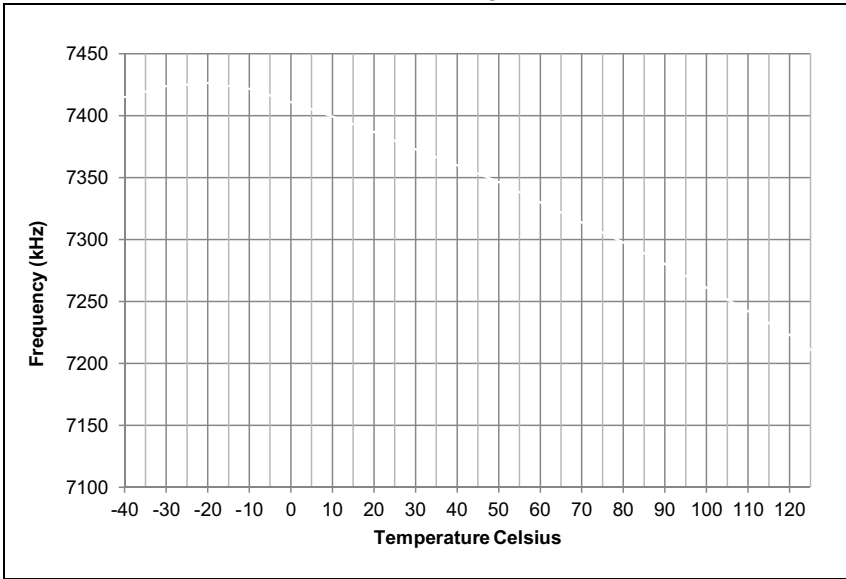
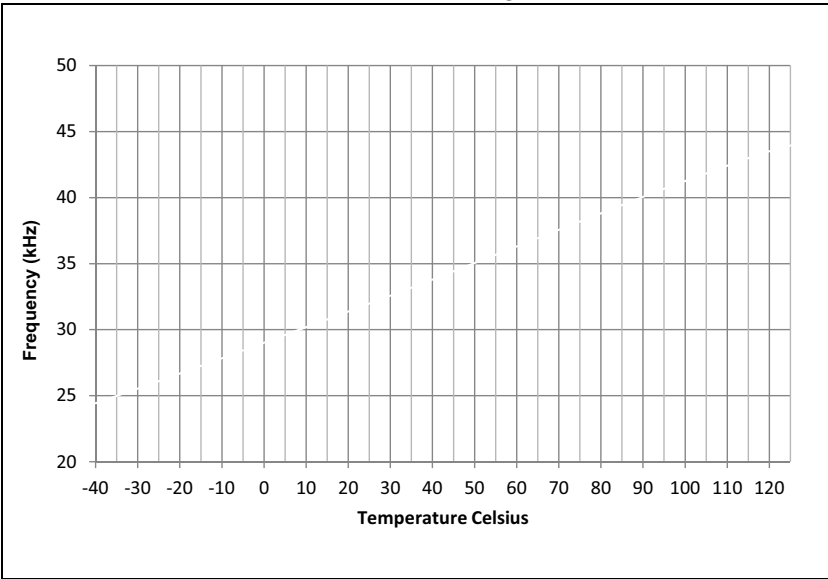


FIGURE 26-10: TYPICAL LPRC FREQUENCY @ VDD = 3.3V



PIC24HJXXXGPX06A/X08A/X10A

R

Reader Response	322
Registers	
ADxCHS0 (ADCx Input Channel 0 Select)	217
ADxCHS123 (ADCx Input Channel 1, 2, 3 Select)	216
ADxCON1 (ADCx Control 1)	211
ADxCON2 (ADCx Control 2)	213
ADxCON3 (ADCx Control 3)	214
ADxCON4 (ADCx Control 4)	215
ADxCSSH (ADCx Input Scan Select High)	218
ADxCSSL (ADCx Input Scan Select Low)	218
ADxPCFGH (ADCx Port Configuration High)	219
ADxPCFGL (ADCx Port Configuration Low)	220
CiBUFPNT1 (ECAN Filter 0-3 Buffer Pointer)	193
CiBUFPNT2 (ECAN Filter 4-7 Buffer Pointer)	194
CiBUFPNT3 (ECAN Filter 8-11 Buffer Pointer)	195
CiBUFPNT4 (ECAN Filter 12-15 Buffer Pointer)	196
CiCFG1 (ECAN Baud Rate Configuration 1)	190
CiCFG2 (ECAN Baud Rate Configuration 2)	191
CiCTRL1 (ECAN Control 1)	182
CiCTRL2 (ECAN Control 2)	183
CiEC (ECAN Transmit/Receive Error Count)	189
CiFCTRL (ECAN FIFO Control)	185
CiFEN1 (ECAN Acceptance Filter Enable)	192
CiFIFO (ECAN FIFO Status)	186
CiFMSKSEL1 (ECAN Filter 7-0 Mask Selection)	198, 199
CiINTE (ECAN Interrupt Enable)	188
CiINTF (ECAN Interrupt Flag)	187
CiRXFnEID (ECAN Acceptance Filter n Extended Identifier)	197
CiRXFnSID (ECAN Acceptance Filter n Standard Identifier)	197
CiRXFUL1 (ECAN Receive Buffer Full 1)	201
CiRXFUL2 (ECAN Receive Buffer Full 2)	201
CiRXMnEID (ECAN Acceptance Filter Mask n Extended Identifier)	200
CiRXMnSID (ECAN Acceptance Filter Mask n Standard Identifier)	200
CiRXOVF1 (ECAN Receive Buffer Overflow 1)	202
CiRXOVF2 (ECAN Receive Buffer Overflow 2)	202
CiTRBnDLC (ECAN Buffer n Data Length Control)	205
CiTRBnEID (ECAN Buffer n Extended Identifier)	204
CiTRBnSID (ECAN Buffer n Standard Identifier)	204
CiTRBnSTAT (ECAN Receive Buffer n Status)	206
CiTRmnCON (ECAN TX/RX Buffer m Control)	203
CiVEC (ECAN Interrupt Code)	184
CLKDIV (Clock Divisor)	128
CORCON (Core Control)	27, 74
DMACS0 (DMA Controller Status 0)	119
DMACS1 (DMA Controller Status 1)	121
DMAxCNT (DMA Channel x Transfer Count)	118
DMAxCON (DMA Channel x Control)	115
DMAxPAD (DMA Channel x Peripheral Address)	118
DMAxREQ (DMA Channel x IRQ Select)	116
DMAxSTA (DMA Channel x RAM Start Address A)	117
DMAxSTB (DMA Channel x RAM Start Address B)	117
DSADR (Most Recent DMA RAM Address)	122
I2CxCON (I2Cx Control)	168
I2CxMSK (I2Cx Slave Mode Address Mask)	172
I2CxSTAT (I2Cx Status)	170

ICxCON (Input Capture x Control)	154
IEC0 (Interrupt Enable Control 0)	85
IEC1 (Interrupt Enable Control 1)	87
IEC2 (Interrupt Enable Control 2)	89
IEC3 (Interrupt Enable Control 3)	91
IEC4 (Interrupt Enable Control 4)	92
IFS0 (Interrupt Flag Status 0)	77
IFS1 (Interrupt Flag Status 1)	79
IFS2 (Interrupt Flag Status 2)	81
IFS3 (Interrupt Flag Status 3)	83
IFS4 (Interrupt Flag Status 4)	84
INTCON1 (Interrupt Control 1)	75
INTCON2 (Interrupt Control 2)	76
IPC0 (Interrupt Priority Control 0)	93
IPC1 (Interrupt Priority Control 1)	94
IPC10 (Interrupt Priority Control 10)	103
IPC11 (Interrupt Priority Control 11)	104
IPC12 (Interrupt Priority Control 12)	105
IPC13 (Interrupt Priority Control 13)	106
IPC14 (Interrupt Priority Control 14)	107
IPC15 (Interrupt Priority Control 15)	107
IPC16 (Interrupt Priority Control 16)	108, 110
IPC17 (Interrupt Priority Control 17)	109
IPC2 (Interrupt Priority Control 2)	95
IPC3 (Interrupt Priority Control 3)	96
IPC4 (Interrupt Priority Control 4)	97
IPC5 (Interrupt Priority Control 5)	98
IPC6 (Interrupt Priority Control 6)	99
IPC7 (Interrupt Priority Control 7)	100
IPC8 (Interrupt Priority Control 8)	101
IPC9 (Interrupt Priority Control 9)	102
NVMCON (Flash Memory Control)	61
OCxCON (Output Compare x Control)	157
OSCCON (Oscillator Control)	126
OSCTUN (FRC Oscillator Tuning)	130
PLLFBF (PLL Feedback Divisor)	129
PMD1 (Peripheral Module Disable Control Register 1)	135
PMD1 (Peripheral Module Disable Control Register 1)	135
PMD2 (Peripheral Module Disable Control Register 2)	137
PMD3 (Peripheral Module Disable Control Register 3)	139
RCON (Reset Control)	66
SPIxCON1 (SPIx Control 1)	162
SPIxCON2 (SPIx Control 2)	164
SPIxSTAT (SPIx Status and Control)	161
SR (CPU Status)	26, 74
T1CON (Timer1 Control)	146
TxCON (T2CON, T4CON, T6CON or T8CON Control)	150
TyCON (T3CON, T5CON, T7CON or T9CON Control)	151
UxMODE (UARTx Mode)	175
UxSTA (UARTx Status and Control)	177
Reset	
Clock Source Selection	67
Special Function Register Reset States	68
Times	67
Reset Sequence	69
Resets	65

PIC24HJXXXGPX06A/X08A/X10A

S

Serial Peripheral Interface (SPI)	159
Software Simulator (MPLAB SIM)	239
Software Stack Pointer, Frame Pointer	
CALL Stack Frame	53
Special Features	221
SPI Module	
SPI1 Register Map	41
SPI2 Register Map	41
Symbols Used in Opcode Descriptions	230
System Control	
Register Map	52

T

Temperature and Voltage Specifications	
AC	252, 291
Timer1	145
Timer2/3, Timer4/5, Timer6/7 and Timer8/9	147
Timing Characteristics	
CLKO and I/O	255
Timing Diagrams	
10-bit Analog-to-Digital Conversion (CHPS<1:0> = 01, SIMSAM = 0, ASAM = 1, SSRC<2:0> = 111, SAMC<4:0> = 00001)	284
10-bit Analog-to-Digital Conversion (CHPS<1:0> = 01, SIMSAM = 0, ASAM = 0, SSRC<2:0> = 000)	284
12-bit Analog-to-Digital Conversion (ASAM = 0, SSRC<2:0> = 000)	282
ECAN I/O	278
External Clock	253
I2Cx Bus Data (Master Mode)	274
I2Cx Bus Data (Slave Mode)	276
I2Cx Bus Start/Stop Bits (Master Mode)	274
I2Cx Bus Start/Stop Bits (Slave Mode)	276
Input Capture (CAPx)	260
OC/PWM	261
Output Compare (OCx)	260
Reset, Watchdog Timer, Oscillator Start-up Timer and Power-up Timer	256
Timer1, 2 and 3 External Clock	258
Timing Requirements	
ADC Conversion (10-bit mode)	295
ADC Conversion (12-bit Mode)	295
CLKO and I/O	255
External Clock	253
Input Capture	260
SP1x Master Mode (CKE = 0)	292
SP1x Module Master Mode (CKE = 1)	292
SP1x Module Slave Mode (CKE = 0)	293
SP1x Module Slave Mode (CKE = 1)	293

Timing Specifications

10-bit Analog-to-Digital Conversion	
Requirements	285
CAN I/O Requirements	278
I2Cx Bus Data Requirements (Master Mode)	275
I2Cx Bus Data Requirements (Slave Mode)	277
Output Compare Requirements	260
PLL Clock	254, 291
Reset, Watchdog Timer, Oscillator Start-up Timer, Power-up Timer and Brown-out	
Reset Requirements	257
Simple OC/PWM Mode Requirements	261
Timer1 External Clock Requirements	258
Timer2 External Clock Requirements	259
Timer3 External Clock Requirements	259

U

UART Module	
UART1 Register Map	40
UART2 Register Map	41

V

Voltage Regulator (On-Chip)	226
-----------------------------------	-----

W

Watchdog Timer (WDT)	221, 227
Programming Considerations	227
WWW Address	321
WWW, On-Line Support	13

PIC24HJXXXGPX06A/X08A/X10A

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

	PIC	24	HJ	256	GP	6	10	A	T	I/PT	-	XXX
Microchip Trademark	_____	_____	_____	_____	_____	_____	_____	_____	_____	_____	_____	_____
Architecture	_____	_____	_____	_____	_____	_____	_____	_____	_____	_____	_____	_____
Flash Memory Family	_____	_____	_____	_____	_____	_____	_____	_____	_____	_____	_____	_____
Program Memory Size (KB)	_____	_____	_____	_____	_____	_____	_____	_____	_____	_____	_____	_____
Product Group	_____	_____	_____	_____	_____	_____	_____	_____	_____	_____	_____	_____
Pin Count	_____	_____	_____	_____	_____	_____	_____	_____	_____	_____	_____	_____
Revision Level	_____	_____	_____	_____	_____	_____	_____	_____	_____	_____	_____	_____
Tape and Reel Flag (if applicable)	_____	_____	_____	_____	_____	_____	_____	_____	_____	_____	_____	_____
Temperature Range	_____	_____	_____	_____	_____	_____	_____	_____	_____	_____	_____	_____
Package	_____	_____	_____	_____	_____	_____	_____	_____	_____	_____	_____	_____
Pattern	_____	_____	_____	_____	_____	_____	_____	_____	_____	_____	_____	_____

Architecture:	24	=	16-bit Microcontroller
Flash Memory Family:	HJ	=	Flash program memory, 3.3V, High-speed
Product Group:	GP2	=	General purpose family
	GP3	=	General purpose family
	GP5	=	General purpose family
	GP6	=	General purpose family
Pin Count:	06	=	64-pin
	10	=	100-pin
Temperature Range:	I	=	-40°C to +85°C (Industrial)
	E	=	-40°C to +125°C (Extended)
	H	=	-40°C to +150°C (High)
Package:	PT	=	10x10 or 12x12 mm TQFP (Thin Quad Flatpack)
	PF	=	14x14 mm TQFP (Thin Quad Flatpack)
	MR	=	9x9x0.9 mm QFN (Thin Quad Flatpack)
Pattern:	Three-digit QTP, SQTP, Code or Special Requirements (blank otherwise)		
	ES	=	Engineering Sample

Examples:

- PIC24HJ256GP210AI/PT:
General-purpose PIC24H, 256 KB program memory, 100-pin, Industrial temp., TQFP package.
- PIC24HJ64GP506AI/PT-ES:
General-purpose PIC24H, 64 KB program memory, 64-pin, Industrial temp., TQFP package, Engineering Sample.

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Information contained in this publication regarding device applications and the like is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION, INCLUDING BUT NOT LIMITED TO ITS CONDITION, QUALITY, PERFORMANCE, MERCHANTABILITY OR FITNESS FOR PURPOSE. Microchip disclaims all liability arising from this information and its use. Use of Microchip devices in life support and/or safety applications is entirely at the buyer's risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights.

Trademarks

The Microchip name and logo, the Microchip logo, dsPIC, KEELOQ, KEELOQ logo, MPLAB, PIC, PICmicro, PICSTART, PIC³² logo, rfPIC and UNI/O are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

FilterLab, Hampshire, HI-TECH C, Linear Active Thermistor, MXDEV, MXLAB, SEEVAL and The Embedded Control Solutions Company are registered trademarks of Microchip Technology Incorporated in the U.S.A.

Analog-for-the-Digital Age, Application Maestro, chipKIT, chipKIT logo, CodeGuard, dsPICDEM, dsPICDEM.net, dsPICworks, dsSPEAK, ECAN, ECONOMONITOR, FanSense, HI-TIDE, In-Circuit Serial Programming, ICSP, Mindi, MiWi, MPASM, MPLAB Certified logo, MPLIB, MPLINK, mTouch, Omniscent Code Generation, PICC, PICC-18, PICDEM, PICDEM.net, PICKit, PICtail, REAL ICE, rfLAB, Select Mode, Total Endurance, TSHARC, UniWinDriver, WiperLock and ZENA are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

SQTP is a service mark of Microchip Technology Incorporated in the U.S.A.

All other trademarks mentioned herein are property of their respective companies.

© 2009-2012, Microchip Technology Incorporated, Printed in the U.S.A., All Rights Reserved.

Printed on recycled paper.

ISBN: 978-1-62076-345-2

QUALITY MANAGEMENT SYSTEM
CERTIFIED BY DNV
= ISO/TS 16949 =

Microchip received ISO/TS-16949:2009 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.