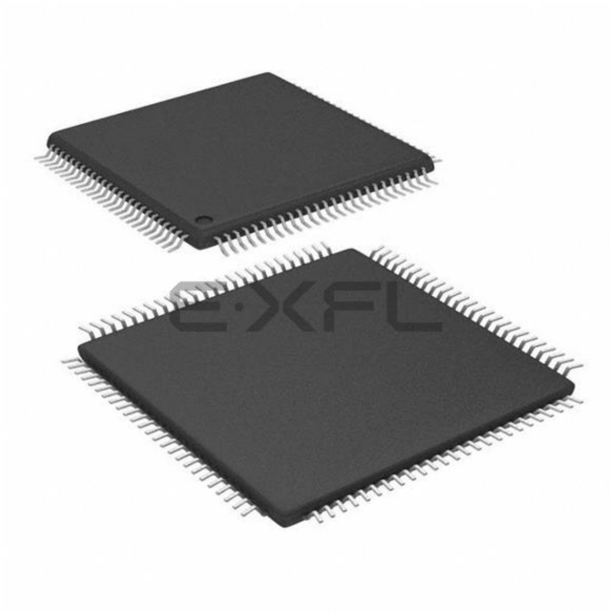
Microchip Technology - PIC24HJ128GP510AT-I/PT Datasheet

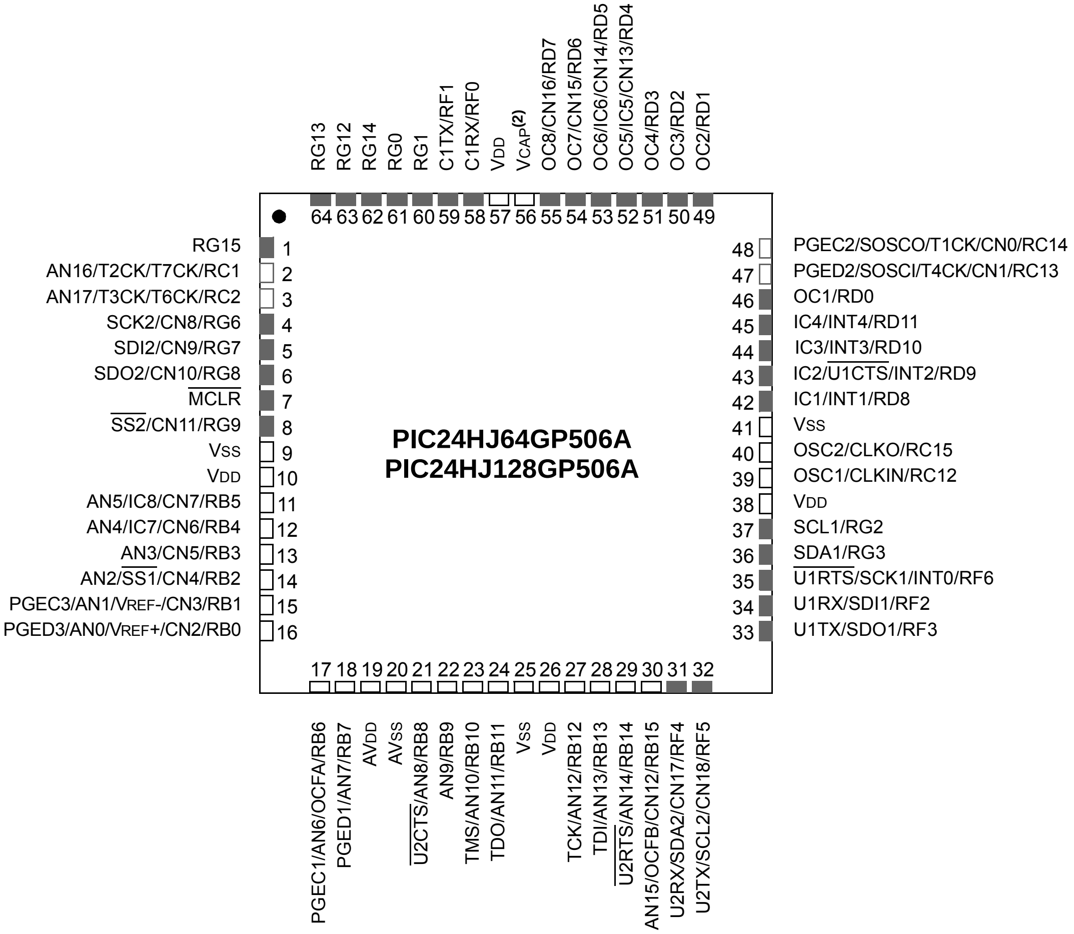


Details	
Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	40 MIPs
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	85
Program Memory Size	128KB (43K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 32x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24hj128gp510at-i-pt

Pin Diagrams (Continued)

64-Pin QFN[1]

■ = Pins are up to 5V tolerant



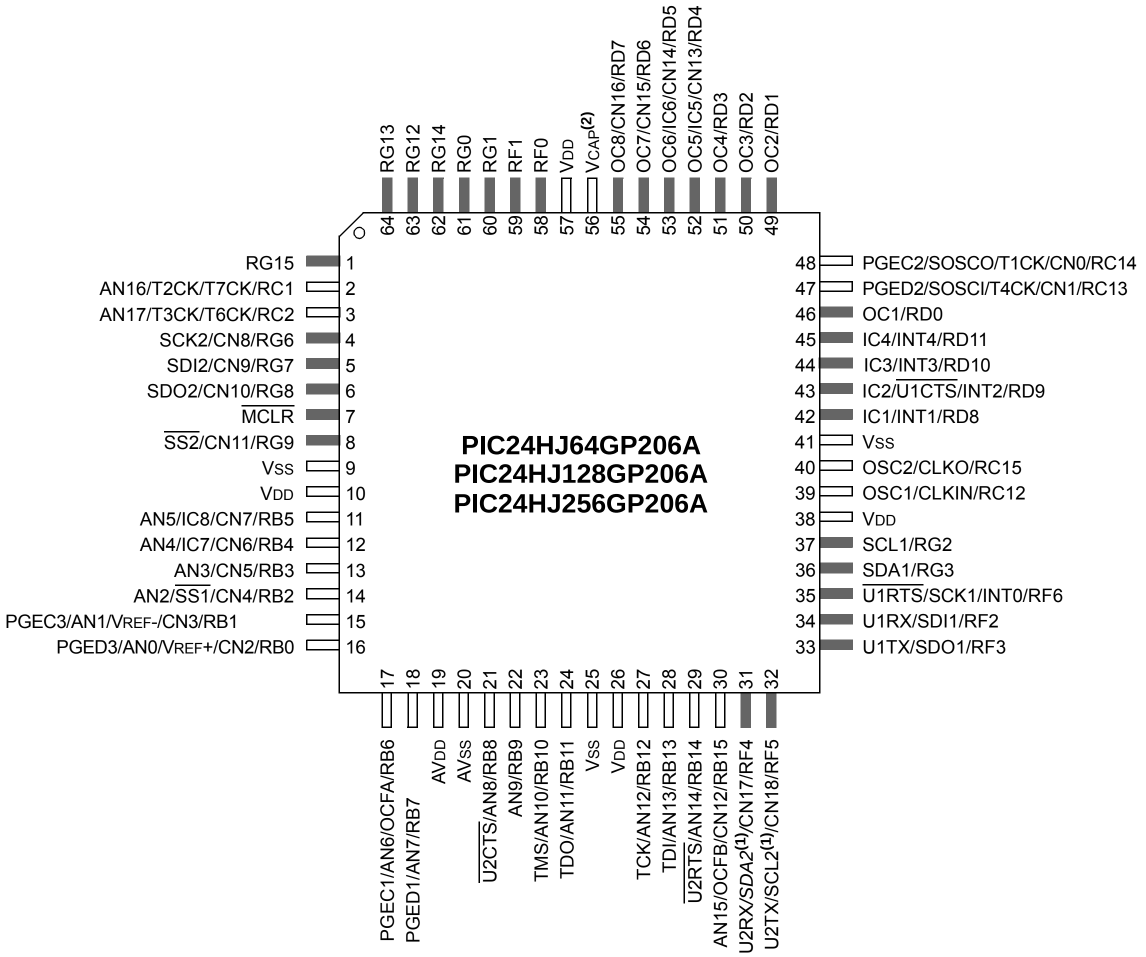
Note 1: The metal plane at the bottom of the device is not connected to any pins and should be connected to VSS externally.

2: Refer to **Section 2.3 "CPU Logic Filter Capacitor Connection (VCAP)"** for proper connection to this pin.

Pin Diagrams (Continued)

64-Pin TQFP

▨ = Pins are up to 5V tolerant



Note 1: This pin is not present on the PIC24HJ64GP206A device.

2: Refer to **Section 2.3 "CPU Logic Filter Capacitor Connection (VCAP)"** for proper connection to this pin.

TABLE 4-19: ECAN1 REGISTER MAP WHEN C1CTRL1.WIN = 0 FOR PIC24HJXXXGP506A/510A/610A DEVICES ONLY

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
	0400-041E	**See definition when WIN = x**																
C1RXFUL1	0420	RXFUL15	RXFUL14	RXFUL13	RXFUL12	RXFUL11	RXFUL10	RXFUL9	RXFUL8	RXFUL7	RXFUL6	RXFUL5	RXFUL4	RXFUL3	RXFUL2	RXFUL1	RXFUL0	0000
C1RXFUL2	0422	RXFUL31	RXFUL30	RXFUL29	RXFUL28	RXFUL27	RXFUL26	RXFUL25	RXFUL24	RXFUL23	RXFUL22	RXFUL21	RXFUL20	RXFUL19	RXFUL18	RXFUL17	RXFUL16	0000
C1RXOVF1	0428	RXOVF15	RXOVF14	RXOVF13	RXOVF12	RXOVF11	RXOVF10	RXOVF9	RXOVF8	RXOVF7	RXOVF6	RXOVF5	RXOVF4	RXOVF3	RXOVF2	RXOVF1	RXOVF0	0000
C1RXOVF2	042A	RXOVF31	RXOVF30	RXOVF29	RXOVF28	RXOVF27	RXOVF26	RXOVF25	RXOVF24	RXOVF23	RXOVF22	RXOVF21	RXOVF20	RXOVF19	RXOVF18	RXOVF17	RXOVF16	0000
C1TR01CON	0430	TXEN1	TX ABT1	TX LARB1	TX ERR1	TX REQ1	RTREN1	TX1PRI<1:0>		TXEN0	TX ABAT0	TX LARB0	TX ERR0	TX REQ0	RTREN0	TX0PRI<1:0>		0000
C1TR23CON	0432	TXEN3	TX ABT3	TX LARB3	TX ERR3	TX REQ3	RTREN3	TX3PRI<1:0>		TXEN2	TX ABAT2	TX LARB2	TX ERR2	TX REQ2	RTREN2	TX2PRI<1:0>		0000
C1TR45CON	0434	TXEN5	TX ABT5	TX LARB5	TX ERR5	TX REQ5	RTREN5	TX5PRI<1:0>		TXEN4	TX ABAT4	TX LARB4	TX ERR4	TX REQ4	RTREN4	TX4PRI<1:0>		0000
C1TR67CON	0436	TXEN7	TX ABT7	TX LARB7	TX ERR7	TX REQ7	RTREN7	TX7PRI<1:0>		TXEN6	TX ABAT6	TX LARB6	TX ERR6	TX REQ6	RTREN6	TX6PRI<1:0>		xxxx
C1RXD	0440	Recieved Data Word																xxxx
C1TXD	0442	Transmit Data Word																xxxx

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal for PinHigh devices.

TABLE 4-20: ECAN1 REGISTER MAP WHEN C1CTRL1.WIN = 1 FOR PIC24HJXXXGP506A/510A/610A DEVICES ONLY

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
	0400-041E	**See definition when WIN = x**																
C1BUFPNT1	0420	F3BP<3:0>				F2BP<3:0>				F1BP<3:0>				F0BP<3:0>				0000
C1BUFPNT2	0422	F7BP<3:0>				F6BP<3:0>				F5BP<3:0>				F4BP<3:0>				0000
C1BUFPNT3	0424	F11BP<3:0>				F10BP<3:0>				F9BP<3:0>				F8BP<3:0>				0000
C1BUFPNT4	0426	F15BP<3:0>				F14BP<3:0>				F13BP<3:0>				F12BP<3:0>				0000
C1RXM0SID	0430	SID<10:3>								SID<2:0>			—	MIDE	—	EID<17:16>		xxxx
C1RXM0EID	0432	EID<15:8>								EID<7:0>								xxxx
C1RXM1SID	0434	SID<10:3>								SID<2:0>			—	MIDE	—	EID<17:16>		xxxx
C1RXM1EID	0436	EID<15:8>								EID<7:0>								xxxx
C1RXM2SID	0438	SID<10:3>								SID<2:0>			—	MIDE	—	EID<17:16>		xxxx
C1RXM2EID	043A	EID<15:8>								EID<7:0>								xxxx
C1RXF0SID	0440	SID<10:3>								SID<2:0>			—	EXIDE	—	EID<17:16>		xxxx
C1RXF0EID	0442	EID<15:8>								EID<7:0>								xxxx
C1RXF1SID	0444	SID<10:3>								SID<2:0>			—	EXIDE	—	EID<17:16>		xxxx

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal for PinHigh devices.

5.0 FLASH PROGRAM MEMORY

Note 1: This data sheet summarizes the features of the PIC24HJXXXGPX06A/X08A/X10A family of devices. However, it is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 5. "Flash Programming"** (DS70191) of the *"dsPIC33F/PIC24H Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The PIC24HJXXXGPX06A/X08A/X10A devices contain internal Flash program memory for storing and executing application code. The memory is readable, writable and erasable during normal operation over the entire VDD range.

Flash memory can be programmed in two ways:

1. In-Circuit Serial Programming™ (ICSP™) programming capability
2. Run-Time Self-Programming (RTSP)

ICSP programming capability allows a PIC24HJXXXGPX06A/X08A/X10A device to be serially programmed while in the end application circuit. This is simply done with two lines for programming clock and programming data (one of the alternate programming pin pairs: PGECx/PGEDx, and three other lines for power (VDD), ground (VSS) and Master Clear ($\overline{\text{MCLR}}$). This allows customers to manufacture boards with unprogrammed devices and then program the digital signal controller just before shipping the product. This also allows the most recent firmware or a custom firmware to be programmed.

RTSP is accomplished using `TBLRD` (table read) and `TBLWT` (table write) instructions. With RTSP, the user can write program memory data either in blocks or 'rows' of 64 instructions (192 bytes) at a time, or single instructions and erase program memory in blocks or 'pages' of 512 instructions (1536 bytes) at a time.

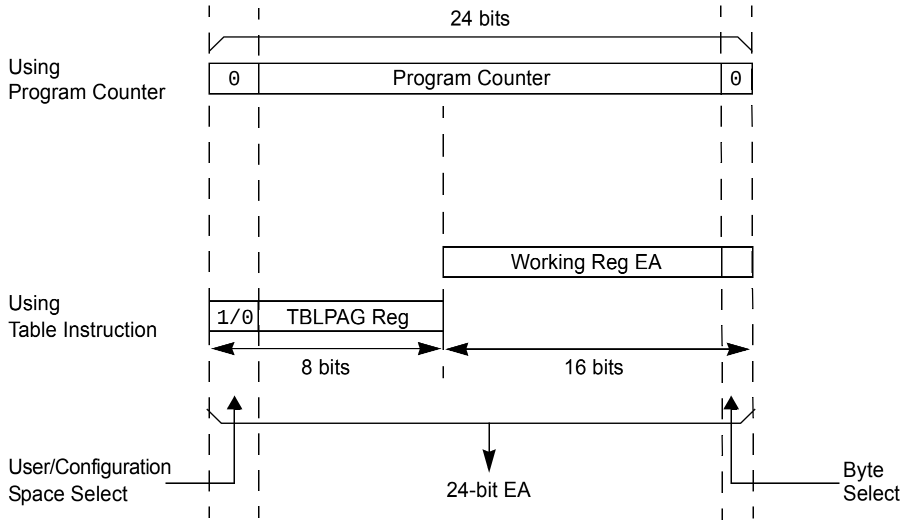
5.1 Table Instructions and Flash Programming

Regardless of the method used, all programming of Flash memory is done with the table read and table write instructions. These allow direct read and write access to the program memory space from the data memory while the device is in normal operating mode. The 24-bit target address in the program memory is formed using bits<7:0> of the TBLPAG register and the Effective Address (EA) from a W register specified in the table instruction, as shown in Figure 5-1.

The `TBLRDL` and the `TBLWTL` instructions are used to read or write to bits<15:0> of program memory. `TBLRDL` and `TBLWTL` can access program memory in both Word and Byte modes.

The `TBLRDH` and `TBLWTH` instructions are used to read or write to bits<23:16> of program memory. `TBLRDH` and `TBLWTH` can also access program memory in Word or Byte mode.

FIGURE 5-1: ADDRESSING FOR TABLE REGISTERS



6.0 RESET

Note 1: This data sheet summarizes the features of the PIC24HJXXXGPX06A/X08A/X10A family of devices. However, it is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 8. "Reset"** (DS70192) of the *"dsPIC33F/PIC24H Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The Reset module combines all Reset sources and controls the device Master Reset Signal, $\overline{\text{SYSRST}}$. The following is a list of device Reset sources:

- POR: Power-on Reset
- BOR: Brown-out Reset
- $\overline{\text{MCLR}}$: Master Clear Pin Reset
- SWR: RESET Instruction
- WDT: Watchdog Timer Reset
- TRAPR: Trap Conflict Reset
- IOPUWR: Illegal Opcode and Uninitialized W Register Reset

A simplified block diagram of the Reset module is shown in Figure 6-1.

Any active source of Reset will make the $\overline{\text{SYSRST}}$ signal active. Many registers associated with the CPU and peripherals are forced to a known Reset state. Most registers are unaffected by a Reset; their status is unknown on POR and unchanged by all other Resets.

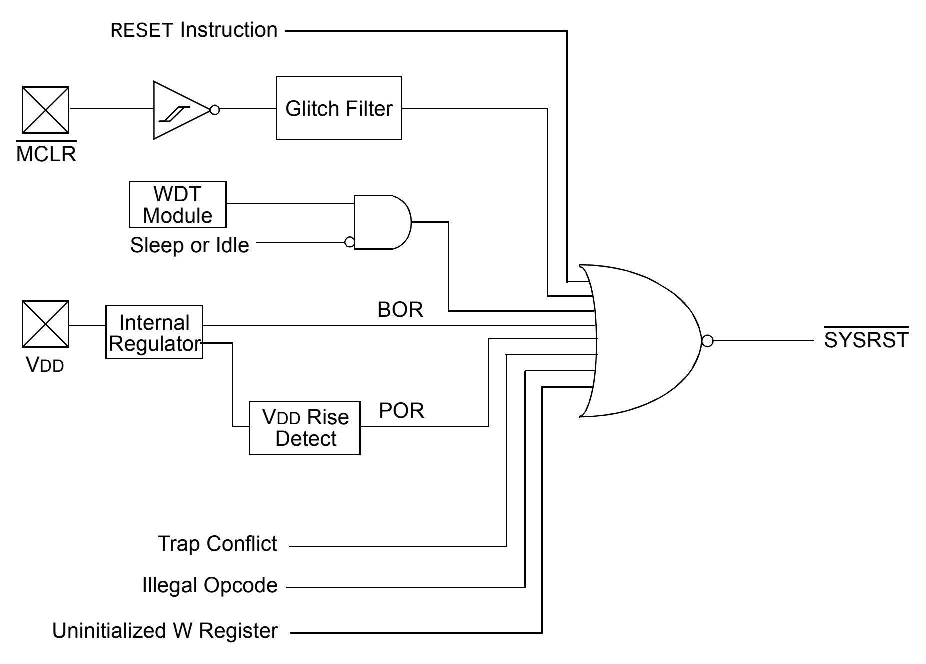
Note: Refer to the specific peripheral or CPU section of this data sheet for register Reset states.

All types of device Reset will set a corresponding status bit in the RCON register to indicate the type of Reset (see Register 6-1). A POR will clear all bits, except for the POR bit (RCON<0>), that are set. The user can set or clear any bit at any time during code execution. The RCON bits only serve as status bits. Setting a particular Reset status bit in software does not cause a device Reset to occur.

The RCON register also has other bits associated with the Watchdog Timer and device power-saving states. The function of these bits is discussed in other sections of this manual.

Note: The status bits in the RCON register should be cleared after they are read so that the next RCON register value after a device Reset will be meaningful.

FIGURE 6-1: RESET SYSTEM BLOCK DIAGRAM



REGISTER 7-6: IFS1: INTERRUPT FLAG STATUS REGISTER 1 (CONTINUED)

bit 3	**CNIF:** Input Change Notification Interrupt Flag Status bit 1 = Interrupt request has occurred 0 = Interrupt request has not occurred
bit 2	**Unimplemented:** Read as ‘0’
bit 1	**MI2C1IF:** I2C1 Master Events Interrupt Flag Status bit 1 = Interrupt request has occurred 0 = Interrupt request has not occurred
bit 0	**SI2C1IF:** I2C1 Slave Events Interrupt Flag Status bit 1 = Interrupt request has occurred 0 = Interrupt request has not occurred

REGISTER 7-15: IPC0: INTERRUPT PRIORITY CONTROL REGISTER 0

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	T1IP<2:0>			—	OC1IP<2:0>		
bit 15							bit 8

U-0	R/W-1	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
—	IC1IP<2:0>			—	INT0IP<2:0>		
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15	**Unimplemented:** Read as ‘`0`’
bit 14-12	**T1IP<2:0>:** Timer1 Interrupt Priority bits `111` = Interrupt is priority 7 (highest priority interrupt) • • • `001` = Interrupt is priority 1 `000` = Interrupt source is disabled
bit 11	**Unimplemented:** Read as ‘`0`’
bit 10-8	**OC1IP<2:0>:** Output Compare Channel 1 Interrupt Priority bits `111` = Interrupt is priority 7 (highest priority interrupt) • • • `001` = Interrupt is priority 1 `000` = Interrupt source is disabled
bit 7	**Unimplemented:** Read as ‘`0`’
bit 6-4	**IC1IP<2:0>:** Input Capture Channel 1 Interrupt Priority bits `111` = Interrupt is priority 7 (highest priority interrupt) • • • `001` = Interrupt is priority 1 `000` = Interrupt source is disabled
bit 3	**Unimplemented:** Read as ‘`0`’
bit 2-0	**INT0IP<2:0>:** External Interrupt 0 Priority bits `111` = Interrupt is priority 7 (highest priority interrupt) • • • `001` = Interrupt is priority 1 `000` = Interrupt source is disabled

REGISTER 8-3: DMAxSTA: DMA CHANNEL x RAM START ADDRESS OFFSET REGISTER A

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
STA<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
STA<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-0	**STA<15:0>:** Primary DMA RAM Start Address bits (source or destination)

REGISTER 8-4: DMAxSTB: DMA CHANNEL x RAM START ADDRESS OFFSET REGISTER B

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
STB<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
STB<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-0	**STB<15:0>:** Secondary DMA RAM Start Address bits (source or destination)

9.1 CPU Clocking System

There are seven system clock options provided by the PIC24HJXXXGPX06A/X08A/X10A:

- FRC Oscillator
- FRC Oscillator with PLL
- Primary (XT, HS or EC) Oscillator
- Primary Oscillator with PLL
- Secondary (LP) Oscillator
- LPRC Oscillator
- FRC Oscillator with postscaler

9.1.1 SYSTEM CLOCK SOURCES

The FRC (Fast RC) internal oscillator runs at a nominal frequency of 7.37 MHz. The user software can tune the FRC frequency. User software can optionally specify a factor (ranging from 1:2 to 1:256) by which the FRC clock frequency is divided. This factor is selected using the FRCDIV<2:0> (CLKDIV<10:8>) bits.

The primary oscillator can use one of the following as its clock source:

- XT (Crystal): Crystals and ceramic resonators in the range of 3 MHz to 10 MHz. The crystal is connected to the OSC1 and OSC2 pins.
- HS (High-Speed Crystal): Crystals in the range of 10 MHz to 40 MHz. The crystal is connected to the OSC1 and OSC2 pins.
- EC (External Clock): External clock signal is directly applied to the OSC1 pin.

The secondary (LP) oscillator is designed for low power and uses a 32.768 kHz crystal or ceramic resonator. The LP oscillator uses the SOSCI and SOSCO pins.

The LPRC (Low-Power RC) internal oscIllator runs at a nominal frequency of 32.768 kHz. It is also used as a reference clock by the Watchdog Timer (WDT) and Fail-Safe Clock Monitor (FSCM).

The clock signals generated by the FRC and primary oscillators can be optionally applied to an on-chip Phase-Locked Loop (PLL) to provide a wide range of output frequencies for device operation. PLL configuration is described in **Section 9.1.3 “PLL Configuration”**.

The FRC frequency depends on the FRC accuracy (see Table 24-19) and the value of the FRC Oscillator Tuning register (see Register 9-4).

9.1.2 SYSTEM CLOCK SELECTION

The oscillator source that is used at a device Power-on Reset event is selected using Configuration bit settings. The oscillator Configuration bit settings are located in the Configuration registers in the program memory. (Refer to **Section 21.1 “Configuration Bits”** for further details.) The Initial Oscillator Selection Configuration bits, FNOSC<2:0> (FOSCSEL<2:0>), and the Primary Oscillator Mode Select Configuration bits, POSCMD<1:0> (FOSC<1:0>), select the oscillator source that is used at a Power-on Reset. The FRC primary oscillator is the default (unprogrammed) selection.

The Configuration bits allow users to choose between twelve different clock modes, shown in Table 9-1.

The output of the oscillator (or the output of the PLL if a PLL mode has been selected) FOSC is divided by 2 to generate the device instruction clock (FCY) and the peripheral clock time base (FP). FCY defines the operating speed of the device, and speeds up to 40 MHz are supported by the PIC24HJXXXGPX06A/X08A/X10A architecture.

Instruction execution speed or device operating frequency, FCY, is calculated, as shown in Equation 9-1:

EQUATION 9-1: DEVICE OPERATING FREQUENCY

$$F_{CY} = \frac{F_{OSC}}{2}$$

9.1.3 PLL CONFIGURATION

The primary oscillator and internal FRC oscillator can optionally use an on-chip PLL to obtain higher speeds of operation. The PLL provides a significant amount of flexibility in selecting the device operating speed. A block diagram of the PLL is shown in Figure 9-2.

The output of the primary oscillator or FRC, denoted as ‘FIN’, is divided down by a prescale factor (N1) of 2, 3, ... or 33 before being provided to the PLL’s Voltage Controlled Oscillator (VCO). The input to the VCO must be selected to be in the range of 0.8 MHz to 8 MHz. Since the minimum prescale factor is 2, this implies that FIN must be chosen to be in the range of 1.6 MHz to 16 MHz. The prescale factor ‘N1’ is selected using the PLLPRE<4:0> bits (CLKDIV<4:0>).

The PLL Feedback Divisor, selected using the PLLDIV<8:0> bits (PLLFBD<8:0>), provides a factor ‘M’, by which the input to the VCO is multiplied. This factor must be selected such that the resulting VCO output frequency is in the range of 100 MHz to 200 MHz.

The VCO output is further divided by a postscale factor ‘N2’. This factor is selected using the PLLPOST<1:0> bits (CLKDIV<7:6>). ‘N2’ can be either 2, 4 or 8, and must be selected such that the PLL output frequency (FOSC) is in the range of 12.5 MHz to 80 MHz, which generates device operating speeds of 6.25-40 MIPS.

For a primary oscillator or FRC oscillator, output ‘FIN’, the PLL output ‘FOSC’ is given by:

EQUATION 9-2: FOSC CALCULATION

$$F_{OSC} = F_{IN} \cdot \left(\frac{M}{N1 \cdot N2}\right)$$

10.0 POWER-SAVING FEATURES

Note 1: This data sheet summarizes the features of the PIC24HJXXXGPX06A/X08A/X10A family of devices. However, it is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 9. "Watchdog Timer and Power-Saving Modes"** (DS70196) of the *"dsPIC33F/PIC24H Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The PIC24HJXXXGPX06A/X08A/X10A devices provide the ability to manage power consumption by selectively managing clocking to the CPU and the peripherals. In general, a lower clock frequency and a reduction in the number of circuits being clocked constitutes lower consumed power. PIC24HJXXXGPX06A/X08A/X10A devices can manage power consumption in four different ways:

- Clock frequency
- Instruction-based Sleep and Idle modes
- Software-controlled Doze mode
- Selective peripheral control in software

Combinations of these methods can be used to selectively tailor an application's power consumption while still maintaining critical application features, such as timing-sensitive communications.

10.1 Clock Frequency and Clock Switching

PIC24HJXXXGPX06A/X08A/X10A devices allow a wide range of clock frequencies to be selected under application control. If the system clock configuration is not locked, users can choose low-power or high-precision oscillators by simply changing the NOSC bits (OSCCON<10:8>). The process of changing a system clock during operation, as well as limitations to the process, are discussed in more detail in **Section 9.0 "Oscillator Configuration"**.

10.2 Instruction-Based Power-Saving Modes

PIC24HJXXXGPX06A/X08A/X10A devices have two special power-saving modes that are entered through the execution of a special `PWRSAV` instruction. Sleep mode stops clock operation and halts all code execution. Idle mode halts the CPU and code execution, but allows peripheral modules to continue operation. The assembly syntax of the `PWRSAV` instruction is shown in Example 10-1.

Note: `SLEEP_MODE` and `IDLE_MODE` are constants defined in the assembler include file for the selected device.

Sleep and Idle modes can be exited as a result of an enabled interrupt, WDT time-out or a device Reset. When the device exits these modes, it is said to "wake-up".

10.2.1 SLEEP MODE

Sleep mode has these features:

- The system clock source is shut down. If an on-chip oscillator is used, it is turned off.
- The device current consumption is reduced to a minimum, provided that no I/O pin is sourcing current
- The Fail-Safe Clock Monitor does not operate during Sleep mode since the system clock source is disabled
- The LPRC clock continues to run in Sleep mode if the WDT is enabled
- The WDT, if enabled, is automatically cleared prior to entering Sleep mode
- Some device features or peripherals may continue to operate in Sleep mode. This includes items such as the input change notification on the I/O ports, or peripherals that use an external clock input. Any peripheral that requires the system clock source for its operation is disabled in Sleep mode.

The device will wake-up from Sleep mode on any of these events:

- Any interrupt source that is individually enabled
- Any form of device Reset
- A WDT time-out

On wake-up from Sleep, the processor restarts with the same clock source that was active when Sleep mode was entered.

EXAMPLE 10-1: `PWRSAV` INSTRUCTION SYNTAX

```
PWRSAV  #SLEEP_MODE    ; Put the device into SLEEP mode
PWRSAV  #IDLE_MODE     ; Put the device into IDLE mode
```

REGISTER 10-2: PMD2: PERIPHERAL MODULE DISABLE CONTROL REGISTER 2 (CONTINUED)

bit 3 **OC4MD:** Output Compare 4 Module Disable bit

`1` = Output Compare 4 module is disabled
`0` = Output Compare 4 module is enabled

bit 2 **OC3MD:** Output Compare 3 Module Disable bit

`1` = Output Compare 3 module is disabled
`0` = Output Compare 3 module is enabled

bit 1 **OC2MD:** Output Compare 2 Module Disable bit

`1` = Output Compare 2 module is disabled
`0` = Output Compare 2 module is enabled

bit 0 **OC1MD:** Output Compare 1 Module Disable bit

`1` = Output Compare 1 module is disabled
`0` = Output Compare 1 module is enabled

14.1 Input Capture Registers

REGISTER 14-1: ICxCON: INPUT CAPTURE x CONTROL REGISTER

U-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
—	—	ICSIDL	—	—	—	—	—
bit 15							bit 8

<table>
<tr><td>R/W-0</td><td>R/W-0</td><td>R/W-0</td><td>R-0, HC</td><td>R-0, HC</td><td>R/W-0</td><td>R/W-0</td><td>R/W-0</td></tr>
<tr><td>ICTMR[1]</td><td colspan="2">ICI<1:0></td><td>ICOV</td><td>ICBNE</td><td colspan="3">ICM<2:0></td></tr>
<tr><td colspan="4">bit 7</td><td colspan="4" align="right">bit 0</td></tr>
</table>

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as ‘0’

-n = Value at POR ‘1’ = Bit is set ‘0’ = Bit is cleared x = Bit is unknown

bit 15-14	**Unimplemented:** Read as ‘`0`’
bit 13	**ICSIDL:** Input Capture Module Stop in Idle Control bit `1` = Input capture module will halt in CPU Idle mode `0` = Input capture module will continue to operate in CPU Idle mode
bit 12-8	**Unimplemented:** Read as ‘`0`’
bit 7	**ICTMR:** Input Capture Timer Select bits[1] `1` = TMR2 contents are captured on capture event `0` = TMR3 contents are captured on capture event
bit 6-5	**ICI<1:0>:** Select Number of Captures per Interrupt bits `11` = Interrupt on every fourth capture event `10` = Interrupt on every third capture event `01` = Interrupt on every second capture event `00` = Interrupt on every capture event
bit 4	**ICOV:** Input Capture Overflow Status Flag bit (read-only) `1` = Input capture overflow occurred `0` = No input capture overflow occurred
bit 3	**ICBNE:** Input Capture Buffer Empty Status bit (read-only) `1` = Input capture buffer is not empty, at least one more capture value can be read `0` = Input capture buffer is empty
bit 2-0	**ICM<2:0>:** Input Capture Mode Select bits `111` = Input capture functions as interrupt pin only when device is in Sleep or Idle mode (Rising edge detect only, all other control bits are not applicable.) `110` = Unused (module disabled) `101` = Capture mode, every 16th rising edge `100` = Capture mode, every 4th rising edge `011` = Capture mode, every rising edge `010` = Capture mode, every falling edge `001` = Capture mode, every edge (rising and falling) (ICI<1:0> bits do not control interrupt generation for this mode.) `000` = Input capture module turned off

REGISTER 18-1: UxMODE: UARTx MODE REGISTER (CONTINUED)

bit 4	**URXINV:** Receive Polarity Inversion bit `1` = UxRX Idle state is ‘`0`’ `0` = UxRX Idle state is ‘`1`’
bit 3	**BRGH:** High Baud Rate Enable bit `1` = BRG generates 4 clocks per bit period (4x baud clock, High-Speed mode) `0` = BRG generates 16 clocks per bit period (16x baud clock, Standard mode)
bit 2-1	**PDSEL<1:0>:** Parity and Data Selection bits `11` = 9-bit data, no parity `10` = 8-bit data, odd parity `01` = 8-bit data, even parity `00` = 8-bit data, no parity
bit 0	**STSEL:** Stop Bit Selection bit `1` = Two Stop bits `0` = One Stop bit

Note 1: Refer to **Section 17. “UART”** (DS70188) in the *“dsPIC33F/PIC24H Family Reference Manual”* for information on enabling the UART module for receive or transmit operation.

2: This feature is only available for the 16x BRG mode (BRGH = `0`).

REGISTER 19-26: CiTRmnCON: ECAN™ MODULE TX/RX BUFFER m CONTROL REGISTER (m = 0,2,4,6; n = 1,3,5,7)

R/W-0	R-0	R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0
TXENn	TXABTn	TXLARBn	TXERRn	TXREQn	RTRENn	TXnPRI<1:0>	
bit 15							bit 8

R/W-0	R-0	R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0
TXENm	TXABTm[1]	TXLARBm[1]	TXERRm[1]	TXREQm	RTRENm	TXmPRI<1:0>	
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-8 **See Definition for Bits 7-0, Controls Buffer n**

bit 7 **TXENm:** TX/RX Buffer Selection bit
`1` = Buffer TRBn is a transmit buffer
`0` = Buffer TRBn is a receive buffer

bit 6 **TXABTm:** Message Aborted bit[1]
`1` = Message was aborted
`0` = Message completed transmission successfully

bit 5 **TXLARBm:** Message Lost Arbitration bit[1]
`1` = Message lost arbitration while being sent
`0` = Message did not lose arbitration while being sent

bit 4 **TXERRm:** Error Detected During Transmission bit[1]
`1` = A bus error occurred while the message was being sent
`0` = A bus error did not occur while the message was being sent

bit 3 **TXREQm:** Message Send Request bit
Setting this bit to ‘`1`’ requests sending a message. The bit will automatically clear when the message is successfully sent. Clearing the bit to ‘`0`’ while set will request a message abort.

bit 2 **RTRENm:** Auto-Remote Transmit Enable bit
`1` = When a remote transmit is received, TXREQ will be set
`0` = When a remote transmit is received, TXREQ will be unaffected

bit 1-0 **TXmPRI<1:0>:** Message Transmission Priority bits
`11` = Highest message priority
`10` = High intermediate message priority
`01` = Low intermediate message priority
`00` = Lowest message priority

Note 1: This bit is cleared when TXREQ is set.

TABLE 24-4: DC TEMPERATURE AND VOLTAGE SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
Operating Voltage							
DC10	**Supply Voltage**						
	VDD		3.0	—	3.6	V	Industrial and Extended
DC12	VDR	**RAM Data Retention Voltage(2)**	1.8	—	—	V	—
DC16	VPOR	**VDD Start Voltage** to ensure internal Power-on Reset signal	—	—	VSS	V	—
DC17	SVDD	**VDD Rise Rate** to ensure internal Power-on Reset signal	0.03	—	—	V/ms	0-3.0V in 0.1s

Note 1: Data in “Typ” column is at 3.3V, 25°C unless otherwise stated.

2: This is the limit to which VDD can be lowered without losing RAM data.

TABLE 24-9: DC CHARACTERISTICS: I/O PIN INPUT SPECIFICATIONS (CONTINUED)

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ[1]**	**Max**	**Units**	**Conditions**
DI60a	IICL	**Input Low Injection Current**	0	—	-5[5,8]	mA	All pins except VDD, VSS, AVDD, AVSS, $\overline{\text{MCLR}}$, VCAP, SOSCI, SOSCO, and RB11
DI60b	IICH	**Input High Injection Current**	0	—	+5[6,7,8]	mA	All pins except VDD, VSS, AVDD, AVSS, $\overline{\text{MCLR}}$, VCAP, SOSCI, SOSCO, RB11, and all 5V tolerant pins[7]
DI60c	∑ IICT	**Total Input Injection Current** **(sum of all I/O and control pins)**	-20[9]	—	+20[9]	mA	Absolute instantaneous sum of all ± input injection currents from all I/O pins (| IICL + | IICH |) ≤ ∑ IICT

Note 1: Data in “Typ” column is at 3.3V, 25°C unless otherwise stated.

2: The leakage current on the $\overline{\text{MCLR}}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as current sourced by the pin.

4: See **“Pin Diagrams”** for a list of 5V tolerant pins.

5: VIL source < (VSS – 0.3). Characterized but not tested.

6: Non-5V tolerant pins VIH source > (VDD + 0.3), 5V tolerant pins VIH source > 5.5V. Characterized but not tested.

7: Digital 5V tolerant pins cannot tolerate any “positive” input injection current from input sources > 5.5V.

8: Injection currents > | 0 | can affect the ADC results by approximately 4-6 counts.

9: Any number and/or combination of I/O pins not excluded under IICL or IICH conditions are permitted provided the mathematical “absolute instantaneous” sum of the input injection currents from all pins do not exceed the specified limit. Characterized but not tested.

TABLE 24-39: ADC MODULE SPECIFICATIONS

AC CHARACTERISTICS			**Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic**	**Min.**	**Typ**	**Max.**	**Units**	**Conditions**
Device Supply							
AD01	AVDD	Module VDD Supply	Greater of VDD – 0.3 or 3.0	—	Lesser of VDD + 0.3 or 3.6	V	—
AD02	AVSS	Module VSS Supply	VSS – 0.3	—	VSS + 0.3	V	—
Reference Inputs							
AD05	VREFH	Reference Voltage High	AVSS + 2.5	—	AVDD	V	
AD05a			3.0	—	3.6	V	VREFH = AVDD VREFL = AVSS = 0
AD06	VREFL	Reference Voltage Low	AVSS	—	AVDD – 2.5	V	
AD06a			0	—	0	V	VREFH = AVDD VREFL = AVSS = 0
AD07	VREF	Absolute Reference Voltage	2.5	—	3.6	V	VREF = VREFH - VREFL
AD08	IREF	Current Drain	—	—	10	μA	ADC off
AD08a	IAD	Operating Current	— —	7.0 2.7	9.0 3.2	mA mA	10-bit ADC mode, See **Note 1** 12-bit ADC mode, See **Note 1**
Analog Input							
AD12	VINH	Input Voltage Range VINH	VINL	—	VREFH	V	This voltage reflects Sample and Hold Channels 0, 1, 2, and 3 (CH0-CH3), positive input
AD13	VINL	Input Voltage Range VINL	VREFL	—	AVSS + 1V	V	This voltage reflects Sample and Hold Channels 0, 1, 2, and 3 (CH0-CH3), negative input
AD17	RIN	Recommended Impedance of Analog Voltage Source	— —	— —	200 200	Ω Ω	10-bit ADC 12-bit ADC

Note 1: These parameters are not characterized or tested in manufacturing.

TABLE 24-42: ADC CONVERSION (12-BIT MODE) TIMING REQUIREMENTS

AC CHARACTERISTICS			**Standard Operating Conditions: 3.0V to 3.6V** **(unless otherwise stated)** Operating temperature -40°C ≤ T_A ≤ +85°C for Industrial -40°C ≤ T_A ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic**	**Min.**	**Typ[2]**	**Max.**	**Units**	**Conditions**
Clock Parameters[1]							
AD50	T_{AD}	ADC Clock Period	117.6	—	—	ns	—
AD51	t_{RC}	ADC Internal RC Oscillator Period	—	250	—	ns	—
Conversion Rate							
AD55	t_{CONV}	Conversion Time	—	14 T_{AD}		ns	—
AD56	F_{CNV}	Throughput Rate	—	—	500	ksps	—
AD57	T_{SAMP}	Sample Time	3 T_{AD}	—	—	—	—
Timing Parameters							
AD60	t_{PCS}	Conversion Start from Sample Trigger[2]	2.0 T_{AD}	—	3.0 T_{AD}	—	Auto convert trigger not selected
AD61	t_{PSS}	Sample Start from Setting Sample (SAMP) bit[2]	2.0 T_{AD}	—	3.0 T_{AD}	—	—
AD62	t_{CSS}	Conversion Completion to Sample Start (ASAM = `1`)[2]	—	0.5 T_{AD}	—	—	—
AD63	t_{DPU}	Time to Stabilize Analog Stage from ADC Off to ADC On[2,3]	—	—	20	µs	—

Note 1: Because the sample caps eventually loses charge, clock rates below 10 kHz may affect linearity performance, especially at elevated temperatures.

2: These parameters are characterized but not tested in manufacturing.

3: t_{DPU} is the time required for the ADC module to stabilize when it is turned on (AD1CON1<ADON> = `1`). During this time, the ADC result is indeterminate.

Revision D (June 2012)

This revision includes typographical and formatting changes throughout the data sheet text.

All other major changes are referenced by their respective section in the following table.

TABLE B-3: MAJOR SECTION UPDATES

Section Name	Update Description
Section 2.0 "Guidelines for Getting Started with 16-Bit Microcontrollers"	Updated the Recommended Minimum Connection (see Figure 2-1).
Section 9.0 "Oscillator Configuration"	Updated the COSC<2:0> and NOSC<2:0> bit value definitions for '`001`' (see Register 9-1).
Section 20.0 "10-bit/12-bit Analog-to-Digital Converter (ADC)"	Updated the Analog-to-Digital Conversion Clock Period Block Diagram (see Figure 20-2).
Section 21.0 "Special Features"	Added Note 3 to the On-chip Voltage Regulator Connections (see Figure 21-1).
Section 24.0 "Electrical Characteristics"	Updated **"Absolute Maximum Ratings"**. Updated Operating MIPS vs. Voltage (see Table 24-1). Removed parameter DC18 from the DC Temperature and Voltage Specifications (see Table 24-4). Updated the notes in the following tables: • Table 24-5 • Table 24-6 • Table 24-7 • Table 24-8 Updated the I/O Pin Output Specifications (see Table 24-10). Updated the Conditions for parameter BO10 (see Table 24-11). Updated the Conditions for parameters D136b, D137b, and D138b (T_A = 150ºC) (see Table 24-12).
Section 25.0 "High Temperature Electrical Characteristics"	Updated **"Absolute Maximum Ratings"**. Updated the I/O Pin Output Specifications (see Table 25-6). Removed Table 25-7: DC Characteristics: Program Memory.

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